Translating Dataflow Programs to Efficient Hardware: an *MPEG–4 Simple Profile* Decoder Case Study

Jörn W. Janneck[1], Ian D. Miller[1], Dave B. Parlour[1],
Marco Mattavelli[2], Christophe Lucarz[2], Matthieu Wipliez[3], Mickaël Raulet[3], Ghislain Roquier[3]

[1] Xilinx, Inc.
San Jose, CA, U.S.A
{jorn.janneck,ian.miller,dave.parlour}@xilinx.com

[2] Microelectronic Systems Laboratory (GR-LSM)
Ecole Polytechnique Fédérale de Lausanne
CH-1015 Lausanne, Switzerland
{marco.mattavelli,christophe.lucarz}@epfl.ch

[3] IETR, UMR CNRS 6164, Image and Remote Sensing laboratory
Institut National des Sciences Appliquées de Rennes
F-35043 Rennes, France
{mwipliez,mraulet}@insa-rennes.fr

Dataflow programming

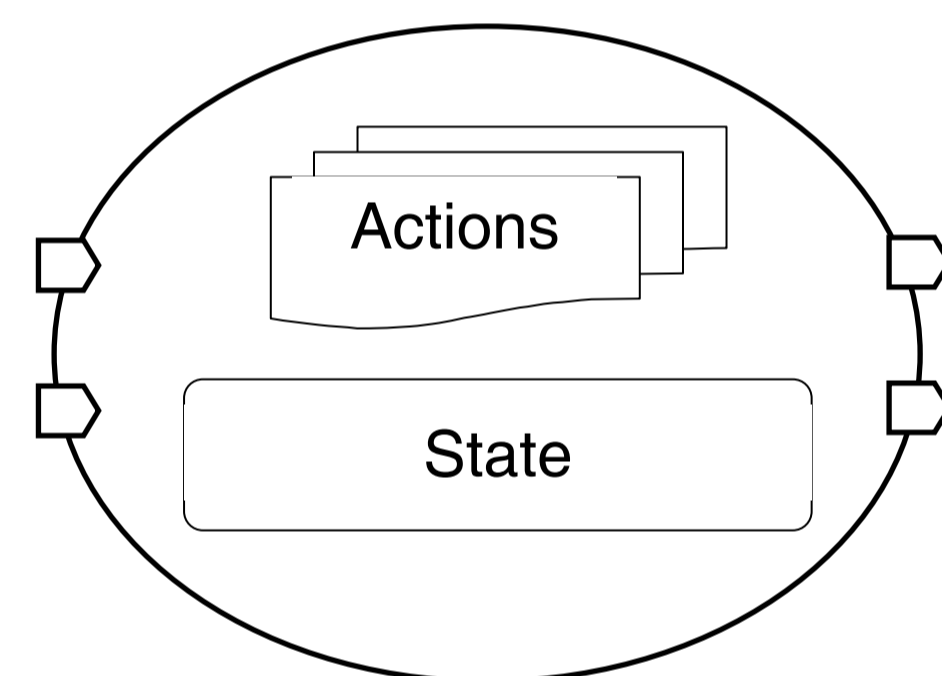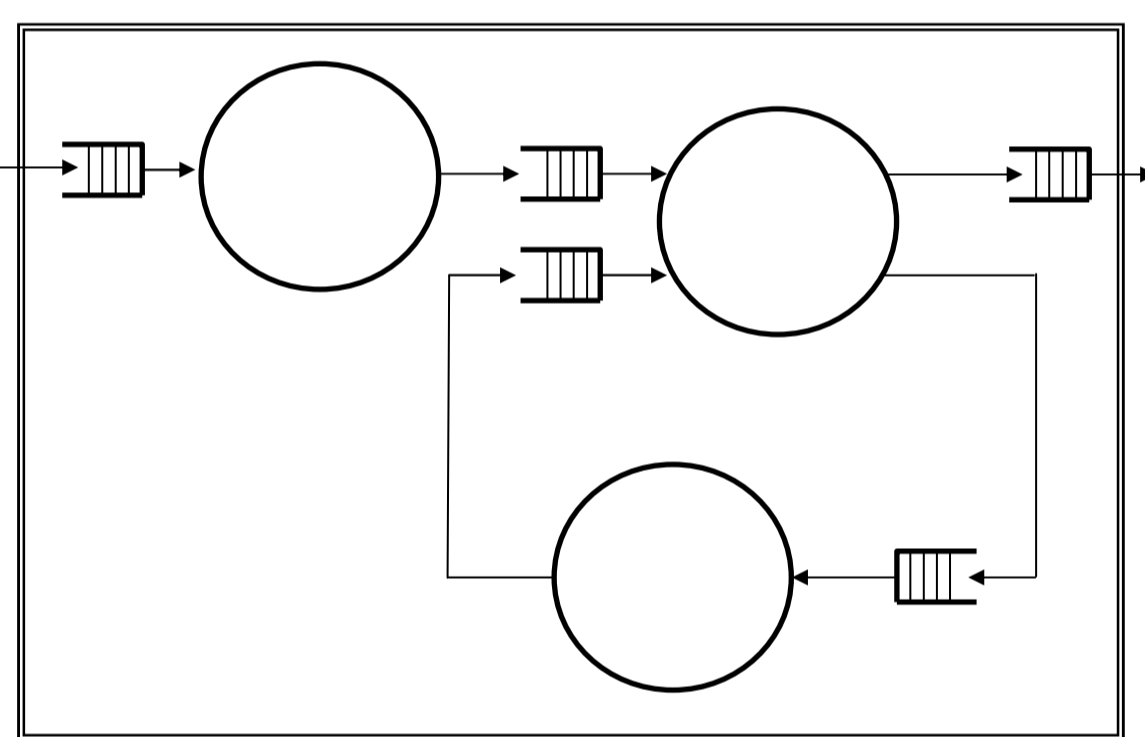### Highly parallel computing platform
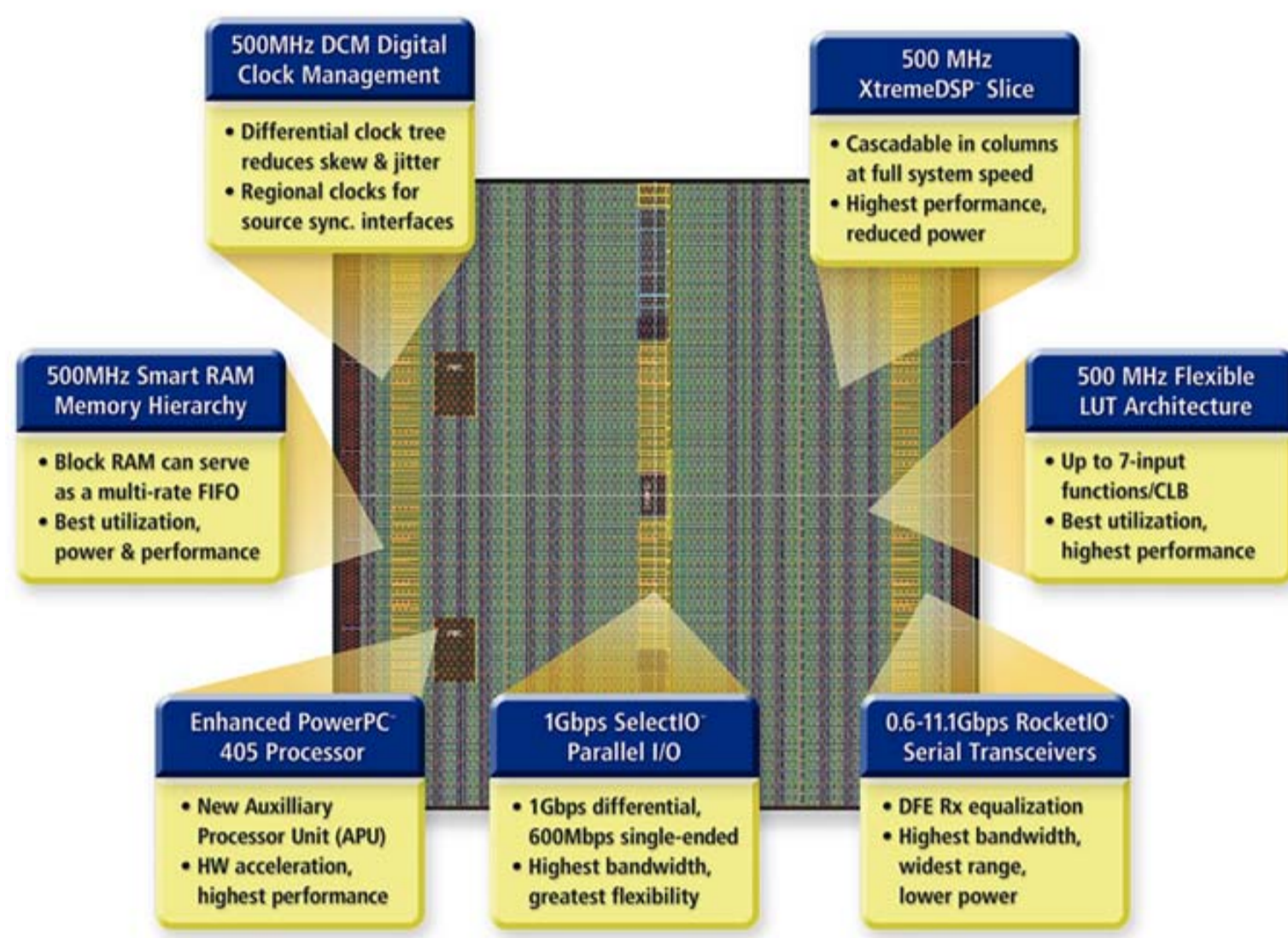
**Example:
Xilinx Virtex-4**
(XC4VFX140)
- 142k logic cells
- 552 RAMs
  x 18Kbits each
- 192 DSP ALUs
- 2 PowerPC 405
- 4 Ethernet MACs

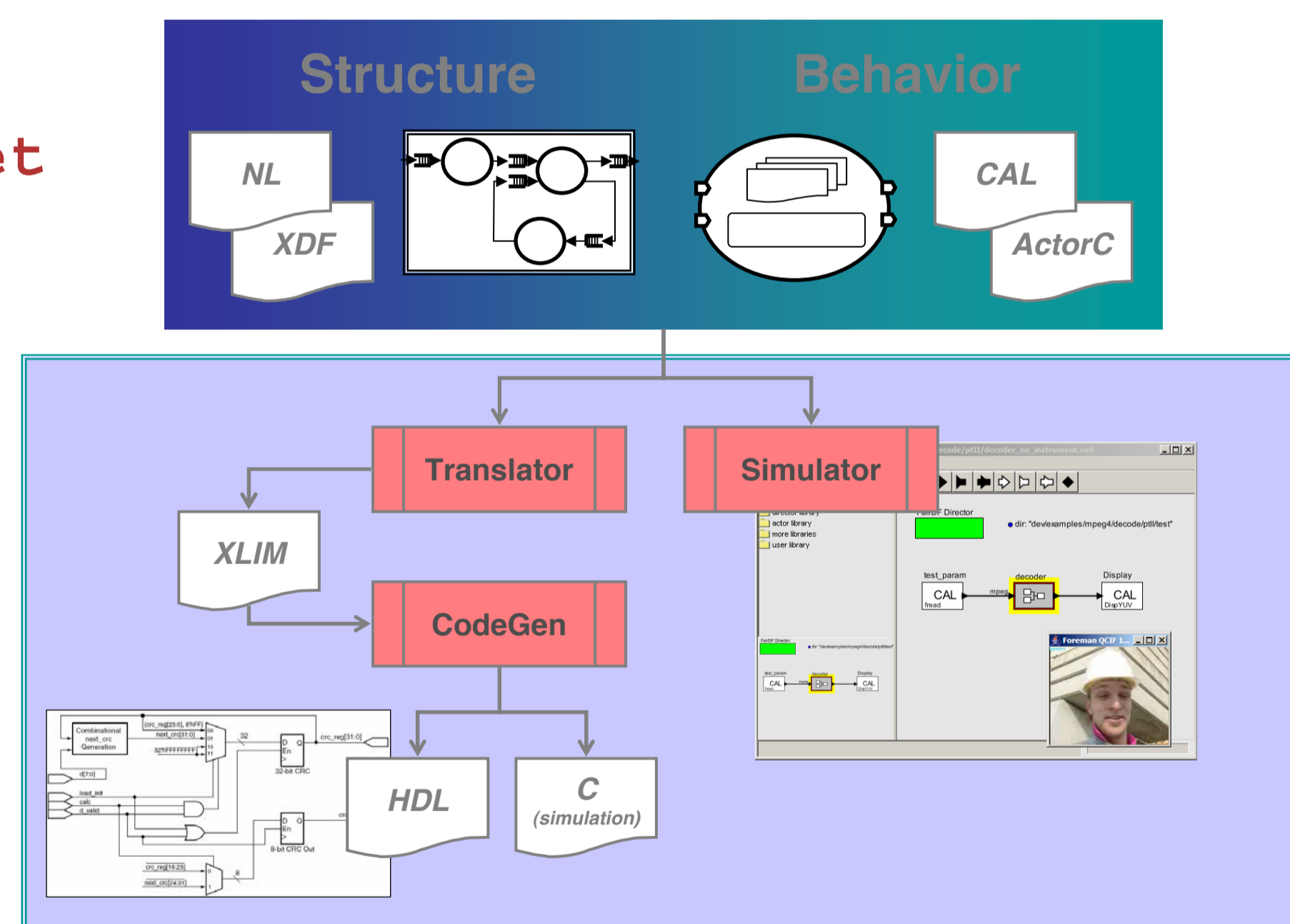### Programming model: dataflow with actors

- FIFO connections
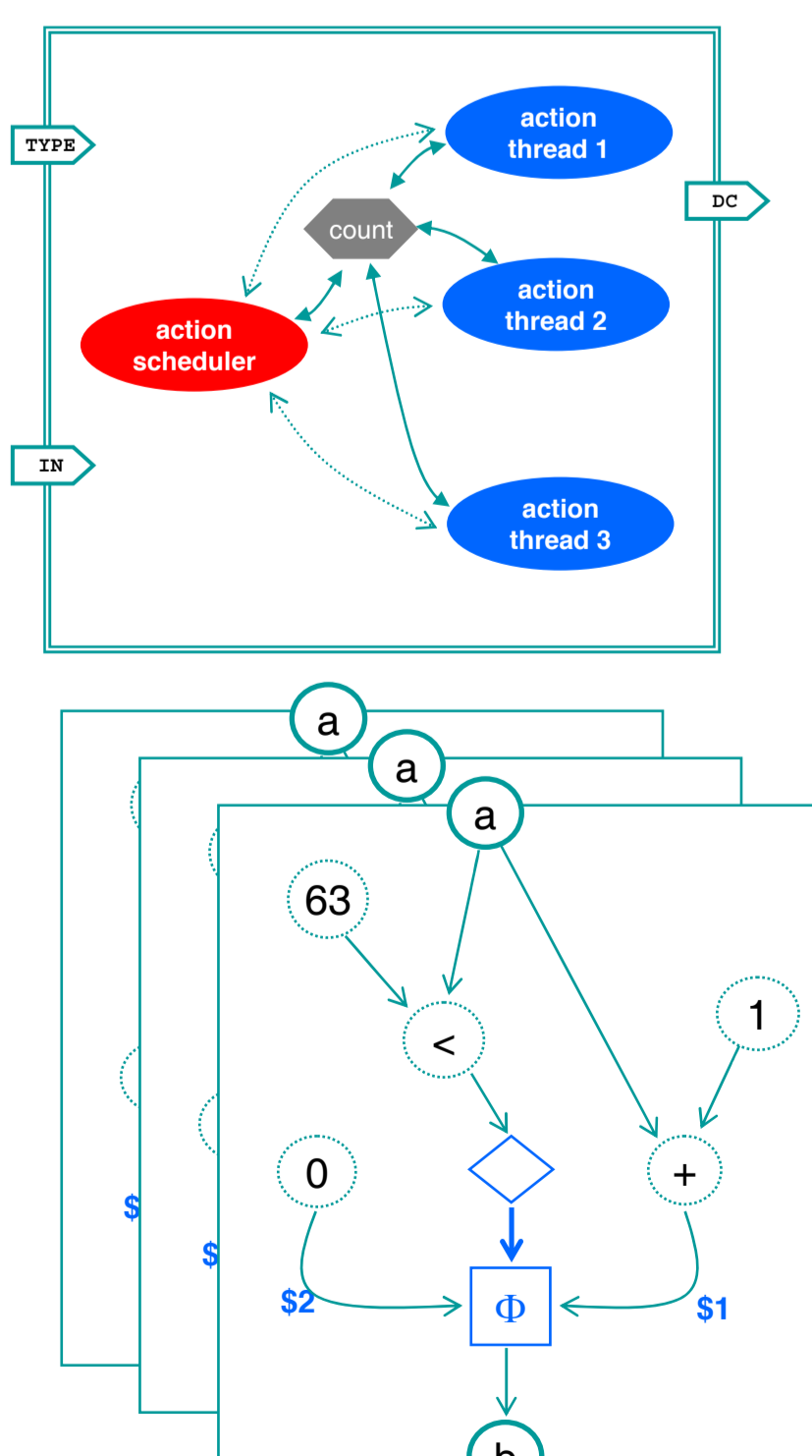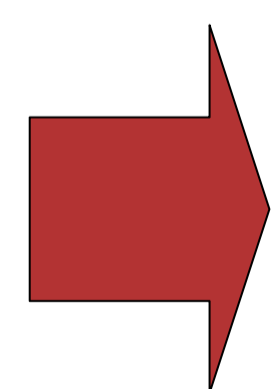- encapsulated state
- atomic state transitions

Dataflow Tools

opendf.sourceforge.net

- various input languages e.g. CAL
- untimed simulation
- HDL code generation

Translation Process

Threads… …in SSA form.

1. Actor code split into threads:
   1 thread per action
   +1 thread for the scheduler
2. Each thread represented in SSA form.
3. Produce circuit from SSA form.
4. Optimize data paths (bit-accurate constant prop).
5. Schedule operations when possible.
6. Insert registers where required.

Application: MPEG-4 Simple Profile Decoder

...0101001111010010010
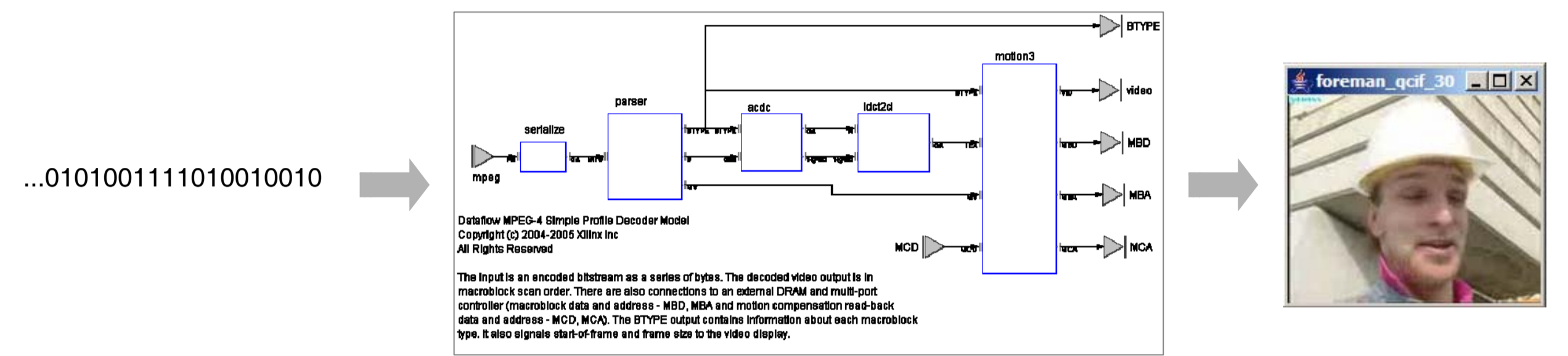
Actors, big and small

CAL actor language

ParseHeaders
1320 lines
(without header comments)
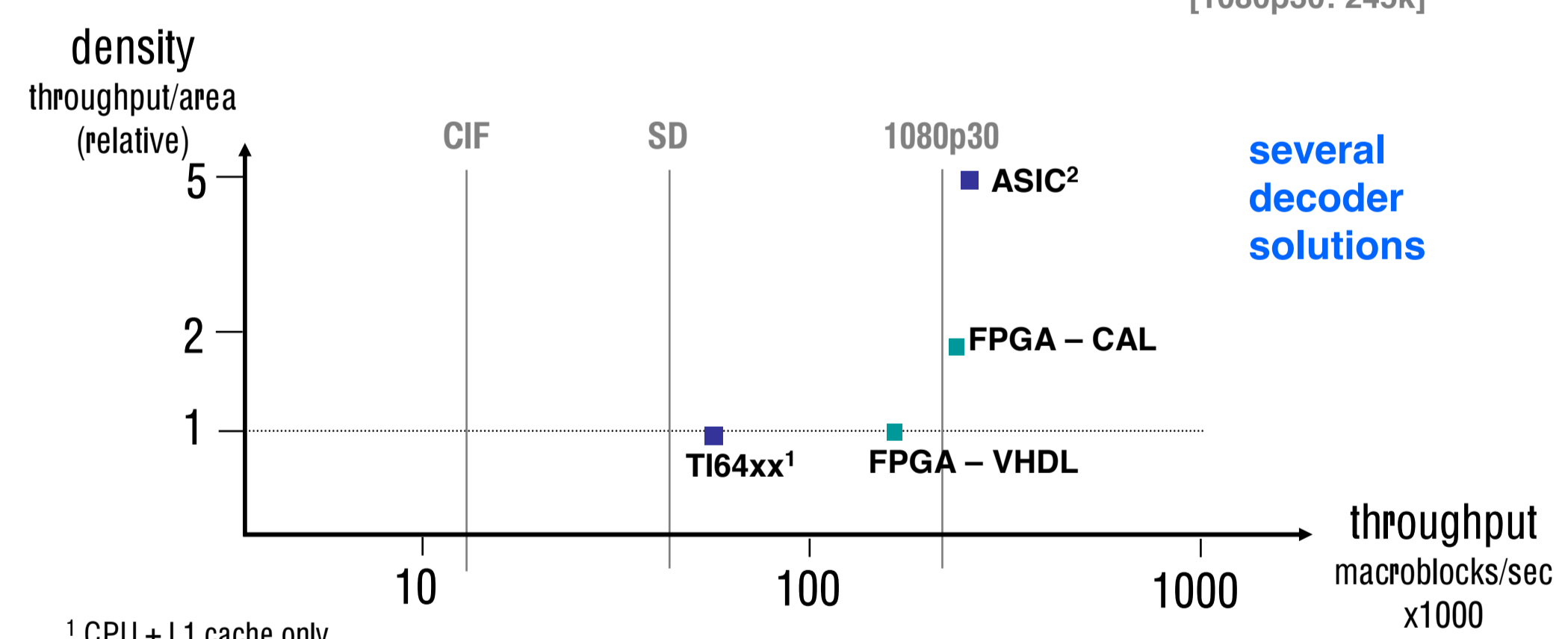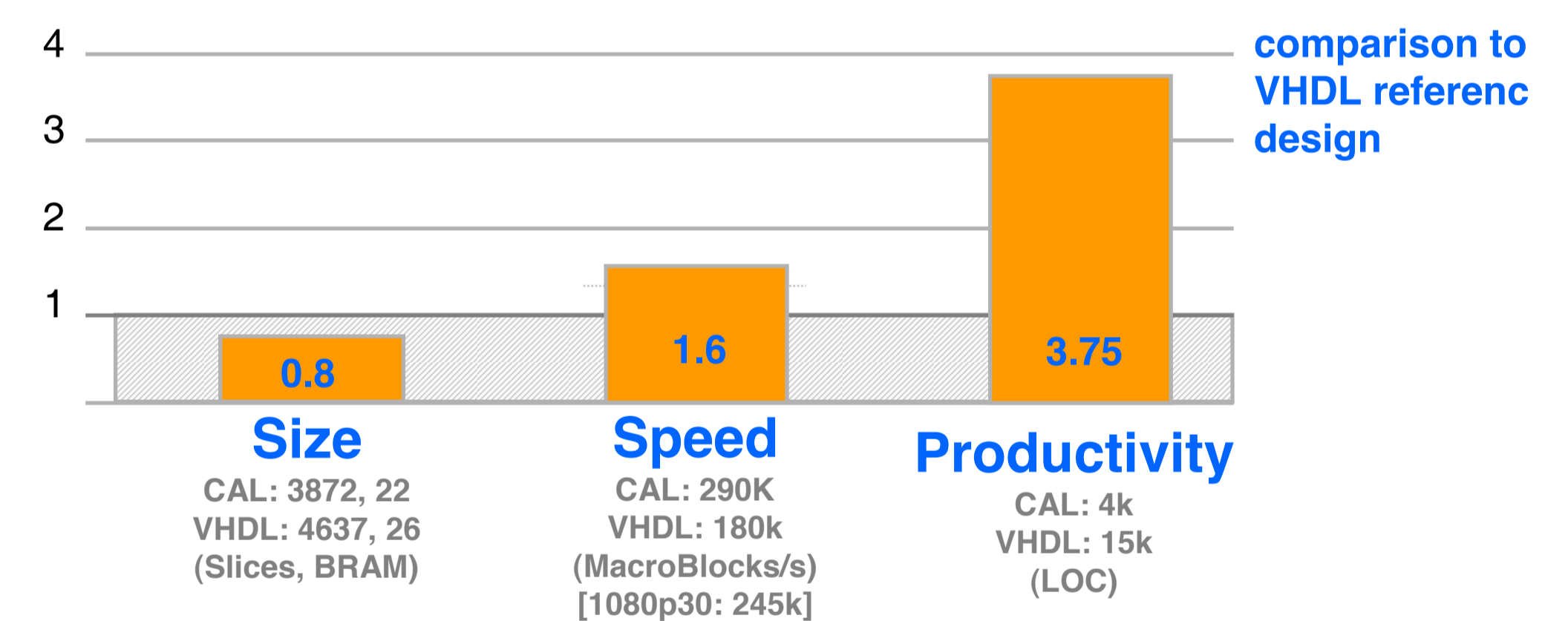
Range of actors
- small compute kernels
- large control-dominated actors

Compare
23 lines
(without header comments)

Hardware Synthesis - Quality of Result

Smaller, faster, and earlier than VHDL reference.

comparison to VHDL reference design

	Size	Speed	Productivity
	0.8	1.6	3.75

Size
CAL: 3872, 22
VHDL: 4637, 26
(Slices, BRAM)

Speed
CAL: 290K
VHDL: 180k
(MacroBlocks/s)
[1080p30: 245k]

Productivity
CAL: 4k
VHDL: 15k
(LOC)

density
throughput/area
(relative)

CIF   SD   1080p30

ASIC[2]
FPGA – CAL
TI64xx[1]   FPGA – VHDL

several decoder solutions

throughput
macroblocks/sec
x1000

[1] CPU + L1 cache only
[2] ISSCC'06, H.264 capable, not a programmable solution

Conclusion

- Parallel platforms require parallel programming models.
- Dataflow is a general and portable way to describe highly parallel computational systems.

- MPEG-4: an at-size, real world application, with a broad spectrum of computational elements.
- All actors built in the CAL actor language, and composed using the NL network language.

- Our tools generate implementations that actually beat the VHDL reference in terms of QoR.

- Any abstraction cost was dwarfed by the ability to quickly iterate over multiple versions of the design.