

A (256x256) Pixel 76.7mW CMOS Imager/ Compressor Based on Real-Time In-Pixel Compressive Sensing

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Abstract—A CMOS imager is presented which has the ability to perform localized compressive sensing on-chip. *In-pixel* convolutions of the sensed image with measurement matrices are computed in real time, and a proposed programmable two-dimensional scrambling technique guarantees the randomness of the coefficients used in successive observation. A power and area-efficient implementation architecture is presented making use of a single ADC. A 256×256 imager has been developed as a test vehicle in a 0.18μm CIS technology. Using an 11-bit ADC, a SNR of 18.6dB with a compression factor of 3.3 is achieved after reconstruction. The total power consumption of the imager is simulated at 76.7mW from a 1.8V supply voltage.

I. INTRODUCTION

Compressive sensing has recently emerged as a powerful algorithmic method enabling the compression of signals, specifically still images, and enabling the hardware integration of the compression algorithm on-chip. The compressive sampling hardware has a very dense integration, and the hardware overhead on-chip is extremely limited. The complexity is shifted from the lightweight embedded image sensor system towards a heavy computing-load computer system which is in charge of image reconstruction.

Two earlier attempts have been made in integrating a compressive sensing imager, to date. In [1], a micro-electromechanical mirror system is used to reflect each pixel of the image onto a single-pixel photodetector, which processed to image acquisition in a sequential way. The system has already proved to be operative in a laboratory environment. Still, the mechanical nature of some of its components imposes strict constraints on the alignments of all constituting elements, making it impractical as an embedded or field sensor system.

In [2] an integrated 256 × 256 pixels imager has been developed in a 0.35μm CMOS technology. The circuit-level developments, and issues related to coefficient generation are not presented.

The theoretical framework underlying the CMOS realization presented in this paper has been described in detail by the authors in [3]. The original compressive sensing algorithm is adapted to enable VLSI integration, and is briefly described in Section II. The hardware architecture of a 256 × 256 pixels imager with compressive sensing embedded *in-situ* is presented in Section III. The circuit realization of the proposed architecture is discussed in Section IV.

II. COMPRESSIVE SENSING: THEORY AND ALGORITHM

A. Theoretical Background

Let $x \in N \times N$ be an image with N^2 pixels. For simplicity, x is vectorized into an element of \bar{N} with $\bar{N} = N^2$, keeping the notation $x_{(p,q)}$ to address individual pixels. Moreover, we assume that the image has a sparse representation on some basis Ψ , that is $x = \Psi\alpha$ where most of the entries α are very small and very few are significant. Classical transform coding strategies consist in observing all the x_i , i.e. at Nyquist rate, computing all the components of $\alpha = \Psi^T x$ and in further steps, only keeping the $K \ll \bar{N}$ first coefficients of α to keep the essential information of x .

The compressive Sensing (CS) theory [4] introduces the idea of acquiring only $M \leq \bar{N}$ projections of the data, i.e. $y = \Phi x$ and directly use this compressed description at the decoder to reconstruct the signal. The signal is thus sensed and compressed at once. CS shows that if x only has K non-zero components and $M \geq O(K \log N/K)$, then a large class of measurement matrices Φ can be used to reconstruct x with very high probability. In common practice, the matrix entries preselected randomly from simple distributions. The decoder reconstructs the signal from the observations by solving a convex optimization problem of the form:

$$x = \arg \min_u \mathcal{S}(u) \quad \text{subject to} \quad \|y - \Phi \Psi u\|_2 \leq \epsilon \quad (1)$$

where $\mathcal{S}(u)$ enforces the sparsity of the representation, typically $\mathcal{S}(u) = \|u\|_1 = \sum_i |u_i|$.

B. Practical Implementation

As theoretically explained in [3], in the sensing model $y = \Phi x$ of our imager, we have chosen the Random Convolution strategy explained in a recent work of J. Romberg [5]. In short, it dictates to uniformly pick M values at random in the convolution of the image $x \in \bar{N}$ with a random filter a . The random convolution of an image $x \in \bar{N}$ by a random filter $a \in \bar{N}$ is mathematically described by

$$y_i = (\Phi x)_i = \sum_j a_{r(i)-j} x_j = (x * a)_{r(i)} \quad (2)$$

where $r(i)$ corresponds to the random selection of one index in the set \mathcal{N} . In this work, a filter a is defined in the spatial domain as a Rademacher sequence of ± 1 . The random

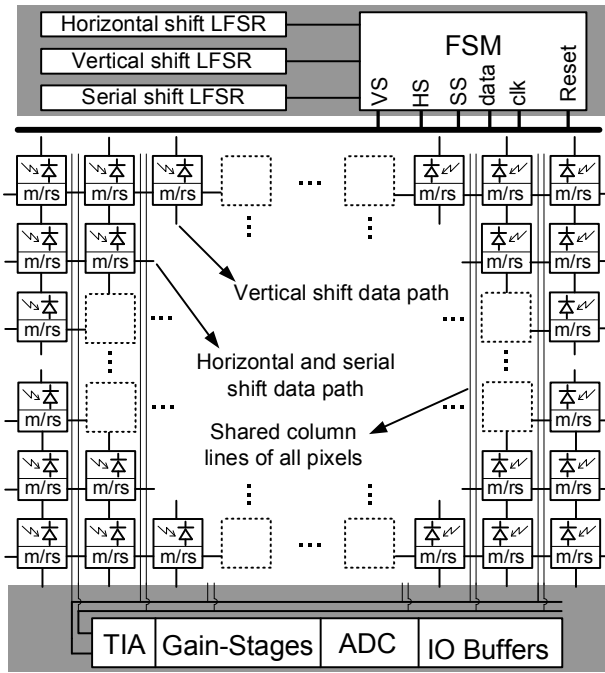


Fig. 1. Architecture of the CMOS imager. The block named *m/rs* represents the memory point which is implemented as a DFF, and column routing selection, as depicted in Fig. 2.

sensing strategy combined with this particular filter has a direct translation in the CMOS architecture of our imager.

III. ARCHITECTURE OF THE CMOS IMAGER

A. System Architecture

In a conventional imager, the output of each pixel is serially scanned and captured by column-parallel ADCs which has a high cost in terms of power and silicon area consumption, and floorplanning complexity. The required sampling rate at the ADC is determined by the horizontal resolution and the frame-rate. In the compressive sensing imager presented in this work, no scanning of the columns is needed and the image is acquired and processed by random convolution from all pixels, simultaneously. The reduced number of conversions that is needed to acquire one still image [3] enables the use of a single ADC for medium-size imagers. The silicon area that is saved this way is appropriately used to increase the imager resolution. The proposed system architecture is presented in Fig. 1 consisting of a core photosensor array with *in-situ* convolution processing in the current domain, a finite state machine (FSM) providing general control of the circuit, three linear feedback shift registers (LFSRs), and a mixed-signal processing unit implemented as one transimpedance amplifier (TIA), and two switched-capacitor gain stages driving a two-stage algorithmic ADC, and the input/output buffers (IO Buffers).

B. Embedded Photodiode Array

The convolution operation is performed by the electronics in the analog domain at the pixel level, i.e., *in-situ*, enabling

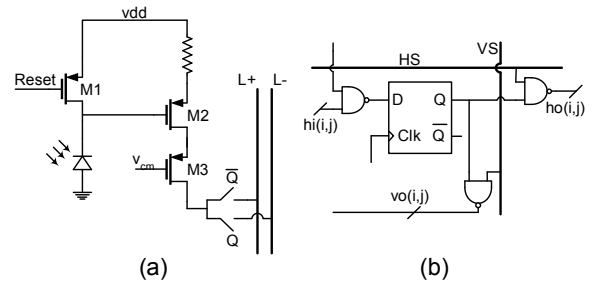


Fig. 2. (a) Active pixel sensor, and (b) local memory with logic control.

taking full benefit of very compact, and power-efficient implementations of parallel analog operations. As shown in Fig. 2(a), when the Reset control is low, the gate capacitance of M2 is charged to V_{dd} , and during the recording phase, M2 drives a current which is proportional to the captured light intensity. M3 boosts the output impedance of the recording site in order to prevent the loading of the TIA input impedance. The small junction capacitance of M3 also isolates the TIA input from the large well parasitic capacitance of the photodiode.

Digital control circuits are embedded into each pixel as depicted in Fig. 2(b). Each multiplication coefficient, i.e. ± 1 is stored in a local memory, as a binary value, which is used to drive the active pixel current output to one of two summation columns L_+ or L_- . The control logic gates (NANDs) are used to load the local memory with a new multiplicand coefficient during the initialization or scrambling phases.

C. Two-Dimensional Coefficient Scrambling

In compressive sampling of images, the generation of two-dimensional uncorrelated coefficients is a crucial step. A strategy and hardware enabling the generation of random coefficients, and guaranteeing the decorrelation of the coefficients used in successive image acquisition steps is proposed, as shown in Fig. 3(a). Each coefficient is locally stored in a D flip-flop, as a binary value, inside the pixel it has to be applied. The serial-shift LFSR (SS-LFSR) is used to generate the initial set of coefficients during the initialization phase. As depicted in Fig. 3(b), control signal SS is at logic 1, and the serial data provided by SS-LFSR is shifted from each memory point to its next horizontal neighbor, at each clock cycle. A coefficient reaching the last column is routed to the first column in the next row. The initialization phase lasts 256×256 cycles, and is followed by M cycles which is needed for M conversions required for one observation of the still image. Each measuring cycle is always preceded by the insertion of one new coefficient which is generated by the SS-LFSR and serially shifted to the memory array. The initial seed for next consecutive M conversions is provided by two-dimensional scrambling of coefficients. When the horizontal-shift control signal (HS) is activated, horizontal shift of the array is executed according to a number of shift steps dictated by the horizontal-shift LFSR (HS-LFSR). By construction, each coefficient memory point is connected to its four neighbors. All coefficients are horizontally shifted,

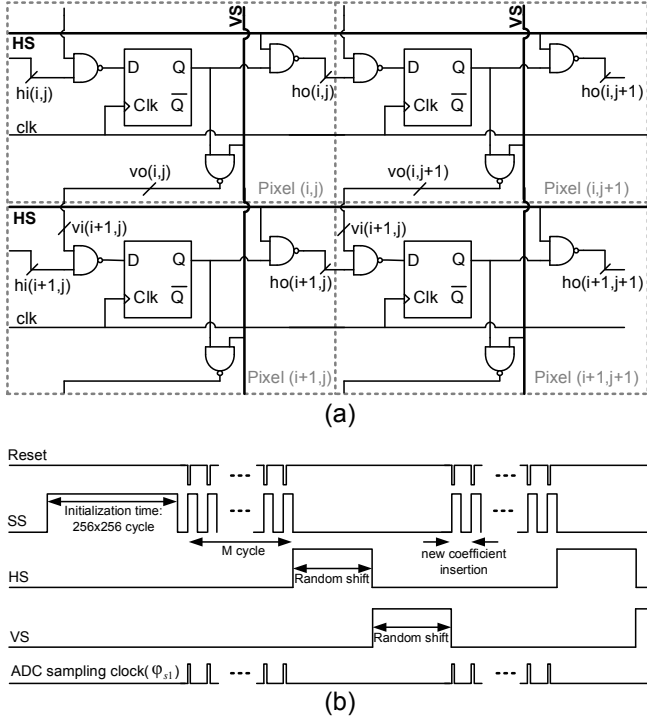


Fig. 3. (a) Two-dimensional scrambling scheme, and (b) timing diagram of the imager.

simultaneously. During this cycle, the output of memory points located on column 256 are connected to the input of memory points located in column 1, forming a cylindrical coefficients shifting. When the vertical-shift signal (VS) is activated, in a similar way, the vertical-shift LFSR (VS-LFSR) dictates a number of vertical shifts to be performed in a subsequent phase. In subsequent image processing, horizontal and vertical shift and image acquisition have to be repeated.

In a 256×256 pixel imager, 4-bit random shifts in horizontal and vertical directions are assessed to be sufficient to decorrelate successive coefficients seed for each observation. HS-LFSR and VS-LFSR generate decorrelated shifting numbers, and one specific coefficient seed can be randomly placed in the array, after several successive observation. It reduces the number of clock cycles which is required for initialization and inserting new seed at start of each observation. Also, a side benefit of the proposed two-dimensional technique resides in the very secure imaging and compression. The digital logic included into the pixels located in the first column must accommodate three possible input sources, as depicted in Fig. 4. All other pixels use the hardware described in Fig. 3(a).

IV. CIRCUIT REALIZATION AND ARCHITECTURE EVALUATION

A. Trans Impedance Amplifier (TIA)

The random multiplication of the pixel output is achieved by exchanging the positive and negative inputs of the fully differential TIA. For each pixel, this operation is partially done at pixel level (*in-situ*) by conveying the diode current

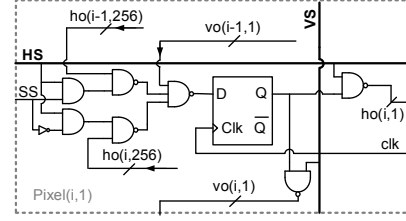


Fig. 4. Local memory and control logic in the first column of the imager array.

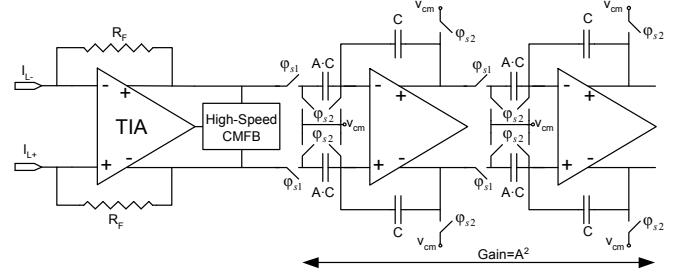


Fig. 5. Transimpedance amplifier, followed by a two-stage switched-capacitor gain stage.

either to the L_+ or the L_- column line. A single TIA shared between all pixels provides differential output voltage. Since the probability of multiplication by random sequence of +1 and -1 is almost equal, the differential output swing of the TIA is very small and a large value feedback resistor can be used to increase the trans-impedance gain and also simplify the design of the output stage. The large variation of the TIA's output common-mode voltage due to large common-mode currents flowing to differential inputs is fixed by a high-speed common mode feedback (CMFB) circuit at output, which is shown in Fig. 5. The power penalty due to the high-speed operation of the CMFB is negligible, because the high-speed operation, large bias currents in CMFB, is only activated when the ADC sampling clock is high, which is a negligible fraction of the total conversion cycle illustrated in Fig. 3(b). The TIA is a two-stage OTA, where the first stage employs a folded-cascode gain boost architecture to provide 90 dB of DC gain. This large value of the DC gain achieved in first stage alleviates the need for a low output impedance output stage required to drive a resistive feedback load. The output stage consists of a class AB amplifier. The TIA's output is followed by two non-delayed switched-capacitor gain-stages to scale up the output of the TIA to the reference voltage of the ADC.

B. Two-Step Algorithmic ADC

The Quantization noise of the ADC introduces error into the reconstruction algorithm. High-level simulation results prove that 8-bit of resolution in the ADC is sufficient to preserve SNR after reconstruction with compression factor of a 3.3. Moreover, the non-linearity of the recording circuit affects the reconstruction. Using the lumped model of non-linearity in image reconstruction, only a third order type of non-linearity is used, which demonstrates that a total harmonic distortion

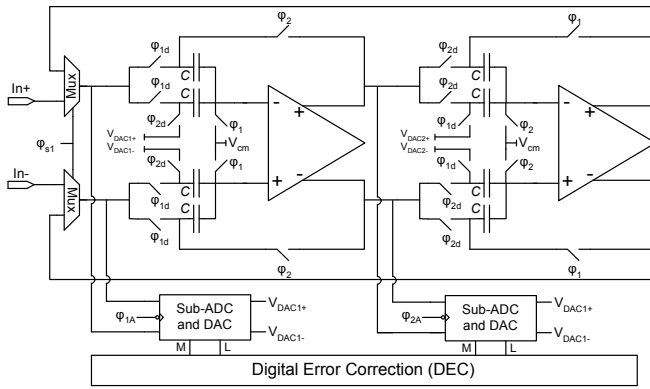


Fig. 6. Two-step algorithmic ADC with digital error correction.

(THD) better than -47 dB is required. Therefore, superpositioning of all these effects including the thermal noise of the circuit, a 11-bit two-stage algorithmic ADC [8] is adapted to fulfill the requirements. Fig. 6 shows the ADC architecture, where two-step 1.5-bit gain stages results in a 11-bit output code in 5 clock cycles. Analog multiplexers are used to feed the residue voltage back to the input stage for consecutive recycling. The sub-ADC and DAC blocks provide the required DAC voltages according to the comparison results. Dynamic comparators with switched-capacitor subtractions are used to save static power consumption [6].

C. Architecture Evaluation

Table 1 shows the main performance summary of the imager circuit which is developed in a $0.18\mu\text{m}$ 1P4M CMOS Image Sensor (CIS) technology. As a benefit of the compressive sensing technique, the required speed of the TIA and the ADC is reduced by the compression factor, here 3.3 times. Therefore, a sampling rate of 4 MHz in the ADC allows to capture images up to 60fps with an oversampling ratio of three in order to reduce the circuit thermal noise. Without oversampling, the frame rate can be increased up to 180fps. Hence, the proposed architecture is capable to perform as well as a live imager. The power consumption is dominated by two step switched-capacitor gain stages, which provide additional closed loop gain of 256. The total power consumption is simulated to be 76.7mW from 1.8V supply voltage. The power consumption is comparable with state-of-the-art compressing imagers [7] thanks to the reduced number of measurements. Including the non-ideal effects due to the circuit realization to the image reconstruction algorithm, the simulation results are shown in Fig. 7 for the original image and reconstructed counterpart. The reconstruction is performed using a Nesterov iterative boosting inside a convex minimization based on operator splitting and proximal methods. The SNR is measured to be 18.6 dB with compression factor of 3.3 without any oversampling.

V. CONCLUSION

A monolithic compressive sensing imager is presented, which has been developed in a $0.18\mu\text{m}$ 1P4M CIS technology.

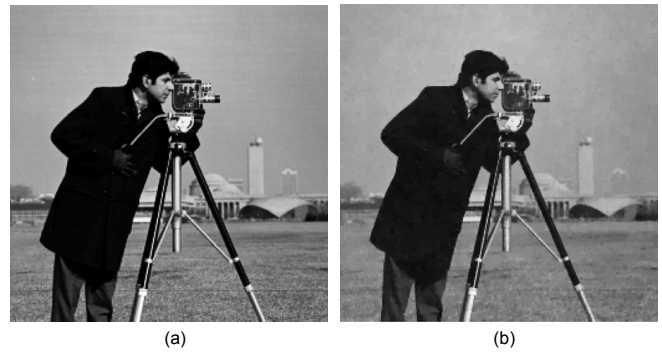


Fig. 7. (a) Original image, and (b) reconstructed image with 11-bit ADC.

TABLE I
PERFORMANCE SUMMARY OF THE IMAGER CIRCUIT.

Technology		0.18 μm 1P4M CIS
Supply voltage		1.8V
Array Dimension		256×256
Max Frame Rate		60fps
ADC Resolution		11-bit
ADC Sampling Rate		4MS/s
SFDR		61 dB
Power Consumption	ADC	8.6 mW
	TIA+Gain Stages	68.1mW
	Total	76.7mW

The 256×256 imager array only consumes 76.7mW, which is dominated by the TIA and gain stages. 60fps imaging is achieved with a 4MHz sampling clock thanks to the reduced number of measurements required in compressive sensing. Random coefficient matrix are generated by an original two-dimensional scrambling technique making use of local memory. High-level simulations of image reconstruction prove the effectiveness of the proposed architecture.

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