TEXTURED SILICON HETEROJUNCTION SOLAR CELLS WITH OVER 700 MV OPEN-CIRCUIT VOLTAGE STUDIED BY TRANSMISSION ELECTRON MICROSCOPY

S. Olibet[1*], C. Monachon[1,2], A. Hessler-Wyser[2], E. Vallat-Sauvain[1+], S. De Wolf[1], L. Fesquet[1], J. Damon-Lacoste[1], C. Ballif[1]
[1]University of Neuchâtel, Institute of Microtechnology (IMT), Breguet 2, 2000 Neuchâtel, Switzerland
[2]Ecole Polytechnique Fédérale de Lausanne (EPFL), CIME, 1015 Lausanne, Switzerland
[+]present address: Oerlikon Solar-Lab SA, 2000 Neuchâtel, Switzerland
[*]sara.olibet@unine.ch, phone: +41 32 718 33 18

ABSTRACT: In this article, we report on the use of transmission electron microscopy (TEM) for the fabrication of high-performance textured amorphous/crystalline silicon (a-Si:H/c-Si) heterojunction (HJ) solar cells. Whereas classical thin-film characterization techniques allowed us to optimize the a-Si:H layer properties for flat HJ solar cells (open-circuit voltages (V_{OC}) up to 710 mV and energy conversion efficiencies up to 19.1%), these techniques can not always be fully exploited on textured c-Si surfaces. Nevertheless, in this situation, TEM micrographs permit us to identify device performance limiting factors, such as, e.g., local epitaxy in pyramid valleys as the main source of our V_{OC}-loss. Minimizing this local epitaxy by adjusting the amorphous Si based layers growth conditions and improving the c-Si surface morphology yields Si HJ solar cells with V_{OC}s over 700 mV.

Keywords: Silicon, Heterojunction, Texturisation

1 INTRODUCTION

The high efficiency potential of a-Si:H/c-Si HJ solar cells [1] is based on the excellent surface passivation of c-Si by intrinsic a-Si:H. The doping capability of a-Si:H additionally allows for low-temperature emitter and back surface field (BSF) formation. In standard c-Si solar cells processing, the passivating layer is deposited on top of the diffused emitter but has to be locally opened (i.e. depassivated) to draw current from the solar cell. When growing intrinsic/doped thin-film Si layer stacks on c-Si to form HJ solar cells, the c-Si's surface passivation takes place right at the junction. While this bears the advantage of avoiding a direct contact between the metal and the electrically active semiconductor, the requirements on the c-Si's surface quality become higher [2].

In the past, we reported on high performance Si HJ solar cells on double-side polished c-Si [3,4]. However, the further improvement of these flat Si HJ solar cells is limited by the current loss due to excessive front surface reflection and the absence of internal reflection linked to the planar optical features. Random pyramidal surface texture, as commonly used in industry for monocrystalline Si, greatly reduces such reflection. Though, care has to be taken when applying the a-Si:H based layers optimized for the flat HJ directly to such pyramidal textured c-Si substrates: For our case, e.g., the short-circuit current density (J_{SC}) effectively improves by introducing texture, but at the cost of lowered values for the V_{OC} and fill factor (FF), as illustrated in Fig. 1. A one-to-one transfer of process parameters from flat to textured c-Si is thus not necessarily appropriate.

For flat HJ solar cells, the doped layers are optimized in terms of conductivity on a dummy structure consisting of ultra-thin (~5 nm) intrinsic a-Si:H film on glass. On this dummy structure, conductive layers are grown at the onset of the a-Si:H/µc-Si:H transition, which are referred to as µc-Si:H layer in this paper. Such films show the highest conductivity. Thus, Raman crystallinity measurements greatly help in finding appropriate doped film deposition conditions. Finally, layer thickness can be easily evaluated with a mechanical profilometer.

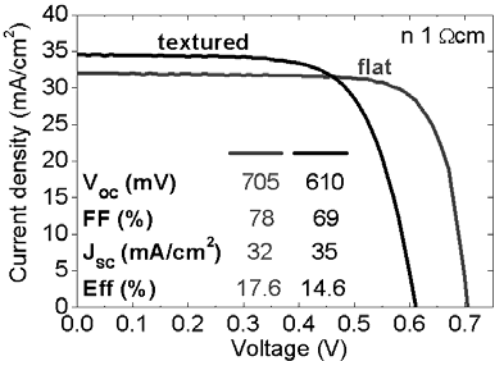

Figure 1: Si HJ solar cell performances on flat and textured c-Si. Wafers are both n 1 Ωcm FZ type and thin-film Si emitter and BSF layer stacks are deposited with identical PECVD process parameters.

On textured c-Si, unfortunately, such classical layer characterization techniques can not be exploited to their full extent. For this, we present here our study on film optimization based on lifetime measurements on Si heterostructures linked to TEM for the identification of key microstructural interfacial features, circumventing these issues. We will argue that such a procedure presents a powerful tool for achieving high-V_{OC} HJ solar cells.

2 EXPERIMENTAL

2.1 Layer growth and characterization

Monocrystalline Si wafers for Si HJ solar cell fabrication are of 1 Ωcm n-type. Their thickness ranges from 180 µm to 250 µm. The random pyramidal surface texture is formed by alkaline anisotropic wet-chemical etching. This is followed by a simplified RCA clean before immersion in diluted HF for native oxide removal. Intrinsic a-Si:H and doped µc-Si:H layers (PH_3 for n-type and TMB for p-type) are grown by VHF-PECVD (70 MHz) in a single chamber for emitter and BSF formation. ITO is used as transparent conductive oxide (TCO) and is

DC-sputtered on both sides of the wafer, on the front via a shadow mask to define round cells with 4.5 mm of diameter. Probes for electrical measurements are directly placed on the front ITO, whereas on the back a subsequently sputtered Al serves as reflector and electrical contact. Our HJ solar cells consist thus of an Al - ITO back contact / n μc-Si:H – i a-Si:H BSF / n-type c-Si / i a-Si:H – p μc-Si:H emitter / front ITO. Finally, samples are annealed for 90 min at 180 °C under nitrogen flow.

Doped layers for flat Si HJ solar cells are first optimized according to the procedure mentioned above. Layer and layer stacks on c-Si wafers are then further optimized by means of injection level dependent lifetime measurements.

2.2 Lifetime measurements

The quality and nature of the a-Si:H/c-Si interface passivation [3] is determined via effective carrier lifetime (τ_{eff}) measurements made with the contactless WCT-100 photoconductance tool from Sinton consulting [5]. To measure the widest possible injection level range (excess carrier density Δn), transient and QSS measurements (the latter in the generalized mode [6]) are combined.

Using symmetrical surface passivation and when measuring high lifetimes (typically > 100 μs), the effective surface recombination velocity S_{eff} is related to τ_{eff} by the simple equation $S_{eff} = (\tau_{eff}^{-1} - \tau_{bulk}^{-1})\cdot W/2$, where W is the wafer thickness [7]. We set τ_{bulk} to be only limited by intrinsic recombination, and use the intrinsic lifetime parameterization of Kerr *et al.* [8].

2.2 Transmission electron microscopy

(TEM) permits material characterization with subnanometer resolution. TEM is thus a powerful tool to gain information on the structure, phases and crystallographic features of materials. A proper interface characterization is decisive to obtain high performance a-Si:H/c-Si heterostructure devices [9]. No other present technique but TEM allows studying a-Si:H growth on c-Si pyramids, but sample preparation is challenging [10]. Here, samples are prepared by tripod polishing followed by low voltage ion milling, except for the TEM micrograph shown in Fig. 2a (that is prepared by the cleaved corner method). TEM observations are made on a Philips CM300 aligned at 200 kV (Philips CM200 for Fig. 2a).

3 RESULTS

3.1 Atomic structure of flat Si HJ solar cells

Fig. 2 shows TEM and HR-TEM micrographs of the flat i a-Si:H / p^+ μc-Si:H solar cell emitter layer stack on n-type c-Si. The abrupt nature of the interfaces yields V_{OC}s of up to 710 mV.

3.2 Crystallographic structure of interfaces in textured Si HJ solar cells

Optimal process parameters for flat layer and layer stacks are obtained by stacked layer optimization on glass. However, the a-Si:H based layers optimal for the flat HJ did result in low V_{OC}s when applied directly to textured c-Si substrates based on the same n 1 Ωcm FZ-wafer, as shown in Fig. 1. In fact, on textured c-Si, neither do we know the intrinsic a-Si:H passivation layers thickness which is known to have a narrow optimal range [11], nor do we know whether the layer's microstructures are as-desired. In this situation, TEM and SEM, combined with lifetime measurements allow for faster process parameter optimization.

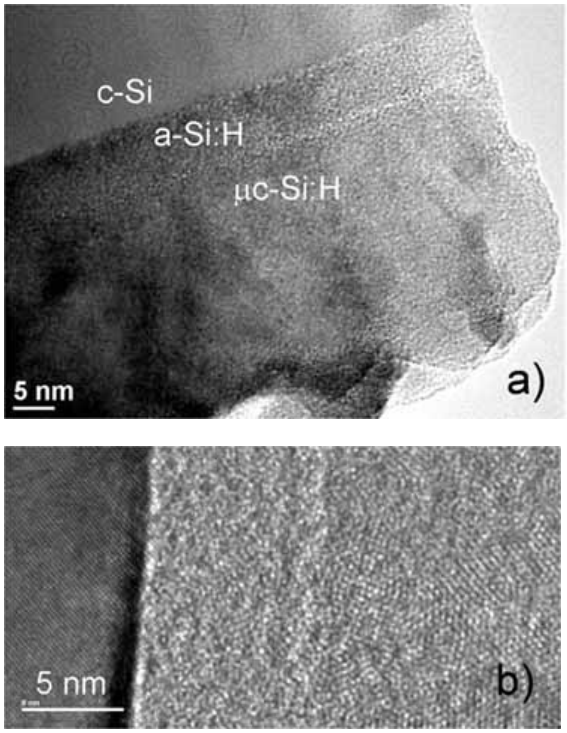

Figure 2: TEM (a) and HR-TEM (b) micrographs of i a-Si:H / p^+ μc-Si:H emitter layer stacks on flat n c-Si showing the interfaces abrupt nature that is crucial for the high performance of a-Si:H/c-Si heterostructure devices.

The fact that the device performance drops when applying identical process parameters to textured c-Si as on flat c-Si, originates firstly from the insufficient thickness of the emitter and BSF layer stacks: A too thin i a-Si:H layer passivates insufficiently the c-Si surface, whereas the insufficient deposition time of the doped layers inhibits the development of their specific microstructure and their corresponding high conductivity.

When growing our standard i a-Si:H layer on textured c-Si, we verify its directional growth by SEM micrographs, as illustrate the example in Fig. 3: To grow a thickness of 45 nm perpendicular to the surface, the deposition time needed on flat c-Si has to be multiplied by a factor of 1.7.

After adapting the deposition time of the i a-Si:H / p^+ μc-Si:H emitter layer stack, we observe abrupt (beneficial) crystallographic interfaces on the pyramidal facets, as already observed between the different layers on flat c-Si, as shown in Fig. 4a, bottom. However, in the pyramidal valley, we observe local epitaxy after the growth of the μc-Si:H on top of the a-Si:H layer. As a consequence, the crystalline interfaces become ill-defined. This is a second point that is limiting our device performance, in case textured wafers are being used. Details of the valley's structure are observed in the HR-TEM image of Fig. 4b.

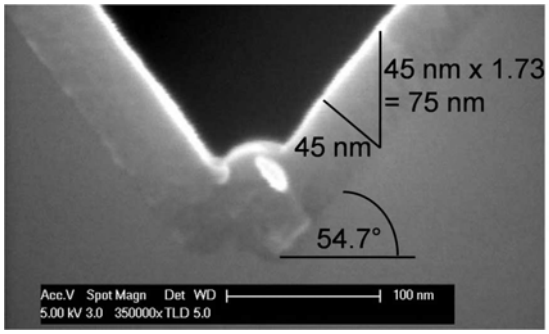

Figure 3: Measurement of a thin-film a-Si:H layer's thickness on random pyramidal textured c-Si from a SEM cross-sectional micrograph. The deposition time needed to deposit a 45 nm thick layer on such a wafer will result in a thickness of 75 nm on flat c-Si.

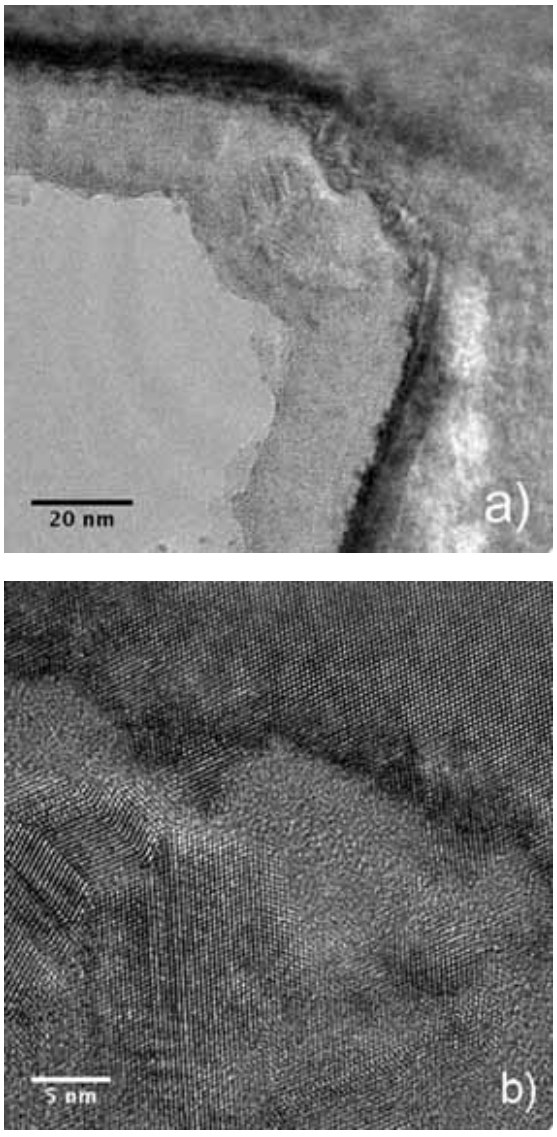

Figure 4: TEM (a) and HR-TEM (b) micrographs of i a-Si:H / p^+ μc-Si:H emitter layer stack on pyramidal textured n c-Si. One can observe local epitaxy of the a-Si:H based passivation layer at the bottom of the pyramidal valleys. Such local epitaxial regions are ill-defined crystallographic interfaces and identified here as unsatisfactory passivated spots at the a-Si:H/c-Si interface.

3.3 Effect of epitaxial growth on c-Si surface passivation

To study the effect of this local epitaxial growth at the bottom of the pyramidal valleys on final solar cell performances, we grow highly diluted (10% of silane in H_2) intrinsic a-Si:H layers (~45 nm thick) on differently oriented and textured c-Si. As observed already by other authors, epitaxial growth is detrimental for good interface passivation and occurs more easily on <100> than on <111> oriented c-Si surfaces [9,12,13].

On <111> oriented flat c-Si, we measure a lowest S_{eff} of 1 cm/s (lifetime of 7.5 ms). The corresponding abrupt nature of the a-Si:H/c-Si crystallographic interface (i.e. without any epitaxial growth) is verified by TEM (image similar to the one shown in Fig. 2b for a Si HJ solar cell on <100> oriented c-Si). On <100> oriented flat c-Si, the highly diluted i a-Si:H layer initially grows epitaxial, as shown by Fig. 5a. Corresponding measured lifetimes are more than an order of magnitude lower than the ones measured when the crystallographic interface between the layers is abrupt (Fig. 5b). That the carrier lifetime is a direct measure of the limit imposed on V_{OC} by recombination is evidenced by the drastic drop in implied V_{OC} from 710 to 600 mV. This observation is additional evidence of the detrimental effect of local epitaxial growth along the interface on the final device electrical performance.

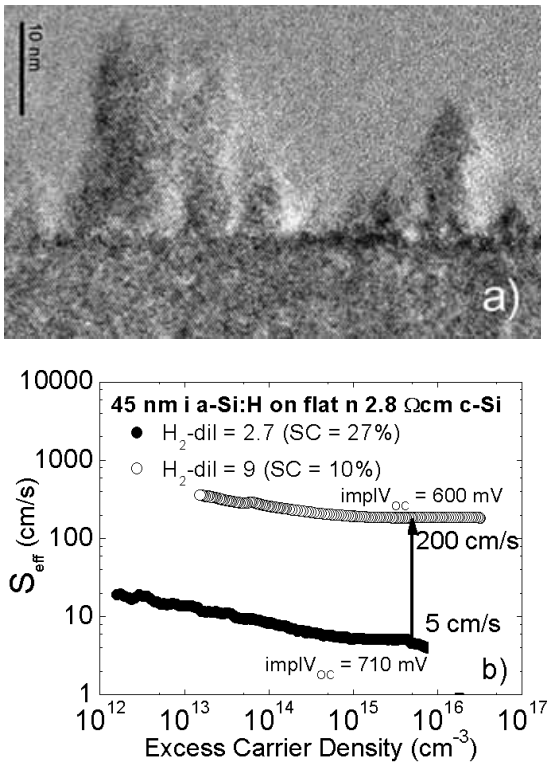

Figure 5: a) Initial epitaxial growth of a highly diluted i a-Si:H layer (10% of silane in H_2) on <100> oriented c-Si. With the same deposition conditions, on <111> oriented c-Si, the crystallographic interface between the wafer and the passivation layer is abrupt. b) Resulting increase of interface recombination rate by a factor of 40. The V_{OC} of a solar cell based on such a passivation scheme is reduced from the excellent 710 mV down to 600 mV.

On textured c-Si, the highly diluted i a-Si:H layer provides an abrupt crystallographic interface on the <111> oriented pyramid facets, as expected from the abrupt amorphous growth on flat <111> oriented c-Si, see Fig. 6. However, in the pyramidal valleys, small epitaxial structures can still be observed.

Figure 6: Growth of a highly diluted i a-Si:H layer on pyramidally textured c-Si: On the <111> oriented facets abrupt amorphous growth prevails, even if small epitaxial structures can be recognized at the bottom of the pyramidal valleys.

Compared to the standard i a-Si:H passivation (yielding on this textured wafer a very high implV$_{OC}$ of 720 mV), interface recombination is increased by a factor of 4 (resulting in a decreased implV$_{OC}$ value down to 675 mV) on this wafer.

3.4 Improvement of textured Si HJ solar cells

Lifetime measurements show that adapting the thickness of the layers forming the i a-Si:H / p$^+$ µc-Si:H emitter layer stack is sufficient to maintain a V$_{OC}$ close to that obtained with a 45 nm thick fully intrinsic a-Si:H layer passivation, see Fig. 7. As a result, it is rather the specific surface morphology of these wafers that limits the performance (implV$_{OC}$ of 680 mV) than the nature of the layer stack (provided that the p-type layer is microcrystalline).

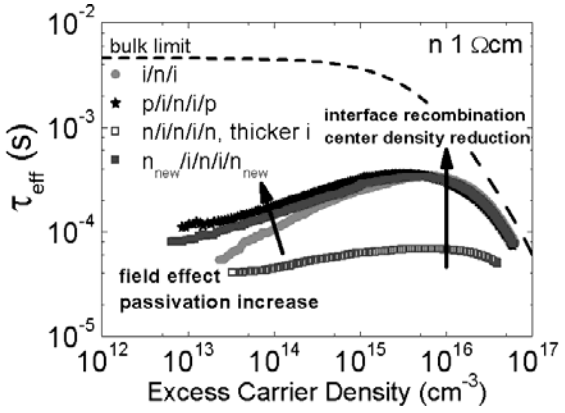

Figure 7: Symmetric intrinsic, emitter and back surface field a-Si:H based layer stack passivation.

Only the development of a new n$^+$ µc-Si:H, allowed to reach lifetimes similar as for the fully i a-Si:H passivation case.

For textured Si HJ solar cell formation, we subsequently applied the thickness adapted i/p-layer stack emitter and the texture adapted growth conditions of the n-layer in the i/n-BSF layer stack. Epitaxial growth is still moderately present in the pyramidal bottoms as shown in Fig. 4. To avoid this situation, better suited anisotropic etching conditions (instead of standard pyramidally textured c-Si) to form the random pyramids were used, by which, the detrimental influence of these epitaxized regions at the pyramidal bottoms is reduced. Thanks to these improvements a solar cell V$_{OC}$ of 660 mV is reached, as shown in the JV-characteristic of the resulting cell in Fig. 8.

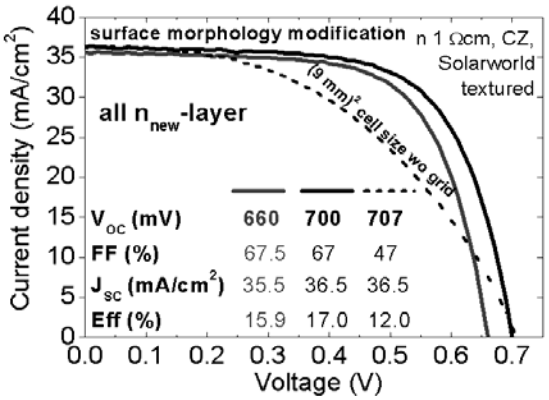

Figure 8: JV-characteristics of Si HJ solar cells based on excellently textured c-Si. In terms of interface microstructure, improved n-layer growth and additional post-texturing surface morphology modification finally yields a V$_{OC}$ over 700 mV.

Further fine-tuning of the pyramid shape allowed then for an increase in this cell efficiency by 7%, see again Fig. 8, with a V$_{OC}$ of over 700 mV.

4 DISCUSSION

In the case of single-junction µc-Si:H solar cells, it is well documented that inhomogeneous growth resulting in a sharp LP-CVD ZnO bottom texture is detrimental for the electrical performances of these thin-film Si solar cells [14]. In analogy, we observe growth inhomogeneities of the ultra-thin i a-Si:H / doped µc-Si:H layer stack in the pyramidal valleys of textured Si HJ solar cells (Fig. 4). Opposite to the case of growth problems on sharply peaked LP-CVD ZnO, we observe an epitaxial onset of the i a-Si:H passivation layer after the subsequent µc-Si:H layers deposition in the pyramidal valleys.

An epitaxial structure in the pyramid bottom is also observed when growing a highly H$_2$-diluted i a-Si:H layer of double device layer stack thickness on textured c-Si (Fig. 6). This local epitaxy and not the different surface orientation (pyramid facets are <111> oriented) is the cause of the decrease of the implV$_{OC}$ (by 45 mV), as can be concluded from the excellent passivation of the <111> oriented flat c-Si obtained by using the same a-Si:H layer. Because the intrinsic a-Si:H layer grows initially epitaxial on <100> oriented flat c-Si but fully amorphous on <111> oriented flat c-Si, under the same high H$_2$-dilution deposition conditions, one could conclude that the different crystalline orientation in the pyramidal bottom provokes epitaxial growth. But in fact,

in the pyramid valleys, one can assume the presence of a distribution of facets of different orientation (between <111> and <100>) whose effect in terms of local epitaxy is not known yet.

On flat c-Si, the best i a-Si:H layer thickness is chosen and then doped µc-Si:H layers with maximal conductivity are developed on top of this i a-Si:H layer on glass. The major factor penalizing the efficiency in our textured Si HJ solar cells is identified as the local epitaxy provoked by the subsequent doped µc-Si:H layers growth on i a-Si:H in pyramidal valleys. Thus, on textured c-Si, in first approach we search to reduce the crystallization of the i-layer resulting of the doped µc-Si:H layer's deposition, while keeping the i a-Si:H layer's thickness in its narrow optimal range. As a result, the Si HJ solar cell incorporating this newly developed n-layer and being additionally based on excellently textured c-Si has a V_{OC} of 660 mV. The newly developed n-layer induces less field effect passivation because it is less doped than the flat standard one (as can be seen by comparing the respective $\tau_{eff}(\Delta n)$-curves in Fig. 7). Thus, the origin of the textured cell's FF loss (Fig. 8) as compared to the flat solar cell (Fig. 1) can be partly explained. Finally, a surface morphology modification of the textured c-Si wafers prior to the a-Si:H based stack layer growth leads to an efficiency gain of 7%, mainly thanks to the achievement of a V_{OC} of over 700 mV.

5 CONCLUSIONS

The a-Si:H based layers optimized for the flat HJ result in low V_{OC}s when applied directly to textured c-Si. An adaptation of the passivation- and BSF-layers thickness permits in a first step to increase the V_{OC}. TEM allows identifying the predominant importance of the Si HJ's crystallographic interface. Regions of epitaxial growth of the PECVD layers are identified in the pyramid bottoms. Increased surface recombination and a lower V_{OC} of finished solar cells can be related with the observation of a non-abrupt crystallographic interface between the wafer and the passivating layer.

a-Si:H yields in fact even better passivation of <111> oriented c-Si (S_{eff} = 1 cm/s), in contrast to SiO_2 and SiN_x which are better passivating <100> oriented c-Si. In view of industrial monocrystalline Si solar cell production being based on random pyramidal structures, featuring <111> oriented facets, this is an important finding.

However, the overall passivation of random pyramids by a-Si:H is very sensitive to growth inhomogeneities in the pyramid bottoms and this imposes an improvement of the texture's quality. Further studies will be needed to clarify the role of stress and bottom orientation on local epitaxy. By reducing the amount of the resulting local recombination by *i)* improving the texture quality, *ii)* adapting the doped µc-Si:H layers growth conditions and *iii)* modifying the textured surface's morphology, we succeeded in fabricating Si HJ solar cells with open-circuit voltages exceeding 700 mV on 1 Ωcm n-type CZ c-Si.

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