Low noise, low power front-end electronics for pixelized TFA sensors

C. Ballif[3], W. Dabrowski[2], M. Despeisse[3],
P. Jarron[1], J. Kaplon[1], K. Poltorak[1,2] N. Wyrsch[3]

[1]*CERN, Geneva, Switzerland*

[2]*Faculty of Physics and Applied Computer Science, AGH University of Science and Technology, Krakow, Poland*

[3] *Ecole Polytechnique Fédérale de Lausanne, EPFL/STI, Neuchatel, Switzerland*

Outline

- Thin Film on ASIC technology
- Front-end electronics,
- Noise optimisation,
- Noise measurements,
- 405 nm blue laser results,
- Conclusions.

TFA – Thin Film on ASIC technology

→A thin film sensor layer is deposited directly on top of the ASIC,

→Sensors are made of hydrogenated amorphous silicon (a-Si:H),

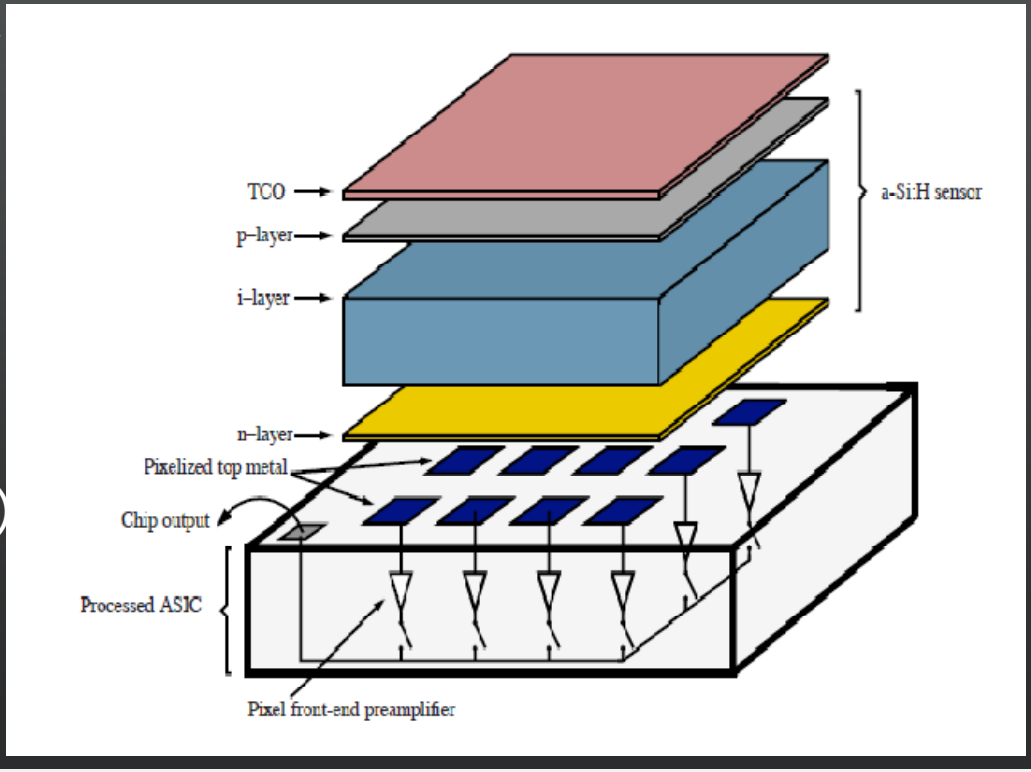
→Full chip area is covered by sensor layer,

→It does not require bump bonding,

→Low deposition temperature

(around 200 ºC) is compatible with post processing on finished electronics wafers,

→Deposition method: VHF PE-CVD (very high frequency plasma enhanced chemical vapor deposition)



Applications and requirements

→Tracking detectors for linear colliders , imaging,

→ Expected charges generated in a-Si:H sensors by MIPs are ~40e-/μm

→ 10-15 μm thick films of a-Si:H were deposited directly on the demonstrator chip (Amorphous Frame Readout Pixel - AFRP)

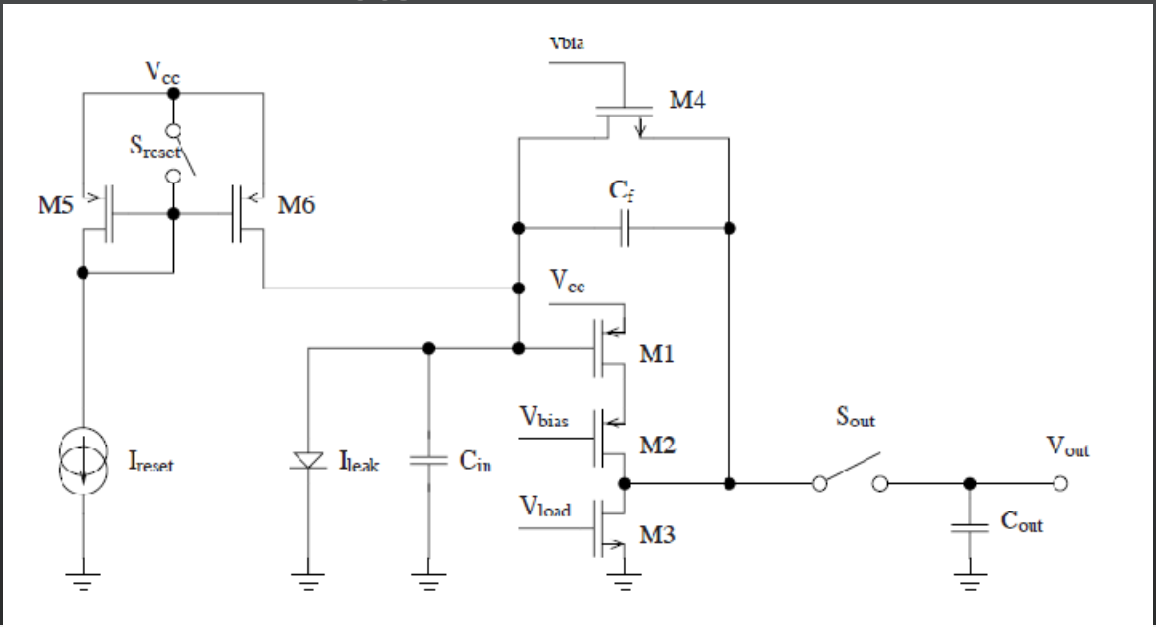
→ Pixel dimension of the demonstrator chip: 40 μm x 40 μm, input capacitance :~40fF (including detector capacitance)

→ Requirements for front end electronics:

- ✓ High gain (800mV/fC), ideally in a single stage
- ✓ Low noise (<30e- ENC), to work with signal to noise ratio
- ✓ Low power consumption (10μW/pixel).

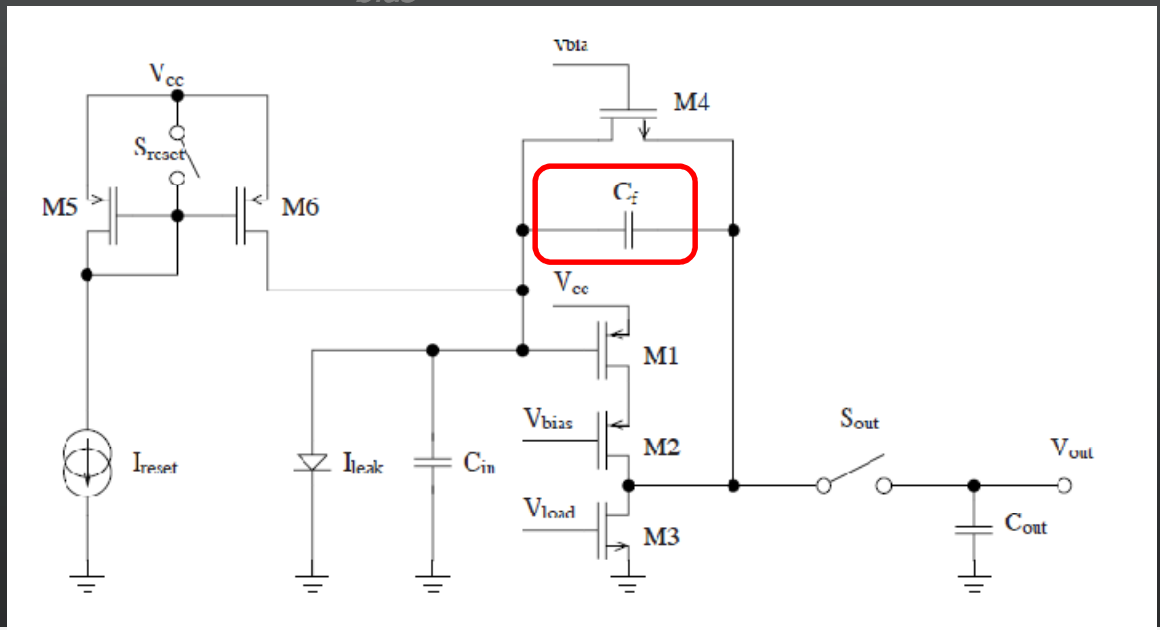
Front-end design

- Non buffered cascode stage,
- Very small feedback capacitor (1.3fF) to ensure very high gain,
- Preamplifier works as a gated integrator with gate time t_{acq} and integration time constant τ,
- Reset of the feedback capacitor is provided by the transistor M4, which is biased with constant voltage at the gate (V_{bias}),
- In the reset phase switch S_{reset} is open and the reset current is delivered to M4 in the feedback loop, In this phase the circuit operates as a transimpedance amplifier.



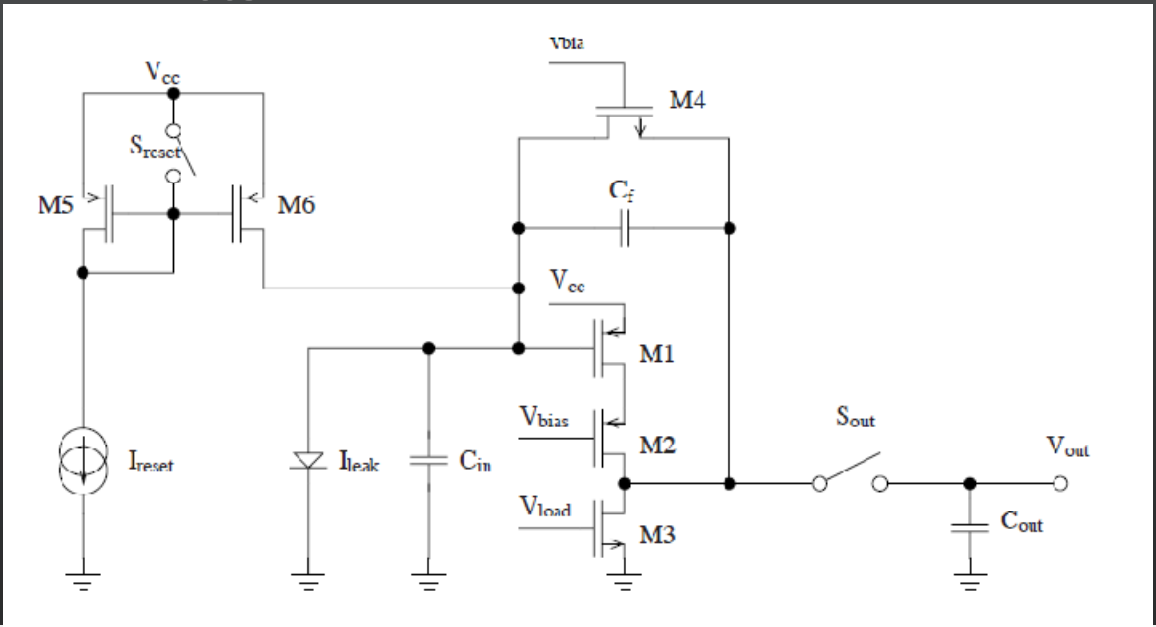
Front-end design

- Non buffered cascode stage,
- Very small feedback capacitor (1.3fF) to ensure very high gain,
- Preamplifier works as a gated integrator with gate time t_{acq} and integration time constant τ,
- Reset of the feedback capacitor is provided by the transistor M4, which is biased with constant voltage at the gate (V_{bias}),
- In the reset phase switch S_{reset} is open and the reset current is delivered to M4 in the feedback loop, In this phase the circuit operates as a transimpedance amplifier.



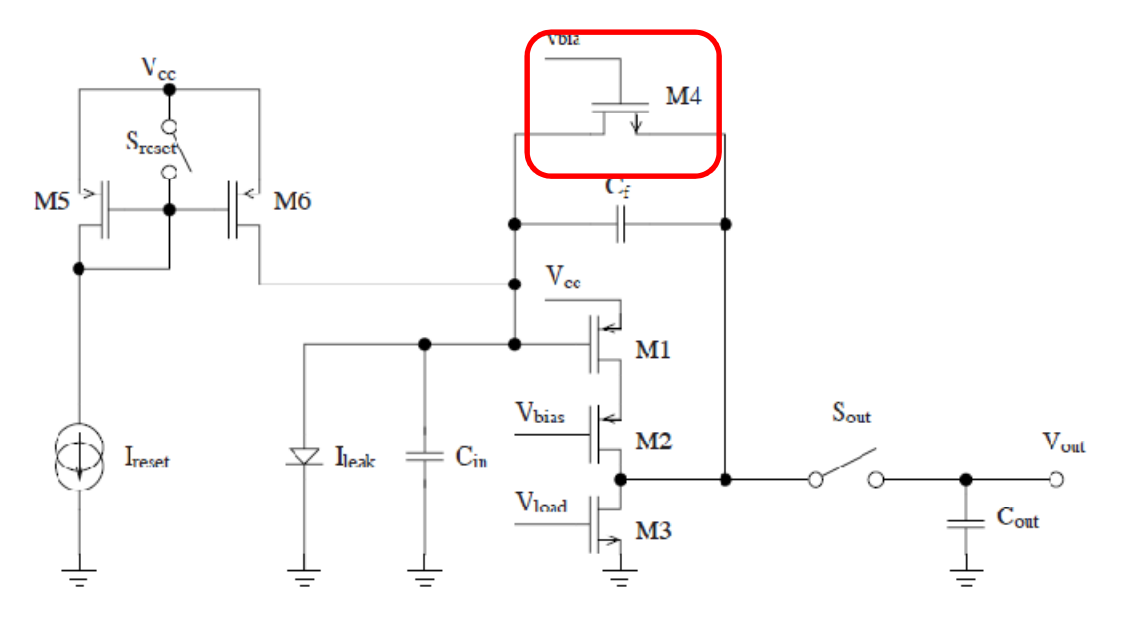
Front-end design

- Non buffered cascode stage,
- Very small feedback capacitor (1.3fF) to ensure very high gain,
- Preamplifier works as a gated integrator with gate time t_{acq} and integration time constant τ,
- Reset of the feedback capacitor is provided by the transistor M4, which is biased with constant gate voltage (V_{bias}),
- In the reset phase switch S_{reset} is open and the reset current is delivered to M4 in the feedback loop, In this phase the circuit operates as a transimpedance amplifier.



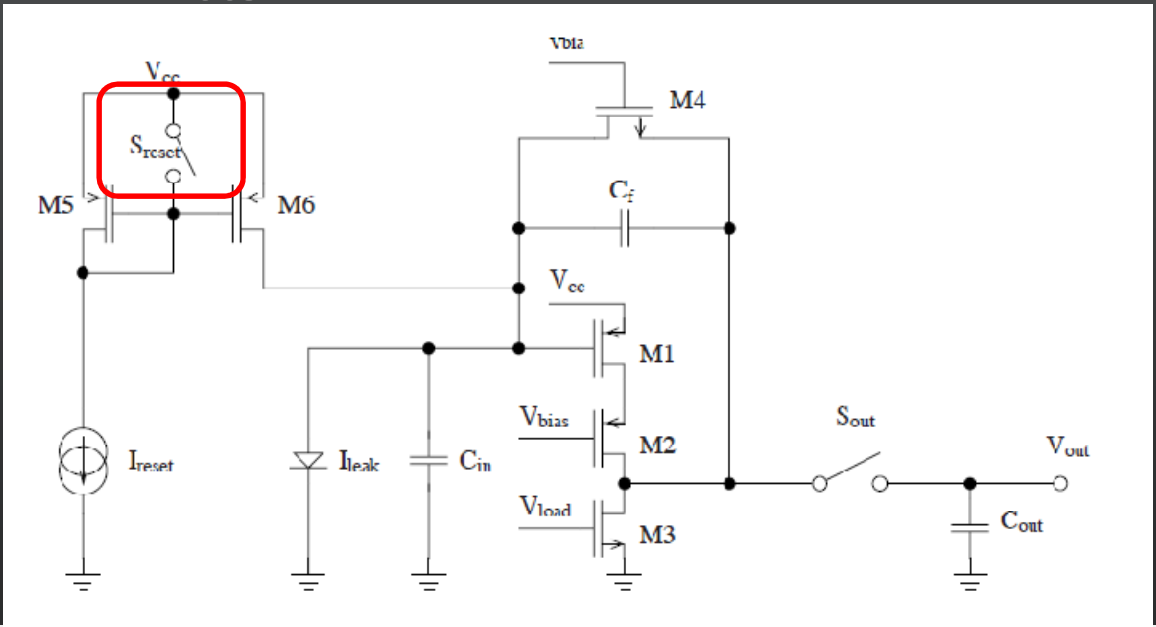
Front-end design

- Non buffered cascode stage,
- Very small feedback capacitor (1.3fF) to ensure very high gain,
- Preamplifier works as a gated integrator with gate time t_{acq} and integration time constant τ,
- Reset of the feedback capacitor is provided by the transistor M4, which is biased with constant gate voltage (V_{bias}),
- In the reset phase switch S_{reset} is open and the reset current is delivered to M4 in the feedback loop, In this phase the circuit operates as a transimpedance amplifier.



Front-end design

- Non buffered cascode stage,
- Very small feedback capacitor (1.3fF) to ensure very high gain,
- Preamplifier works as a gated integrator with gate time t_{acq} and integration time constant τ,
- Reset of the feedback capacitor is provided by the transistor M4, which is biased with constant gate voltage (V_{bias}),
- In the reset phase switch S_{reset} is open and the reset current is delivered to M4 in the feedback loop, In this phase the circuit operates as a transimpedance amplifier.

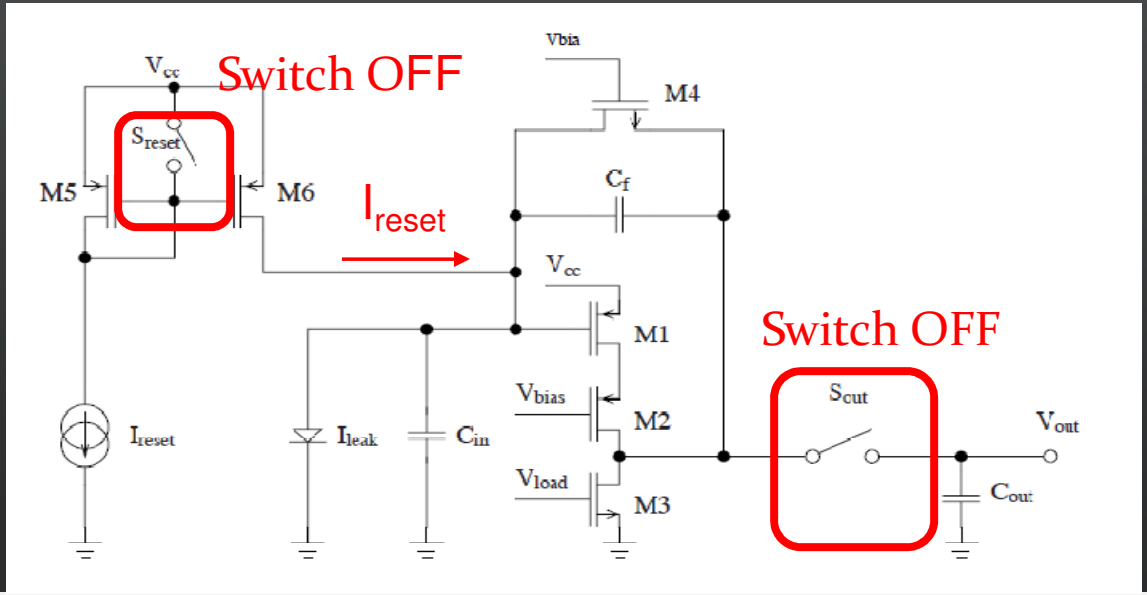


Operation sequence

[1] Reset phase – feedback capacitor is discharged through transistor M4 biased with a constant reset current I_{reset} (this design ensures lower parasitic injection from the reset signal to the 1.3fF feedback capacitor in comparison with a voltage controlled reset transistor),

[2] Acquisition phase – the input signal is integrated on feedback capacitor C_f and stored on C_{out} while switch S_{out} is closed. The acquisition time t_{acq} is much longer than integration time constant τ,

[3] Readout phase –data are read out from 4096 pixels "frame by frame" by a serial multiplexer.

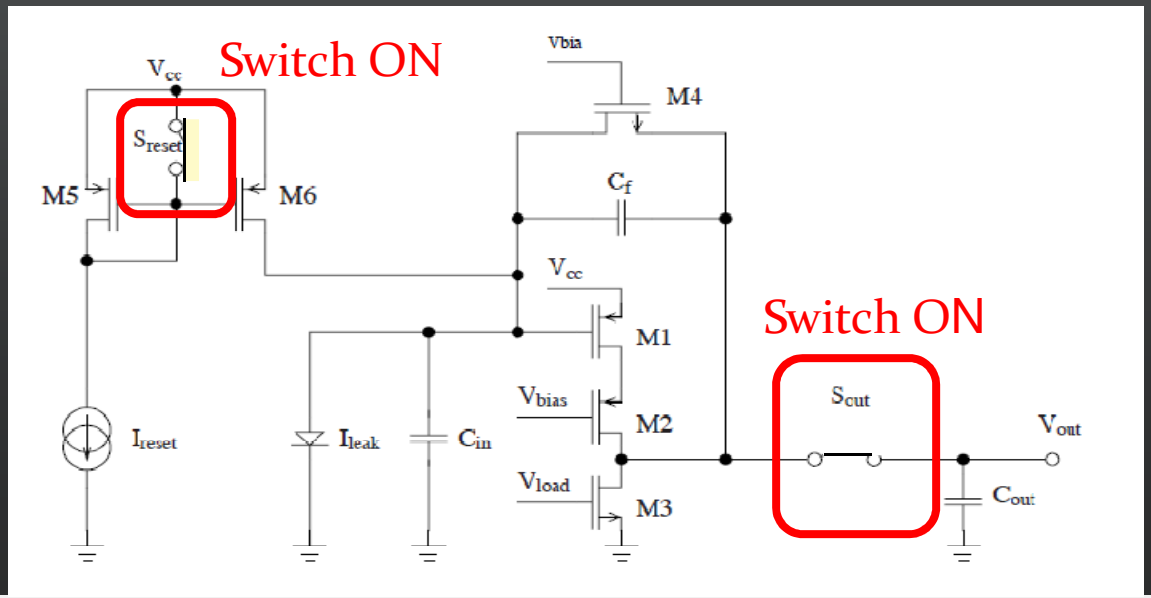


Operation sequence

[1] Reset phase – feedback capacitor is discharged through transistor M4 biased with a constant reset current Ireset (this design ensures lower parasitic injection from the reset signal to the 1.3fF feedback capacitor in comparison with a voltage controlled reset transistor),

[2] Acquisition phase – the input signal is integrated on feedback capacitor C_f and stored on C_{out} while switch S_{out} is closed. The acquisition time t_{acq} is much longer than integration time constant τ,

[3] Readout phase –data are read out from 4096 pixels "frame by frame" by a serial multiplexer.

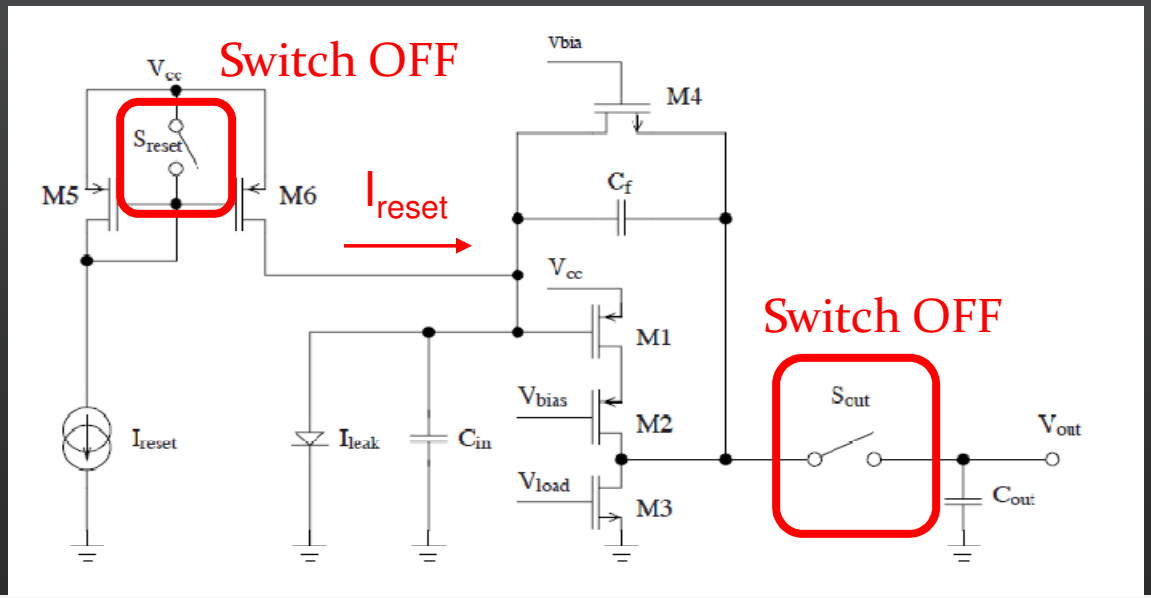


Operation sequence

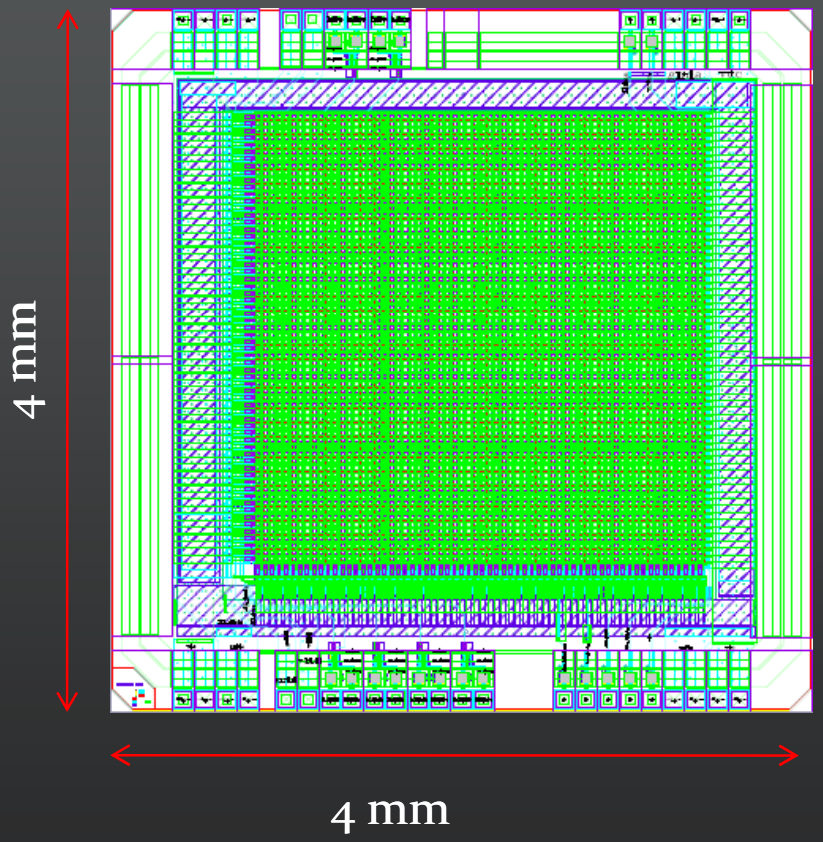
[1] Reset phase – feedback capacitor is discharged through transistor M7 biased with a constant reset current I_{reset} (this design ensures lower parasitic injection from the reset signal to the 1.3fF feedback capacitor in comparison with a voltage controlled reset transistor),

[2] Acquisition phase – the input signal is integrated on feedback capacitor C_f and stored on C_{out} while switch S_{out} is closed. The acquisition time t_{acq} is much longer than integration time constant τ,

[3] Readout phase –data are read out from 4096 pixels "frame by frame" by a serial multiplexer.



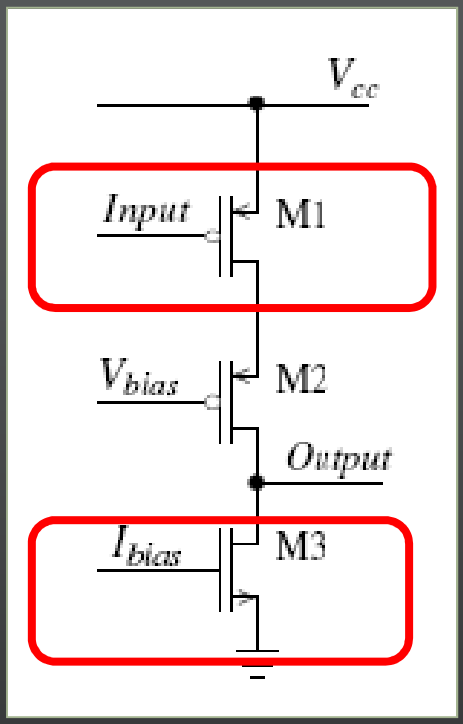
Demonstrator chip



- Matrix of 64x64 pixels,
- Pixel size: 40 µm x 40 µm,
- Analog and digital grounds and power supply busses are separated to reduce the noise in the preamplifier,
- Two clock signals to read out rows and columns of the chip,
- Master readout clock set to 10 MHz,
- Readout time: ~2.5 ms (600ns/pixel),
- The AFRP1 chip was designed and manufactured in 0.25 µm CMOS process.

Expected noise in the acquisition phase

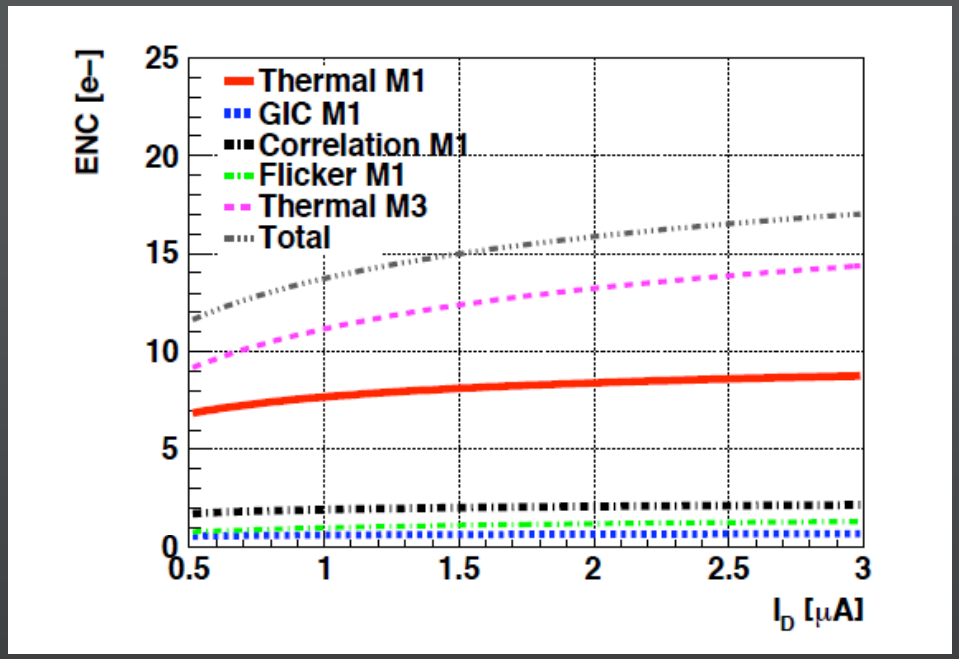
- Noise from the cascode transistors M1 and M3,
- Noise calculated employing the EKV model (the following noise terms are taken into account: thermal noise, gate inducted current noise, correlation term, and the flicker noise),
- The overall signal shaping function $K_{readout}$ of the preamplifier is equivalent to $K_{int}(f) \bullet K_{gate}(f)$



$$K_{readout}(f) = K_{\text{int}}(f)K_{gate}(f) = \frac{1}{1+(2\pi f\tau)} \frac{2ft_{gate}}{\sqrt{1+(2ft_{gate})^2}}$$

- The integration time constant τ depends on the bandwidth of the un-buffered cascode stage, which is loaded with the input, output and the feedback capacitance.

Expected noise in the acquisition phase



ENC as a function of bias current t_{acq}=1 μs, $C_{int}=C_f+C_{in}+C_{g1}$= 40fF, C_{out}=120fF.

• The channel thermal noise of load (M3) and input (M1) transistors dominates:

$$ENC_{thermal} = \frac{1}{2\sqrt{\pi\frac{\tau_i^2}{t_{samp}}+\tau_i}}\sqrt{\frac{4kT n\gamma}{g_m}}(C_{in}+C_f+C_{g1})\frac{1}{q},$$

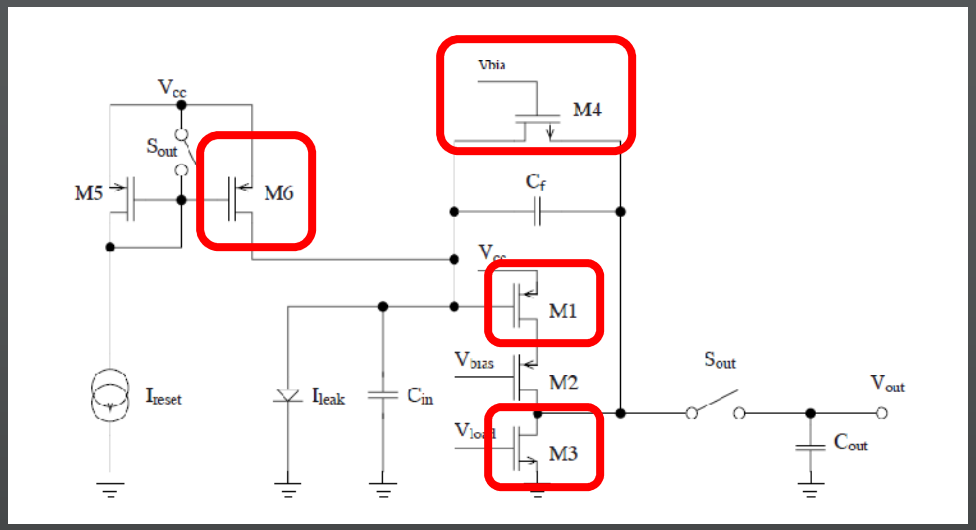
• For un-buffered cascode τ depends on C_{int}, C_f and C_{out} capacitances as well as on gm1 of the input transistor M1 and gds3 of the load transistor M3:

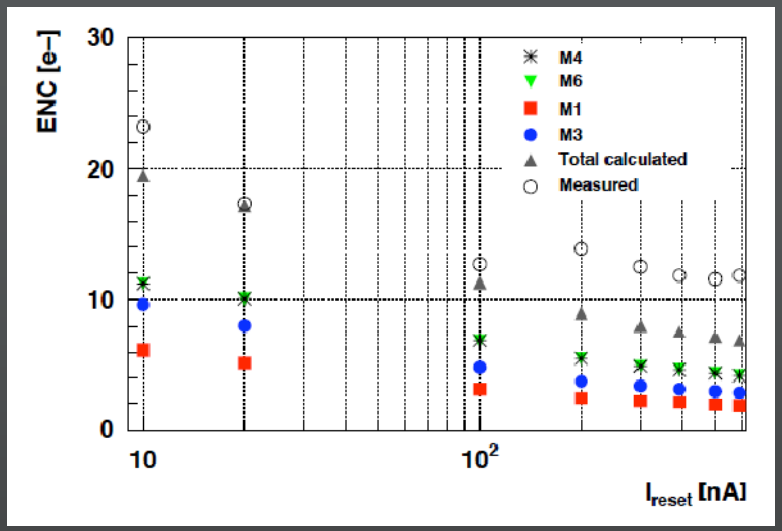
$$\tau = \frac{C_{int}C_{out} - C_f(C_{int}+C_{out})}{-C_{int}g_{ds3} + C_f(g_{ds3}+g_{m1})},$$

•<u>The noise is expected to be below 18 e- ENC</u>,

• I_D has been chosen to optimize the power consumption and integration time constant τ, which limits minimum acquisition time t_{acq}.

Expected noise in the reset phase



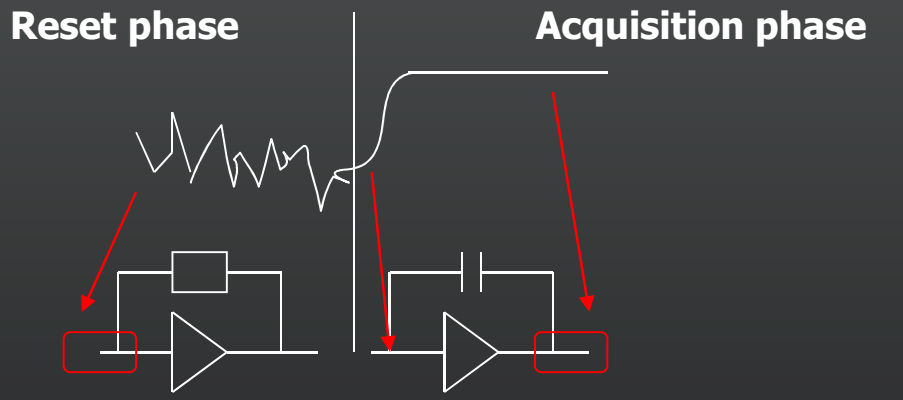


- Preamplifier in the reset mode works as a transimpedance amplifier with parallel noise sources from feedback transistor M4, reset transistor M6, as well as cascode transistors M1 ans M3.
- The dominating noise is the channel thermal noise,
- Theoretical estimation agrees quite well with measurements performed in the reset phase
- This result might suggest that higher values of the reset current are preferable.

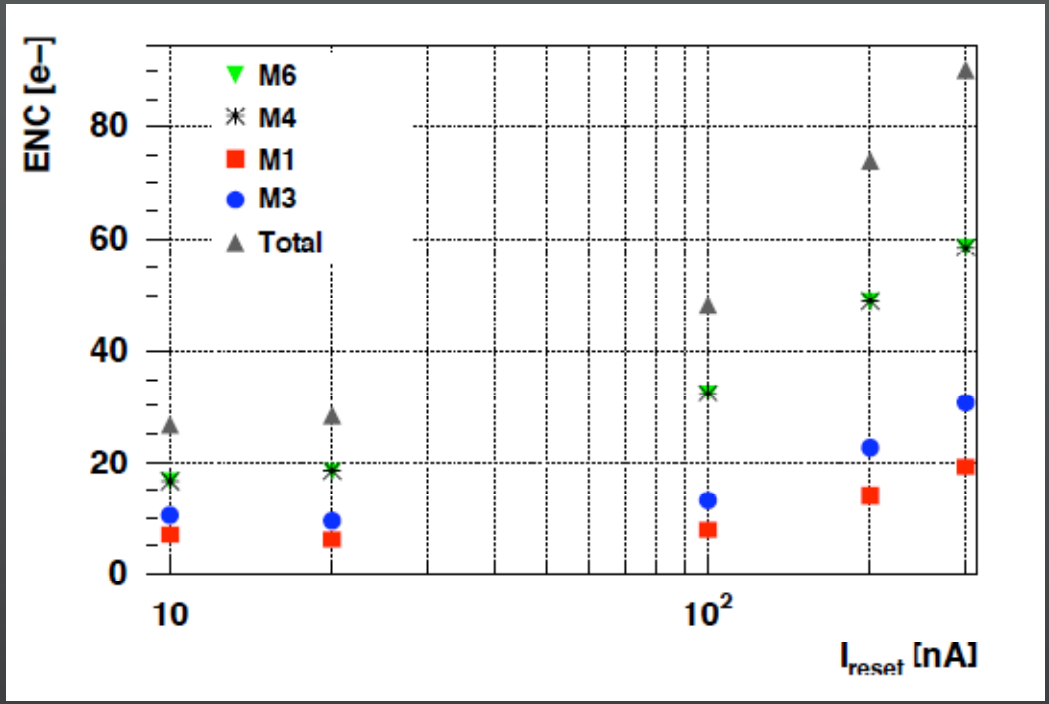
Reset noise seen in the acquisition phase

Preamplifier transfer functions changes between the reset phase and the acquisition phase. To evaluate noise in the frequency domain we use the following approximation:

- Output noise in the reset is fed back to input, sampled during switching to acquisition phase, and then amplified with acquisition phase gain,
- Ratio $K = K_{vacq}/K_{vres}$ is introduced to estimate contribution of the reset noise in the acquisition phase.



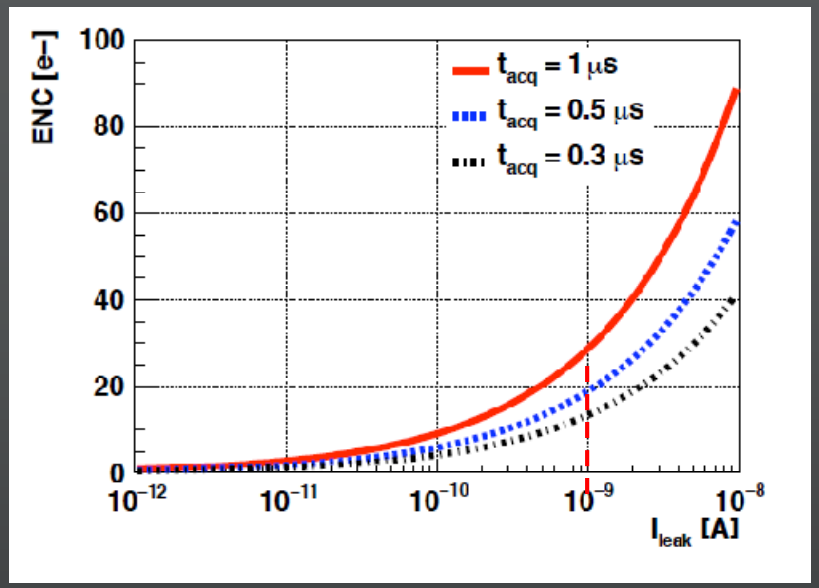
Reset noise seen in the acquisition phase



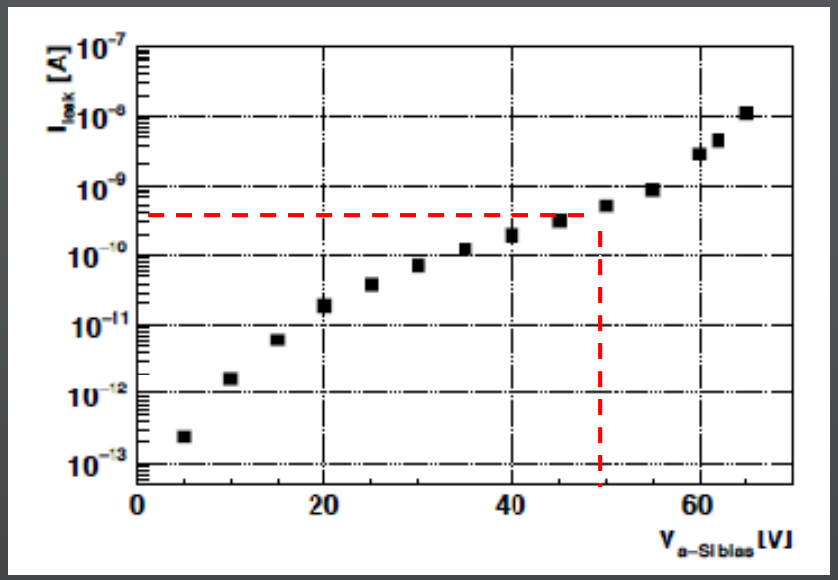
ENC as a function of the reset current *in the acquisition phase*

- The noise originating from the reset phase increases for higher reset currents,
- For reset current of 10 nA, reset noise, seen in the acquisition phase is estimated be below 28 e- ENC.

Noise from the detector leakage



Calculated noise originating from a-Si diode.



Measured leakage current per pixel

- Increasing the acquisition time (t_{acq}) increases contribution of the parallel noise from detector leakage current,
- For given τ, t_{acq} should be longer than τ,
- This puts some constraint on τ, which affects the preamplifier design,
- The measured average leakage current per pixel on a-Si:H sensors bias with 55V is around 1 nA, what indicate the expected noise related to this noise source below 30 e- ENC.

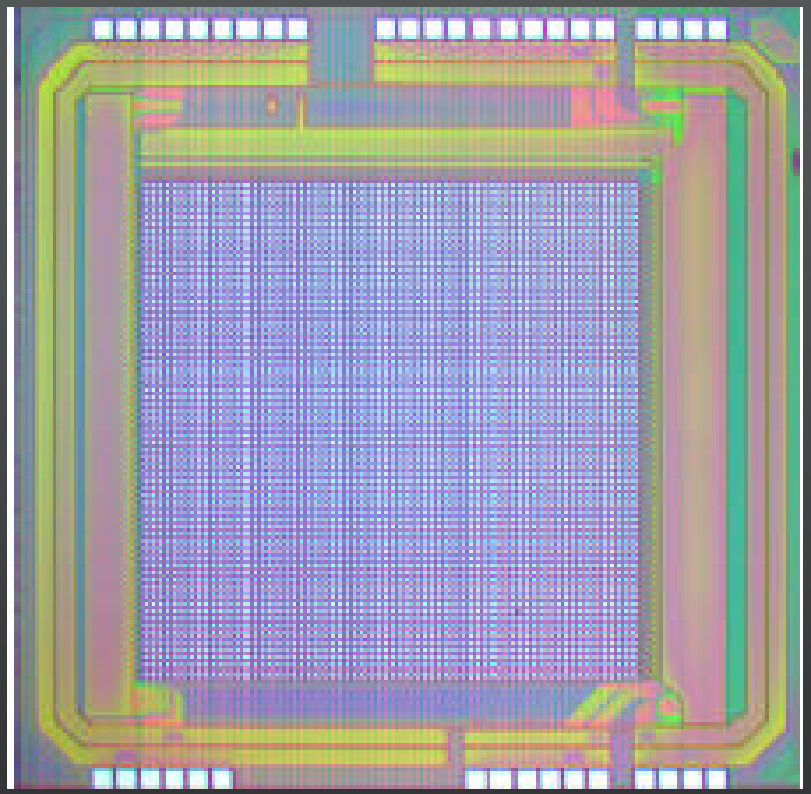
Measurement results

- The noise was measured in the acquisition phase on:
  → bare AFRP1 chip,
  → TFA structure with 10 μm a-Si diode deposited on top,

- Measured noise is compared with calculations

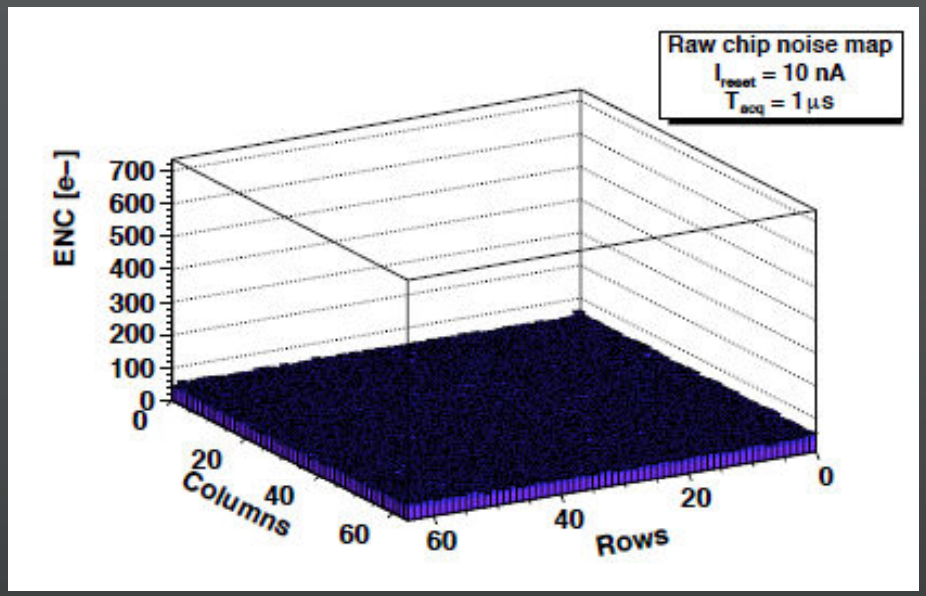
Test set-up

- NI PCI-6562 high speed digital input output card with LVDS signaling :
  - 200 MHz maximum clock rate,
  - 16 channels with per-channel direction control in single-data-rate mode.
- NI 5112 oscilloscope card,
- Labview environment
- Analyses made in ROOT environment (http://root.cern.ch).

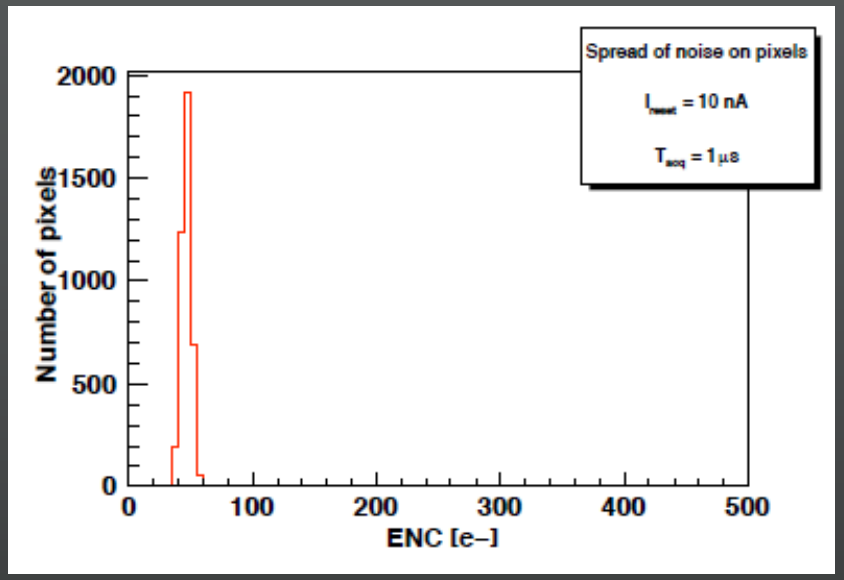


Test results – bare chip

AFRP1 chip noise map

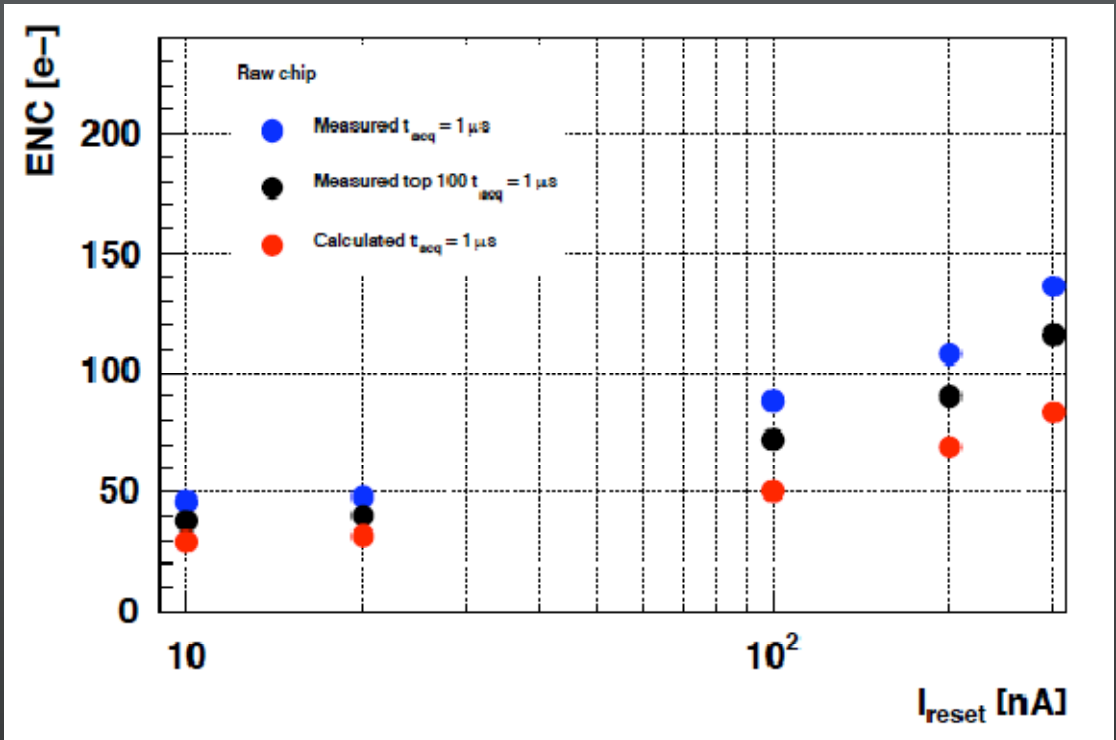


Distribution of noise on the chip



The noise of redadout pixels with open inputs is very uniform across the whole chip.

Test results – bare chip

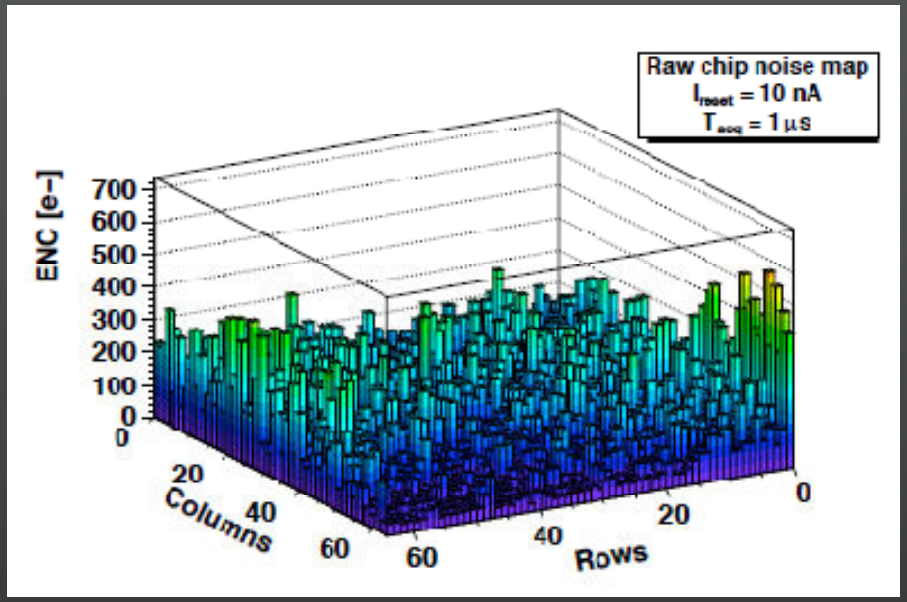


Measured ENC taken as the most probable noise over 4096 pixels

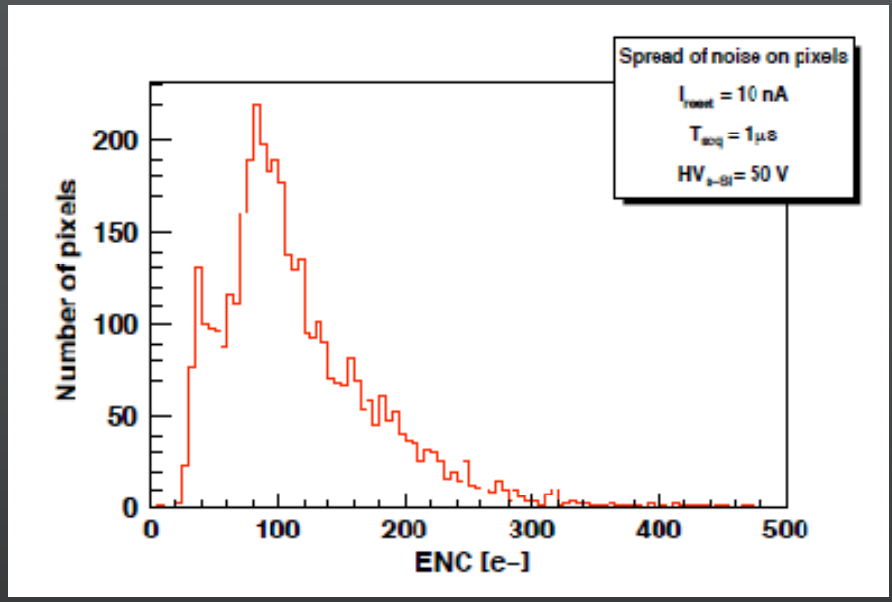
- Measured noise is slightly higher compared to calculations.
- Taking into account top 100 pixels with the best noise performance, the most probable noise is below 40 e- ENC

Noise performance – TFA

Noise map



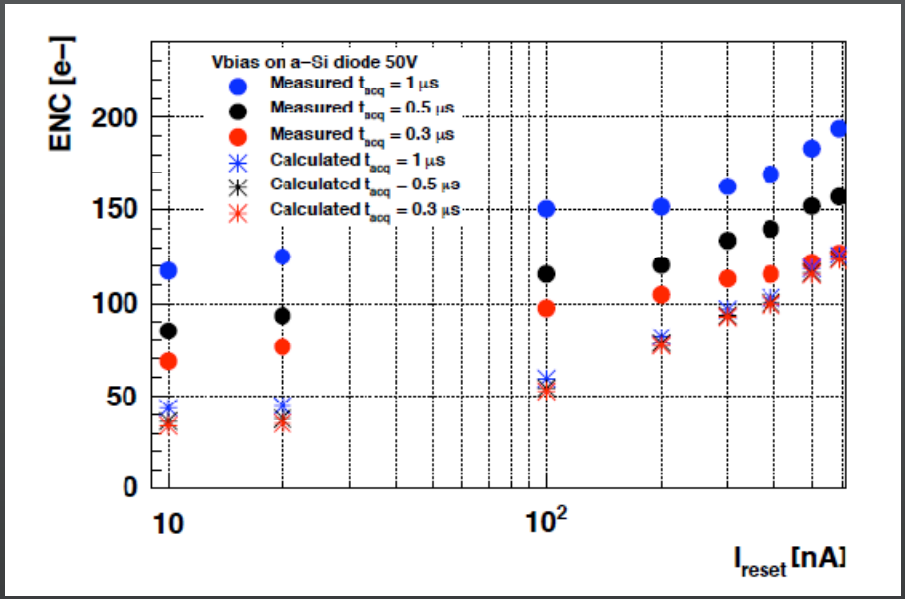
Distribution of noise on the chip



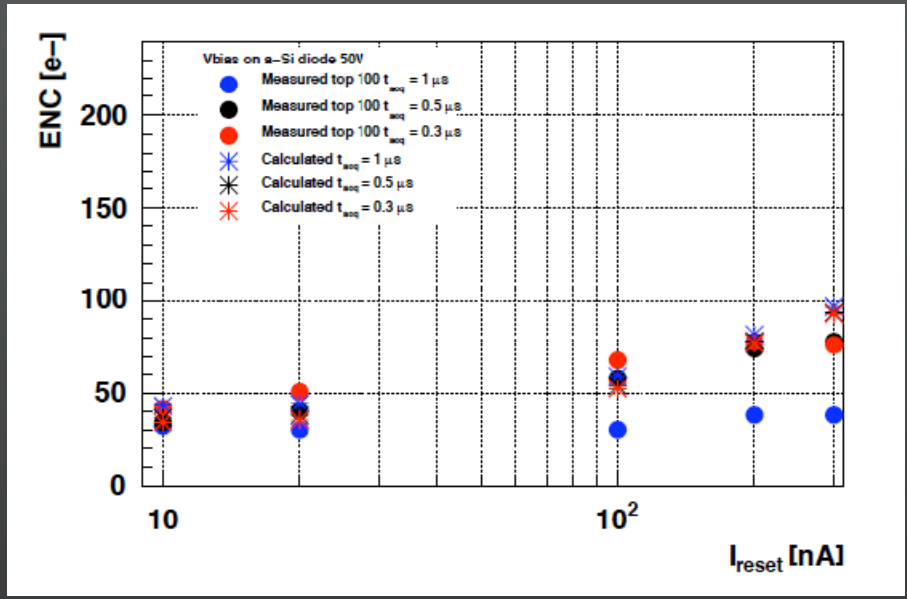
- Measured noise is significantly higher than expected
- We observe very large spread of noise across the chip.

Noise performance – TFA

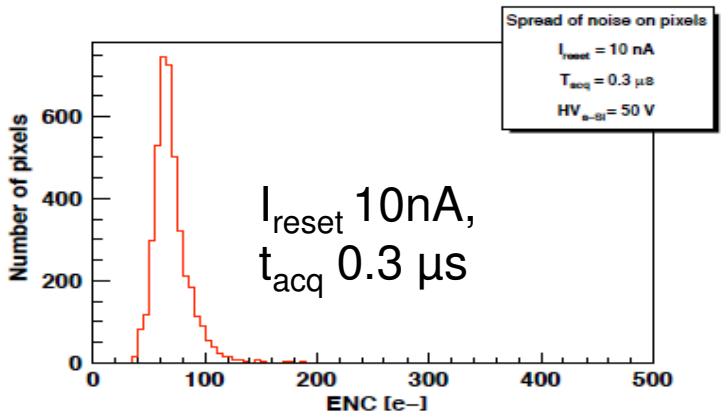
Measured ENC taken as the most probable noise over 4096 pixels

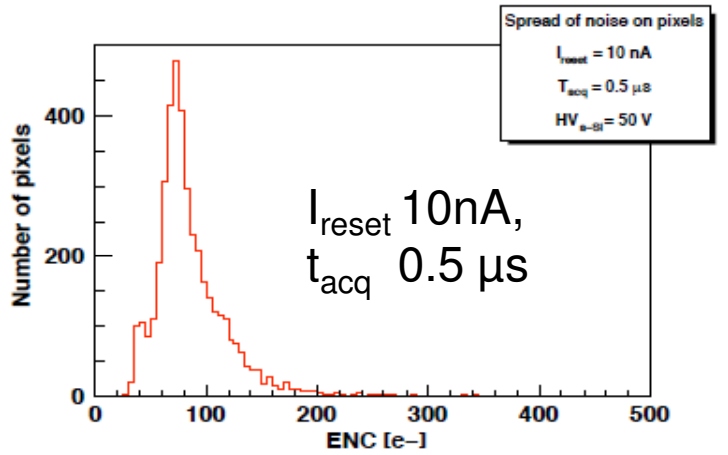


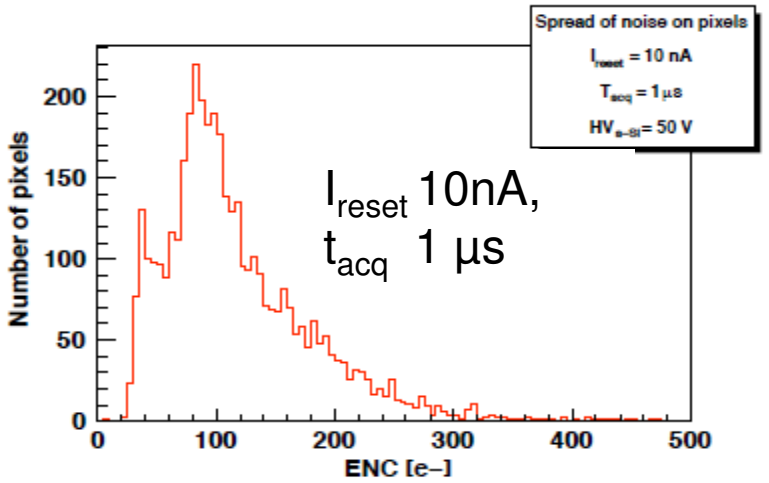
Measured ENC taken as the most probable noise over 100 pixels



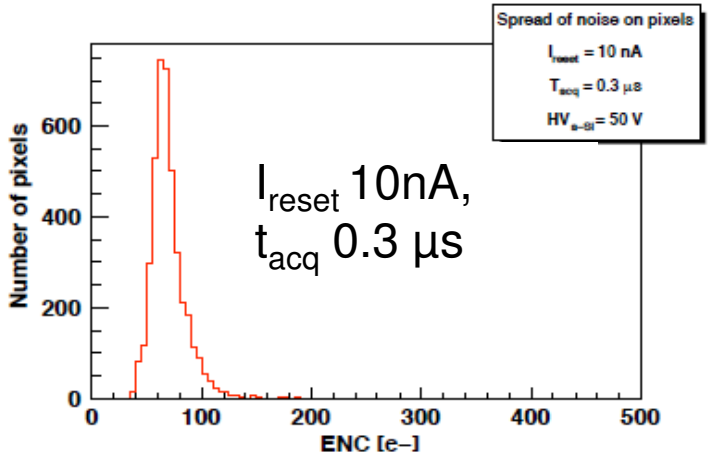
- 100 top pixels with the best noise performance are much closer to calcultions
- The noise stays below 48 e- ENC for parameters I_{reset} of 10 nA and t_{acq} of 0.3 µs,

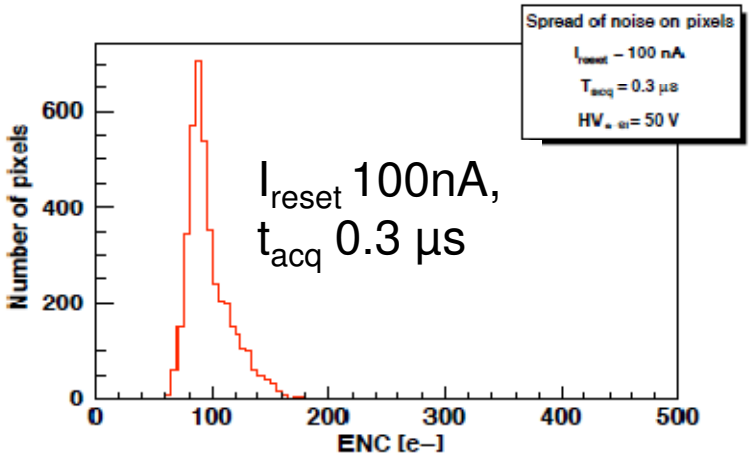


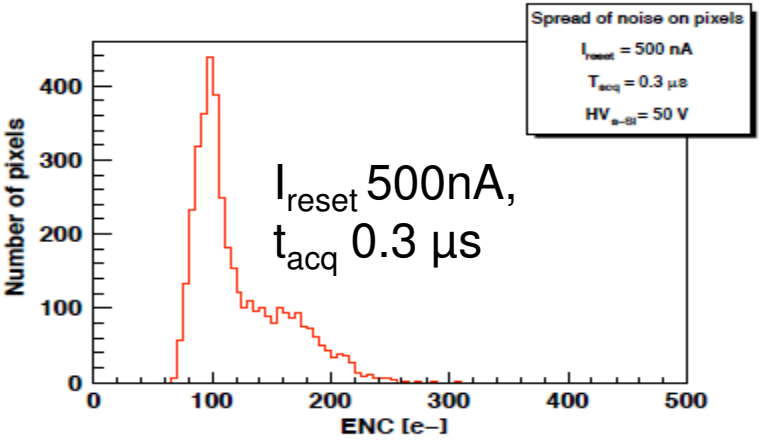




Distribution of the ENC across 4096 pixels for reset current of 10 nA and different acquisition times





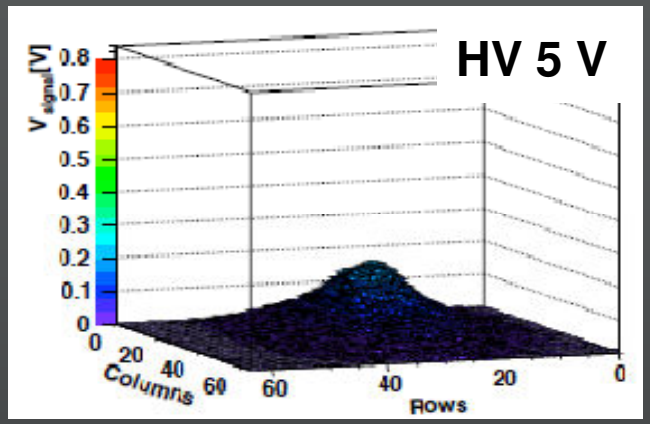


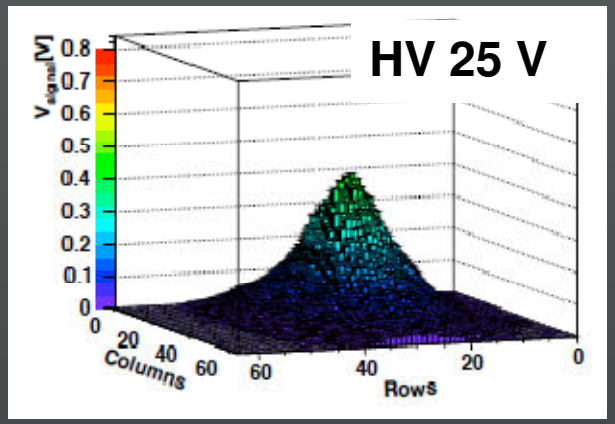
Distribution of the ENC across 4096 pixels for acquisition time of 0.3 µs and different reset currents

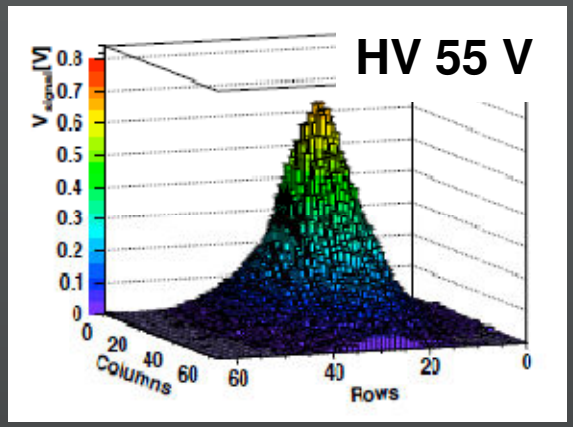
Calibration

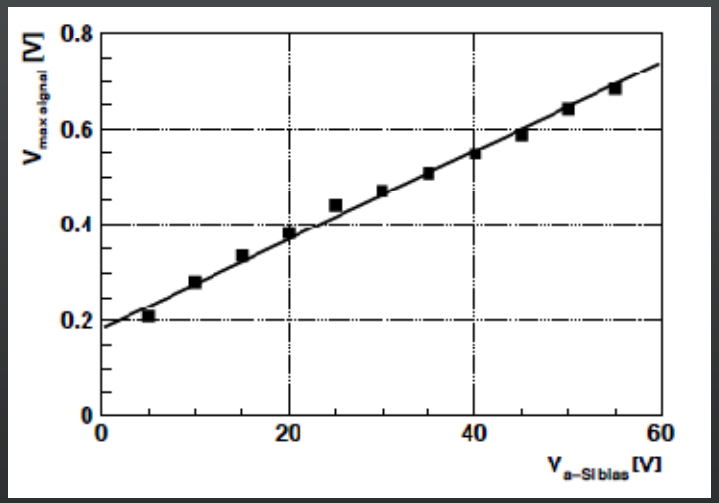
- No calibration capacitor was implemented on the citcuit in order to keep the noise at low level,
- Calibration with the radiation sources (Fe-55, Sr-90) is difficult due to very high a-Si diode leakage current (t_{acq} too short to collect acceptable hits statistics),
- The TFA structure was calibrated with a 405 nm blue laser by comparison to TFA structure based on MacroPad chip measured gain: 713 mV/fC (designed value: 800 mV/fC).

405 nm blue laser tests









- According to [1] the full depletion bias voltage for a-Si sensor is defined as: $Vd = 0.48\ d^2 = 48V$ for 10μm thick diode,
- The signal from the blue laser, measured on TFA structure based on AFRP1 chip, does not increase for bias voltages above 55 V.

[1] M. Despeisse et al.**Hydrogenated Amorphous Silicon Sensor Deposited on Integrated Circuit for Radiation Detection**, IEEE Transactions On Nuclear Science, Vol. 55, No. 2, 2008, pp. 802-811.

Conclusions

- Noise performance:
  - ✓ The calculated reset noise behavior, as a function of I_{reset}, agrees quite well with the measurement results
  - ✓ Discrepancy in total noise level can be attributed to parasitic capacitance in the preamplifier structure
  - ✓ The best noise performance was obtained for the reset current of 10 nA. For acquisition times 300 – 500 ns the noise of TFA structure is below 48 e- ENC
  - ✓ At present noise performance is limited by the sensor leakage crrent
- High a-Si diode leakage current makes the calibration with radiation source difficult because achievable rates ara low and require long acquisition times
- The TFA structure was calibrated with a 405 nm blue laser by comparison to TFA structure based on Macro Pad chip. As a result the gain of 713 mV/fC was found