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RESEARCH ARTICLE

Microcrystalline silicon solar cells: effect of substrate temperature on cracks and their role in post-oxidation

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ABSTRACT

Microcrystalline silicon (μc-Si:H) cells can reach efficiencies up to typically 10% and are usually incorporated in tandem micromorph devices. When cells are grown on rough substrates, ''cracks'' can appear in the μc-Si:H layers. Previous works have demonstrated that these cracks have mainly detrimental effects on the fill factor and open-circuit voltage, and act as bad diodes with a high reverse saturation current. In this paper, we clarify the nature of the cracks, their role in post-oxidation processes, and indicate how their density can be reduced. Regular secondary ion mass spectrometry (SIMS) and local nano-SIMS measurements show that these cracks are prone to local post-oxidation and lead to apparent high oxygen content in the layer. Usually the number of cracks can be decreased with an appropriate modification of the substrate surface morphology, but then, the required light scattering effect is reduced due to a lower roughness. This study presents an alternative/complementary way to decrease the crack density by increasing the substrate temperature during deposition. These results, also obtained when performing numerical simulation of the growth process, are attributed to the enhanced surface diffusion of the adatoms at higher deposition temperature. We evaluate the cracks density by introducing a fast method to count cracks with good statistics over approximately 4000 μm of sample cross-section. This method is proven to be useful to quickly visualize the impact of substrate morphology on the density of cracks in microcrystalline and in micromorph devices, which is an important issue in the manufacturing process of modules. Copyright © 2010 John Wiley & Sons, Ltd.

KEYWORDS

microcrystalline silicon; cracks; oxygen; post-oxidation; temperature; SIMS; nano-SIMS; SEM; TEM

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1. INTRODUCTION

Microcrystalline silicon (μc-Si:H) can be used for single junction thin film solar cells that reach confirmed efficiency up to 10.1% [1]. However, its major use is in micromorph tandem cells, which consist in a stacked of amorphous and microcrystalline cells [2] which can reach stabilized efficiencies above 11% [3,4]. In μc-Si:H cells, zones of porous material, called thereafter cracks, appear typically when the device is deposited on substrates with V-shape morphology (i.e., sharp and steep valleys) [5–8], as is usually needed to achieve good light trapping properties. The same effects also appear in micromorph devices as will also be shown here, and can be a severe limitation to the final module performances. Hence, further increase of the conversion efficiency of the solar cells containing a μc-Si:H sub-cell component [9,10] over 12 or 13% stabilized efficiency will require a careful management of such detrimental features in the devices.

Although ''cracks'' have been reported in the past by several authors [11–14], their full role in limiting the device performance has only been evidenced recently [15–18]. In our laboratory, μc-Si:H p–i–n solar cells are deposited on glass covered by low pressure chemical vapor deposition zinc oxide (LPCVD ZnO), which possesses a natural texture, with as-grown pyramids at the surface, exhibiting typically a V-shape structure [19,20]. Depending on the transparent conductive oxide (TCO) growth process conditions and on the ''sharpness'' of the V-shapes, such as TCO surface morphology, can lead to severe degradation of the performances of μc-Si:H solar cells, as those are particularly sensitive to cracks that appear in the

intrinsic layer because of the V-shape. As already demonstrated in previous works [15,16], these cracks have mainly detrimental effects on the fill factor (FF) and open-circuit voltage (V_{oc}), and act as bad diodes with a high reverse saturation current. In Ref. [17] the creation of defects is attributed, based on numerical model of the layer growth, to shadowing effect and to the poor diffusion length of the adsorbed precursors.

An existing approach to decrease crack density is to modify the surface morphology from V-shape to U-shape by applying a surface treatment [14,21]. However, the surface treatment decreases the light scattering capabilities of the LPCVD ZnO [22] because of the change in morphology.

In this work, we demonstrate, with the help of a simulation program described in details in Refs. [16,17] that an increase in diffusion length during the deposition should lead to a decrease of the number of cracks in the film. Such a decrease can be experimentally verified when increasing the substrate temperature during the deposition of the intrinsic layer. The increase of substrate temperature enhances the diffusion length of precursors at the surface of the growing layer. The shadowing effect due to surface morphology is then lowered, because the particles can more easily reach, e.g., the bottom of the pyramids. Other consequences of the increase in temperature (increase in crystallinity, decrease in open-circuit voltage (V_{oc}), and increase in FF) are presented and justified. The influence of substrate temperature on μc-Si:H was partially studied in Ref. [23] but the reason why the substrate temperature increases the performances of the resulting solar cells was not completely explained. In this paper, a substrate temperature series for intrinsic layer (p- and n-layers were deposited at the same temperature, 200°C) was prepared on identical ZnO layers. An extensive characterization was performed with the help of electrical and optical characterizations (current density–voltage $J(V)$ measurement, external quantum efficiency, Fourier transform photocurrent spectroscopy (FTPS), micro-Raman spectroscopy) and electron microscopy.

Several results of the study were acquired using an original and fast method for counting cracks, based on scanning electron microscopy (SEM) observation, which was developed and used in this work and called hereafter ''1 face polishing.'' This method, which is presented here, avoids the complex preparation for transmission electron microscope (TEM) samples [24]. Moreover, the observable area is 4000 μm wide instead of 40–50 μm for a standard TEM sample.

Finally, secondary ion mass spectrometry (SIMS) measurements show that oxygen concentration is higher in solar cells containing more cracks. With the preparation method: ''1 face polishing,'' an analysis of chemical content of the cross-section of solar cells has been performed with nano-SIMS experiment. Even if dopants (boron or phosphine) have not been observed in the p- or n-layer, respectively, this experiment shows univoquely that cracks contain more oxygen than the bulk dense device grade material used for μc-Si:H solar cells.

2. SAMPLE FABRICATION, CHARACTERIZATION, AND METHOD FOR COUNTING CRACKS

The substrates were prepared by depositing a 5 μm thick LPCVD-ZnO layer, from a vapor–gas mixture of water, diethyl-zinc, and diborane [25], on an AF45 glass substrates from Schott. Thanks to the versatility of the LPCVD process, the growth conditions could be chosen to give initially sharp V-structures. The surface morphology was subsequently modified by applying a plasma surface treatment (as in Ref. [14]) on the ZnO layers for 40 and 60 min. As previously mentioned, this treatment allows for morphologies ranging from V-shape (initial) to U-shape (with treatment). μc-Si:H single junction solar cells were deposited on these substrates in a small area plasma-enhanced chemical vapor deposition (PECVD) reactor, working at very-high excitation frequency (VHF) [14,26]. The thickness of the μc-Si:H intrinsic layer is approximately 1.8 μm. The deposition of μc-Si:H was performed in p–i–n structure with the same p-layer and n-layer for every cell and intrinsic layers were deposited at different substrate temperatures (controlled by the electrode temperature) from 170 to 270°C in order to compare the influence of the substrate temperature on both electrical performances and crack density. A second series was prepared to verify the influence of the crystallinity on the crack density at constant deposition temperature. This μc-Si:H solar cells series, deposited on LPCVD ZnO treated 20 min, was prepared at various silane concentrations (i.e., the flux of silane divided by the total gas flux) from 5.2 to 6.9% for the intrinsic layer by increasing the silane flow.

Cracks can be observed by TEM and appear as a white line in bright field mode, slightly under-focused, as presented in Figure 1a. Solar cell samples for TEM can be prepared by ion milling [27], wet polishing (tripod method) [24], or focused ion beam (FIB) [28]. Nevertheless, preparation for TEM samples is complex and time consuming. In order to estimate the density of cracks, another, easier and faster sample preparation method is presented below. With this method, SEM is sufficient for observation. The procedure is inspired from the TEM sample preparation with tripod from Benedict *et al.* [24] and is called: ''1 face polishing.''

- First, a ''sandwich'' is prepared by cutting the solar cell in two pieces of $2 \times 10\,mm^2$ and gluing them in front of each order with epoxy glue. The glue needs 40 min of heating at 100°C before cooling at room temperature. The cutting is performed with a ''Well 3242'' composed of a diamond wire with a diameter of 170 μm.
- Second, the sandwich is placed on a tripod in order to polish the face. Allied papers (High Tech Products, Inc.) with various grain sizes: 30, 15, 6, 3, 1, 0.5, and 0.1 μm are consecutively used to achieve a surface as flat as possible. The last step of polishing is performed with silicate colloidal on velvet plate on a ''Struers LaboPol-4.''

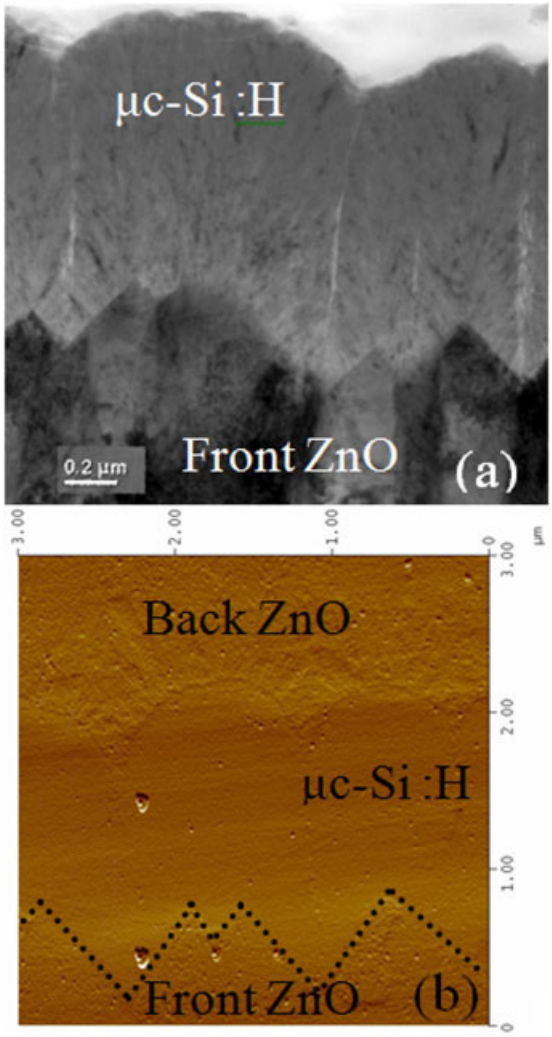

Figure 1. (a) Microcrystalline silicon on as-grown ZnO by TEM. The cracks look like white lines in the silicon layers (Fresnel interference due to different densities). (b) AFM amplitude image (tapping mode). The surface shows no trenches in region of cracks. Dotted lines suggest the interface between the ZnO and the µc-Si:H layers.

- Third, the sandwich is cut under 1 mm of the polishing face and stuck on a carbon scotch (polished face up). A few nanometers of carbon are deposited by evaporation on the surface and a small wire of carbon is placed to connect the top surface with the sample holder via the carbon scotch to avoid surface charging during SEM observation.
- Finally, the surface is observed under a SEM in ''back scattered electron'' (BSE) or ''secondary electron'' mode (SE).

The SEM observations were carried out with a Philips XL-30 ESEM microscope. The BSE can originate from a depth between 10 and 1000 nm and SE from only 1 to 10 nm [29]. Notice that the SE detector also collects around 15% of BSE. Then, the contrast obtained in both BSE and SE micrographs is not only sensitive to the surface but also to sub-surface feature. The lateral resolution is around 50 nm. A linear cracks density (crack/µm) is estimated by counting the number of cracks along the substrate plane on SEM micrographs, such as on the one presented in Figure 2.

A commercial Renishaw Raman imaging microscope (System 2000) equipped with a long working-distance objective was operated with a helium–neon (HeNe) laser (633 nm). Micro-Raman experiments were performed on the solar cells in two ways: with focused excitation light arriving either through the TCO on the top, last-deposited silicon layer of the device (i.e., on the n-layer for the p–i–n devices), or through the glass substrate and the TCO on the bottom, first deposited silicon layer of the device. FTPS was performed with a Nicolet 8700 to analyze the material quality of the solar cells [30]. A sample was prepared as cross-section for TEM observation on a Philips CM200 microscope operated at 200 kV. AFM topography and amplitude imaging (tapping mode) were performed on the substrates prepared as for SEM with ''1 face polishing'' method. A 1.2 µm thick µc-Si:H solar cell deposited on non-treated LPCVD ZnO was prepared with ''1 face polishing'' method for the analysis of SIMS with nano-metrical spot size (nano-SIMS) on Cameca NanoSIMS50.

3. RESULTS

3.1. Nature of so-called ''cracks''

Figure 1a shows a TEM micrograph with cracks (white lines) that cross the µc-Si:H from bottom of the V-shape valley of the ZnO layer up to the top of the layer. These cracks are porous material (not lack of material). Indeed, high resolution TEM micrographs in these cracks show silicon near and above the cracks. With these results, we assume that cracks are zone of porous material with nanovoid size below 70 nm (estimation of the thickness of the TEM sample). Moreover, AFM imaging indicates no trenches with a similar polished sample as seen in Figure 1b. The contrast in SEM micrograph in Figure 2 is explained by assuming a low density material in the region above the V-shape valley of the ZnO. This contrast is observed with both BSE and SE detectors.

3.2. Effect of substrate temperature on cracks

The method described in Section 2 allows counting of cracks in µc-Si:H solar cells (see Figure 2). Good statistics are possible thanks to the large observable area (4000 µm) of each sample. As shown in Figure 3a, the cracks density decreases from 0.23 cracks/µm for deposition of intrinsic layer at 170°C to 0.13 cracks/µm at 270°C for µc-Si:H

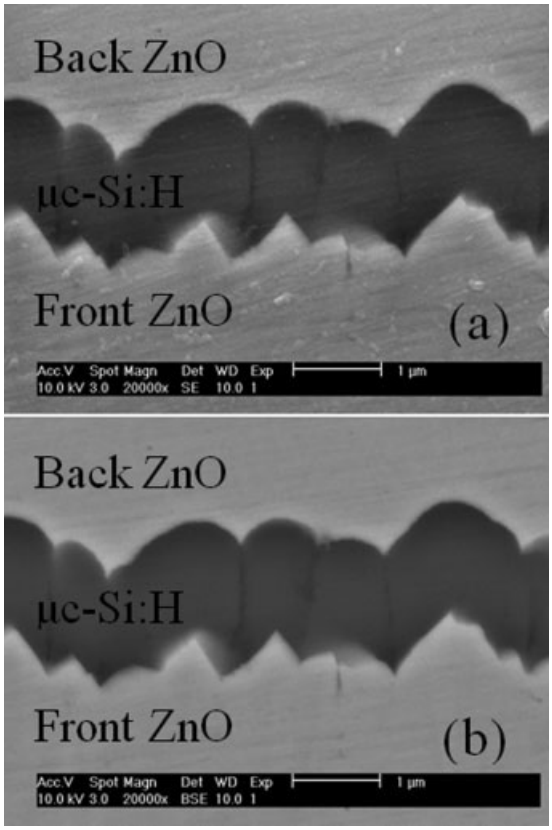

Figure 2. SEM on solar cell cross-section: μc-Si:H appears gray between front and back ZnO (light gray). Cracks appear darker in silicon. (a) Micrograph obtained by electron back-scattered (EBS) detector. (b) Micrograph obtained by secondary electron (SE) detector.

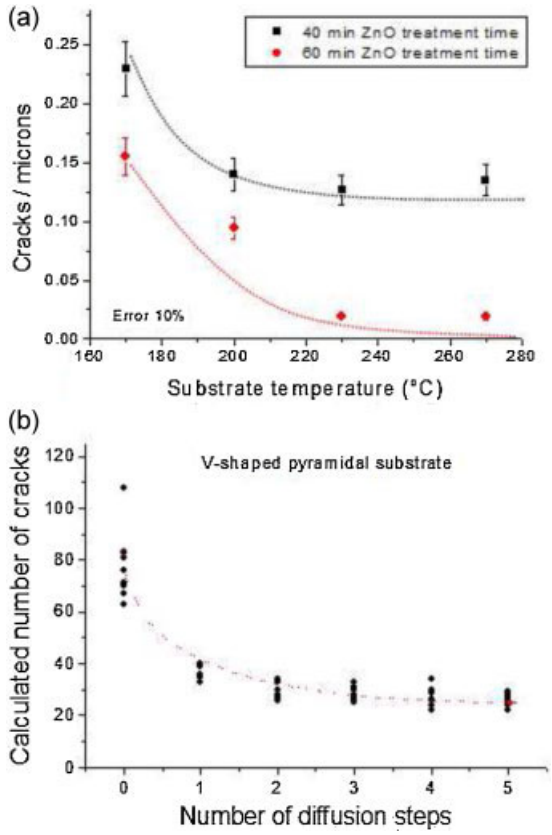

Figure 3. (a) Decrease of crack density with the increase of substrate temperature. Notice that for the same temperature, crack density is higher for solar cells deposited on ZnO treated 40 min compared to 60 min. (b) Simulation result of number of cracks in function of number of diffusion steps obtained with MANEMO program. Lines are visual guides.

solar cells on ZnO treated 40 min. The same behavior is observed for solar cells deposited on ZnO treated 60 min: the density of cracks decreases from 0.16 to 0.02 cracks/μm. Hence, for both ZnO series (on LPCVD ZnO treated 40 and 60 min), the increase of substrate temperature is linked to a decrease of cracks density. This effect is also observed with the simulation program MANEMO (presented in Refs. [16,17]) when the number of diffusion steps is increased (see Figure 3b).

3.3. Effect of substrate temperature on Raman crystallinity

The variations of micro-Raman crystallinity with substrate temperature are presented in Figure 4a. A larger substrate temperature induces an increased Raman crystallinity of the solar cells, with a saturation to 50–55% at 270°C (average value as measured from the glass and cell side with 633 nm laser). The losses of V_{oc} observed in $J(V)$ curves (see Figure 5b) can be related to the increase of crystallinity [31]. However, crystallinity cannot be held responsible for the variations of silicon density (i.e., number of cracks). Indeed, a similar work was done on the series of sample prepared at various silane concentrations and the cracks density is found to be approximately constant even though the Raman crystallinity is ranging from 25 to 70% (Figure 6).

3.4. Effect of substrate temperature on electrical performances

This analysis demonstrates that the FF increases in average from 67 to 70% for temperatures from 170 to 230°C (see Figure 5a). A larger temperature (270°C) leads to lower electrical performances. FTPS measurements in Figure 7 show that the quality of the i-layer material (as deduced from the measured absorption at 0.8 eV) remains low for samples deposited at 170, 200, and 230°C. On the contrary, the defect density in the bulk material for the sample deposited at 270°C is 4 times higher. That can be explained by diffusion of boron from p- to i-layer due to too high substrate temperature.

The improvement of FF between 170 and 230°C can then be attributed, as expected, to the decrease of cracks

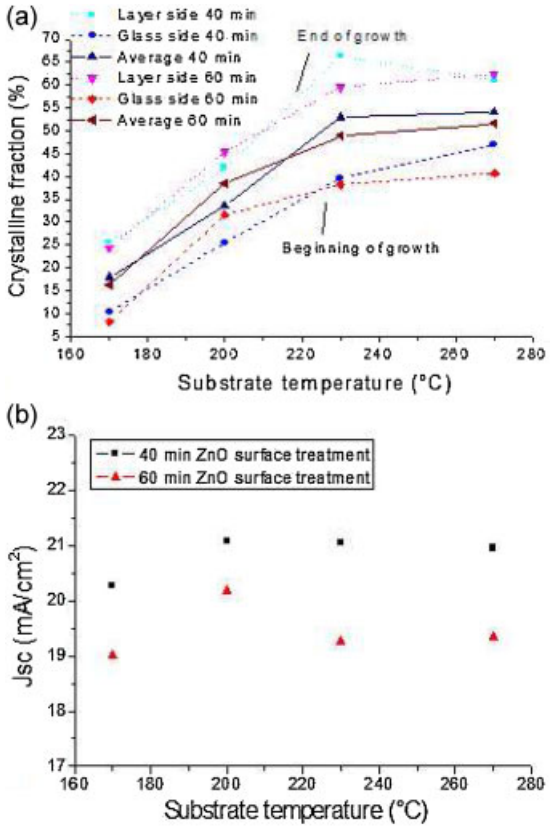

Figure 4. (a) Raman crystalline fraction increase as a function of substrate temperature with saturation at 270°C. This increase is responsible for the decrease of V_{oc}. (b) EQE measurements with bias voltage.

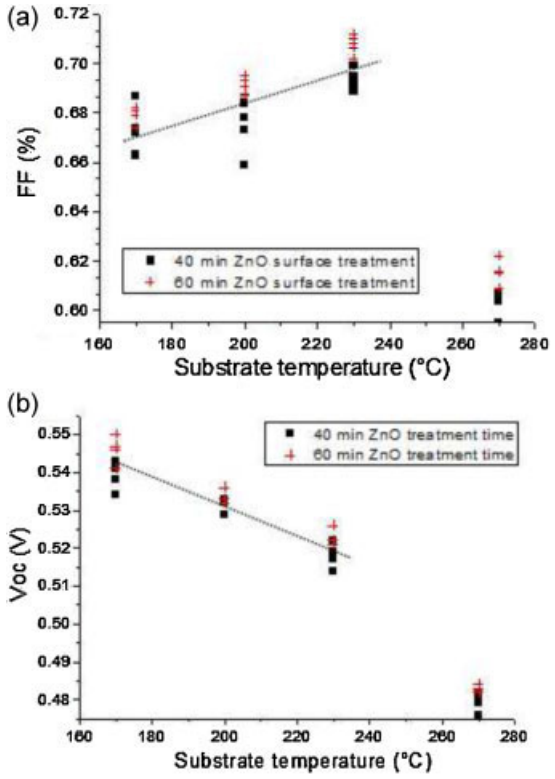

Figure 5. *J*(*V*) curve parameters obtained under one-sun illumination condition. (a) Increase of fill factor (FF) in function of substrate temperature. This increase is related to the cracks in the solar cells. FF at 270°C is low because of bad quality of bulk material (see Fig. 7). (b) Decrease of V_{oc} as a function of substrate temperature. The losses are related to the Raman crystallinity (see Fig. 4a): higher crystallinity leads to lower V_{oc}. Lines are visual guides.

density (already seen in Ref. [15]). Indeed, this latter is reduced by 50% for slightly surface treated ZnO (black squares on Figure 3a) and by 87% for strongly surface treated ZnO (red circles on Figure 3a) when the temperature is raised from 170 to 270°C. Note that FTPS is not influenced by the crack density in the i-layer material since the measured absorption at 0.8 eV is similar for solar cells deposited on both ZnO (treated 40 and 60 min), even though the cracks density differ by a factor 1.5–6 depending on the substrate temperature.

The short-circuit current density was increased between 170 and 200°C as expected with increase of crystallinity, but is constant with the other substrate temperatures. Note that the cells deposited at 200°C are optimal (Figure 4b) and that the current is higher for cells deposited on ZnO treated 40 min than 60 min due to better light trapping properties.

3.5. Effect of cracks in post-oxidation of microcrystalline silicon solar cells

The cross-section of solar cells deposited on non-treated LPCVD ZnO shows cracks at the V-shaped valley (Figures 1 and 2) as already observed and discussed in

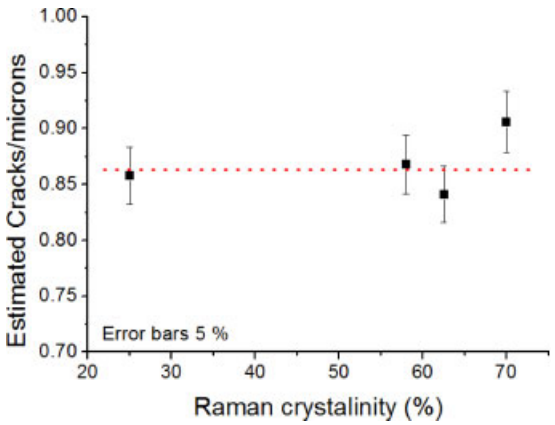

Figure 6. Second series investigation: effect of silane concentration (crystallinity) on density of microcrystalline silicon. The number of cracks is stable with crystallinity. Line is visual guide.

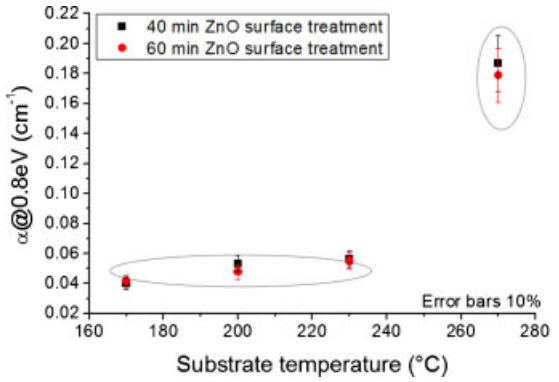

Figure 7. Results of FTPS measurement: absorption at 0.8 eV as a function of substrate temperature. The absorption remains low except for 270°C indicating that the material quality is not good at such high temperature. Notice that we see no difference for ZnO treated 40 or 60 min at the same temperature, meaning that cracks do not influence FTPS measurement.

Refs. [16,17]. However, the nature of these cracks was yet not studied; here, the concentration of impurities in the cracks was analyzed by SIMS. A comparison between a solar cell with high crack density (deposited on ZnO treated 20 min) and low crack density (deposited on ZnO treated 40 min) was performed. The measurements show that the cell with more cracks contains more oxygen (Figure 8). With nano-SIMS measurement, as presented in Figure 9, a mapping in oxygen concentration was possible: zones of cracks contain more oxygen than dense material. The difference of oxygen concentration between dense material and cracks indicate that cracks are active in the mechanisms responsible for post-oxidation of μc-Si:H solar cells.

4. DISCUSSION

The original method for counting cracks presented in this paper is revealed to be powerful for this kind of study. Even

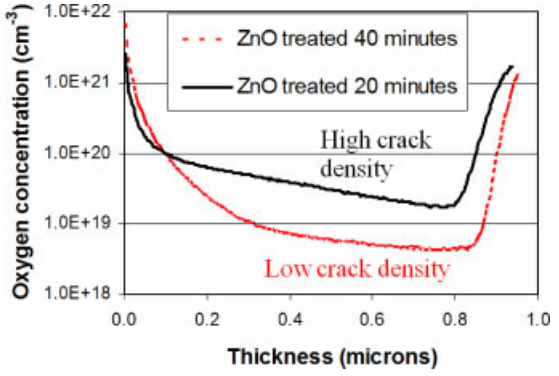

Figure 8. SIMS measurements of μc-Si:H solar cell deposited various surface morphologies. The black line is the measurement for a solar cell containing more cracks than the cell represented by the dotted line.

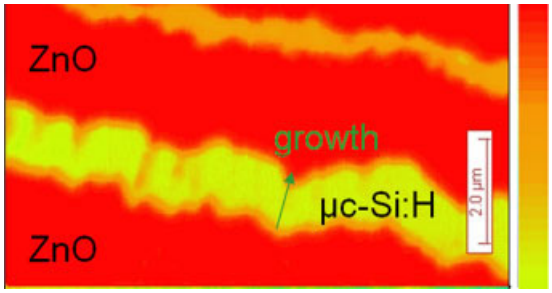

Figure 9. Qualitative mapping of oxygen concentration obtained by nano-SIMS method on a polished device cross-section. Arbitrary units in linear scale.

if it is neither suitable for accurately measuring thicknesses (p-, i-, or n-layer) nor to observe the microcrystalline growth, it is 4 times faster than TEM sample preparation by wet polishing or ion milling and makes it easier to prepare samples for counting cracks. With the help of this method, each sample could be analyzed by SEM and good statistics could be applied on the resulting crack density. From the SEM, TEM, and AFM images, cracks are confirmed to be 2D-like zones of porous, less dense material (all around the perimeter of the as-grown pyramidal shape ZnO). Note that the SEM micrographs (Figure 2) obtained with this sample preparation method look similar to images obtained in a previous study by scanning Kelvin probe microscopy (SKPM) [32]. In this previous work the SKPM technique allowed us, for similar samples, to identify a higher local work-function at the cluster boundaries formed by this porous μc-Si:H material. The measurements with SIMS and nano-SIMS methods clearly identify the cracks as responsible for oxygen contamination, which origin is here attributed to post-oxidation. Indeed, cells with cracks tend to degrade, even when stored in darkness. Such an effect is also observed for low quality μc-Si:H material, as is often obtained at high deposition rate [11]. In this case, it is a bulk effect and it is not linked to preferential diffusion channel as is assumed to happen with cracks.

As already seen in previous paper [14] and confirmed here, the treatment of the surface of the substrate facilitates a decrease of the number of cracks, because the shadowing effect, due to both rms roughness and height of pyramids (''peak to valley''), decreases and the collision of growing fronts is less strong that with V-shape morphology. Indeed, the solar cells deposited on LPCVD ZnO treated 60 min have fewer cracks that on which treated 40 min.

The substrate temperature has also a strong influence on the growth of μc-Si:H by PECVD: it is demonstrated here that the number of cracks can also be decreased by increasing the substrate temperature during the intrinsic layer deposition. As shown in Figure 3a, the cracks density decreases strongly between 170 and 270°C. However, too high temperature (270°C) leads to reduce i-layer quality, and hence, to bad electrical solar cell performances (Figure 7). For 170, 200, and 230°C, the increase of FF can

be linked to the decrease in crack density. Larger temperatures increase the adatoms energy at the growing surface and, thus, the diffusion. This effect is observed in both simulated and experimental results.

In parallel, the crystallinity increases for the 3 first temperatures investigated and leads to a decrease of V_{oc} in the solar cells performances. The relation between the crystallinity and the V_{oc} is already well known [31]. An optimization of Raman crystallinity is hence necessary to improve the electrical performance of the solar cells deposited at higher temperatures in order to benefit to both increase of FF and high V_{oc}. It is also demonstrated with Figure 6 that the crystallinity does not influence the crack density. Hence, we can attribute the crack reduction to the increase of temperature and not to the increase in crystallinity. This finally leads us to the picture that, at otherwise constant plasma parameters and arrival of Si and H radical on the growing surface, the surface diffusion of Si is increased at higher temperature and the closing of voids is better performed. This is in agreement with the growth simulation presented in Ref. [17]. Interestingly our results gives some indication on the local growth mechanisms, as the a-Si to μc-Si transition is usually attributed either to an enhancement of the surface diffusion of the SiH_x precursors [33] or to a selective etching of the weakly bonded Si atoms [34–37]. In our case, the increase of the hydrogen content at constant temperature leads to an increase of crystallinity because the selective etching mechanism start to dominate (whereas the surface diffusion remains moderate), while, for constant radical flows, the increase of temperature leads to a strong enhancement of the surface diffusion, leading both to an increase in crystallinity and to a filling of the cracks.

Finally, we show in Figure 10 that cracks in micromorph devices can appear even if the beginning of the device is crack free. The onset of cracks in the μc-Si:H cell, directly after the a-Si layer, indicates that a-Si growth can lead to a pinching of the substrate which will then lead to a degradation of the μc-Si cell, and consequently of the full device. Mastering both the substrate morphology and the growth conditions to avoid such cracks in the second layer is a key to the successful fabrication of high V_{oc} and high FF micromorph tandem devices. Indeed, in micromorph module production environment, when using APCVD SnO_2 or LPCVD-ZnO as front TCO, it is possible to reduce the crack densities by tuning the deposition parameters during the growth of the TCO. In particular, the LPCVD process versatility allows to some extent to move away from the sharp V-features and, by reducing the roughness, this will tend to lead module with better V_{oc} and FF. We also note that micromorph (tandem) cells could benefit from the improvement of crack density as obtained at higher deposition temperature in the n–i–p configuration. In this case the p-layer could be fabricated at lower temperature, on contrary to p–i–n structures where the amorphous silicon solar cell is deposited first and then, the high substrate temperature used for the intrinsic layer of microcrystalline may lead to amorphous silicon top cell degradation.

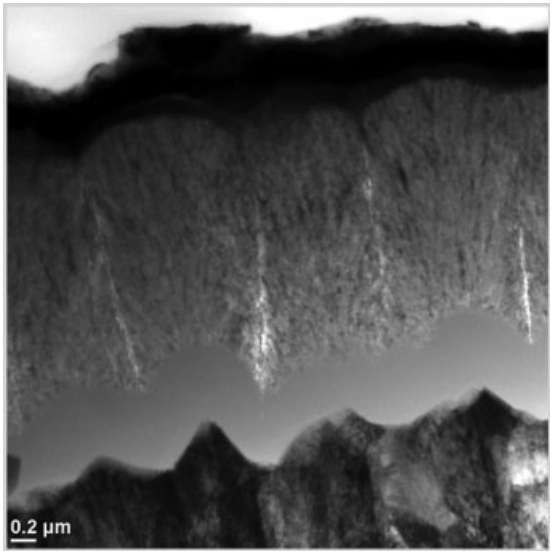

Figure 10. TEM cross-section view of a micromorph p–i–n device.

5. CONCLUSION

A reduction in crack density is a key point for developing high efficiency thin film μc-Si:H solar cells and micromorph cells. Indeed, zone of cracks are clearly pointed out to be responsible for bad electrical performances [15], and this less-dense material permits the incorporation of oxygen after the deposition of the silicon layers (post-oxidation). To increase the density of μc-Si:H material, one way is to modify the substrate morphology from V-shape to U-shape, but this will influence the scattering of the light, and hence, the short-circuit current density of the solar cells. In this paper, we show that by increasing the substrate temperature during the intrinsic layer deposition, the crack density can be further decreased, without any influence on the scattering of the light, because the surface morphology of the substrate is unchanged. We attribute this reduction in crack density with substrate temperature to a ''filling'' of cracks due to an enhanced surface diffusion of the silicon atoms. We also show that, at constant temperature, the crack density is independent on the crystalline fraction. Hence, our results tend to show that the enhancement of the surface diffusion of the Si adatoms by the higher hydrogen fraction is not as efficient as when obtained by a larger substrate temperature. Finally an original quantification method proposed for counting the cracks is proven to be a useful tool to evaluate the influence of the TCO morphology on the cell structural properties. This will be of crucial importance for the production of micromorph modules on various kinds of TCOs.

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