High mobility bottom gate microcrystalline silicon TFT deposited by VHF PECVD

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Abstract

The use of microcrystalline silicon (μc-Si:H) for thin-film transistor (TFT) is a very attractive alternative to both amorphous silicon (a-Si:H) in terms of performance and to low temperature poly silicon (LTPS) in terms of manufacturing costs. However, due to the complex structural morphology of μc-Si:H (Si grains embedded in an amorphous tissue) and the usually observed evolution of the crystalline fraction along the growth axis, their incorporation in TFTs required very careful optimisation of the material growth in order to obtaid high performance.

In this work we focus on bottom gate μc-Si:H TFTs which are even more demanding in controlling material growth on the gate dielectric. Such TFTs have been optimized to obtain μc-Si:H layer without any a-Si:H incubation layers. Various TEM SEM and Raman analyses have been performed to achieve and determine optimum μc-Si:H growth conditions; such analyses were then correlated with TFT performance. Bottom gate TFTs with field effect mobility as high as 5.2 $cm^2V^{-1}s^{-1}$ for electrons have been fabricated on glass by VHF PECVD. TFT performance as a function of μc-Si:H deposition conditions and structural characteristics will be presented and discussed.

1. Introduction

Thin-film electronics is nowadays mainly based on amorphous silicon (a-Si:H) thin-film transistors (TFT) while low temperature poly-Si (LTPS) TFT are restricted to more demanding electronics (high resolution/small pixel size flat panel displays, electronic circuits on glass, etc). In terms of performance, the low mobility of a-Si:H TFTs only allows the use of n-type transistors and strongly limits the development of electronic circuits based on such TFTs. On the other hand LTPS offer better performance and full CMOS circuit capability but requires expensive fabrication techniques and processing temperatures incompatible with flexible polymeric substrates. In this context, microcrystalline silicon (μc-Si:H) TFTs offer an attractive alternative to both a-Si:H in terms of performance and to LTPS in terms of manufacturing costs.

Recently, μc-Si:H TFTs with field effect mobility values as high as 400 $cm^2V^{-1}s^{-1}$ have been fabricated in top gate configuration [1]. Due to the usual evolution of the μc-Si:H crystalline fraction as a function of the deposition thickness, such configuration allows the formation of the channel in the part of the layer which is not affected by any a-Si:H incubation layer and exhibit an optimal structural morphology.

In this paper, we focus on the bottom gate configuration (inverted staggered configuration) which is far more demanding in term of material growth and interface control. Furthermore, this configuration is fully compatible with current process (and process equipments) widely used for a-Si:H TFT technology and therefore very attractive from an industrial point of view. For the same reasons other groups have chosen the same strategy and have achieved very encouraging results with mobilities up to 3 $cm^2V^{-1}s^{-1}$ [2,3,4]. The main objectives of this work are to study the influence of μc-Si:H crystalline fraction and growth on the performance of n-type bottom gate μc-Si:H TFTs using SiO_x gate dielectric.

Without careful optimization of the growth of μc-Si:H, such layers exhibit an a-Si:H incubation layer as seen in Fig.1. For bottom gate TFTs such layer is very detrimental for the performance and an immediate μc-Si:H growth has to be insured from the dielectric/semiconductor interface in order to have optimal transport in the TFT channel.

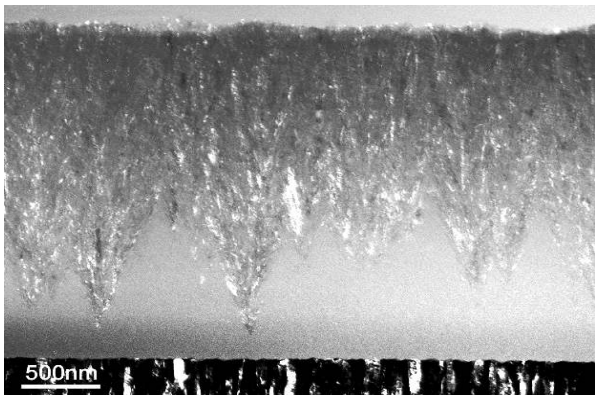

Figure 1: TEM dark field cross-view of a typical μc-Si:H layer deposited without any initial control of the growth. An a-Si:H incubation layer is deposited before the start of the μc-Si:H growth.

In this study, we analyzed the influence of three different intrinsic microcrystalline layers on the performance of thin film transistor. The power and the high hydrogen dilution were kept constant, while the temperature and the pressure were changed.

2. Experimental

2.1 TFT fabrication

All TFTs were fabricated on AF45 glass substrate by very high frequency plasma enhanced chemical vapour deposition (VHF PECVD) at 80 MHz excitation frequency for both SiO_x gate dielectric and for the μc-Si:H channel. Deposition of the SiO_x were made from a mixture of N_2O and SiH_4 in a proportion 141 sccm/5.3 sccm, at a pressure of 0.5 mbar and a RF power of 37.5 mW/cm^2. Intrinsic μc-Si:H layers for the channels were deposited from a mixture of 400 sccm of H_2 and 4 sccm of SiH_4 under a RF power of 69 mW/cm^2. The very high hydrogen dilution ration $R=H_2/SiH_4$ ensures the

high cristallinity of the film. Source and gate layers were formed by depositing µc-Si:H layers doped by adding phosphine to the process gas mixture.
Three sets of TFTs (or samples) were fabricated by varying the intrinsic layer deposition conditions as indicated in Table 1. Each set or samples comprises several TFTs with various geometries with channel width varying between 80 and 600 µm and channel length varying between 20 and 100 µm. Gate electrode overlap with respect to source and drain electrode was either 10 or 20 µm.

Table 1: Sample sets and corresponding deposition parameters.

Sample # TFT set #	SiO_x deposition temperature	µc-Si:H deposition temperature	Pressure
1	200°C	200°C	0.1 mbar
2	250°C	200°C	0.75 mbar
3	250°C	250°C	0.75 mbar

The TFT stacks consisted in 50 nm of thermally evaporated Al for the gate electrode (patterned by wet etching), a 200 nm thick dielectric SiO_X layer followed by a 150 nm thick intrinsic <i> µc-Si:H and a 50 nm µc-Si:H n-type doped layer. Finally a drain/source Al layer was deposited on top. and patterned by wet etching. The TFTs were finally completed by back channel etch as well as TFT isolation (and gate electrode recovery) were obtained by reactive ion etching.

2.2 Raman spectroscopy

Raman spectroscopy is typically used for the measurement of the crystalline fraction of the µc-Si:H material. Raman spectra were deconvoluted using commercial software (Grams), assuming Gaussian shape for the three peaks of interest. The amorphous silicon phase of the µc-Si:H leads to the appearance of a broad peak centered at 480 cm^{-1} whereas the microcrystalline silicon phase results in an asymmetric peak centered at 520 cm^{-1}. The low wave number tail of this peak (around 510 cm^{-1}) is attributed to the defective, but yet crystalline part of the nano-crystals [5]. By integrating the surface below these peaks, one obtains the Raman crystalline fraction Φ_c from the following relationship:

$$\Phi_C = \frac{I_{510}+I_{520}}{I_{480}+I_{510}+I_{520}}$$

where I_{480}, I_{510}, I_{520} are the integrated areas of the peaks at 480 cm^{-1}, 510 cm^{-1} and 520 cm^{-1}, respectively. Note that Φ_c represents a lower limit for the actual crystalline fraction
The result is a volumic average Raman crystalline fraction given by the excitation laser interaction volume in the sample. Raman spectra were measured using a green laser (Argon, 514nm). The corresponding high light absorption in a-Si and µc-Si, implies that the Raman spectra is controlled by the 50 - 100 nm top part of the layer.

2.3 Electron Microscopy

Transmission Electron microscope (TEM) images were taken from a wedge shaped thin sliced obtained from mechanically polishing of samples followed by a short ion beam cleaning and polishing procedure. TEM observations were made on a Philips CM200 microscope operated at 200 kV. They allow one to observe directly the amorphous/crystalline nature of the layer as well as the crystallite size.
Scanning Electron Microscope (SEM) observations were made on polished samples (‘1 face polishing” using a tripod) with “back scattered electron” (BSE) detector in a Philips XL-30 E-SEM .

3. Results and discussion

The samples used for the Raman measurement consist of glass/SiO_X/µc-Si:H stacks. As the substrate has a significant influence on the microstructure of a microcrystalline layer [6], we used the same deposition sequence as for TFT, but we stopped the deposition after 50 nm of <i> layer in order to observe the initial growth of the channel layer.
The Raman spectra are plotted on Figure 2. The measured crystalline fraction of sample 1 is Φ_C=80.7%. Knowing that the measured crystalline volume fraction is the average fraction of 50 nm of material, one can expect that the incubation layer is very thin or not present.

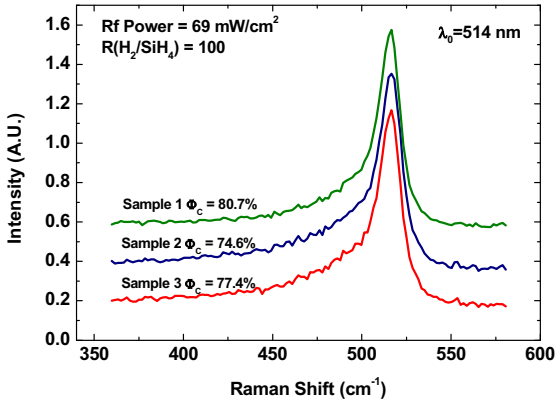

Figure 2: Raman spectra and corresponding Raman crystalline fraction of three different <i> µc-Si:H layer deposition conditions (see Table 1), as measured with an Ar laser (514nm).

Despite its excellent structural characteristics, sample 1 exhibited large internal mechanical stress which led to peeling problem for layers thicker than 100nm. As we need some over-etch tolerance for the back channel etch step, the use of such a layer make the fabrication of TFTs more critical. By increasing the total pressure of deposition, we obtain a less stressed <i> layer while keeping a high crystalline volume fraction of Φ_C = 74.6% for sample 2. Several studies [7,8,9] showed that increasing the deposition temperature may increase the crystalline fraction of the film. Changing the temperature from 200°C to 250°C leads to a small increase of the crystalline fraction to Φ_C = 77.4% for sample 3.
For the TEM analysis, micrographs of sample 1 are presented but sample 2 and 3 show similar characteristics and no observable differences in the TEM micrographs.

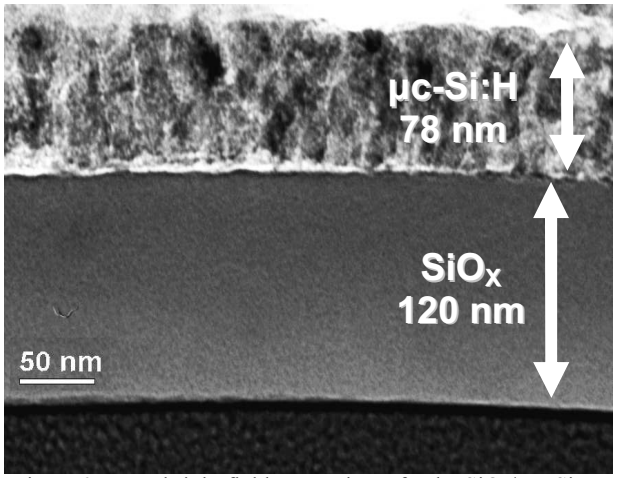

Figure 3: TEM bright field cross-view of a the SiO_x/ µc-Si:H interface of a µc-Si:H TFT (sample 1).

Figure 3 is a TEM micrograph in brightfield mode of the interface between the SiO_X and the intrinsic µc-Si:H layer. In the latter mode, microcrystalline region are dark, and amorphous region are grey. The mobility of the transistor is considerably affected by the crystalline volume fraction at the interface, crystallite size should be as big as possible and density of crystallite must be maximized for best performances. On Figure 3, one can observe that there isn't any incubation layer and that we achieve a microcrystalline growth directly from the SiO_x surface. The crystalline fraction is difficult to evaluate on TEM micrograph, but we know from the Raman measurement that the average crystalline fraction is close to 80% and no clear evolution of the crystalline fraction can be observed on the micrograph, meaning that the crystalline volume fraction is high even close to the interface. On the high resolution TEM micrograph of the same sample (Figure 4), more details of the microcrystalline structure can be observed. One can clearly see atomic plans of the well oriented crystallites, and their average size is about 5-10 nm.

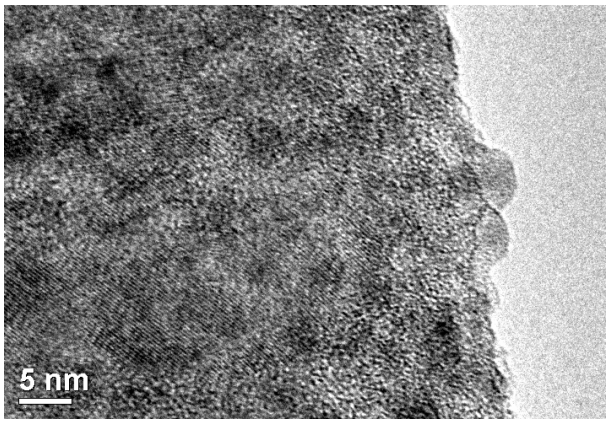

Figure 4: High Resolution TEM bright field cross-view of a the SiO_x/ µc-Si:H interface of a µc-Si:H TFT (sample 1).

The drain-source current and the gate-source current in function of the gate voltage for drain voltage of 0.1 V and 1 V are plotted on Figure 5 for Sample 1. The electron mobility and the threshold voltage of the TFT were extracted from the transfer characteristics measured at drain voltage of 0.1 V on a TFT with a channel length of 40 µm and a channel width of 600 µm. The linear mobility extracted is 5.2 cm^2/Vs, the threshold voltage is 6.1 V and the I_{ON}/I_{OFF} Ratio is about 10^{-6}. For all TFTs, no particular dependence was observed as a function of the TFT geometry (at least for the various TFT channel lengths and channel widths analysed here) for this sample.

The high mobility, significantly higher than the mobility of conventional a-Si TFTs (1 cm^2/V s), was achieved thanks to the high quality of the intrinsic µc-Si:H layer. The crystalline fraction at the interface between dielectric and the channel layer seems to be a key issue to obtain high mobility bottom gate transistor. Another issue is the O_2 contamination of highly crystalline layers but the low I_{OFF} shows that oxygen contamination was minimized during the different process steps [10]. Dark conductivity measurement on similar <i> layer confirmed the latter result with a conductivity $\sigma_d \sim 10^{-6}$ S/cm.

The transfer characteristic of the three samples with a channel length of 40 µm and a channel width of 600 µm are shown on Figure 6. Linear mobility of 0.33 cm^2/Vs and a threshold voltage of 4.59 V were extracted from the transfer characteristic of sample 3. Electrical parameters of sample 2 were not extracted due to the lack of field effect behaviour. Several TFTs with same deposition parameters were fabricated to be sure that this behaviour does not arise from a fabrication problem. As for sample 1, no particular dependence of the TFT performance as a function of geometry was observed for samples 2 and 3.

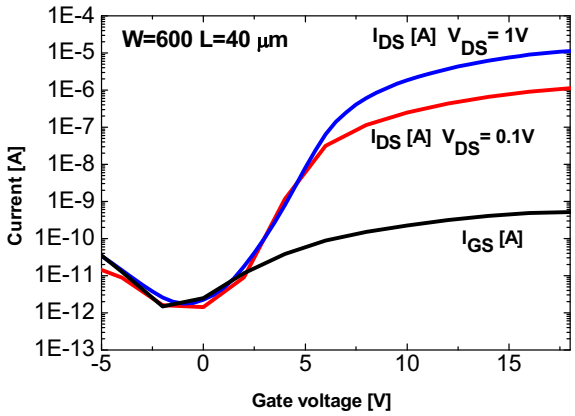

Figure 5: Drain-source I_{DS} and gate-source I_{GS} as a function of gate voltage V_G of our best n-type bottom gate µc-Si:H TFT. Other TFT characteristics are given in Table 2.

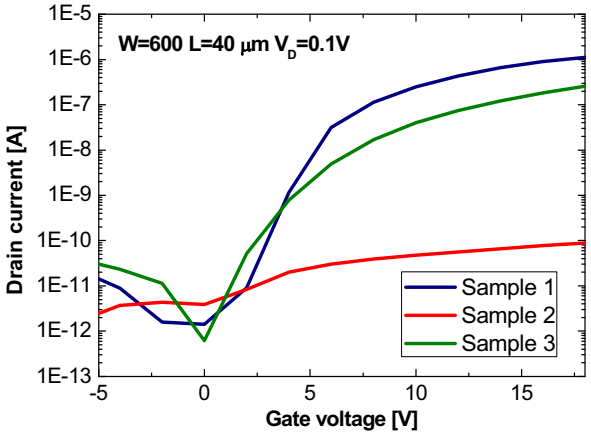

Figure 6: Drain-source I_{DS} as a function of gate voltage V_G of the three n-type bottom gate µc-Si:H TFT. Deposition parameters of the samples are given in Table 2.

Table 2: Main characteristics of n-type bottom gate µc-Si:H TFT plotted in Figure 6.

	Sample 1	Sample 3
μ_{FET} [$cm^2V^{-1}s^{-1}$]	5.23	0.33
V_{TH} [v]	6.1	4.59
S [V/dec]	0.95	1.04
I_{ON}/I_{OFF}	$\sim 10^6$	$\sim 10^5$

As the crystalline fraction of sample 1 is similar to sample 2 and 3, the decrease of performance was quite surprising. In order to better understand this phenomenon, further SEM analyses were performed.

The "1 face polishing" method was originally developed to highlights crack and void in microcrystalline silicon for solar cells on textured substrate [9]. Figure 7 shows SEM micrograph of sample 2. Microcrystalline silicon appears grey and cracks or voids appear as dark region in silicon. SEM micrographs look slightly blurry as we were working at the maximum resolution allowed by the E-SEM. For this reason the focus could not be adjusted perfectly. (as its is usually set at a higher resolution). One can clearly see on Figure 7 a large amount of voids in the µc-Si:H layer. Figure 8 shows a SEM micrograph of sample 3 fabricated under the same deposition parameters as sample 2 except the temperature increasing from 200°C to 250°C.

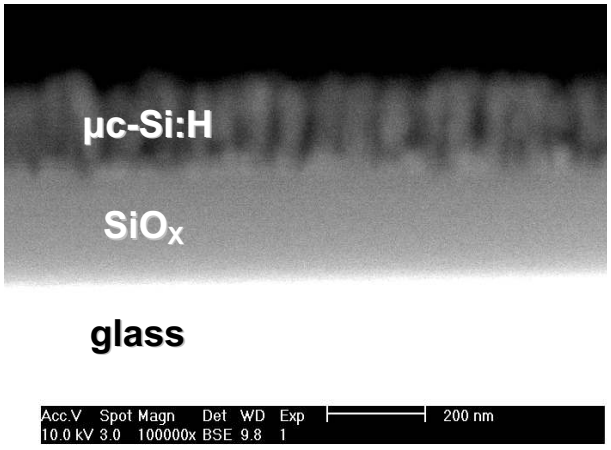

Figure 7: SEM micrograph of sample 2. Voids appear as dark region due to the lower density of material.

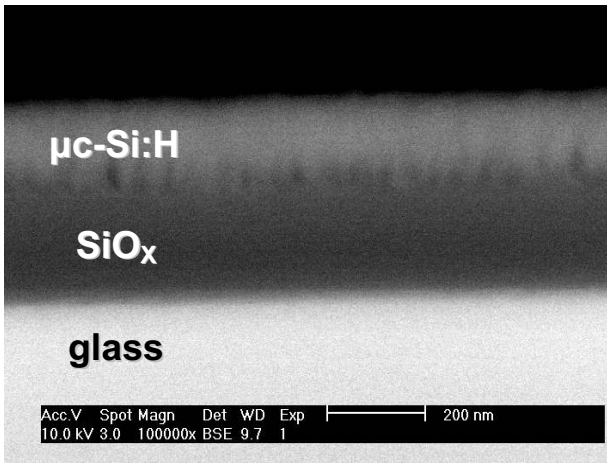

Figure 8: SEM micrograph of sample 3 deposited at 250ºC.

Microcrystalline growth mechanism are generally attributed either to an enhancement of the surface diffusion of the SiH_X precursors [7] or to models related to hydrogen interaction at the surface like selective etching [11]. At a constant temperature of 200°C (sample 1 and 2) a change in the deposition pressure leads to a huge increase of the voids density due to change of the hydrogen surface interaction (change of the ion bombardment energy). The stronger ion bombardment occurring at low pressure (for sample 1) is supposed to improve the density of the material and resulting in less voids formation. This hypothesis is supported by the slightly higher Raman crystalline fraction as well as higher mechanical stress present in these films. On the other hand, the increase of the temperature leads to a strong enhancement of the surface diffusion, resulting in both an increase of crystalline fraction and a better filling of voids.

Despite the fact that all samples exhibit high crystalline fraction, performances of the TFTs are also clearly related to the amount of voids present in the channel layer. Additional investigations, including high resolution TEM, are planned to better understand the detailed influence of structural characteristics of the µc-Si:H layers on the performance of TFTs and especially why sample 1 exhibit much better mobility than sample 3.

4. Impacts and Conclusion

Bottom gate µc-Si:H TFTs with mobility values for electrons above 5 $cm^2V^{-1}s^{-1}$ were successfully fabricated by VHF PECVD at 200°C using deposition equipment and process flow identical with those used for a-Si:H TFT fabrication. Furthermore, such process temperature would be compatible with the use of polymeric substrates in order to fabricate flexible TFTs. Such mobility values for electrons, as well as the expected one for holes (given the fact that hole mobility values found in µc-Si:H is usually approximately half the value of those of holes) would allow the use of these transistors in more complex circuits for improved displays using the existing production equipment.

Achieving high crystalline fraction is mandatory for achieving high performance for bottom gate µc-Si:H TFTs. However, depending on the deposition conditions, voids or crack may form easily at the gate dielectric/channel interface leading to very detrimental effect on the TFT performance. Best performances (field effect mobility values) are obtained at relatively low deposition pressure and therefore increased ion bombardment. Unfortunately, such deposition conditions also produce µc-Si:H films with higher mechanical stress leading in some cases to delamination. Further device and material optimization to mitigate the stress build up are still needed and will allow getting the full potential of this TFT technology. Further electrical characterizations of these high mobility transistors with respect mainly to stability are also required.

5. Acknowledgements

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6. References

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