Stenciled conducting bismuth nanowires[a)]

Veronica Savu,[b)] Sam Neuser, Guillermo Villanueva, Oscar Vazquez-Mena, Katrin Sidler, and Juergen Brugger
Microsystems Laboratory, Ecole Polytechnique Fédérale de Lausanne (EPFL), 1015 Lausanne, Switzerland

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Stencil lithography is used here for the fabrication of bismuth nanowires using thermal evaporation. This technique provides good electrical contact resistance by having the nanowire structure and the contact pads deposited at the same time. It has also the advantage of modulating nanowires' height as a function of their width. As the evaporated material deposits on the stencil mask, the apertures shrink in size until they are fully clogged and no more material can pass through. Thus, the authors obtain variable-height (from 27 to 95 nm) nanowires in the same evaporation. Upon their morphological (scanning electron microscopy and atomic force microscopy) and electrical characterizations, the authors obtain their resistivity, which is independent of the nanowire size and is the lowest reported for physical vapor deposition of Bi nanowires (1.2×10^{-3} Ω cm), only an order of magnitude higher than that of bulk bismuth. © *2010 American Vacuum Society.*
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I. INTRODUCTION

Bismuth (Bi) is an extensively studied material. In bulk form it is a semimetal with small effective mass, long mean free path, and low carrier density, ideal for studying size effects in low-dimensional structures. Its large thermoelectric power and low thermal conductivity also make Bi a good thermoelectric material. It has been shown that when the critical dimension is below 50 nm, a semimetal-to-semiconductor transition occurs,[1,2] which increases the thermoelectric figure of merit even more. Thus, exploring new ways for batch fabrication of easy-to-contact Bi nanowires (NWs) with controlled positions can be of interest for electronic transport properties[3] and thermoelectric applications.[4]

Polycrystalline Bi NWs can be obtained via physical vapor deposition (PVD),[5] lithographically patterned electrodeposition,[6] while single-crystalline NWs are usually fabricated by electrodeposition in an anodic aluminum oxide template,[7,8] ion track-etched polycarbonate membranes,[9] or molecular beam epitaxy followed by etching.[10] For most top-down techniques, fabricating NWs involves an e-beam exposure step, which is serial and expensive. The upside is the control of the position and dimensions of the patterns. The bottom-up processes, while parallel and cheaper, cannot control the NW position on the substrate, thus requiring a serial and customized electrode deposition step for electrical characterization. Stencils provide a unique bottom-up approach, where submicrometer structures can be patterned in parallel.

Stencil lithography brings added value when using Bi in particular. Being a soft material, it is difficult to pattern Bi top-down at the nanoscale. Previous work has shown that Bi quality is strongly dependent on the substrate and deposition conditions used.[11] When using e-beam lithography, achieving Bi NWs narrower than 200 nm on an insulating substrate proved to be a challenge due to charging and then lift-off challenges.[12] As stencil lithography is not a charged-beam technique, it is equally useful for conducting and insulating substrates. If the Bi NWs are fabricated on top of existing electrodes, step-coverage issues will prevent a good contact between the thick electrode material and the thin Bi. On the other hand, if the NWs are created first and then the electrodes are added, the bismuth oxide created once the Bi is in the presence of oxygen is extremely hard to remove and prevents the formation of good electrical contact to the wire. When using a stencil, the thickness of the NW can be smaller than that of micropatterns deposited in the same step. This happens because of the gradual accumulation of the evaporated material on the aperture walls, leading to the eventual clogging of the apertures that have a dimension the same order of magnitude as the deposited thickness. Thus, one can pattern thin and narrow wires, while maintaining good step coverage of the electrodes by the Bi.

In this work stencil lithography was used for the first time to fabricate conducting Bi NWs. Their morphology is explored and their room temperature resistivity is shown to be constant for all the measured wires, down to wires with relatively high aspect ratios and dimensions below 50 nm, 2.6 μm $\times$ 80 nm $\times$ 27 nm.

II. FABRICATION

We start by fabricating the nanostencils. We deposit 100 nm low-stress SiN on both sides of a Si wafer. Electron beam lithography is used to pattern the front side of the wafer with arrays containing a total of 2240 nanoslits. The nominal width and length of the slits vary from 25 to 400 nm and from 1 to 10 μm respectively. Each nanoslit is connected at both ends by larger micropads. These will ensure a better step coverage and electrical contact of the material deposited through the nanostencil on a substrate prepatterned with larger contacts, intended for wire bonding. Then the back

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[b)]Electronic mail: veronica.savu@epfl.ch

side windows corresponding to the membranes and aligned to the front side design are patterned. The SiN and part of the Si on the back side are dry etched, then wet KOH etching is used for etching the remaining Si down to the front side SiN membrane.

Contact electrodes for wire bonding are deposited with standard photolithography and lift-off on a Si wafer with 200 nm SiO_2 on it, by evaporating 5 nm Ti and 80 nm Au. We align the nanostencil to the patterned substrate using a SUSS MA/BA 6 bond aligner system, customized for full-wafer stencil alignment and clamping, with an alignment accuracy of 1–2 μm. The clamped set is introduced in a UNIVEX 450B thermal evaporator and pumped down to 5×10^{-7} mbar, where Bi nanowires are locally patterned. Bismuth pieces with 99.999% purity are melted in a 4.8×1.9 cm^2 molybdenum boat and evaporated at a rate of 0.5 nm/s. Due to geometrical effects of the source size on the accuracy of the pattern transfer from stencil to substrate,[13] the smaller the size of the material source, the sharper the deposited nanopattern is. Thus, a molybdenum cover with a 3 mm diameter hole in it is used for constraining the effective Bi source size.

III. MORPHOLOGICAL AND ELECTRICAL CHARACTERIZATIONS

The nanowire morphology was characterized using scanning electron microscopy (SEM) and atomic force microscopy (AFM). The lateral size was obtained from the SEM micrographs, while the structures' height was extracted from AFM measurements.

The Bi reaching the substrate forms grains that become connected if enough material is deposited. The lateral dimension of the structure is influenced not only by the membrane aperture dimensions but also by the source-stencil-substrate geometry and the spread of the deposited material on the substrate. The setup geometrical parameters—the source-stencil distance D, the stencil-substrate gap G, and the material source size S—induce an enlargement $B=G\times S/D$ of the structure compared to the stencil aperture A. Thus, given a fixed D and G, the pattern transfer accuracy can be increased by minimizing the source size. The spreading of the Bi atoms on the substrate creates nucleation points even farther away than distance B. This effect can be seen in the grain size distribution from the SEM images: The grain size of the main structures is much larger than that of the unconnected grains around it [Fig. 1(a)]. This morphology is typical for stencil lithography, where the mask (membrane) is not in intimate contact with the substrate, allowing the material to diffuse.

The grain size of the Bi varies also as a function of NW thickness. In Fig. 1(a), three NWs are shown with increasing thickness and width, from top to bottom, while the respective stencil apertures through which the NWs were deposited are presented in Fig. 1(b). The grains from thinner wires are smaller than those from thicker wires or larger deposited structures. Since there are not enough grains in a NW to perform a significant statistical analysis of the mean grain size, we can only estimate it qualitatively, ranging from about 30 to 60 nm in the three NWs shown, top to bottom. An estimation of the grain size after 95 nm Bi was deposited on the back side of the SiN is obtained using an optimized algorithm for IMAGE-J image processing software. Assuming square grain geometry, the mean grain size is extracted to be 61 nm.

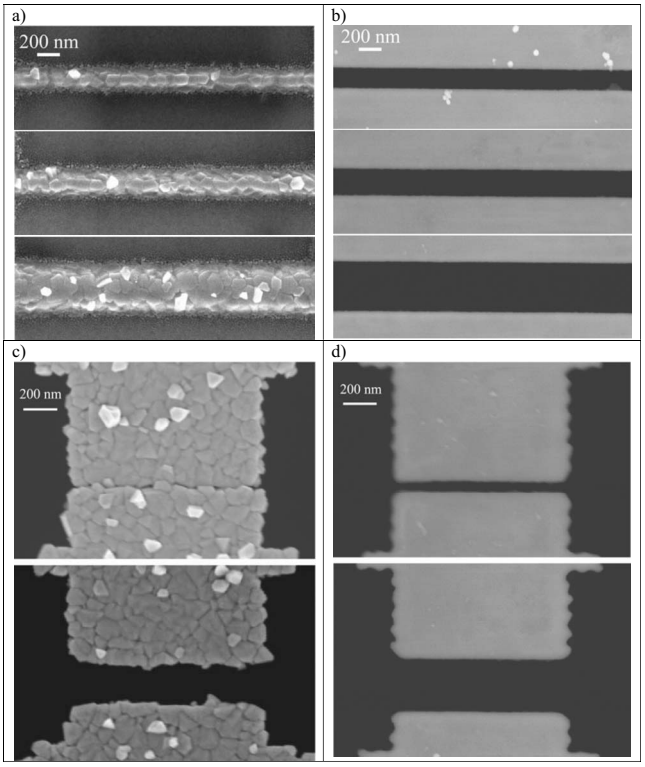

FIG. 1. (a) Scanning electron micrograph of 2.6 μm long Bi NWs deposited on SiO_2 substrate in the same step with widths of 200, 260, and 440 nm, respectively. (b) Scanning electron micrograph of stencil apertures through which the NWs from (a) were deposited. (c) Scanning electron micrograph with 1 μm long stencil apertures of 70 and 320 nm wide, respectively, after the deposition of 95 nm Bi and (d) after the Bi was cleaned off. One can notice the narrower one is fully clogged, while the second one is merely reduced in size.

The material is deposited both through the apertures onto the substrate and onto the stencil side facing the source. As it accumulates, the effective apertures are continuously shrunk, until they are fully clogged. When the Bi grain size (60 nm on the average) is comparable to the stencil aperture, grains can also grow on the edge of the membrane apertures and bridge across the wall sides, creating a "bottleneck" or shadow mask which blocks more material from being deposited onto the substrate. This can give rise to thinner regions or even interruptions in the NWs, which cause failure during electrical measurements.

We plotted the aperture widths when 95 nm Bi was deposited on them versus when they were clean. When fitted to a line, we obtained an intercept of 100 nm. From this we conclude that on each edge of the SiN aperture there is an accumulation of overhanging Bi of about half the thickness of the deposited material. Thus we estimated the amount of clogging to be roughly 1:1 to the amount of deposited mate-

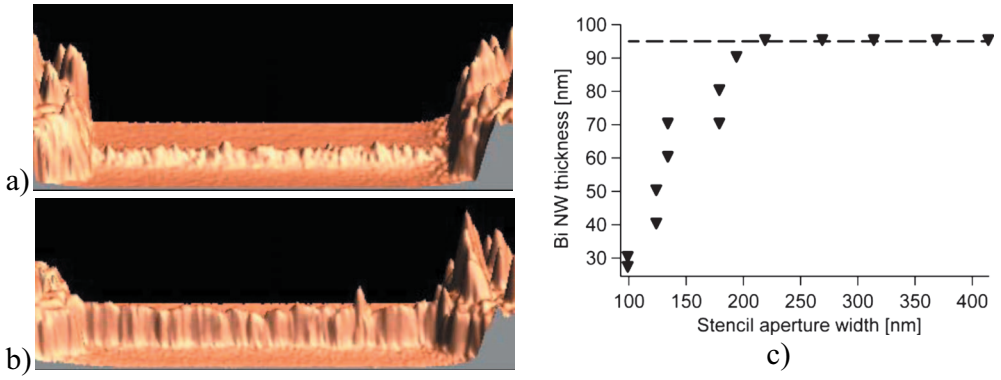

FIG. 2. (Color) Atomic force microscope image of two NWs fabricated in the same step by the deposition of 95 nm Bi nominally, through two different-size stencil apertures of 100 and 220 nm, respectively, illustrating their different thicknesses of (a) 27 nm and (b) 95 nm as a function of width due to stencil aperture clogging; (c) graph showing the dependence of the nanowire thicknesses on the stencil aperture size.

rial, consistent with previous results for other metals.[14] Figure 1(c) shows a SEM micrograph of two apertures of 70 and 320 nm, respectively, through which 95 nm Bi has been evaporated. After the stencil is cleaned of Bi by wet etching in a solution of $HCl:H_2O=1:10$ for 3 h, the apertures recover their initial dimensions and are ready to be used for the next evaporation [Fig. 1(d)].

The clogging phenomenon allows for pattern height control within a single evaporation when the aperture dimensions range from the same order of magnitude to much larger than the amount of evaporated material.[15] The narrower apertures will allow less material to go through than the larger ones; hence the narrower structures will also be thinner. This can be seen in the AFM images from Figs. 2(a) and 2(b). Here the nominal Bi thickness is 95 nm. While the larger structures, deposited through microapertures, reach the full height, the narrower the NW slits become, the thinner the wires deposited through them are. Similar results have been reported for Au and Al.[15] In Fig. 2(c) the NW thickness versus the nanoaperture width is plotted. One can see that the minimum width for which the NW has the same thickness as nominally deposited is around 200 nm, with a slope of 0.6 in the sub-200-nm region. This sets a lower limit to the narrowest NW that can be achieved since for a very narrow slit, not enough material might be allowed to pass for creating a continuously connected structure.

The stencils were successfully reused after being cleaned several times for Bi deposition. Two sets of factors influence the pattern reproducibility: the local substrate conditions and the deposition geometry. At the sub-100-nm length scale, the local surface chemistry could be altered by the removal of the substrate stencil from the clean room environment for several tens of minutes before loading into the evaporator (located outside of the clean room). The variable part of the setup geometry is the gap between the clamped stencil and the substrate stack. It varies across the wafer between roughly 5 and 30 μm, depending on the stencil and substrate curvatures. When the ratio of substrate-stencil gap G to aperture width A becomes larger than the ratio of source-stencil distance D to source size S, $G/A > D/S$, the effective source size as seen from the substrate through the aperture shrinks and the material flux decreases.[16] In our case $D=50$ cm and $S=0.3$ cm. For a local gap $G=20$ μm, the source size is effectively shrinking starting with an aperture width $A=120$ nm. Thus, the local deposition conditions (effective source size and deposition rate) can vary across the wafer even within the same deposition step. For the wider apertures (larger than 200 nm), where smaller surface variations are probably averaged and the $G/A > D/S$ limit is not reached, the pattern dimensions are reproducible.

The room temperature resistance of the NWs was measured using a quasi-four-probe technique and the resistivity was extracted. A current and a voltage probe were connected to one of the two Ti/Au pads from each wire and the current was ramped up to 100 nA in 5 nA steps while recording the voltage. All the NWs showed linear current-voltage characteristics, as shown in the inset of Fig. 3. The electrical resistance R was plotted against the ratio of the number of squares L/w to thickness t, with all the dimensions measured individually for each wire. By fitting the curve to a line, the resistivity is extracted and found to be 1.2×10^{-3} Ω cm. Compared to previously reported results for PVD Bi using

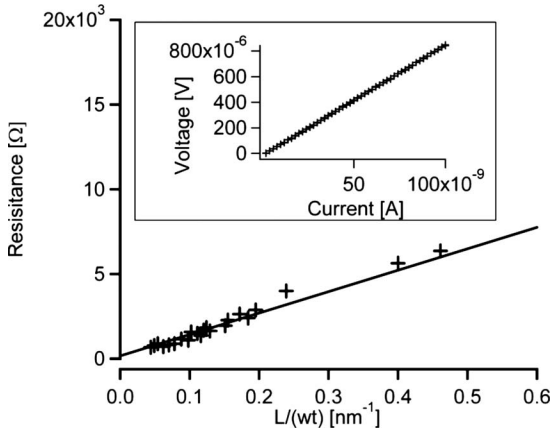

FIG. 3. Plot of resistance vs the ratio of number of squares to thickness for wires with various aspect ratios deposited in the same step. The extracted resistivity from the linear fit is 1.2×10^{-3} Ω cm and is independent of wire dimensions. The inset shows a typical current-voltage characteristic, linear for all measured NWs.

standard lithography,[17] the resistivity is independent of the NW dimensions and a factor of 3 better for the smallest wires. The resistivity value is comparable to that of evaporated thin films[18] and only an order of magnitude larger than that of bulk Bi.[19]

IV. CONCLUSION

Conducting Bi NWs were fabricated using stencil lithography for the first time, reaching critical dimensions below 50 nm. The NW thickness is correlated with its width when the amount of material deposited is on the order of the NW width. This is due to the accumulation of Bi on the stencil apertures during evaporation, which leads to their eventual clogging. This effect also modulates the mean grain size, with smaller grains corresponding to thinner NWs. The NW morphology was explored using SEM and AFM techniques. The NW resistivity was extracted from fitting a linear curve to the electrical resistance versus the ratio of the number of squares to thickness and was found to be 1.2×10^{-3} Ω cm and size independent.

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