Investigation of Strain Profile Optimization in Gate-All-Around Suspended Silicon Nanowire FET

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***Abstract*— In this paper, we investigate the optimization of tensile strain caused by thermal oxidation in a doubly-clamped silicon nanowire FET to enhance the mobility of its carriers. Spacer technology combined with sacrificial oxidations was used to fabricate ≈ 100 nm wide nanowires. The temperature and the duration of sacrificial wet oxidation are the main parameters that determine the induced strain. The strain in the nanowire will be measured using Raman spectroscopy at various stages during fabrication to evaluate the strain build-up throughout processes.**

I. Introduction

Multiple-gate architectures are foreseen as a possible replacement for planar CMOS [1], to overcome the issues related to short channel effects [2]-[3] as a result of the improved gate control, and thereby allow for continued downscaling of electronic devices.

In general, there are two technologies to fabricate nanowires: bottom-up that includes the growing or self-assembly of wires onto the substrate, and top-down that consists of typical micromachining processes on the substrate e.g. lithography and etching to create suspended nanowires [4]-[8]. In the present work, a top-down technology, described in [5] is used to fabricate suspended nanowires, which may be either tri-gate or gate-all-around.

Inducing a tensile strain in the channel of NMOS devices and a compressive strain in the channel of PMOS devices are typical ways to boost the performance by increasing the mobility of carriers [9]-[13]. In the present work we focus on NMOS devices only, thus we are only considering tensile strain. There are several ways to induce tensile strain in the silicon channel. In CMOS technologies either stressor technologies such as SiGe source/drain for compressive strain and SiC source/drain for tensile strain or contact etch stop layers are used, as well as alternative substrates [10]-[11], [14]-[23]. For research a common way to correlate stress and mobility is by die bending [24], but this is not a technology suited for fabrication. Here we induce tensile strain into a nanowire by wire bending as a result of oxidation, the mobility of the carriers for NMOS devices increases.

In this paper, we focus on investigation of important parameters e.g. the conditions of oxidation on this built-in tensile strain in a top-down fabricated nanowire called a bended gate-all-around nanowire FET (see fig. 1). To investigate the built-in strain in the channel during the process, Raman spectroscopy can be used. Electrical characterization of the previous fabricated and evaluated devices shows mobility enhancement of about 100% [25].

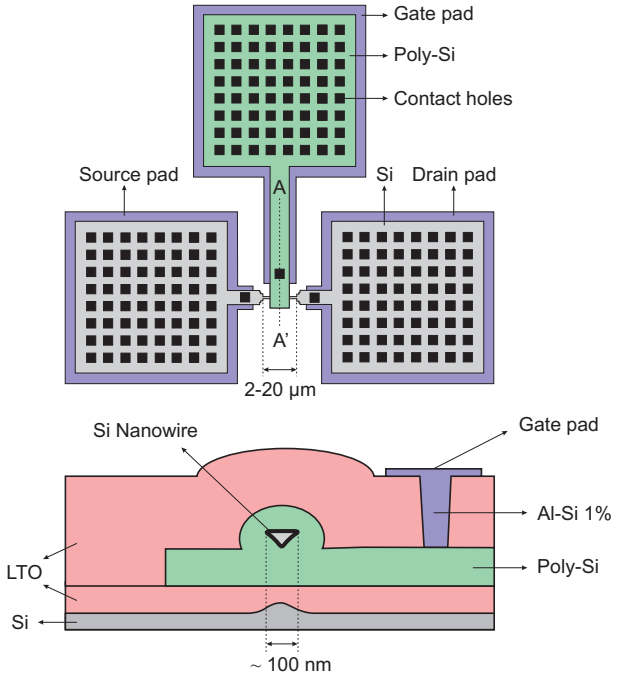

Fig. 1. Schematic of the design of gate-all-around suspended silicon nanowire FET (top); Cross-section A-A' of the device (bottom).

II. Design and top-down fabrication of a bended nanowire FET

The main steps in the process of the gate-all-around wires are presented in fig. 2; the process is verified using 2D process emulation by TCAD Dios (see fig. 3). The process was started by dry oxidation of 100 mm (100) silicon wafers at $1000\,^{\circ}C$ to produce 15 nm of oxide and followed by LPCVD deposition of 80 nm of nitride. After hard mask creation, the designed pattern was transferred on the wafer using 0.8 μm resolution

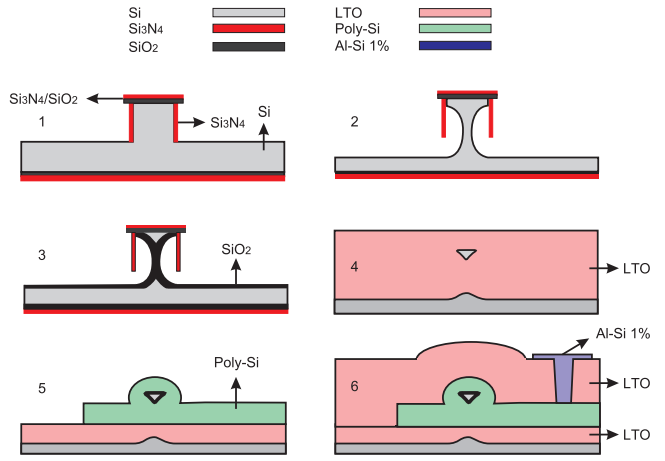

Fig. 2. Main steps in the process of the GAA nanowires: (1) Lithography, dry etching of hard mask and silicon to make the rib, nitride deposition and anisotropic dry etching of nitride to create the spacer layer, (2) Dry isotropic etching of silicon, (3) Sacrificial wet oxidation of silicon, (4) Wet etching of hard mask, LTO deposition and CMP planarization, (5) Thinning the LTO layer using BHF, dry oxidation (gate-oxide), LPCVD poly-Si deposition, $POCl_3$ doping, BHF etching of $POCl_3$, photolithography and poly-Si dry etching (6) P implantation, LTO deposition, lithography and dry etching to make contact holes, metallization, lithography and dry etching of metal.

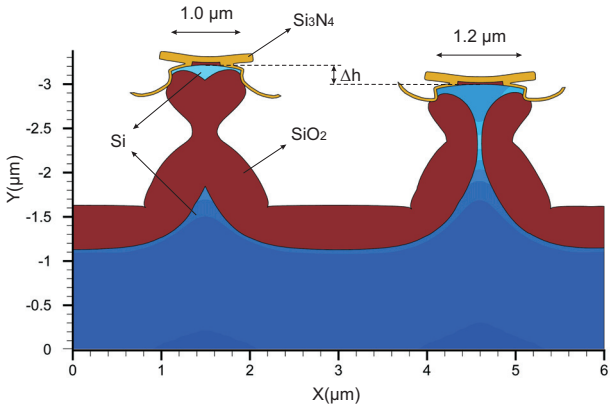

Fig. 3. 2D process emulation using TCAD Dios done to verify the process flow (the snapshot of the process emulation after the third step of the process presented in fig. 2). The height difference between the top of the disconnected wire and the connected wire to the substrate (Δh) represents indirectly the induced strain during sacrificial wet oxidation.

lithography. The pattern consists of different wires with 0.8-1.8 μm variation in width and 2-20 μm variation in length. The hard mask was etched using an anisotropic fluorine based dry etching to create a hard mask pattern and the dry etching was continued with a different recipe to etch silicon to create 300-400 nm high ribs. A sacrificial wet oxidation step was done to oxidize the side walls to create 300 nm of oxide and the oxide was etched using a BHF solution ($NH_4F(40\%) : HF(49\%)$ [7:1]) to create the needed undercut for the creation of spacer layer on the side walls and make the side walls smoother. A layer of 35 nm of nitride was deposited on the wafer using LPCVD and the nitride was etched anisotropically using a fluorine based dry etching to keep the nitride layer only on the side walls of the ribs to create the spacer layer. Silicon was etched isotropically using dry etching to create the first wire shape. Fig. 4 represents the cross-section of this first wire shape taken by FIB-cut.

A sacrificial oxidation was done to oxidize the silicon between the wire and the substrate and also to decrease the dimension of the wire. This oxidation is the main step that determines the induced tensile strain into the nanowire. After removing the hard mask and oxide using a pure HF solution, the wires were released and significant bending could be observed because of volume expansion of the oxide. However, the induced bending was also observed after oxidation of a nanowire disconnected from the substrate (before the oxidation step) using only silicon dry etching (see fig. 5). The conditions of this oxidation step can determine the induced tensile strain on the wire.

Before metallization, a gate stack including a 10-20 nm gate oxide and a poly silicon layer with an approximate thickness of 500 nm will be created around the suspended wire, but

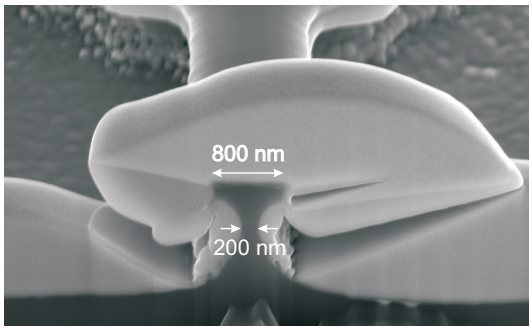

Fig. 4. The cross-section of the first wire shape created by dry silicon etching taken by FIB-cut.

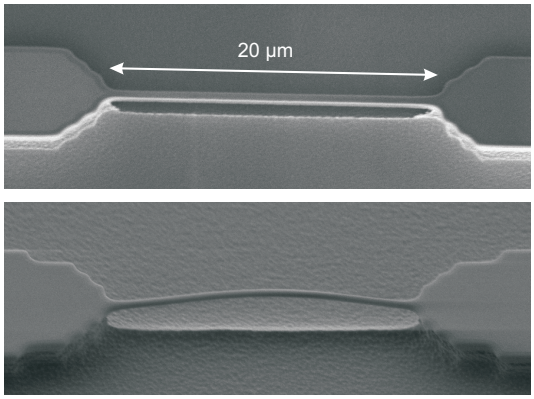

Fig. 5. SEM picture of a 20 μm long suspended nanowire before oxidation (top) and after oxidation at 850^oC (bottom).

TABLE I

THE PROCESSES TO STUDY, OPTIMIZE AND CONTROL THE INDUCED TENSILE STRAIN.

Process	Hard mask (nm)	Spacer (nm)	T(oxidation) ($°C$)
I	nitride (80)/oxide (15)	nitride (35)	850
II	nitride (80)/oxide (15)	nitride (35)	1050
III	nitride (150)/oxide (15)	nitride (35)	850
IV	nitride (250)/oxide (15)	nitride (35)	1050
V	oxide (500)	oxide (300)	850
VI	oxide (500)	oxide (300)	1050

the present work aims to investigate the strain build-up in the wires, in order to allow us to control and optimize it to eventually improve device performance.

III. STRAIN INVESTIGATION IN BENDED NANOWIRES USING RAMAN-SPECTROSCOPY

Optimization of built-in strain during processing is the first goal of this project. Raman spectroscopy can be used to measure strain and stress directly along a nanowire. In the intensity-wavenumber curves, down-shift and up-shift of the wavenumber correspond to tensile and compressive stress, respectively. Because of the penetration depth of about 760 nm of its 514 nm laser, it is possible to recognize the interactions between phonons and atoms from the nanowire and the substrate and therefore, measure the presence of strain or stress inside the wire.

To investigate, understand and exploit the strain development throughout the process the following studies will be done:

- Oxidation with different conditions on duration and temperature e.g. temperatures in the rage of $800 - 1100°C$.
- The type of hard mask and spacer and their thicknesses.
- LTO deposition conditions e.g. temperature and duration.

Table I also represents some of the conditions. The processes are in progress and strain measurement should be done after each sacrificial oxidation, hard mask removal and thinning the LTO layer step. Fig. 6 represents one of the typical stress profiles along a 20 μm long silicon nanowire after oxidation at $1000°C$.

It is also reported that for the nanowires with the length of 5-20 μm fabricated using the same technology, the built-in stress is in the range of 200 MPa to 4 GPa [5]. However, previously we have not monitored the development of the stress throughout the processing, nor have we tried to optimize or control it. Thus, the purpose of the current work is to understand and control the stress during the process, in order to be able to further optimize device mobility.

Usually there is a non-uniform strain profile along the wire and in a test, the maximums of stress were observed at the ends of the nanowire and the strain was almost constant in the rest parts of the wire (see fig. 6). However, shorter wires have presented a quasi-parabolic profile [25].

It is also reported in our previous work [25] that strain increases when decreasing the width of the wire and increasing

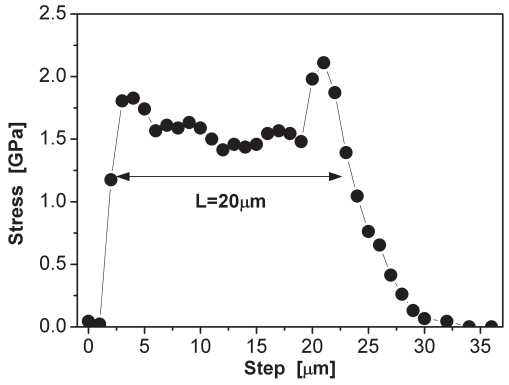

Fig. 6. Tensile stress measurement using Raman spectroscopy along a 20 μm long wire.

the length of the wire, the length dependence might be partly due to longer wires also being thinner for a given design width [5]. E-beam lithography can be used to obtain high resolution thin structures to be able to possibly get a higher strain.

IV. ROUNDING THE SHARP CORNERS RESULTING FROM DRY ETCHING

Rounding the sharp corners of the nanowire resulting from dry etching of silicon is another goal of the project. Having the sharp corners may result in a thinner gate oxide in the sharp corners. Because of also having a greater electric field in the corners, rounding the corners is essential to improve device reliability.

Silicon migration in hydrogen ambient at high temperature is one of the solutions [26], which will be investigated. Other solutions e.g. etching of sharp corners using silicon wet etching with TMAH ($(CH_3)_4NOH$), Trilogy ($HNO_3/NH_4F/H_2O$), HNA ($HF/HNO_3/CH_3COOH$), $NH_3(aq)$ or hydrazine are also possible but it is not our prime interest because of the associate silicon consumption mechanism on the nanowire. In the silicon migration mechanism, hydrogen atoms act as catalyst to help the silicon atoms migrate to the places leading a lower Gibbs energy level, due to increasing interaction with more silicon atoms in the rounded areas than in the sharp areas.

This rounding corner step can be done as an additional step after sacrificial oxidation and hard mask removal steps represented in the 4th step of the process flow of fig. 2. This will also be investigated as part of this work in the future.

V. CONCLUSION AND FUTURE WORK

Investigation, understanding and exploitation of the strain during the process is the main goal of this project which is in progress. Afterwards, we will evaluate rounding the sharp corners of the nanowire resulting from silicon dry etching using the silicon migration mechanism in hydrogen ambient at high temperature. The input from both strain evolution and corner rounding will then be used to further optimize the device design accordingly. Finally, multi-finger structures and dense array of wires could be the further steps.

ACKNOWLEDGMENT

This work is partially funded by the Nanosil European network of excellence (FP7).

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