Pentacene - SiO_2 Interface: Role of the Environment Prior to Pentacene Deposition and Its Impact on TFT DC Characteristics

N. V. Cvetković, D. Tsamados, K. Sidler, J. Brugger and A. M. Ionescu

Abstract – In this paper we report on the effect of the environment on the SiO_2/pentacene interface. Two batches of bottom-contact pentacene thin-film transistors have been fabricated with a 100 nm thick SiO_2 as dielectric. Considerable shifts of the threshold voltages have been observed for the TFTs whose dielectric surface has been exposed to air for long periods of storage before depositing the pentacene layer. Based on reports from other research groups in the field, we consider that long exposure of the SiO_2 to air may have the same effect on the SiO_2-pentace interface as short but more aggressive oxygen plasma treatment.

I. Introduction

In recent years several research teams reported on the physics behind the modifications of pentacene TFT characteristics due to humidity and oxygen effects on the pentacene itself, as well as to the dielectric-pentacene interface [1-3]. Threshold voltage shifts are the most pronounced effects and are related to charge transfer from the pentacene molecules to traps located at the interface with the dielectric or in the dielectric itself. Some groups have also investigated the role of oxygen plasma treatment in the creation of residual charges at the SiO_2 surface [5-6]. In this work we have observed that prolonged exposure of the SiO_2 to ambient air can significantly change the behavior of the pentacene devices, causing threshold voltage shifts comparable to those detected after treatment by oxygen plasma of the SiO_2 surface prior to the deposition of the pentacene layer.

II. Experimental Results

Organic TFTs (OTFTs) with two different channel widths (W = 100 µm and 500 µm) and a channel length of L = 3µm were fabricated using commercial pentacene provided by Sigma-Aldrich without any supplementary purification. The bottom-contact transistors were built on a p-type Si wafer with resistivity in the range 1-100 Ohm•cm, with 100 nm of dry SiO_2 as the gate dielectric layer, which was exposed to air for approximately eight months. After this storage period, 50 nm thick gold contacts were deposited and patterned. A 50 nm thick pentacene layer has been deposited at room temperature on top of the SiO_2 dielectric using a Univex 450B thermal evaporator. A second group of transistors was fabricated using the same process, but this time on fresh 100 nm thick dry SiO_2 and used as a reference for the comparison with the first batch of TFTs. A 3D representation of the transistor architecture is presented in Fig. 1.

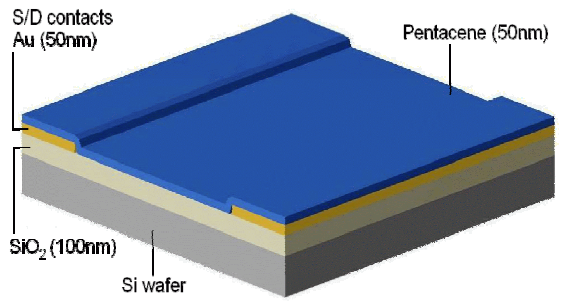

Figure 1: 3D schematic of the fabricated transistors.

The pentacene TFT DC characterization has been performed using an Agilent™ 4156C parameter analyzer on a Cascade™ probing system. The bottom of the wafer was used as the back-gate electrode.

In all the measurements the drain bias value used was V_{DS} = 1V. The extrapolated threshold voltages extracted from $I_D(V_G)$ transfer characteristics were V_T = +16.3V, and V_T = + 15.1V, (Fig.2 and 3 respectively).

The transconductance g_m was also calculated from the same curves, and the values were $g_m = 1.26 \cdot 10^{-9}$ S, and $g_m = 7.37 \cdot 10^{-9}$ S (Fig.2, 3 respectively). The equivalent reference TFTs (right hand side curves in Fig.2,3) had V_T = -7.3V, $g_m = 1.72 \cdot 10^{-9}$S and V_T = -8.1 V, $g_m = 0.82 \cdot 10^{-9}$ S respectively. Fig. 4 and 5 show that I_{on}/I_{off} ratios are ~4 decades for transistor with shifted characteristics and ~2-3 decades for the reference transistors. As I_{off} of the first group of devices we consider the minimum current which occurs at V_G < -20 V in our case. The subthreshold swing was also extrapolated and the obtained values were S ≈ 2

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V/dec (Fig. 4) for the 100 μm-wide OTFTs, and S ≈ 1.4 V/dec for the 500 μm-wide devices (Fig. 5). The hole mobility μ values have been extracted using the method of $I_D/g_m^{1/2}$ in order to avoid the influence of the series resistance R_{SD} at the source and drain (assuming that R_{SD} does not depend on V_G) [4]. For the transistors of the first group we obtain mobilities in the range $\mu = 6{,}8\cdot10^{-4}$ cm²/V/s to $1{,}3\cdot10^{-3}$ cm²/V/s, and for the reference transistors $\mu = 1.1\cdot10^{-4}$ cm²/V/s to $4.4\cdot10^{-4}$ cm²/V/s. All the data and values are summarized in Table I.

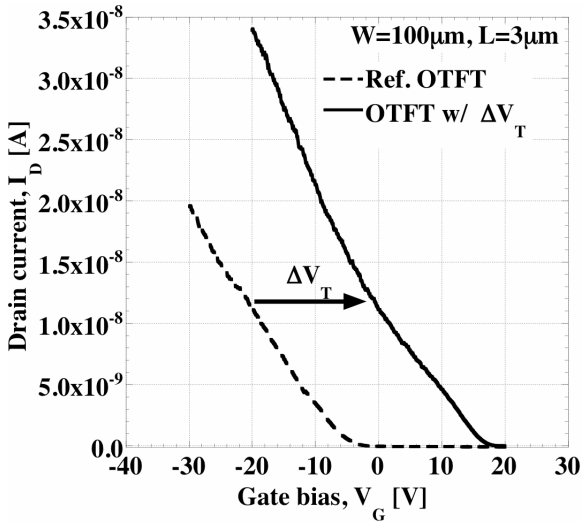

Figure 2: $I_D(V_G)$ transfer characteristics of the pentacene transistor with L = 3μm, W = 100μm. The right, shifted curve, belongs to first group of OTFTs, and the left to reference group of OTFTs.

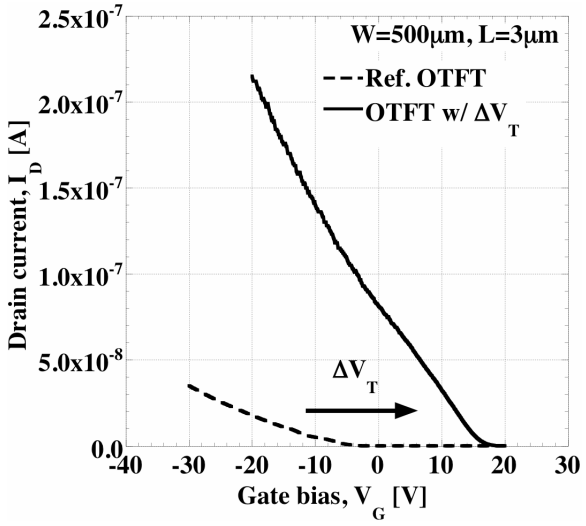

Figure 3: $I_D(V_G)$ transfer characteristics of the pentacene transistor with L = 3μm, W = 500 μm. The right, shifted curve belongs to first group of OTFTs, and the left to reference group of OTFTs.

TABLE I:
PHYSICAL PARAMETERS EXTRACTED FROM $I_D(V_G)$ CURVES

	First group OTFTs		Reference OTFTs	
W [μm]	**100**	**500**	**100**	**500**
L [μm]	**3**	**3**	**3**	**3**
μ [cm²/V/s]	$6.8\cdot10^{-4}$-$1.3\cdot10^{-3}$		$1.6\cdot10^{-4}$-$4.4\cdot10^{-4}$	
g_m [S]	$1.26\cdot10^{-9}$	$7.37\cdot10^{-9}$	$1.72\cdot10^{-9}$	$0.82\cdot10^{-9}$
S [V/dec]	~2	~1.4	~2	~1.4
I_{on}/I_{off}	~3-4 dec		2-3 dec	
V_T [V]	+16.3	+15.1	-7.3	-8.1

III. DISCUSSION

Examining the transfer characteristics of the two groups of OTFTs, we observed a threshold voltage shift ΔV_T is of the order of 23 V, shifting from negative V_Ts (for the reference group) to positive values (for the first group). In addition, the mobility is also affected having slightly higher values for the first group of devices (those with prolonged exposure to air). One can find very similar behavior in the literature [6] where SiO_2 surfaces are treated with oxygen plasma. In that case, one can observe big shifts of V_T accompanied by an increase in the field-effect mobility. It appears that oxygen plasma increases considerably the concentration of residual charges at the SiO_2. This has as a result the creation of free carriers (holes) in pentacene even for positive values of V_G, as it is the case for our samples. We think that the long exposure to air, and consequently to O_2 of the SiO_2 surface prior to pentacene deposition has the same effect as the oxygen plasma in [6].

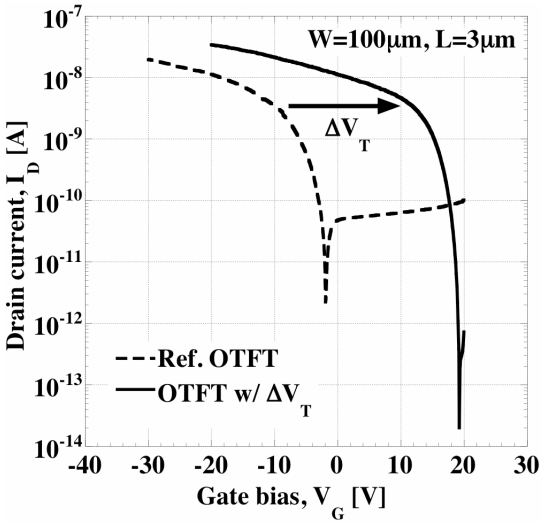

Figure 4: $I_D(V_G)$ curve in log scale, transfer characteristics of the pentacene transistor with L = 3 μm, W = 100 μm. The right, shifted curve belongs to first group of OTFTs, and the left to reference group of OTFTs.

According to [6], the field effect mobility becomes limited by the counter-ions from the surface recombination centers that are non-saturated. When the concentration of residual charges at the SiO_2 surface increases over a certain value, the mobility increases too, as the density of the residual charges may be enough to screen those counter-ions. The increased mobility of the first group of devices indicates that in our case the same explanation could apply.

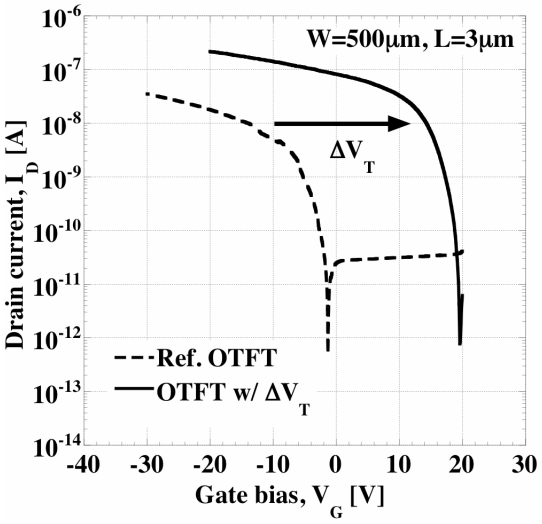

Figure 5: I_D-V_G curve in log scale, transfer characteristics of the pentacene transistor with L=3μm, W=500μm. The right curve belongs to the first group of OTFTs, and the left to reference group.

One point contradicting with [6] for our devices is that the I_{ON}/I_{OFF} ratio for the first group of devices is higher than for the reference transistors. According to [6], when the number of residual charges increases and the channel becomes conductive even for positive V_G, the I_{ON}/I_{OFF} ratio decreases, whereas in our case we observe an increase. This discrepancy could be explained by the role of the contact resistances at the source and drain regions. The existence of residual charges improves in general the contact resistances, resulting in higher I_{ON} currents. It is possible that our reference transistors suffer from higher contact resistances limiting consequently the I_{ON} and I_{ON}/I_{OFF} ratios.

IV. Conclusion

We have fabricated two groups of pentacene TFTs, one with deposited pentacene on fresh SiO_2 and the other on a SiO_2 layer exposed to air for a period of eight months. The characteristics of the two groups of devices are greatly different showing big shifts of the threshold voltages and moderate changes in mobility. Based on reports of other groups that have observed similar behavior after oxygen plasma treatment of the SiO_2 surface we conclude that the prolonged exposure of the SiO_2 to the oxygen from the ambient air has the same effect as oxygen plasma treatment. The creation of residual charges is at the origin of the V_T shifts as well as of the changes in mobility. As a result, the environment prior to pentacene deposition greatly impacts the SiO_2-pentacene interface, and consequently the TFT DC characteristics. It is therefore of crucial importance during fabrication of pentacene TFT to minimize the time the SiO_2 is exposed to oxygen before depositing the pentacene layer as this can have detrimental effects on the devices and circuits.

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References

[1] Wang et al., "Tunable threshold voltage and flatband voltage in pentacene field effect transistors.", Appl. Phys. Lett., 89(11), pp.112109-3, 2006.

[2] D. Li et al., "Humidity effect on electrical performance of organic thin-film transistors." Appl. Phys. Lett., 86(4), pp.042105-3, 2005.

[3] A. Benor et al., "Electrical stability of pentacene thin film transistors", Organic Electronics, 8(6), pp. 749-758, December 2007.

[4] G. Ghibaudo, "New method for the extraction of MOSFET parameters", Electronics Letters, 24(9), pp. 543-545, 1988

[5] M. Daraktchiev et al., "Ultrathin organic transistors on oxide surfaces," New J. Phys., 7, p.133, 2005.

[6] A. von Mühlenen et al., "Controlling charge-transfer at the gate interface of organic field-effect transistors", Phys. Rev. B, 75(11), p.115338, 2007.