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Investigation of oxidation-induced strain in a top-down Si nanowire platform

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ABSTRACT

In this paper, we investigate the effect of different process parameters on oxidation-induced strain (OIS) into a doubly-clamped silicon nanowire FET to control and finally, enhance carrier mobility. Spacer technology together with sacrificial thermal oxidation were used to fabricate ≈100 nm wide Si NWs. The built-in tensile stress in the Si NWs was measured using micro-Raman spectroscopy and a maximum of 2.6 GPa was found.

1. Introduction

Up to now, there are a few reported ways to induce tensile strain into suspended Si NWs or into Si NWs standing on the BOX layer e.g. using SSDOI wafers [1], metal gate [2], and built-in tensile stress induced during thermal oxidation [3–5]. Gate-all-around Si NW with uniaxial tension direction promise both control of n-MOSFET electrostatics, for ultimate device scalability, and enhanced performance.

In this work, we focus on oxidation-induced strain into Si NWs which was originally found in [3]. According to Pyzyna et al. [6], by oxidation of suspended and naked Si nanobeams and afterwards, stripping the grown oxide, an accumulation of tensile strain can be engineered. The origin of the tensile strain was still unknown but it was assumed to be associated with the injection of self-interstitial silicon atoms from the oxidation front during oxidation [6]. In [3], the omega-shaped Si wires with a nitride hard mask on top, created from bulk Si using spacer technology and isotropic Si etching, were oxidized and after stripping the hard mask and the grown oxide, unexplained buckling was reported. We originally report on the effect of oxidation conditions on OIS into the Si NWs after oxidation and after stripping the hard mask and the grown oxide to be able to optimize stress and finally, similar to [1,3], enhance the mobility of carriers in gate-all-around suspended Si NW FETs.

2. Fabrication of suspended strained-Si NWs using bulk Si

The process flow of suspended strained-Si NWs is schematically shown and described in Fig. 1. The process flow has been verified earlier by 2D process simulations using TCAD Dios version 10.0 [7] and Sentaurus Process version A-2007.12. As the first step, 100 mm (1 0 0) bulk silicon wafers were oxidized using dry oxidation at 950 °C to grow 15 nm of oxide and afterwards, 80 nm of silicon nitride was deposited using LPCVD at 770 °C to create the hard mask. The designed pattern, all with $[\bar{1}\,1\,0]$ channel direction, was transferred directly on the wafers using 0.8 μm resolution lithography. In the design, the width and the length of the wires vary from 0.8 to 1.8 μm and 2.0 to 20.0 μm, respectively. To create a pattern of hard mask, the hard mask was etched using anisotropic fluorine based dry etching. Afterwards, Si was etched anisotropically to create 300–400 nm high ribs. A sacrificial wet oxidation at 850 °C was done to nominally oxidize 135 nm of silicon side walls and the oxidized sidewalls were etched using a BHF solution (NH_4F(40%) : HF(49%) [7:1]). Afterwards, 35 nm of silicon nitride was isotropically deposited on the wafer using LPCVD at 770 °C. The nitride was etched anisotropically using a fluorine based dry etching to keep the nitride layer only on the sidewalls and on the top of the ribs as a protection layer. Silicon was etched isotropically using dry etching to create the first wire shape and to at least suspend the 0.8 μm wide wires. To decrease the dimension of the wire and also to oxidize the remained silicon between the wire and the substrate, the wires were thermally oxidized to nominally consume 135 nm of silicon. In this step, two oxidation temperatures were investigated (wet oxidation at 850 and 1050 °C). Figs. 2 and 3 represent the status of the wires after wet oxidation at 850 °C. After stripping the hard mask and the grown oxide layer using a 49% HF solution, the 0.8 and 1.0 μm wide wires (W08 and W10) were released and a significant bending was observed.

Finally, a typical CMOS process can be used to prepare the polysilicon/oxide gate stack including implantation, isolation and metallization to finalize the suspended strained-Si NW FETs.

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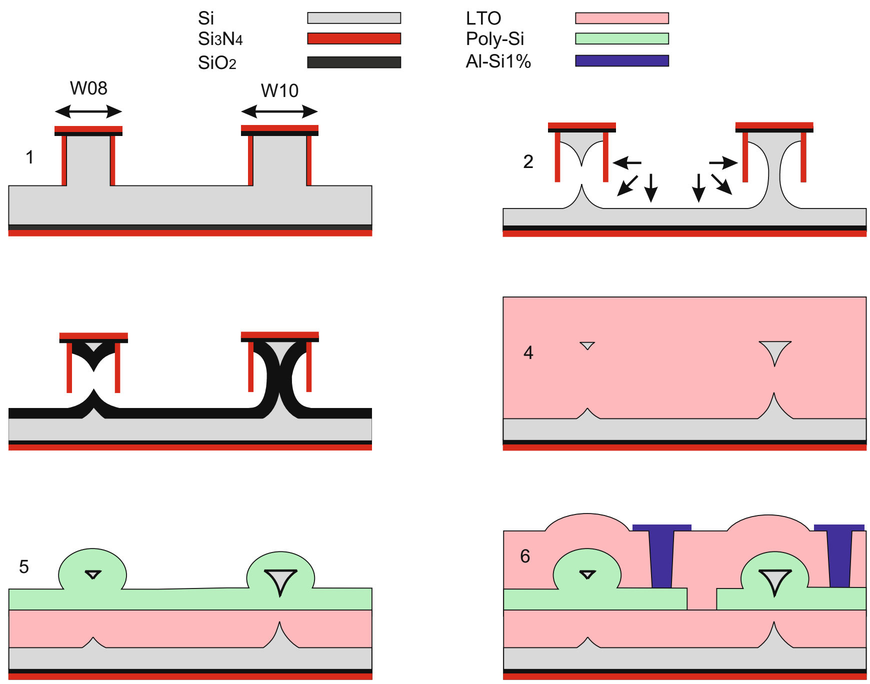

Fig. 1. The CMOS process flow to make FETs from a top-down Si nanowire platform. W08 and W10 represent the initial 0.8 and 1.0 μm width of the wires on the designed mask, respectively.

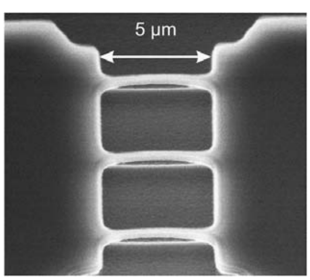

Fig. 2. SEM image of a suspended W08 Si NW with a nitride hard mask after wet oxidation at 850 °C. The buckling is obvious in the presence of hard mask.

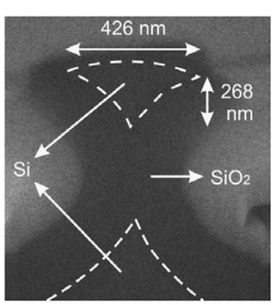

Fig. 3. SEM image of the cross-section of a W10 wire, prepared using FIB-cut, after wet oxidation at 850 °C.

3. Stress characterization of suspended strained-Si NWs using micro-Raman spectroscopy

Micro-Raman spectroscopy was used to measure oxidation-induced strain in the Si nanowires after oxidation and after the stripping step. The measurements were done along and across the wires, all at 20 °C, and the downshift of the Raman signal was translated to the value of tensile stress (see Fig. 4).

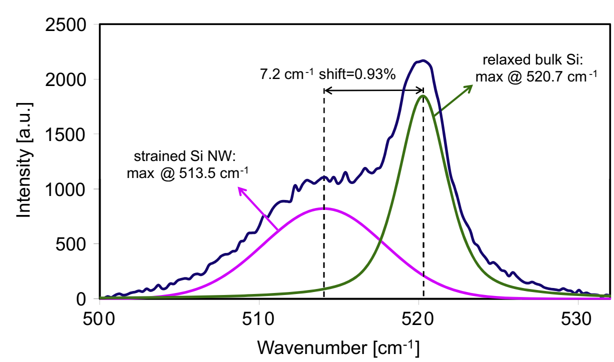

Fig. 4. Micro-Raman spectra at the middle of a 10 μm long W08 Si NW after wet oxidation at 850 °C and stripping steps. The downshift in the wavenumber represents the tensile strain value in the wire.

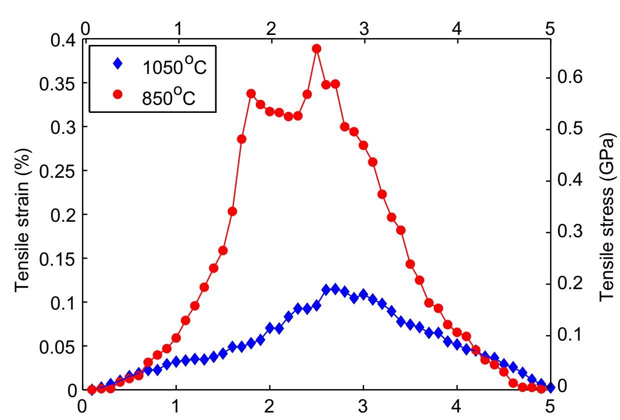

Fig. 5. Tensile strain along two 5 m long W08 Si NWs after wet oxidation (at 850 °C and 1050 °C to nominally grow 300 nm of SiO_2) and stripping steps.

Fig. 5 represents the measured strain values along two 5.0 µm long Si NWs after sacrificial oxidation (to nominally consume 135 nm of Si using wet oxidation) and stripping steps. Both curves represent a non-uniform and almost symmetric distribution of stress along the wires with a maximum almost at the middle of the wire, explained in part by a non-uniform and symmetric distribution of Si thickness along the NW (being thinner at the middle) and by the role of fixed anchors combined with lattice expansion during the oxidation of the suspended wires.

Figs. 6–8 represent approximately the maximum value of stress on different wire lengths after different process conditions. In order to improve the reliability of strain measurement (avoid effect of small vibrations of the optical table that can disturb the place of the laser spot on the beam) these measurements have been done across the wire at the points *x* = 0.25 L and *x* = 0.50 L and the maxima of the measurements were used in the plots.

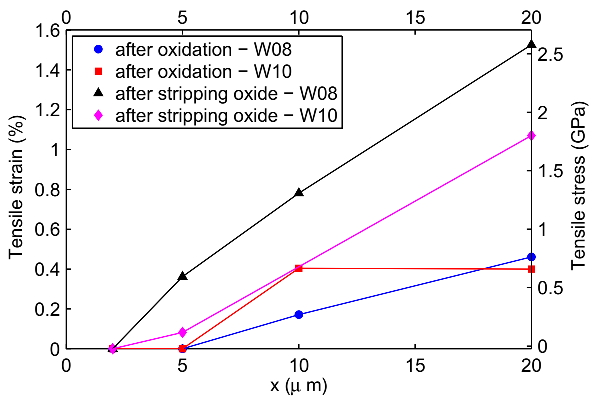

Fig. 6. The peak of tensile strain along four W08 and W10 Si NWs after wet oxidation at 850 °C and after the stripping step.

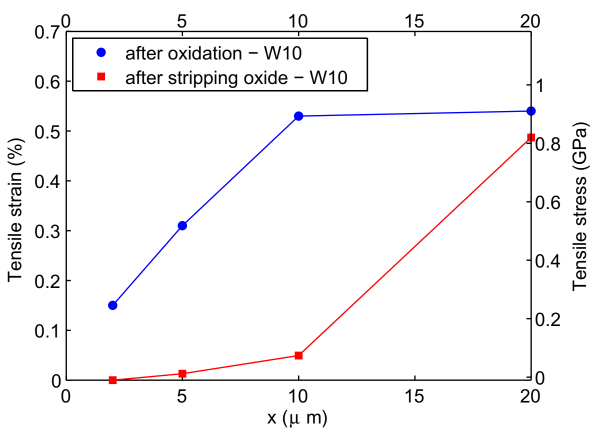

Fig. 7. The peak of tensile strain along two W10 Si NWs after wet oxidation at 1050 °C and after the stripping step.

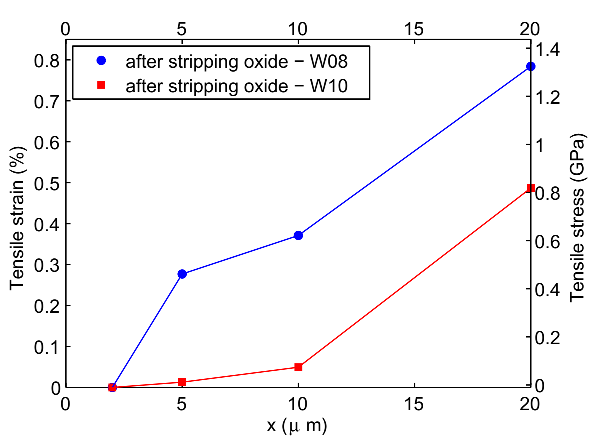

Fig. 8. The peak of tensile strain along two W08 and W10 Si NWs after wet oxidation at 1050 °C and stripping steps.

4. Results and discussion

4.1. Oxidation and strain

The Si NWs covered with a nitride hard mask have shown a tensile strain after the oxidation step at different temperatures because of growth strain, thermal strain and oxidation-induced strain (OIS). The induced tensile growth strain to the Si NW is due to having more molar volume in the growing oxide during consuming Si in the oxidation [8]. Mismatch on thermal expansion coefficients of Silicon and oxide leads also to have more tensile stress in the Si nanowire during cooling down from the oxidation temperature to room temperature [8]. According to [6], a small value of tensile strain also will be accumulated in the Si NW possibly because of the injection of self-interstitial silicon atoms from the oxidation front during oxidation. This part shows itself clearly after stripping the oxide layers with compressive forces inside [8]. For this platform, the level of strain of Si NWs after the oxidation step depends on the width and the length of the wires (see Fig. 6). However, the practical curves show that the level of tensile strain in Si NW is limited to about 0.5–0.6%.

For the process with the oxidation step at 850 °C, a significant increase in the level of tensile strain was observed after stripping the hard mask and the oxide (see Fig. 6). The main source of this stress seems to be due to releasing the stored potential energy in the buckled wire due to restrictions during bending because of a tensile hard mask (nitride) and restrictions on elongation because of dually clamped platform. After stripping the thermal oxide and the hard mask, the sources of growth stress and thermal stress disappear [8] but the wire buckles more perhaps to release the major parts of this stored potential energy by mechanical buckling to be more stable. The final level of strain in the Si NW could be estimated by $\varepsilon_f = \varepsilon_i + \varepsilon_{\text{OIS-SF}} + \varepsilon_{\text{OIS-pot}}$. Where ε_i is the intrinsic strain in the Si NW before oxidation, $\varepsilon_{\text{OIS-SF}}$ is OIS because of perhaps the injection of self-interstitial Si atoms and $\varepsilon_{\text{OIS-pot}}$ is OIS because of the potential energy, stored during oxidation and released during stripping the hard mask.

For the process with the oxidation step at 1050 °C, the level of stress diminishes after stripping the hard mask and the oxide. This is perhaps due to significant viscous flow of oxide and therefore, viscoelastic relaxation in the growing oxide layer and in the thin oxide layer of the hard mask occurring at temperatures higher than the glass transient temperature of SiO_2 (960 °C) causing relaxation of tensile strain in the Si NW [4] and also reducing the stored potential energy during consuming Si in the oxide growth step at high temperature and also during cooling down to room temperature. After hard mask removal, the level of tensile stress drops (see Fig. 7). This is perhaps due to having less stored potential energy in the wire.

4.2. Stress and geometry

For this platform, all the experiments show that the induced tensile stress increases with the length of the wire (see Figs. 6–8). This can be due to the smaller critical load for buckling in longer wires. The critical load for buckling for a beam with *L* length, *t* thickness and Young's modulus of E can be calculated by $\sigma_{cr} = \frac{\pi^2}{3} \cdot E \cdot \left(\frac{t}{L}\right)^2$ [8]. However, for this bulk top-down Si NW platform, the shorter wires are wider and thicker because of pattern dependency of the Si dry etching processes. Therefore, for the current platform, it is not possible to only investigate the effect of length on strain, at constant width.

4.3. Oxidation of suspended wires

As described earlier, the fabrication process was done precisely to only suspend the W08 wires in the isotropic Si etching step and the etch depth and the dimensions of the wire were precisely measured using Tencor Alpha-Step 500 surface profiler, FIB-cut and SEM techniques. After consuming 135 nm of Si in the sacrificial oxidation step and afterwards, stripping the hard mask and the grown oxide, at least both W08 and W10 wires were suspended. After the stripping step, the W08 wires represented a higher strain peak than the W10 wires (see Figs. 6 and 8).

Volume expansion of the solid lattice during oxidation of the W10 wires creates out of plane forces pushing up the wire and causing buckling of the wire during sacrificial oxidation. However, volume expansion is not the only source of buckling because the suspended W08 wires were also buckled. The buckling of the W08 wires can be due to the induced tensile stress to the silicon layer during growing the thermal oxide layer and afterwards, cooling down the wire. According to Fig. 6, the level of strain for both W08 and W10 wires are approximately in the same order after sacrificial oxidation. But after hard mask removal, the W08 wires have shown a higher level of tensile strain than the W10 wires perhaps because of being thinner and therefore, having a smaller critical load for buckling.

5. Conclusion

The effect of oxidation temperature was experimentally investigated to find out the level of tensile strain after thermal oxidation of Si NWs and after stripping hard mask and oxide. Some possible sources behind the buckling after stripping the hard mask and the grown oxide are identified; *potential energy* stored in wires, *restrictions* in clamped–clamped design and *relaxation* of tensile strain are discussed. The optimized process resulting from this study will be used to control and enhance the mobility of carriers in suspended silicon NW FETs.

Acknowledgement

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