

HIGH-PERFORMANCE MICROMACHINED RF PLANAR INDUCTORS

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ABSTRACT

High-Q planar spiral inductors were fabricated by innovative micromachining processes based on sputtered Al or electroplated Ag on top of low-loss substrates. 3 μm -thick Al inductors on high-resistivity silicon (HRS) exhibited peak Q-factor of 30 at 5 GHz for corresponding inductance of 2.4 nH. A peak-Q of 70 at 3.8 GHz for 5.5 nH was obtained from a 10 μm -thick Ag device on glass. Measured data were accurately matched using a new equivalent model based on frequency-independent elements. The fabricated inductors are suitable building-blocks for high-performance RF passive circuits, such as low-insertion loss filters and baluns.

Keywords: Equivalent-circuit model, micromachining, planar inductor, Q-factor.

INTRODUCTION

Low power consumption is certainly one of the most stringent requirements to be met by new generation wireless communication systems. The Q-factor displayed by the numerous passive components of front-end transceivers plays a fundamental role on the overall power consumption of the portable electronic devices. Either in discrete or integrated form, inductors are essential passive components of every RF front-end. A high Q-factor is of utmost importance since it contributes to reduce phase noise in oscillators, power consumption in amplifiers and insertion loss in filters. Generally, the Q-factor exhibited by on-chip inductors fabricated in standard IC technologies is drastically limited by the RF power dissipation through the lossy silicon substrates and by the increase of the metal resistance as a consequence of the skin and proximity effects [1],[2]. Much effort has been devoted to the enhancement of inductor performance in terms of Q-factor and self-resonance by using insulating substrates [3] and by providing thick metal layers [4]. Reported surface micromachining developments have made possible to partially overcome substrate losses by fabricating suspended [5]-[7] or out-of-plane 3-D assembled structures [8],[9]. Although, these architectures exhibit the best performance published to date, fragility to shocks and encapsulation issues are serious bottlenecks that hinder their applications in RFIC's. This work presents the fabrication

and characterization of high-performance miniaturized planar inductors fabricated by innovative micromachining processes addressing paramount issues of power dissipation mechanisms and robustness. For boosting the achievable Q-factor, we investigated low-loss substrates, such as high-resistivity silicon (HRS) and glass. In addition, highly conductive metal layers were provided by sputter deposition of Al or electroplating of Ag. To our best knowledge, this is the first work reporting electroplated Ag inductors. The fabricated devices are dedicated to RF passive circuits, such as low-insertion loss filters and baluns.

FABRICATION

Inductors from 1 to 20 nH were designed for operating frequency above 1 GHz. High-frequency current crowding in metal tracks was mitigated by designing hollow circular spirals [2]. Fig. 1 shows the proposed planar inductor and summarizes the fabrication steps. Glass or HRS with resistivity of 3000 $\Omega\cdot\text{cm}$ were used as substrate materials. In order to insulate the device from the substrate, a thermal oxide film was grown on HRS. As a first step, 200 nm of Al were sputtered and patterned by wet-etching. The underpass thus formed will connect the RF port to the centre of the spiral. Next, 1 μm -thick SiO_2 was sputtered and via-holes through this dielectric layer were opened by dry-etching. We developed two different micromachining options for fabricating thick metal spirals. One was based on sputtered Al films patterned by a highly anisotropic dry-etching process. Structures with aspect ratios up to unity were obtained. This performance is essential for creating a minimum spacing between adjacent tracks of a spiral and consequently for maximizing the total inductance per unit area through an enhanced magnetic coupling. Fig. 2 shows a SEM close-up of a 3 μm -thick dry-etched Al spiral.

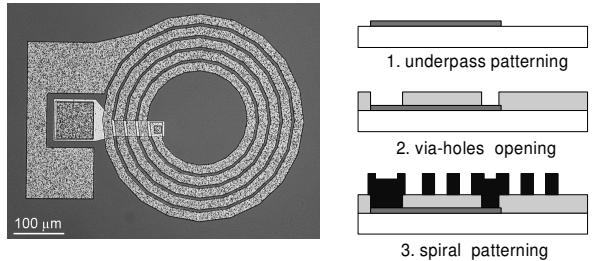


Fig. 1. Image of a fabricated single-port planar inductor (left) and schematic cross-section of the fabrication process (right).

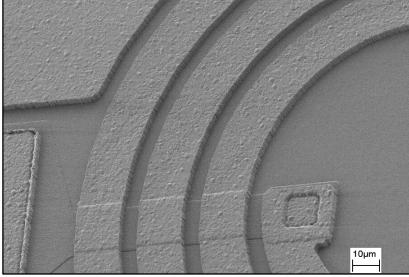


Fig. 2. SEM close-up of 3 μm -thick dry-etched Al tracks.

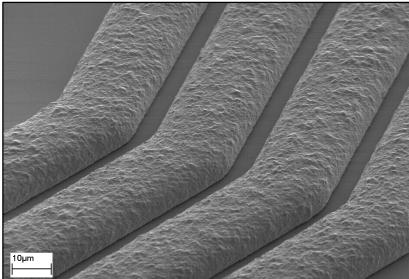


Fig. 3. SEM close-up of 10 μm -thick electroplated Ag tracks.

The second development based on Ag electroplating through polymer molds enabled the fabrication of spirals up to 10 μm -thick (see Fig. 3). In both processes, the fabrication steps did not exceed a temperature of 120°C.

MODELING

Fig. 4 depicts the conventional Π -type model used for simulating the impedance behavior vs. frequency of a two-port inductor on silicon [10]. The physical meaning of the lumped elements is the following: L_s and R_s are the series inductance and resistance, respectively. C_s models the parasitic capacitance due to the underpass-to-spiral coupling and to the fringing field between adjacent tracks. The network involving C_{ox} , R_{sub} and C_{sub} describes the RF losses through the substrate. Since glass and HRS have huge resistances values, R_{sub} , the impedance of the substrate network simply reduces to a single capacitance dominated by the smaller between C_{ox} and C_{sub} .

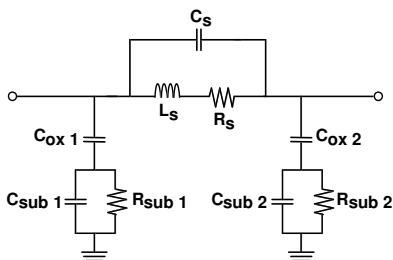


Fig. 4. Conventional Π -type model used for simulating the inductor behavior on silicon substrate.

A major limitation of the Π -model is the lack of a term describing the frequency-dependent increase of the metal resistance. We developed an equivalent model taking into account the skin-effect-like increase of the metal resistance as well as the losses occurring in the dielectric layer. The proposed 6-element compact model used for extracting the inductor parameters is depicted in Fig. 5. Here, a parallel R_f-L_f network mimics the skin-effect behavior of the conductor resistance [11]. Furthermore, compared to the conventional Π -model, our development presents a resistance R_d in series with C_s , accounting for the dielectric losses of this distributed capacitance. Since the proposed model is made of frequency-independent terms it can be implemented on simulators such as Agilent's IC-CAP.

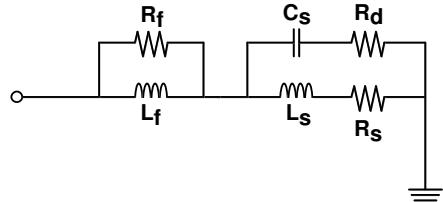


Fig. 5. Equivalent circuit of frequency-independent elements used for simulating the inductor behavior on a low-loss substrate.

RESULTS AND DISCUSSION

S-parameters were measured using a HP 8510C network analyzer and Süss-Rosenberger coplanar probes. A standard SOLT calibration was performed before the device characterization. The measurement was taken for each inductor from 50 MHz to 10 GHz in a linear scale of 25 MHz/step. Open structures were also measured in order to de-embed the inductance measurement from the parasitics associated to the probing pads. The Q-factor was taken as the ratio of imaginary part of impedance, $Im(Z)$ to the real part $Re(Z)$. This definition is meaningful when the inductor operating frequency is well below its self-resonance, f_{SR} .

Fig. 6 emphasizes the role of the substrate type on the measured RF characteristics by comparing two 3 μm -thick Al inductors having identical layouts, but fabricated on top of HRS and glass, respectively. The extracted parameters used for fitting the measured data are listed in Table 1. The inductor fabricated on glass exhibited a simulated peak Q-factor of 31 at 4.2 GHz and a f_{SR} of 9.1 GHz, whereas the peak-Q of its HRS counterpart was 21 at 3.5 GHz for a corresponding f_{SR} of 8 GHz. The insulating nature of glass suppresses energy dissipation. In addition, the roughly halved value of relative permittivity ($\epsilon_{r,glass} = 5-6$) compared to silicon ($\epsilon_{r,Si} = 11.7$), decreases the coupling capacitances. Both effects contribute to the improvement of over 30% of the Q-factor and to increase the self-resonance.

The equivalent inductance, L_s seems not to be affected by the substrate type since both the extracted values are almost identical. The difference observed between the extracted values of R_s is very likely due to a process variation, such as a slightly different metal thickness or conductivity. R_d is 29.9Ω for the inductor on HRS and 14.4Ω for the inductor of glass. This difference is a consequence of more severe RF losses due to the parasitic capacitance towards the HRS substrate. Simulated curves show an excellent agreement with experimental data all over the measured range.

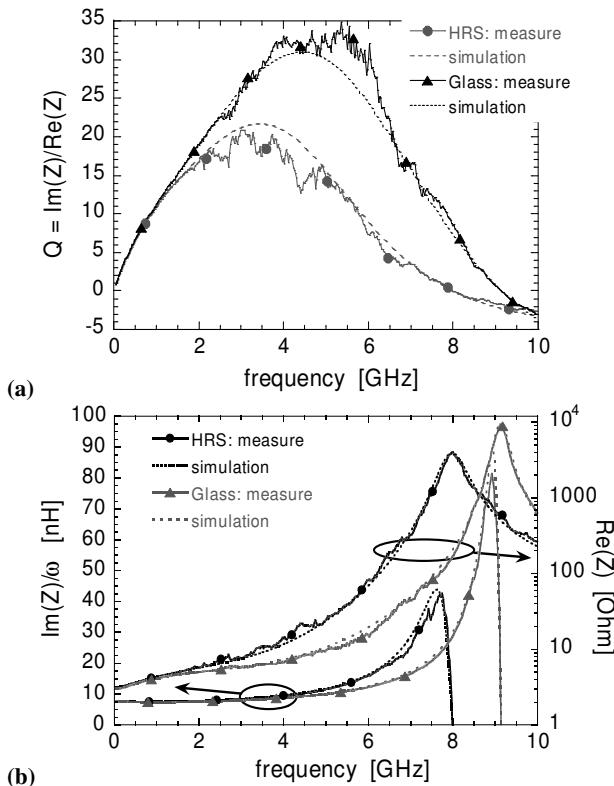


Fig. 6. (a) Q-factor : measure (full lines) vs. simulation (broken lines), (b) $\text{Im}(Z)/\omega$ and $\text{Re}(Z)$ of two $3 \mu\text{m}$ -thick Al inductors with identical layout fabricated on HRS and glass, respectively.

Table 1. Circuit parameters of the measured inductors of Fig. 6

Device	L_f [nH]	R_f [Ω]	L_s [nH]	R_s [Ω]	C_s [fF]	R_d [Ω]
HRS	0.33	2.89	7.19	3.19	55.5	29.9
Glass	0.35	2.03	7.16	2.99	42.42	14.4

Fig. 7 highlights the impact of the spiral conductivity on the device performance. The two curves correspond to a $3 \mu\text{m}$ -thick Al and $10 \mu\text{m}$ -thick Ag inductors with the same layout, fabricated on glass. Table 2 reports the extracted parameters. The Al inductor displayed a peak Q-factor of 36 at 3.9 GHz, whereas the peak-Q of its Ag counterpart

was 64 at 3.7 GHz. The huge Q improvement is already evident below 1 GHz, *i.e.*, where the inductor Q-factor is substantially determined by the metal resistance. As a general remark, the significant discrepancy observed between measured and simulated peak Q-factors is due to the lack of accuracy in measuring the reflection coefficient S_{11} in very high-Q devices [12]. The Ag inductor is self-resonating at 8.3 GHz that is about 0.4 GHz lower compared to the Al inductor. Here, the thicker Ag spiral is responsible for an increase of the parasitic interturn capacitance resulting in a lower f_{SR} , as confirmed by the higher extracted C_s values (see Table 2). The equivalent inductance, L_s of the Ag inductor is about 7% lower. This is possibly due to a weaker magnetic coupling between adjacent metal tracks due to the rounded profiles obtained from the electroplating process (see Fig. 4).

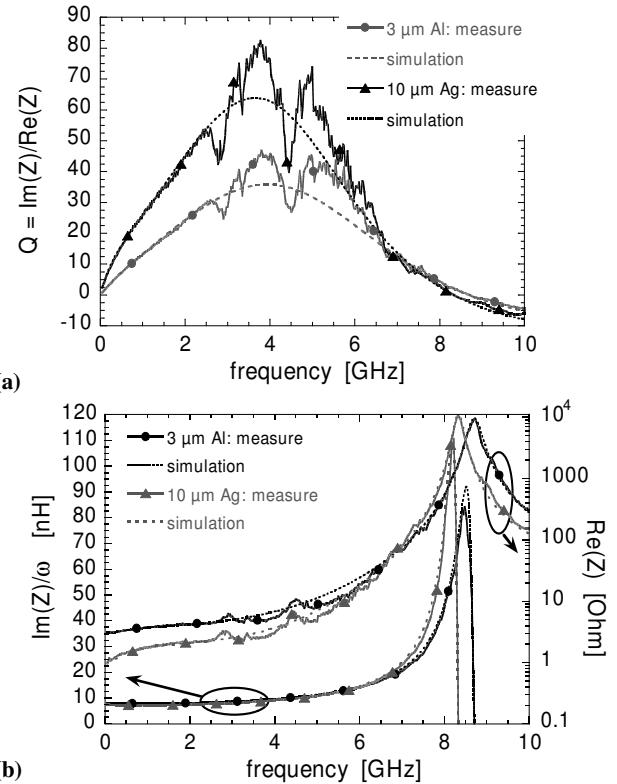


Fig. 7. (a) Q-factor : measure (full lines) vs. simulated (broken lines) and (b) $\text{Im}(Z)/\omega$ and $\text{Re}(Z)$ of two inductors with identical layout fabricated on glass, but having different spiral conductivity.

Table 2. Circuit parameters of the measured inductors of Fig. 7

Device	L_f [nH]	R_f [Ω]	L_s [nH]	R_s [Ω]	C_s [fF]	R_d [Ω]
Al	0.18	0.79	7.6	3.06	44.0	14.95
Ag	0.27	1.03	7.06	1.0	51.7	11.22

Fig. 8 summarizes the performances obtained from the fabricated inductors and provides a comparison with those exhibited by state-of-the-art CMOS-compatible inductors [5]-[9]. By combining low-loss substrates (HRS or glass) with highly conductive Al or Ag layers, the peak Q-factors displayed by our planar inductors challenge those achieved by suspended or 3-D structures. Beside the very promising performance obtained, it has to be pointed out that the presented micromachining processes are not suitable for fabricating inductors directly on standard CMOS substrates. In fact, dramatic Q-factor degradation would occur as a consequence of energy dissipation through doped silicon. The advantages inherent to the proposed planar architecture are the robustness and the simplified packaging procedure.

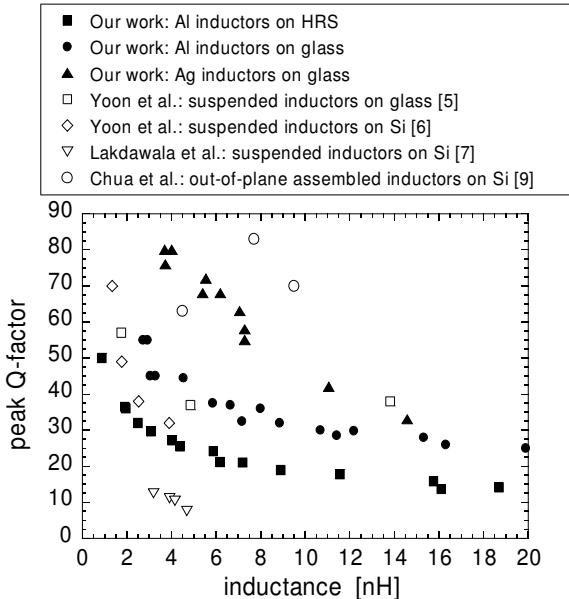


Fig. 8. Outlook and comparison of inductor performances.

CONCLUSION

We have developed two distinct low-cost and low-thermal budget micromachining processes for fabricating high-performance planar inductors up to 20 nH. These are dedicated to low-power consumption RF passive circuits, such as filters and baluns. High-resistivity silicon (HRS) and glass were chosen as substrate materials for reducing or even suppressing RF losses. A Q-factor improvement of more than 30% was obtained using glass instead of HRS. Inductors with a 3 μm -thick Al spiral fabricated on glass exhibited peak-Q's well above 30 for inductance values up to 10 nH, whereas 10 μm -thick Ag inductors on glass have shown Q-factors around 70 for inductances up to 6 nH. Measured data were in excellent agreement with

simulations obtained from an improved equivalent model based on frequency-independent elements. In general, the performance displayed by the proposed inductors challenge those of state-of-the-art micromachined devices.

Acknowledgements

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References

- [1] W.B. Kuhn and N.M. Ibrahim, Analysis of current crowding effects on multiturn spiral inductors, *IEEE Trans. Microwave Theory & Tech.*, **49**, 31-38 (2000).
- [2] J. Crannickx and M. Stayaert, A 1.8-GHz low-phase-noise CMOS VCO using optimized hollow spiral inductors, *IEEE J. Solid-State Circuits*, **32**, 736-744 (1997).
- [3] J.N. Burghartz, D.C. Edelstein, M. Soyuer, H.A. Ainspan and K.A. Jenkins, RF circuit design aspects of spiral inductors on silicon, *IEEE J. Solid-State Circuits*, **33**, 2028-2034 (1998).
- [4] Y.-S. Choi and J.-B. Yoon, Experimental analysis of the effect of metal thickness on the quality factor in integrated spiral inductors for RF IC's, *IEEE Electron Device Lett.*, **25**, 76-79 (2004).
- [5] J.-B. Yoon, C.-H. Han, E. Yoon and C.-K. Kim, High-performance three-dimensional on-chip inductors fabricated by novel micromachining technology for RF MMIC, *1999 IEEE MTT-S Int. Microwave Symp. Dig.*, 1523-1526 (1999).
- [6] J.-B. Yoon, Y.-S. Choi, B.-I. Kim, Y. Eo and E. Yoon, CMOS-compatible surface-micromachined suspended-spiral inductors for multi-GHz silicon RF ICs, *IEEE Electron Device Lett.*, **23**, 591-593 (2002).
- [7] H. Lakdawala, X. Zhu, H. Luo, S. Santhanam, L.R. Carley, and G.K. Fedder, Micromachined high-Q inductors in a 0.18- μm copper interconnect low-K dielectric CMOS process, *IEEE J. Solid-State Circuits*, **37**, 394-403 (2002).
- [8] J. Zou, C. Liu, D.R. Trainor, J. Chen, J.E. Schutt-Ainé and P.L. Chapman, Development of three-dimensional inductors using plastic deformation magnetic assembly (PDMA), *IEEE Trans. Microwave Theory & Tech.*, **51**, 1067-1075 (2003).
- [9] C.L. Chua, D.K. Fork, K. Van Schuylenbergh and J.-P. Lu, Out-of-plane high-Q inductors on low-resistance silicon, *J. Microelectromechanical Systems*, **12**, 989-995 (2003).
- [10] C.P. Yue and S.S. Wong, Physical modeling of spiral inductors on silicon, *IEEE Trans. Electron Devices*, **47**, 560-568 (2000).
- [11] T. Kamgaing, T. Myers, M. Petras and M. Miller, Modeling of frequency dependent losses in two-port and three-port inductors on silicon, *2002 IEEE MTT-S Int. Microwave Symp. Dig.*, 153-156 (2002).
- [12] G.M. Rebeiz, *RF MEMS – Theory, Design, and Technology*, New York: J. Wiley & Sons, 365-366 (2003).