DIRECT ETCHING OF HIGH ASPECT RATIO STRUCTURES THROUGH A STENCIL

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ABSTRACT

This paper reports the feasibility of the fabrication of high aspect ratio structures on substrates via dry etching through a stencil mask placed onto the sample. It demonstrates the possibility to use standard equipment and processes with this novel masking technique, which allows the patterning of fragile and pre-structured surfaces, and avoids the use of resist or additional coating of the sample, reducing costs and processing time. Aspect ratios as high as 13:1 and pattern transfer with a gap of 100 μm are demonstrated.

INTRODUCTION

High Aspect Ratio structures

One of the major challenges of microtechnology fabrication has been, and still is in some cases, the definition of high aspect ratio (HAR) structures. LIGA technology [1, 2] is a very powerful technique allowing incredibly high aspect ratios but with the inconvenient of huge cost, due to the fact that X-Rays are necessary. A similar but much cheaper solution is the use of SU-8 [3, 4], which has been used in many different MEMS applications.

However, silicon has always been the most used material for MEMS [5] and it was not until almost 15 years ago that the invention of the Deep Reactive Ion Etching process (Bosch® process) [6] provided a major advancement in the field of silicon technology. This etching technique combines two different gases in alternating steps of etching (with SF_6) and polymer deposition (with C_4F_8). The polymer is deposited both in the sidewalls and in the horizontal surfaces but removed at a much slower rate from the vertical walls, which eventually yields an anisotropic process. In addition, the etch rates are quite high, allowing to perform bulk micromachining of a standard Si wafer in less than 1 hour (a major breakthrough when compared to previous techniques like KOH or TMAH etching [7]).

Therefore, DRIE allows defining structures in silicon with Aspect Ratios (AR) higher than 15:1 (AR depends on the exact etching conditions and can be 100:1 or 150:1) and with a high etch rate. However, a lithographic step to define the mask is always necessary prior to the etching, which implies the use of photoresist and consequently coating, exposure, development and removal of the resist. This also imposes certain restrictions regarding the materials and substrates that can be patterned, i.e. substrates sensitive to chemicals and non-planarized are incompatible with standard techniques.

As an alternative, we present here the use of DRIE processes using a micro-stencil as a reusable mask for the definition of HAR structures. This work is inspired by the already described dry etching of thin films with sub-micrometer resolution [8, 9] but with a focus for MEMS applications.

Stencil Lithography

Stencil Lithography (SL) has been widely used in the last years to locally deposit metals on a substrate, providing sub-micrometer resolution [10, 11]. The metals deposited can be used either to create electronic structures [12] or to act as a mask for posterior etching of the substrate [13]. Although this technique has mainly been used for the selective deposition of metal, it has also been used to perform ion implantation [14] and etching of different substrates in the several hundreds of microns regime [15, 16] and in the sub-micrometer range [8, 9].

EXPERIMENTS

Stencil fabrication

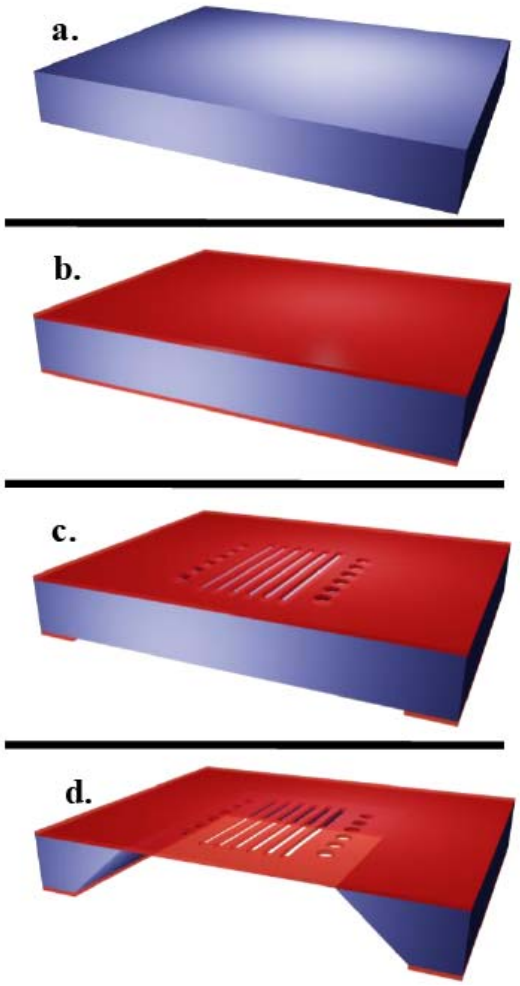

Figure 1: Schematics of the fabrication of a stencil. a) Double side polished wafer, b) deposition of Low Stress Silicon Nitride, c) pattern of apertures in the front-side and windows in the back-side, d) KOH etching to release the membranes.

For this work, low stress silicon nitride (LS-SiN) membranes, 500 nm thick and ~1x1 mm^2 in lateral size, were fabricated in a p-type Si wafer (100 mm). The

fabrication involves standard micro-technology processes and a detailed description can be found elsewhere [4]. It starts with a double sided polished Silicon wafer (100 mm in diameter) (Figure 1.a). A layer of low stress silicon nitride (LS-SiN) (100 to 500 nm thick) is deposited (Figure 1.b) on both sides of the wafer. Then, the nitride layer is patterned opening functional apertures on the front-side and windows for bulk micromachining on the backside (Figure 1.c). Finally, the release of the membranes is made using a KOH etching (Figure 1.d). The dimensions of the different apertures in the membranes used for the experiments presented here were ranging between 2 µm and 200 µm. Some examples of membranes with apertures are presented in Figure 2.

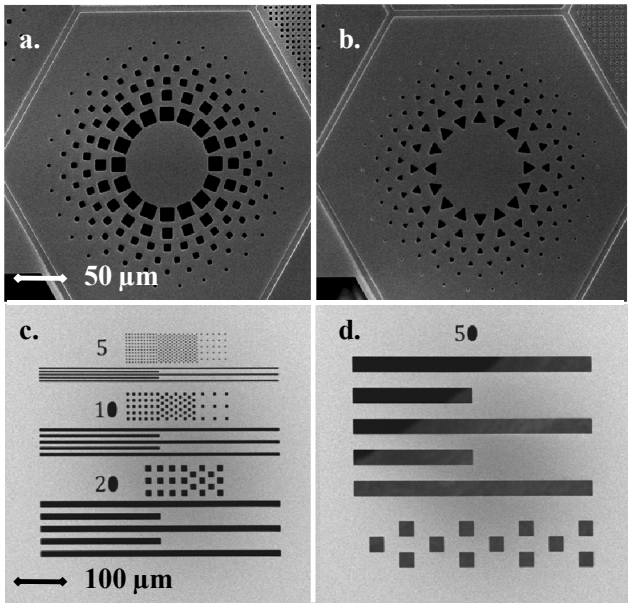

Figure 2: SEM micrographs of different membranes with holes after release. a) Squares and b) triangles ranging from 2 to 10 µm. c, d) squares and lines from 5 to 50 µm.

Once the membranes are released and prior to their use as shadow masks for etching of silicon, both sides of the membranes are covered by a thin Al layer (around 50 nm) in order to avoid damaging the membrane and allow their re-usability. Aluminum is chosen because of its high selectivity with respect to Si in Bosch process.

Table 1: Process conditions in Alcatel ICP-601E used in the presented work

Process	**Si-etch**		**Poly-coat**
Gas	SF_6	$c\text{-}C_4F_8$	$c\text{-}C_4F_8$
Flux (sccm)	300	200	50
Cycle Time (s)	7	2	-
Pressure	41% (6.5 Pa)	41% (4.5 Pa)	3 Pa
Source Power (W)	1800	1800	1800
Platten Power (W)	90	90	0

Substrates preparation

In order to prove that this technique was suited for the patterning of substrates with pre-defined topography, several wafers were prepared with square-shaped wells (Figure 3.a). This topography was defined either by DRIE (vertical sidewalls, conditions in Table I) or by KOH etching (sloped sidewalls). Gaps between 15 and 100 µm were defined.

Etching experiment

Once the membranes were protected, the stencils were placed on top of a p-type Si wafer (substrate, Figure 3.a) and a dry etching using a standard Bosch process (Table 1, "Si etch") was performed in an Alcatel ICP-601E (Figure 3.b). After etching, the stencil is released from the substrate and the resulting patterns can be observed (Figure 3.c). It is worth stressing at this point that the etching recipe used was the same as the one used for silicon etching using conventional etching masks like photoresist, silicon oxide or aluminum.

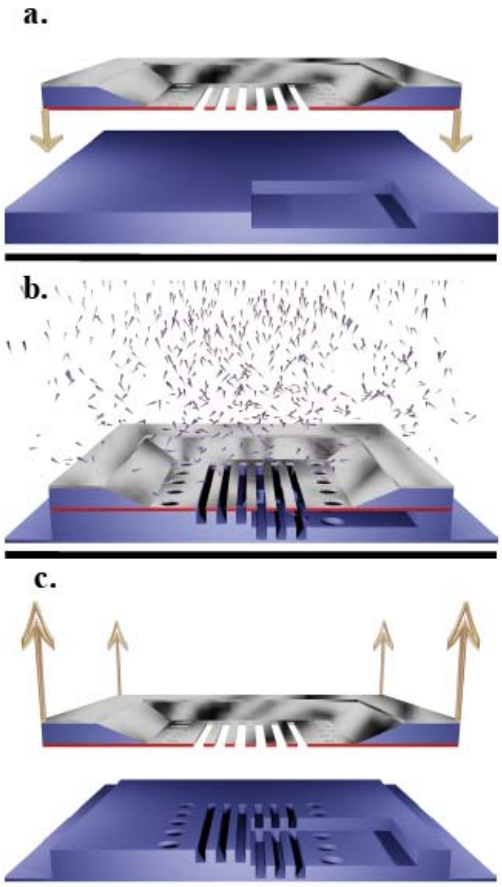

Figure 3: Steps to fabricate deep trenches through stencil: a) Stencil covered with an Al layer is placed on the substrate, c) DRIE is performed, d) stencil is released and the structures have been transferred.

RESULTS

Flat substrate

When etching on a flat substrate, all the patterns included in the membranes were transferred (Figure 4.a and b) yielding a maximum measured AR of 13:1 (for a typical trench of 2.5 µm in width and 33 µm in depth), proving therefore the feasibility of the process. The value for the maximum AR must be compared with the maximum value attained with the same process but using an aluminum layer as a mask, which is 15:1. This means a

reduction of approximately 15% of the maximum AR. A reduction of the etch rate was also observed.

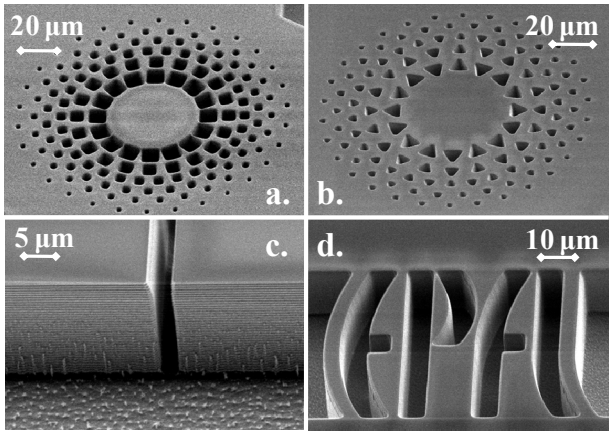

Figure 4: Results after 10 minutes etching of silicon on a flat substrate. Squares (a) and triangles (b) from 2 to 10 µm in size transferred into Si. These patterns correspond to the stencils in Figure 2.a and b. c) Si trench with an AR of 10:1. d) Transfer of arbitrary shaped structures.

Endurance tests were performed on the masks and, due to the Al protective layer and its high selectivity towards Si, it was possible to etch-through a full wafer (525 µm) twice without noticeably degrading the stencil.

However, it is important to note that when Al was not covering both parts of the membrane the corrosion was fast. This is due to the neutral etching species which perform a purely chemical etching in an isotropic way. After going through the apertures in the membrane, those compounds disperse freely in the gap between the membrane and the substrate, damaging the membrane if it is unprotected.

Stepped substrates

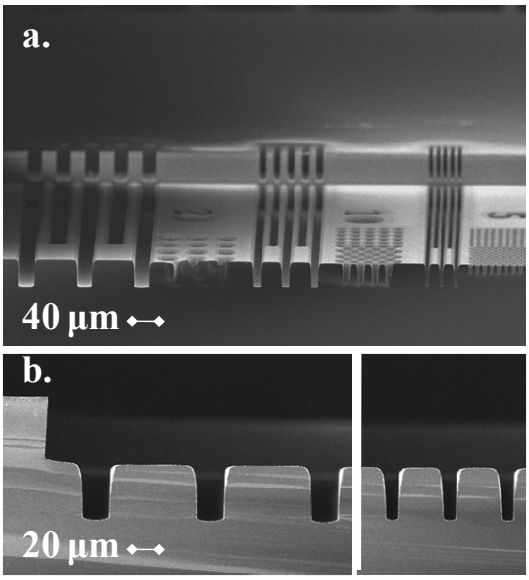

Figure 5: a) and b) 40 µm deep trenches etched in the Si over a gap of 50 µm. Widths from 10 to 50 µm were correctly transferred.

To verify the structuring of non-planar, pre-patterned substrates, we performed etching through openings widths ranging from 10-50 µm over different gaps. Some typical results for 50 µm gaps are shown in Figure 5.

In this case, we observed differences between standard and shadow mask process that increase with the gap, such as: surface damage that can be caused by the neutral species (slight etching, huge extension. Figure 6.a) or by charged particles which are not completely perpendicular to the mask and therefore increase the exposed area (small size, serious damage to corners, Figure 6.b and c). Also loss of Aspect Ratio (Figure 6.d) and reduction on the etch rate (Figure 7) are observed.

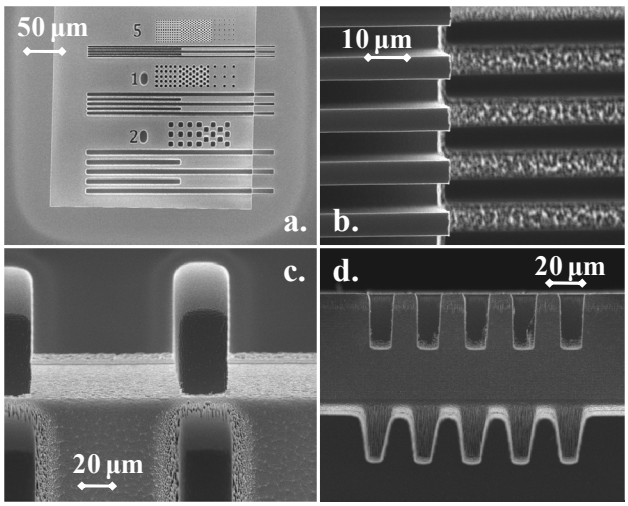

Figure 6: a) Pattern transfer corresponding to the stencil in Figure 2.c. The zone with the bright halo presents damage only in the surface. b) and c) Huge damage of the region close to the corners. d) 20 µm trench opened with and without gap. AR of the structures is smaller after the gap.

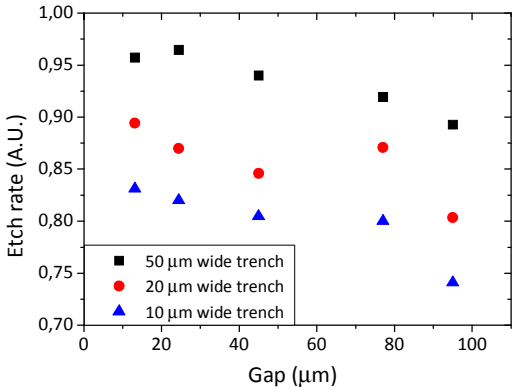

Figure 7: Relative etch rate for different widths as a function of the gap between the stencil and the substrate. The difference in the etch rate for different widths is due to the difference AR. The difference due to the gap is due to the dispersion of the etching species in the chamber after they go through the membrane apertures.

Finally, a novel effect was observed when etching on sloped walls. Figure 8 is showing a SEM micrograph and a schematic of the cross section. It is possible to see that in the etched and sloped region, silicon grass is formed, whereas in the etched and flat regions, clean results are obtained. This behavior is due to the fact that the gas has locally more surface to etch than in the flat case. Then the balance between the two gases is broken and therefore

spikes appear. A possible solution to this issue is to increase the Platen Power, which makes the etching species more energetic and capable of removing those spikes while processing.

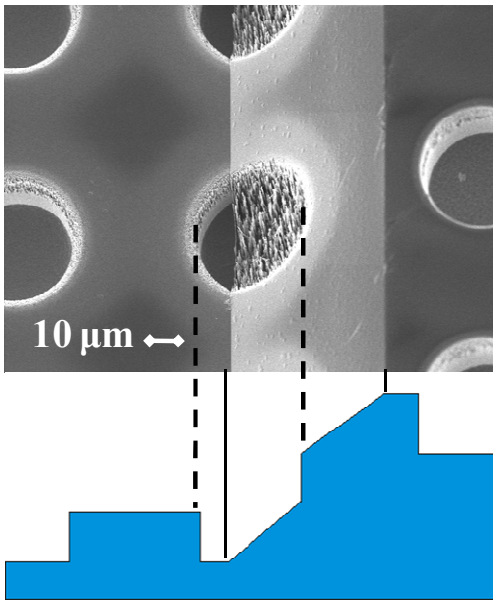

Figure 8: Circles 40 µm deep defined at two different gaps and in a KOH slope simultaneously. In the slope, the effective area is larger, which implies that the etching gas is not enough using a standard recipe. Higher platen power can be used to minimize that effect.

CONCLUSIONS

We have shown in this paper the feasibility of the use of membranes with apertures as a hard mask to perform DRIE on silicon substrates. The gap between the mask and the wafer has a direct effect on the surface damage (increasing when the gap increases), the achievable aspect ratio and the etch rate (both decreasing when the gap increases).

We have achieved AR as high as 13:1, full wafer etching without noticeable degradation of the stencil, definition of structures after a gap of 100 µm and correct pattern into sloped surfaces.

This is therefore a very promising technique which we believe can broaden the use of DRIE techniques for MEMS applications.

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