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Charging dynamics of localized 2D layers of Si nanocrystals embedded into SiO_2 by stencil masked ultra low energy ion implantation process

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Flash memories based on nanoparticles (NPs) offer an attractive alternative for performance enhancement and size downscaling of non-volatile memory cells. In these devices, Coulomb blockade and quantized charging effects can be exploited at room temperature for a limited number of addressed NPs [1]. A successful exploitation of these nanoscale effects requires not only knowledge of the NPs properties (size, nature, structure and location) but also a sound understanding of the charge trapping phenomena that govern the memory behaviour of the devices. In this study, fabrication of 2D arrays pockets of Si nanocrystals (NCs) is demonstrated by implanting 1keV Si ions into thin SiO_2 layer (7nm) through a stencil mask with 50nm to 2µm apertures. Upon thermal annealing, Photoluminescence spectroscopy (PL) and Energy-Filtered Transmission Electron Microscopy (EFTEM) reveal characteristics of NCs in the implanted SiO_2 pockets. Then, charging dynamics examined by I(V) and I(t) measurements on nano-MOS capacitors in the 80K-300K temperature range clearly show an increasing Coulomb gap with decreasing temperature. Moreover, below a critical temperature (T=150K), N-shapes which are voltage sweep ramp dependent, appear on the I(V) curves. Comparison of the C_{DG} capacitance extracted from Q_{DG} (charges of Dots/Gate) calculations on different I(V) ramp measurements and the C_{DG} capacitance evaluated from structural parameters (sizes, tunnel distances…) extracted from EFTEM and PL characterizations provide relevant information regarding the kind and localization of the charge trapping centers. [1] M. Schalchian, J. Grisolia et al. Appl. Phys. Lett. 86, 163111, (2005).