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**KFM detection of quantified charges injected into a thin SiO<sub>2</sub> layer containing Si nps embedded by ultra low energy ion implantation using stencil lithography.**

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Non volatile flash memories based on nanoparticles (nps) are one of the identified routes to a further downscaling of future CMOS technology. New features such as Coulomb blockade and quantized charging effects can appear at room temperature only for a limited number of addressed nanometer sized nps [1]. It has been previously demonstrated that ultra low energy ion implantation (1keV) into an ultra thin SiO<sub>2</sub> layer (7nm) through a stencil mask containing apertures (from 50nm to 2 $\mu$ m) [2], followed by annealing allows to produce 2D arrays of Si nps into localized areas of the gate oxide [3]. The I(t) and I(V) measurements of the nano-MOS capacitors reveal single electron transport at room temperature. At the same time, the C(V) electrical measurements reveal significant flat-band voltage shift as high as 4V denoting strong memory effect in these isolated areas. However, as a result of ion implantation damage into the oxide, the remaining structural defects (e.g. excess of silicon atoms, Si/SiO<sub>2</sub> interface defects...) and their localization play a major part in the electrical characteristics of these devices. In this paper, we propose a complementary electrical study using AFM/Kelvin Probe (KFM) technique. The amount of charges stored in each nps with different sizes can be evaluated from the surface potential change with the electron injection into and extraction from the ncs. Moreover, the temporal decay of the surface potential has been systematically studied as a function of ncs characteristics (density, size, localization...) and the retention time extracted from the exponential decay was found much longer than 4000s in the implanted areas. These measurements clearly add to the understanding of memories based on these nanostructures.

[1] M. Schalchian, J. Grisolia et al. Appl. Phys. Lett. 86, 163111, (2005).

[2] G.M. Kim, M.A.F. van den Boogaart and J. Brugger, Microelectronic Engineering, **67-8** (2003) 609-614.

[3] J. Grisolia et al. Superlattices and Microstructures (2008)