

Bismuth Nanowires with Stencil Lithography

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While bulk Bi is a semimetal, nanostructured Bi with a critical dimension less than 50 nm suffers a semimetal-semiconductor transition [1]. This provides the advantage that in a single Bi deposition step, one would be able to tailor at full-wafer scale the electronic behavior of Bi devices by controlling the pattern dimensions. Another useful effect in Bi nanowires (NWs) is their predicted enhanced thermoelectric characteristics [2]. Converting a temperature gradient into electric voltage and vice versa with high efficiency makes Bi NWs a candidate for energy harvesting applications.

While thin films are easily obtained through vapor and sputtering deposition, Bi NWs are more difficult to pattern by etching or lift-off due to their restricted lateral and vertical dimensions. Electrical measurements require they make a low-resistance contact with metallic electrodes. This is not easy due to the formation of a thick-oxide layer around the Bi NW once in atmospheric environment that is difficult to remove. The bottom-up approach for Bi NW fabrication usually consists of electrodepositing Bi into nanoporous templates [3, 4]. This approach provides a high density of wires with very uniform diameter. The bottleneck here consists of precisely placing the wires at desired locations, as well as obtaining a low-ohmic contact with the electrodes. The top-down approach has a definite advantage regarding the wire positioning, the drawbacks here being the difficulty in patterning narrow and thin Bi structures [5, 6].

In this work stencil lithography was used for the first time for patterning Bi NWs. Stencil lithography is a resist-less, parallel patterning technique [7] incorporating in one step micro to nano features, where the material is deposited onto a substrate through a stencil (see Fig 1). First a 100 mm stencil wafer containing 100 nm thick low-stress SiN membranes with nano-apertures was fabricated. Nanoslits 30 to 500 nm wide and 1 to 10 μm long were designed to span a wide range of wire dimensions. This stencil was clamped to a Si wafer containing a 200 nm SiO₂ layer on top, and the clamped system was placed in a thermal deposition system. Bi was evaporated through a 2 mm diameter hole from a W boat. On each substrate we deposited 65 nm Bi, using deposition rates varying from 0.7 to 4.3 $\text{\AA}/\text{s}$. The analysis of the scanning electron micrographs of the wires showed a direct correlation between both the deposition rate (as a global deposition parameter, determined by a crystal thickness monitor) and the position of the NW apertures with respect to the evaporation source, and the wire topography. A slower deposition rate and a more distant location of the apertures from the material source induced the formation of blurred wires (see Fig. 4a). The only region on the substrate where the pattern transfer from the stencil onto the substrate was not blurred corresponded to the position right above the Bi source, and only for the highest deposition rate (see Fig. 3 and 4b). Wires ranging from 35 to 550 nm in width were thus obtained (see Figure 2). The larger lateral diffusion of Bi under the stencil at lower deposition rates is consistent with the idea that a higher deposition rate lowers the surface mobility, enhances the island nucleation, and provides fewer atoms to the regions shadowed by the stencil [8].

In this work Bi NWs with diameters below 40 nm were fabricated for the first time using stencil lithography. The deposition parameter space was explored and the correct conditions were found for a well-confined wire definition on an oxidized Si wafer substrate. Next steps include incorporating the Bi NWs onto substrates with pre-defined metal electrodes. The electrodes will be fabricated via stencil lithography, a technique that allows the creation of tapered sidewalls (enhanced when a gap exists between stencil and substrate). This will insure a better step coverage of the electrodes by the thin Bi layer, thus allowing transport and thermoelectric characterization of the NWs.

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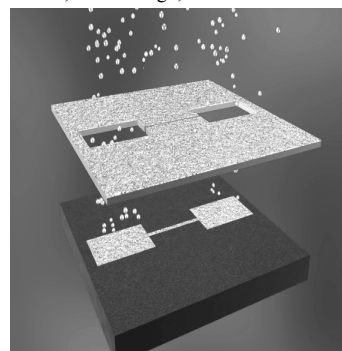


Figure 1. Schematic patterning using stencil lithography: material is evaporated through a stencil mask, which is in contact with the substrate.

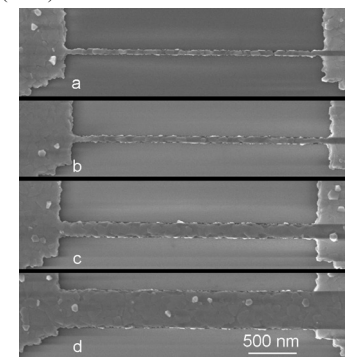


Figure 2. Scanning electron micrograph of 3 μm long Bi NWs a) 65, b) 97, c) 176, and d) 476 nm wide, respectively.

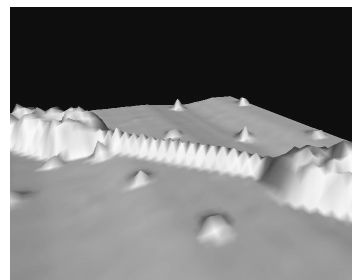


Figure 3. AFM scan of a $3 \times 0.12 \mu\text{m}^2$ Bi nanowire and pads evaporated at the same time as the NW.

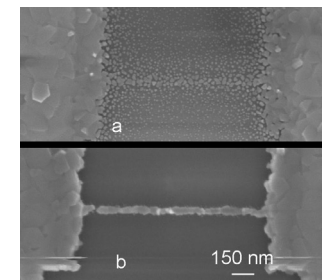


Figure 4. Scanning electron micrograph of high rate Bi deposition a) off-centered and b) centered with respect to the Bi source.