Quick and Clean: Stencil Lithography for Wafer-Scale Fabrication of Superconducting Tunnel Junctions

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This paper presents a full-wafer, resist-less process for parallel fabrication of sub-micron Al/AlOx/Al superconducting tunnel junctions (STJs). A stencil is fabricated out of a Si wafer on which 200 nm low-stress SiN has been deposited. The STJ apertures in the SiN are defined by e-beam lithography on the front side of the wafer, and the Si is etched from the backside for opening SiN membranes. Using a customized full-wafer stencil aligner, the stencil is aligned and clamped to a substrate wafer which contains Au contact pads. The clamped system is placed in a thermal evaporator equipped with two Al sources, from which two Al evaporations are performed, with an intermediate in-situ oxidation step. Once out of the evaporator, the stencil is unclamped from the substrate and *d.c.* measurements are performed down to 0.3 K. One challenge of this technique is the clogging of the stencil, which is due to the material deposited on the side walls of the nanoapertures. The Al deposited on the stencil is removed using wet-etching, making thus the stencil reusable. This technique provides a cheaper and cleaner fabrication of STJs than present fabrication techniques, e.g. e-beam lithography. The advantages of this process are now being investigated in nanojunctions.

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