Results from MPGDs with a Protected TimePix or Medipix-2 Pixel Sensor as Active Anode

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***Abstract*–The functioning of a high-resistive, hydrogenated amorphous Silicon layer as a protection against discharges for Micromegas-based pixel readout gaseous detectors, has been investigated. Chips, protected with a 3 µm thick layer, still broke, but a 20 µm thick layer has proven to be adequate. Images from discharge events disclose their geometrical parameters, enabling to further optimize the discharge protection.**

I. Introduction

A new gaseous detector has been realized combining a Micromegas grid [1], [2] with the Medipix-2 CMOS chip [3]. In a small drift volume of 14 x 14 x 14 mm^3, primary electrons drift towards the grid. After passing a grid hole, they enter the 50 µm wide gap between the Micromegas, put at a potential of around -400 V, and the pixel (anode) chip, put at ground potential. Due to the strong electric field, the electron will initialize an electron avalanche, and the resulting charge signal activates the preamp-shaper-discriminator circuitry in the pixel beneath the hole. We have recorded track images from minimum ionizing cosmic muons. From this data we could derive that the efficiency for detecting single electrons was better than 90 percent [4].

By means of 'wafer post processing' we constructed a Micromegas-like grid onto a Si wafer [5]. With this technology, a CMOS pixel chip can be combined with a grid, forming an integrated monolithic readout device of a gas volume (InGrid). The sub-micron precision of the grid dimensions and avalanche gap size results in a uniform gas gain. The diameter of the insulating pillars between the pixel chip (anode) and the grid can be as small as 30 µm: they can, therefore, be positioned between the grid holes, thus avoiding dead regions.

The 'GridPix' detector can be applied in gas-filled detectors in general, but the application in TPCs, in µ-TPCs and in TRDs may boost their performance since individual 3D information of all primary electrons becomes available. In principle, the only limit to the spatial resolution is diffusion. The drift volume and choice of gas can be optimized for the detection of X-rays: since the position of the interaction point of the quantum with the gas can be reconstructed from the (3D) ionization pattern, precision imaging and quantum energy measurement seems possible. With a 1 mm thin layer of gas as drift gap, GridPix can be applied as light, low-power and radiation-hard GOSSIP vertex detector [6]

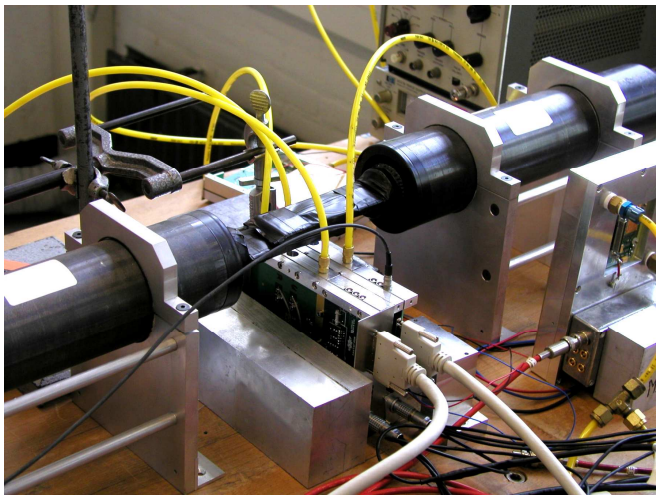

Fig. 1. Cosmic ray trigger station with three GridPix chambers.

II. Discharges

A problem associated with gas-filled proportional chambers is sparking. When an electron avalanche reaches the Raether's limit [7], it may evolve into a discharge, damaging the readout electronics [8]. This is a critical issue in GridPix detectors, where a Micromegas or InGrid is placed directly on a naked (CMOS) pixel chip.

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In Resistive Plate Chambers (RPC) [9], with one or both electrodes made of a high resistive material, the instant drain of the charge deposited by the discharge is intrinsically blocked. The piled-up charge creates an electric field that causes a local drop in the applied field. This causes a quench of the discharge and its amplitude, typical a fraction of the charge stored in the assembly of the participating electrodes, is reduced.

In this work, a high resistive protection layer, made of hydrogenated amorphous silicon (a-Si:H), has been used to cover the pixel chips[10]. Besides its quenching effect, this layer also protects against the evaporation of the CMOS chip surface, i.e. the thin metal pixel input pads, due to the spark plasma.

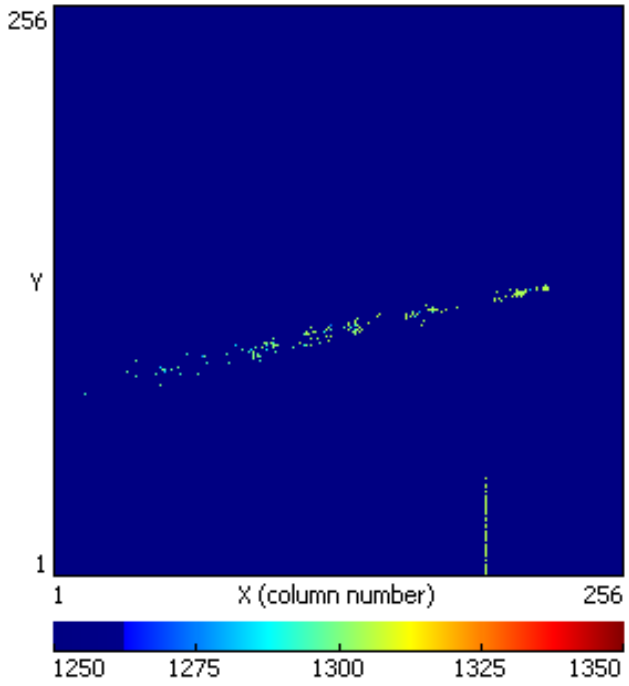

Fig. 2. Cosmic ray track taken with a chamber constructed from a TimePix chip covered with a 20 µm thick protection layer with an InGrid. The read out of the TimePix chip is controlled by the Pixelman software package [11].

Charge from an avalanche, being the result of 'normal' single electrons, will arrive and stay on the a-Si:H layer facing the pixel input pad. A large fraction of this surface charge is induced onto the pixel input pads, forming the avalanche signals at the pixel inputs. The resistance of the a-Si:H layer should be sufficiently small to compensate the surface charge while the potential drop of the surface should be limited to about one volt. The maximum volume resistance of the a-Si:H layer depends therefore on the expected detector current (thus on count rate, gas gain and primary ionization). Since all pixel input pads contribute in parallel to this compensation current, the specific resistance of a-Si:H can be as high as 10^9 Ω.cm for applications like GOSSIP in high radiation environments as vertex detector at the future Super LHC. Away from these extreme irradiation doses, a specific resistance of 10^{11} Ω.cm, typical for non-doped a-Si:H, can be applied, in general.

III. Results

Earlier experiments suggested that in He based mixtures less discharges occur than in Ar based mixtures; this may be expected since the ionizing density in He is about a factor 2 smaller. We first operated a TimePix chip [11], [12] with a 3 µm layer of a-Si:H, equipped with a Micromegas in a He/Isobutane 80/20 mixture successfully during two months, with a gas gain of ~ 5 k (see Fig. 1). We took care that the discharge capacitance of 22 pF, formed by the Micromegas and the TimerPix chip, was not significantly increased by the (effectively parallel) preamp coupling capacitor and the HV filter capacitor.

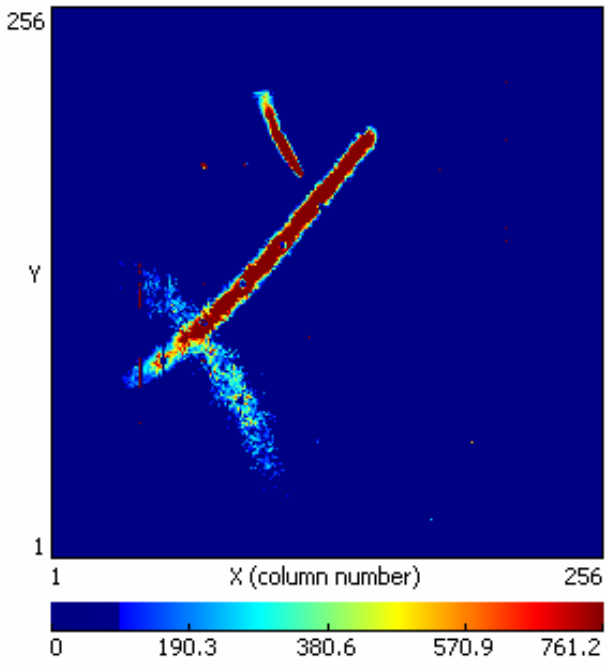

Fig. 3. Typical (double) tracks from α–particles.

After changing to an Ar/Isobutane 80/20 mix, the TimePix chip broke within 8 h of operation. Vision inspection of the chip surface showed no visible damage like evaporated Al or Si_2N_3, as was the case before. Apparently, the chip broke due to a too large charge injected into one or more pixel input pads.

It was decided to have chips covered with a thicker layer. This would 'quench' the discharges in an earlier stage due to the increased ratio of the layer thickness and avalanche gap thickness. In addition, all induced charge signals appearing at the pixel input pads are somewhat reduced due to the larger distance between the avalanche charge and the pixel input pad.

It was realized that charge dilution, as a result of charge spread, would be unavoidable if the thickness of the protection layer is in the order of the pixel pitch. For this reason we choose a new layer thickness of 20 µm.

In Fig. 2 a cosmic ray event is shown with a chamber consisting of a TimePix chip covered with a 20 µm thick layer of a-Si:H, onto which an InGrid was constructed. As gas, a Ar/Isobutane 80/20 mix was used.

We obtained high-density primary ionization events by flushing the gas through a container with Thorium prior to guiding this gas to the chamber [13]. Proportional signals from the α-particles, measured directly with a scope connected to the grid, were clearly seen: see Fig. 3.

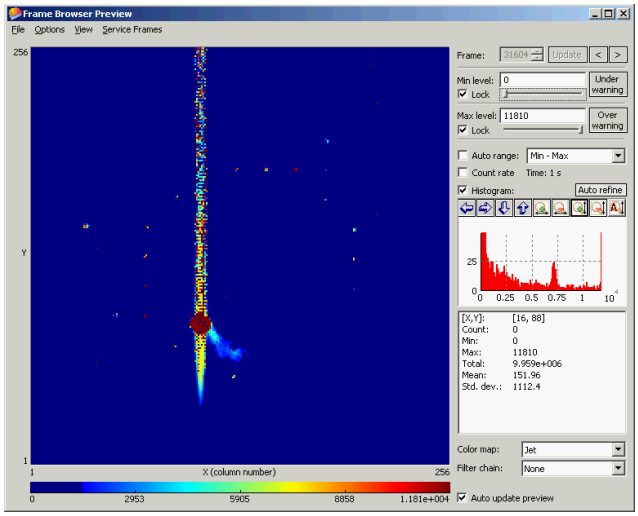

Fig. 4. Typical image of a discharge event.

As expected, in about 1 percent of the α-events, the proportional signal develops into a discharge: the probability for this is clearly higher for α's with a direction perpendicular to the chip. An example is shown in Fig. 4: there where the α enters the grid, the discharge occurs. Some 150 pixels in the area receive a large coincident charge signal and are activated. As a result, the local values of power voltage and threshold references are disturbed. Since these are common within pixel columns, many pixels above and below the discharge area are affected. This does not harm the functionality of the chip.

We measured the total charge, associated with a discharge, from the voltage drop of the grid. This charge has a Gaussian-like distribution with an average of 300 pC and a maximum of 400 pC. The latter corresponds to a fraction of 5 percent of the total stored charge in the grid-chip capacitor (22 pF x 400 V).

Allthough the charge distribution over the discharge-participating pixels is not known, we can obtain a value for the maximum charge that may enter into a pixel pad if we assume that the discharge has a tube-like geometry, with a flat charge distribution within the discharge area. The maximum charge entering the pixels, in that case, equals 2 pC per pixel. The TimePix chips are estimated to be able to withstand charges up to 10 pC per pixel. This tallies with the fact that the chips, protected with a 3 µm layer, do not survive. With a layer of 20 µm, however, the chips do not only keep functioning: discharges can actually be observed and quantified. From this data we may conclude that chips, protected with a 20 µm a-Si:H layer are spark-proof. As a result, future detectors are not required not to spark.

IV. Conclusions

We have constructed and operated MPGDs, using TimePix pixel chips with Micromegas grids or InGrids. The chips were coated with a protection layer of amorphous silicon. The chambers were operated in an Ar/Isobutane mixture with a gain of 5 k, enough to obtain a single-electron efficiency better than 70 percent. In this configuration, a 20 µm thick layer has been demonstrated to be adequate to protect the chip against the largest possible discharges.

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