Cleavage Fracture of Brittle Semiconductors from the Nanometer to the Centimeter Scale**

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The objective of this paper is to present the fundamental phenomena occurring during the scribing and subsequent fracturing process usually performed when preparing surfaces of brittle semiconductors. In the first part, an overview of nano-scratching experiments of different semiconductor surfaces (InP, Si and GaAs) is given. It is shown how phase transformation can occur in Si under a diamond tip, how single dislocations can be induced in InP wafers and how higher scratching load of GaAs wafer leads to the apparition of a crack network below the surface. A nano-scratching device, inside a scanning electron microscope (SEM), has been used to observe how spalling (crack and detachment of chips) and/or ductile formation of chips may happen at the semiconductor surface. In the second part cleavage experiments are described. The breaking load of thin GaAs (100) wafers is directly related to the presence of initial sharp cracks induced by scratching. By performing finite element modelling (FEM) of samples under specific loading conditions, it is found that the depth of the median crack below the scratch determines quantitatively the onset of crack propagation. By carefully controlling the position and measuring the force during the cleavage, it is demonstrated that crack propagation through a wafer can be controlled. Besides, the influence of the loading configuration on crack propagation and on the cleaved surface quality is explained.

1. Introduction

Mastering the cleavage of semiconductors is important when processing III–V optical devices. On a laboratory scale, cleavage is used to generate atomically flat surfaces or to study the cross-sections of thin films. Cleavage is usually performed in two stages. The surface is first scratched with a sharp diamond tip, which induces structural defects. Secondly, by applying a load to the sample, crack propagation is initiated, starting from the defect area. However, the mechanisms leading to high quality cleavage surfaces are often not fully understood. Since, over the years, scientists have scratched semiconductors only to investigate the cleavage operation[1–4] or have only examined the scratching operation, mostly on polymer and/or glasses,[5–7] it has been found of high importance to correlate both phenomena. This paper provides the reader with a global understanding of the various phenomena occurring during scratching and fracturing of different types of semiconductors, which are (100) Indium Phosphide (InP), (100) Silicon (Si) and (100) Gallium-Arsenide (GaAs) wafers.

The first part of this paper deals with the scratching of semiconductor surfaces. Recently, nano-indentation experiments have been thoroughly performed to study semiconduc-

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tor mechanical properties,[8–11] but much less effort has been put into investing the mechanisms and effects of scratching semiconductor surfaces at loads of a few milli-Newtons. The second part focuses on the cleavage of semiconductors after the introduction of an initial defect during scratching. Even though the concepts of fracture mechanics have been strongly established since the pioneering work of Griffith[12] and Irwin[13] in the late fifties, physicists have only recently been interested in the fundamental mechanisms governing crack propagation in brittle materials.[14,15] In particular, for crack propagating above a certain critical speed, crack branching is observed,[2] which leads to surface roughening. This could also be reproduced in molecular dynamics simulations.[16]

Most published works considered, so far, either idealised situations, where, for instance, a crack is loaded in pure tensile stress (called Mode I) or analysed the behaviour of large structures with dimensions in the meter range, typical for engineering applications. The concepts of fracture mechanics have been applied to semiconductors, but mostly to assess the strength of wafers, i.e. to prevent crack propagation.[4] To our knowledge, almost no attention has been given to the intentional fracture of small samples (a few hundreds μm in thickness and lateral size in the millimetre to centimetre range) as used in laboratory, or for the processing of semiconductor devices, such as III-V based lasers.

Three important findings are reported in this work. Firstly, during scratching, a large variety of defects such as dislocations, dislocation bands and/or new phases are generated. Secondly, for reliable cleavage of such small samples, the generation of reproducible initial sharp cracks by scratching is needed. In addition, these cracks must extend by several micrometers inside the substrate. Finally, the surface features observed on the crack surface are determined by the initial crack geometry and the loading configuration of the samples during crack growth. In this paper, we show that the crystal anisotropy of the III–V compounds makes possible to achieve mirror-like surfaces over a length of several centimetres and that, even in materials considered as brittle, it is possible to control crack growth by carefully controlling the displacement of a rod during the application of the force for cleaving.

2. Experiments

InP (100), Si (100) and GaAs (100) wafers were used. The GaAs wafers had a miscut of 2° to the [110] direction, as typically used for epitaxial growth. The nano-scratching experiments were performed using either a manual homemade scratching setup or in a MTS Nano-Indenter XP.

Cross-sectional TEM lamellae were prepared with a focussed ion beam (FIB) FEI Strata DB 235 installation. For all samples, the cutting planes were {110} planes perpendicular to the scratch direction. The TEM microstructure investigations were carried out with a Philips CM30 TEM operated at an acceleration voltage of 200 kV. Atomic Force Microscopy (AFM) measurements were made in non-contact mode using a Topometrix Explorer instrument with a linearised scanner.

In-situ SEM nanoscratching experiments were performed using a home-made system described in details in Refs.[17–18] Two different equipments were employed for the cleavage experiments. The first one is a manual apparatus allowing the cleavage of devices with a constant load (so-called "load-controlled" condition). The second system, integrated into a SEM chamber, has a stroke of several hundred of micrometers and is "displacement-controlled". Its displacement control is better than 100 nm and, for information, the force applied by the cleaving rod is acquired simultaneously.

3. Semiconductor Nano-Scratching

This section illustrates the various phenomena that may occur during nano-scratching. These phenomena, summarised in Figure 1, range from the nucleation and propagation of individual dislocations, to the formation of dislocation bands, as

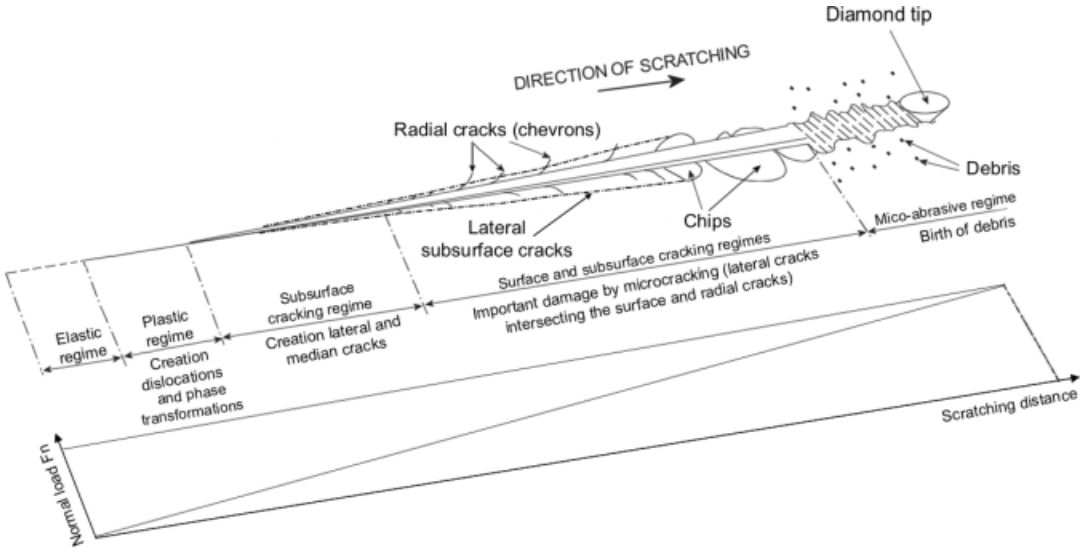

Fig. 1. Typical scratch pattern of semiconductors generated by an increasing load along the scratch path.

well as the generation of new amorphous or crystalline phases. Figure 1 is based on a recent work on scratching of glasses by Le Houérou *et al*.[5] Eventually, the creation of atomically sharp cracks below the scratch is observed when scratching at higher load using a sharp diamond tip. Such cracks might extend in the substrate beyond the plastically deformed area. Another main aspect of scratching at high load is the generation of surface particles or chips, which are likely to be linked to a non-reproducible process (the scratching operation is not smooth).

Some first insight can be gained by considering the analytical equations of the contact problem written by Hanson *et al*.[19,20] for a sphere of radius R (i.e. the indenter) that is loading an isotropic half space in the elastic regime. Hanson's equations describe the elastic field in a spherical Hertzian contact and include sliding friction to study scratching. From this first analysis, it can be shown that the shearing stress at the surface of the material during scratching is strongly influenced by the introduction of the tangential force which can be expressed by the so-called friction coefficient $f = T/P$ with P the normal load and T the tangential load. The friction coefficient is ranging between 0.1 and 0.2 for all currently studied semiconductors, with a typical observed value of 0.15 in our experiments. The maximum shear stress below the tip inside the substrate, however, is slightly influenced by friction. To give an order of magnitude, for a tip radius of few tens of nanometers and a force in the range of micro-Newtons, it is possible to induce dislocations or phase transformation (see below) under the action of shear stress or hydrostatic pressure, respectively in the range of around 1–3 GPa. For a larger tip radius, the onset of plasticity, obviously, takes place at higher forces. Once the maximal shearing stress at the surface under the tip has reached a critical value, dislocation nucleation may take place which is related to the so-called pop-in in indention force-penetration curves on III–V semiconductors.[21,22] The response of a material during scratching can change drastically when a thin layer is added on the surface. For instance, for a given tip radius and by using the proper load, it is possible to remove selectively an oxide at the surface of a silicon wafer without generating dislocations or phase transformations.[23] Finally, by increasing the friction coefficient f from 0 to a typical value of 0.15, the maximum tensile stress (σ_{11}) at the surface is multiplied by a factor three. This rise may facilitate the nucleation of dislocations, and eventually of various kinds of crack patterns behind the scratching tip.[24]

3.1. Dislocation Nucleation: Low Load Scratching of InP

Figure 2a presents a TEM cross-section in the [110] orientation of an InP sample. The scratch is perpendicular to the image plane. The Berkovich diamond tip, having an apex angle of approximately 126°, was employed. The scratch was performed with a load of 600 μN and a scratching speed of 10 μm/s. The scratching operation was carried out with the edge of the three-sided diamond tip first. The radius, however,

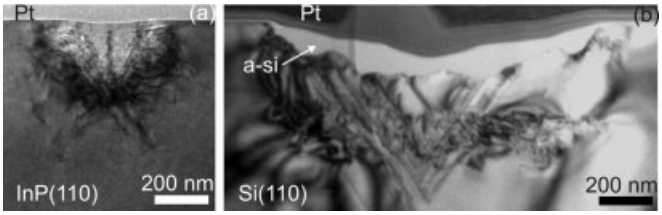

Fig. 2. TEM bright field image cross-section near [110] orientation. (a) InP sample scratched at 600 μN load and a speed of 100 μm/s and (b) Si scratched at 10 mN load and a speed of 100 μm/s. The platinum (Pt) layers have been deposited to protect the surface of the sample

was evaluated to be around 200 nm. Therefore, the Berkovich tip can be approximated by a pseudo-spherical tip. A platinum (Pt) layer deposited for FIB sample preparation is visible at the top of the surface. Dislocations can be seen up to 500 nm inside the substrate under the residual deformation after scratching.[25] Two regions can be distinguished on the image. First, directly under the residual surface imprint, a high disordered region of dislocations that extended to approximately 300 nm is seen. Second, beyond 300 nm, well defined dislocation lines are observed and extend up to 500 nm in the substrate. These dislocations lines make an angle of 54° with the surface and then clearly lay in an equivalent {111} plane. From TEM tilting experiments, the first region is known to be composed of a mixture of shockley partials, stacking faults and micro-twins, while the second is partially filled with perfect dislocation loops extending far away from the scratching zone.[26] Moreover, on the image, a slight deformation at the surface of the scratch is observed. The equivalent radius of this residual imprint is much higher (more than 1 μm) than the tip radius (200 nm) used in this experiment. This suggests that even if a plasticity threshold has been over-reach, a high elastic release of the surface has taken place after scratching.

3.2. Phase Transformation: Scratching of (100) Si Surface

Silicon is a brittle semiconductor that cleaves preferentially along the {111} planes. However, it is possible to cleave it along {110} planes, when forces are applied properly. Hence, the scratches have been made in the <110> direction as for the other samples. Figure 2b illustrates a TEM cross-sectional view of a silicon sample scratched along a <110> direction. Similarly to Figure 2a, the scratch is perpendicular to the image plane and was made with the same Berkovich diamond tip. The load and speed applied during the scratch was 10 mN and 100 μm/s, respectively. The striking feature of Figure 2b is the 100–200 nm thick white layer on the image.[27] This layer is mainly composed of amorphous silicon (a-Si) as revealed by micro-Raman investigation and TEM selected area diffraction (SAD) analysis (not shown here). Silicon is known to undergo phase changes under compression where it can form the high pressure phase Si II (β-Sn structure).[28] During decompression this phase is changed into an amorphous Si (a-Si) at rapid decompression rate. Also, at slow decompression rate, Si II is known to form two new phases III

and XII of silicon. These phases have been observed in nanoindentation experiments.[8–9] It has been shown that these silicon phases influence the electrical contact between the substrate and the indenter.[29] The second important feature is the presence of slip bands below the amorphous zone. These bands are parallel to {111} planes and extend several hundred nanometers inside the substrate. It is still controversial to know whether phase transformations occur prior to dislocation generation during nanoindentation[29] and a fortiori, during nano-scratching.

3.3. Dislocation Bands and Subsurface Median Crack: High Scratching Load of GaAs

The best technique to reveal subsurface cracks has been found to be by performing FIB cuts through the scratches. Figure 3 presents a SEM cross-sectional view prepared by soft FIB milling. The view is perpendicular to a scratch performed at 50 mN with a rounded diamond tip having a radius in the micrometer range. Figure 3b shows the cross-sections taken at different locations along the scratch. A Median Crack (MC) with a depth of approximately 6 μm is seen on all sections, whereas the Lateral Cracks (LC) pattern varies from one place to the other. Contrary to indentation experiments, where cracks are localised around the indenter, it is possible to create long cracks over several millimetres by "pulling" the MC crack with the diamond tip. It is, thus, possible to generate pre-cracks with constant depth and controlled length contained in the (110) plane by scratching GaAs and so extending the median crack.

Figure 4 illustrates a TEM cross-sectional view taken along the [110] direction perpendicular to the scratch in Figure 3. Below the scratch, as for silicon, dislocations are found mostly localised in thin bands, in {111} slip planes. Similar results have been reported after indentations in InP[10] and GaAs,[21] respectively. Depending on the scratching conditions, these bands can also be micro-twins.[30,31] Figure 4 indicates a strong

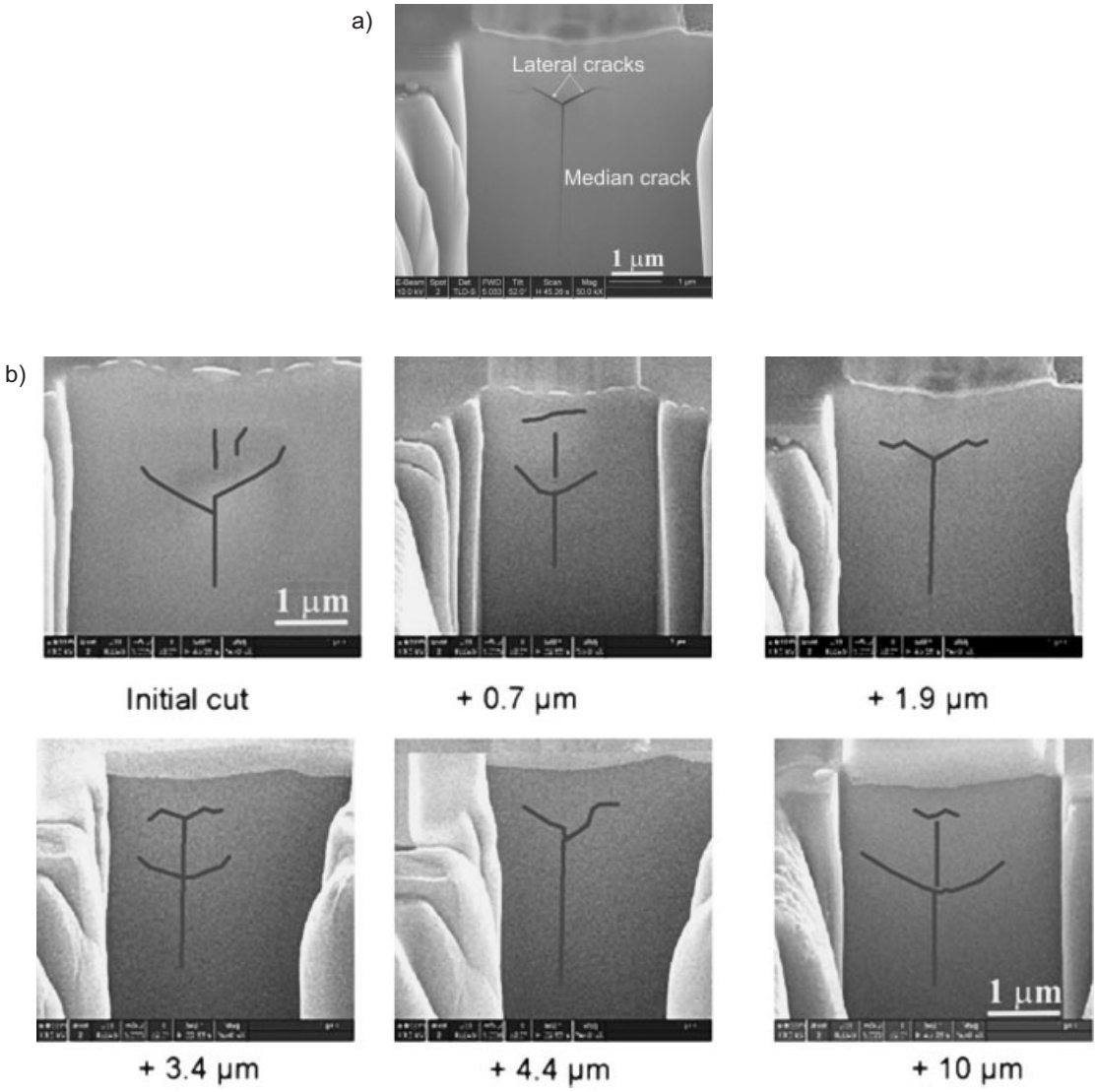

Fig. 3. SEM cross-sectional view, prepared by FIB, under a scratch in GaAs (a) Initial cut. The residual scratch shape can be seen at the top. (b) Illustration of crack patterns at different locations after the initial cut.

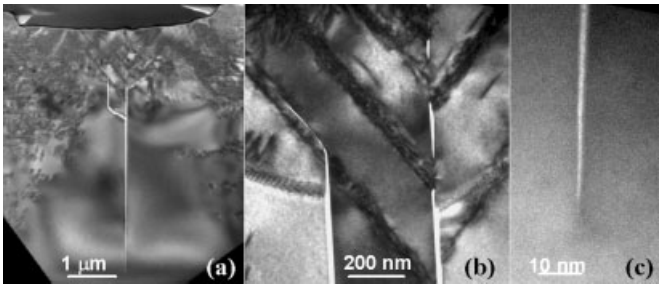

Fig. 4. TEM cross-section in GaAs below a 50 mN scratch. [110] bright beam conditions. (a) Global view featuring the median and lateral cracks surrounded by the area with dislocations. (b) Onset of cracks at the cross-section of the slip bands. (c) Atomically sharp tip of the crack.

plastic deformation on the side of the scratch (rounded part at the top of the image), down to a few microns inside the substrate. A few aligned isolated dislocations can even be observed further down (right and left of the MC crack). In contrast to the silicon, no other crystalline phases are detected. This is consistent with the indentation results of Bradby *et al*.[21] but are in contradiction to Li *et al*.[32] who found amorphous area after indentations at 50 mN load. Our experimental results suggest that the critical shear stress, due to GaAs scratching, is attained prior to the hydrostatic stress necessary to induce phase changes in the material. The striking feature of Figure 4b is the evident onset of the crack network at the crossing of the dislocation bands. Hence, plastic deformation induced by the shear stress inside the wafer eventually leads to the generation of nanoscale cracks (see the 50 nm long crack at the top of Figure 4b and of micro-cracks below the scratching tip. Finally, no dislocation or evenly plastic deformation is found in Figure 4c at the vicinity of the MC crack tip. This confirms the view of an atomically sharp crack in brittle semiconductor.[33]

The depth d of the MC crack is linked experimentally to the scratching force F by a relation of the type generally observed in indentation experiments:[33]

$$d \sim c \cdot F^{2/3} \quad (1)$$

where c is a function of the tip geometry and scratching speed. In the next section, it will be proven that this well-defined median crack is crucial for a proper initiation of fracture.

3.4. Crack at the Surface and Particle Generation: in-situ Scratching

The geometrical parameters of the diamond tip used for scratching will not only affect the subsurface crack pattern, but also the generation of cracks, particles and chips at the wafer surface.[24] These later surface features are likely to be undesirable for a reproducible scribing process, but can be necessary for material removal, such as for ductile machining of GaAs surfaces[34] or wire sawing of silicon.[35] It is therefore important to develop tools permitting to visualise the various scratching mechanisms taking place, with a high spatial resolution and sufficient depth focus.

The nano-scratching tool presented in the experimental section and in the literature[17,18] could be used for GaAs scratching inside an SEM. In particular, the process of particle generation could be observed even for sub-micron particles. Figure 5 illustrates two extreme cases of GaAs scratching, both performed with a cube corner (CC) tip. In Figure 5a, where the edge of the CC tip entered the sample first, the high load and strong ploughing of the edge inside the substrate lead to severe chip generation by cracking and particle detachment. In contrast, by applying a smaller force and for a scratch direction perpendicular to the case of Figure 5a, a ductile formation of chips is obtained and evidence of this process is presented in Figure 5b. The angle of the face pushes the chip to the side. Further in-situ SEM experimental studies are needed to observe and understand the particle generation behaviour of the different semiconductors with respect to moving tip.

3.4. Summary of Section 3

The examples presented in this section illustrate the various mechanisms that play a role during nano-scratching of semiconductors. There is strong interplay between the tip, the crystal orientation in conjunction with its mechanical

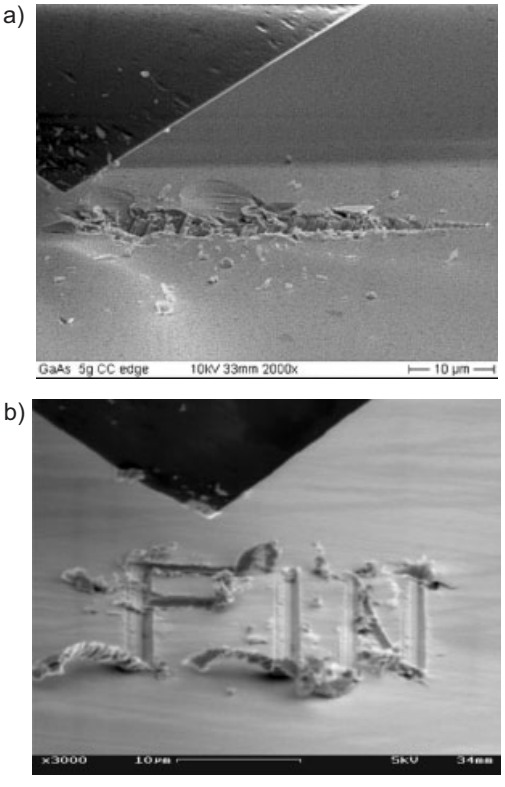

Fig. 5. SEM images of in-situ scratching of a GaAs (100) surface with a cube corner (CC) tip. (a) Scratching along a [011] direction with the edge first. (b) Scratching at lower load in both [011] and [01] direction showing the chips obtained by ductile deformation of GaAs. The insert shows the base of the CC tip in the plane of the sample.

properties and the dislocation / phases generated in the substrate, accompanied in some cases by the nucleation of microscopic cracks. Although the mechanisms presented in this section will always be acting to some extent, the proper choice of the scribing diamond tip is important for a particular application. In particular, when scribing for cleavage applications, it is preferable to choose a tip geometry allowing a reproducible smooth initial median crack creation, with no or as few as possible lateral crack and particle generation.

4. Semiconductor cleavage

4.1. Stress Field Applied to a Semiconductor Sample

In most cleavage experiments, semiconductor samples are clamped between two rigid plates and a rod transmits a force to the sample. Figure 6 illustrates Finite Element (FE) simulations performed on a laboratory experimental configuration used in this investigation. These FE simulations are made with ABAQUS CAE version 6.3.1®.[36] The clamps are 3D discrete rigid bodies whereas the sample is defined as a 3D deformable body. The element type used is the shell 4 node called S4R, as suggested in the literature.[36] The mesh for the GaAs sample, with geometrical dimensions $10 \times 6 \times 0.5$ mm^3, is made of 16985 elements with a refinement close to the crack tip. Half of the sample is fixed between the clamps and the wafer is subjected from the loading rod to a force $F = 3$N. The surface tensile stress σ_1 is displayed (Direction 1). In Figure 6a, a wafer without defect, a wide zone of maximum tensile stress at around 50 MPa is found at the top surface near the upper clamp. This stress is low compared to the strength of GaAs, which is in the GPa range. However, sharp defects, such as cracks, act as stress concentrators and so may lead to sample fracture. This could be the case of the median crack (MC) in Figure 3, whose typical location (in length) is represented by the dashed line in Figure 6a. In Figure 6b, a sample with a crack half the length and a depth of $^2/_3$ of the thickness sample is submitted to the same force. In such a case, the stress of 50 MPa and higher (black zone) concentrates only at the crack tip, and a significant component of tensile stress is still present at the surface.

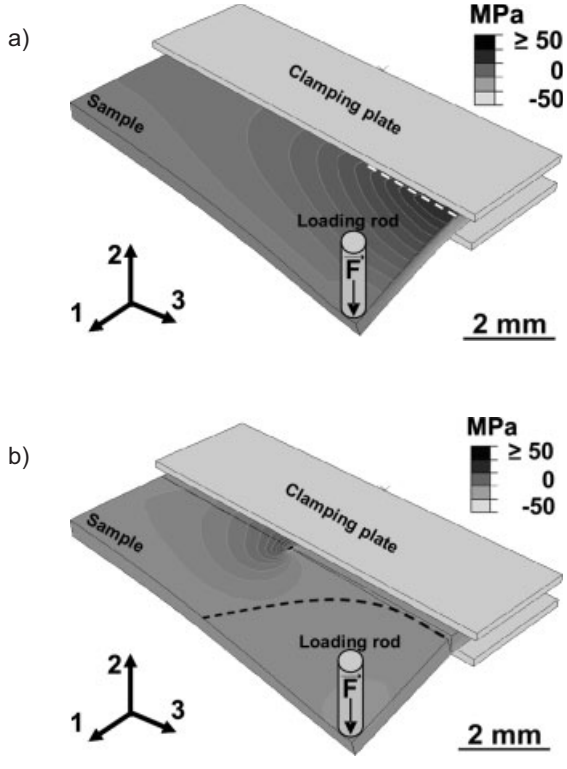

Fig. 6. FE simulations showing the tensile stress component σ 1 of a GaAs sample clamped between two rigid bodies. The deformation is exaggerated by a factor 10. (a) Wafer without defect submitted to a 3 N force. The dash line represents the typical location of a median crack shown in Figure 3. (b) Same, after introduction of a sharp crack half the length and a depth of 2/3 of the thickness sample. The black zone shows stresses higher or equal to 50 MPa. The dashed line illustrates a typical fracture path for an isotropic material such as glass.

4.2. Onset of Crack Propagation

According to the theory of Linear-Elastic Fracture Mechanics[12,13] (LEFM), if a sharp crack is located in an area of tensile stress, as illustrated by the dashed line in Figure 6a, the onset of crack propagation will be controlled by three parameters. They are a) the geometry of the initial crack, b) the magnitude of the applied load and hence the tensile stress perpendicular to the crack plane and c) the fracture toughness K_{IC} of the material. The subscript I indicates the type of loading condition, in this case the mode I or opening mode. Although, the loading configuration presented in Figure 6 is mixed between mode I and III, the mode I is the one which is predominant. In addition, since GaAs is an anisotropic material, the K_{IC} values vary depending on the crystal orientation. Based on the FIB, the median initial crack is expected to lie in the {110} planes which is defined, in Figure 6, by the axes 2 and 3. In this plane and for GaAs, the facture toughness was measured by several authors[37,38] and lies between 0.31 and 0.46 MPa $\cdot$ m$^{1/2}$.

It is well known in the theory of LEFM that a crack starts propagating when the stress intensity factor K_I reaches the critical value K_{IC}. This is also often used as the failure criterion for brittle materials. A simplified model for a semi-infinite crack in a thick sample is given by:[33]

$$K_1 = 1.12 \cdot \sigma_1 \cdot \sqrt{\pi \cdot d} \tag{2}$$

where d is the crack depth and σ_1 the tensile stress. The critical tensile stress σ_c is thus

$$\sigma_c = \frac{K_{IC}}{1.12 \cdot \sqrt{\pi \cdot d}} \tag{3}$$

In a situation as described by Figure 6a, a median crack of depth $d = 6$ μm would start to grow at a tensile stress $\sigma_1 \approx 65$ MPa corresponding to a force on the rod of 3.9 N. For a 100 μm thin wafer with the same median crack, the force necessary to propagate the crack is reduced to 200 mN.

It is evident from Eq. 3 that as the initial median crack gets smaller, higher stresses are required to initiate the crack. As shown in Section 3.4, a lower scratching force leads to a smaller median crack. Hence, scratching a wafer with lower loads will require the application of a larger force to begin the cleave propagation and evidence of this is found in Figure 7, which shows the force-displacement curves obtained from the experiments on four samples. A 150 μm thick GaAs (100) wafer had been scratched with a Cube Corner (CC) diamond tip at 5, 10, 30 and 200 mN loads prior to the cleavage experiment. The scratch was made along the [110] direction at a speed of 100 μm/s and with the edge of the three-sided diamond tip entering the surface first. During loading, the abrupt force fall in the curve marks the point where crack growth initiated. In accordance with Eqs. 1 and 3, the crack starts to grow at higher forces (684 mN) for lower scratch loads, whereas the propagation begins at an applied force of 213 mN for the scratch made with 200 mN load on the diamond tip.

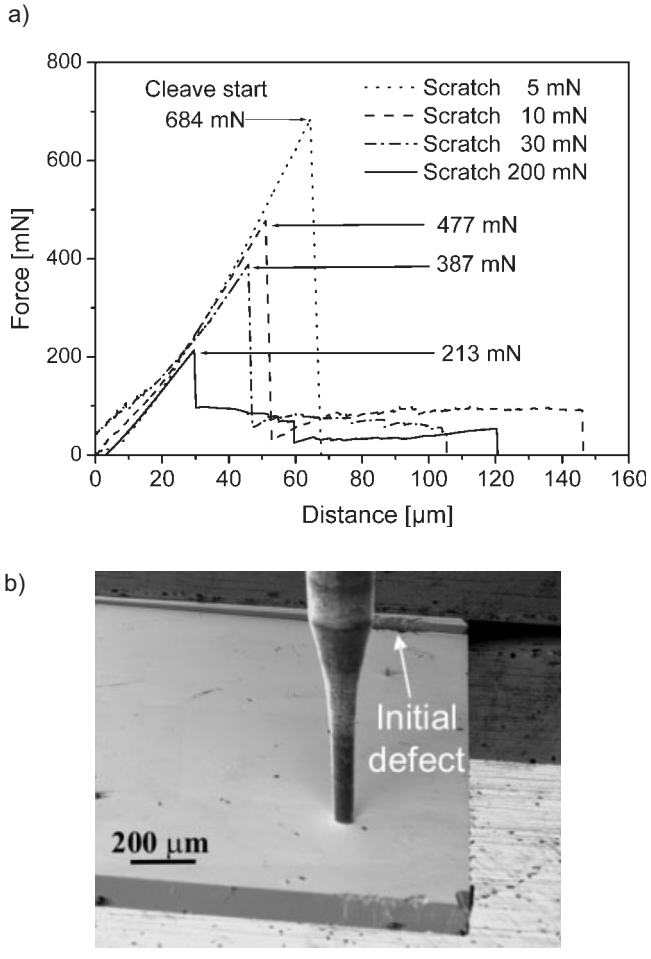

Fig. 7. Experiments performed with the displacement-controlled system. (a) Force-displacement curve obtained during the cleavage of samples scratched on the first 400 μm with a cube corner tip (scratching loads: from 5 mN to 200 mN). (b) SEM image of the sample scratched at 200 mN during the controlled part of the cleavage process; showing a crack opening displacement similar to the one in Figure 6b.

4.3. Crack Propagation over Macroscopic Distances

Depending on the shape of the initial crack and the geometrical configuration of the cleavage experiment, different kinds of crack fronts can develop in the sample. Figure 6b gives an example of FE simulations of a curved crack front due to a faster propagation top surface than through the thickness of the wafer. In this case, the strong crystal anisotropy and the localised tensile stress field in Direction 1 at the crack tip ensure its growth along the prescribed path (here parallel to the clamps' edges). It is, therefore, possible to obtain a cleavage along the whole length of the sample (in this example 10 mm) for material such as GaAs and InP. Note that for isotropic materials with no preferential cleavage plane, such as glass or PMMA, the other components of the stress field originating from the asymmetric loading configuration would have made the crack to bifurcate immediately. A typical path would then be similar to the one sketched as the dashed line in Figure 6b.

The crack propagation can be either unstable or stable.[14,16] The highest curve in Figure 7a illustrates a totally unstable crack growth. This is a classic behaviour when a small defect is present and as a consequence a high force F has to be applied to the sample to initiate fracture. Such behaviour leads to catastrophic failure, i.e. the whole wafer breaks without possible control. Evidence for this is seen for the sample scratched with a 5 mN load, which broke at once after the force reached its maximum value of 684 mN. Hence, the total strain energy accumulated during the application of the force to the sample was transmitted to the crack tip. For deeper initial MC cracks, two stages of crack propagation are observed as can be seen from Figure 7a. Firstly, unstable crack propagation takes place, causing the abrupt change in the measured force. During this phase the crack must accelerate and decelerate within a few micro-seconds as seen in Figure 7a. In the second phase, depending on the loading conditions, steady-state crack propagation may be observed. This is generally the case when the displacement of the rod is controlled. In such situation, the cleaving force remains more or less constant between 5 and 10 mN. It is possible, in this experimental configuration, to modify the average crack front speed by simply increasing the speed of the loading rod. In contrast, for some well defined initial crack geometry and loading conditions, the abrupt jump at the beginning can be avoided, and a steady-state propagation over the whole cleave can be obtained. This is illustrated by the force-displacement curve of Figure 8. By comparing the energy transmitted by the rod to the sample with the surface energy γ_s of the surfaces created during fracture, an upper value for γ_s of {110} planes is obtained at 0.69 J/m^2. Considering the equilibrium relationship given by:[33]

$$\frac{K_{IC}}{E} = 2 \cdot \gamma_s \tag{4}$$

the fracture toughness K_{IC} in the {110} planes in GaAs can be approximated. Taking E = 125 GPa, it is calculated that

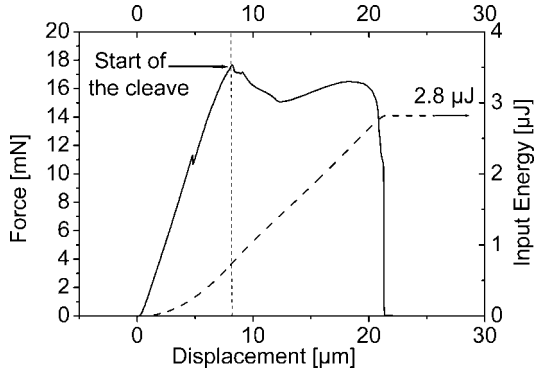

Fig. 8. Force-distance curve obtained during the cleavage of a thin GaAs sample. The dashed curve corresponds to the energy dissipated during fracture. The final work performed by the rod is 2.8 μJ and the cleaved area is 4.1 mm².

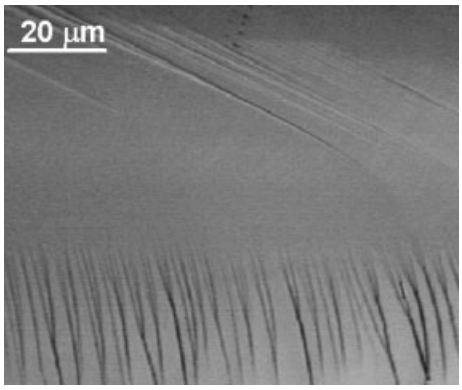

Fig. 9. Interference optical microscopy of GaAs {110} cleaved surface. The surface is roughened by the too fast release of strain energy to the crack tip and / or by mixed mode cracking (tensile and shear stress acting on the crack tip).

$K_{IC} < 0.41$ MPa · m . This value lies in the range of K_{IC} values 0.31–0.46 MPa · m found for GaAs in the literature.[37,38] This also indicates that in the experiment of Fig. 8, the mechanical energy introduced in the system was almost solely released for the creation of two new flat surfaces.

4.4. Surface Features

A number of authors have reported surface analyses of cleaved GaAs samples.[2,3,38] Sauthoff *et al.*[2] noticed that the surface features were correlated with the speed of crack propagation. However, the authors did not correlate these features with factors determining the speed, i.e. Specimen geometry, the loading conditions and rates, and the strain energy stored in the sample before the crack begins to grow. The three main conclusions can be drawn from the experiments discussed in this paper and are as follows:

a) For small initial median crack sizes (as for 5 mN scratch in Fig. 7a), catastrophic fracture ensues, i.e. the sample breaks immediately. In this case, the crack speed reaches a significant fraction of the Rayleigh surface wave speed; the whole cleavage process takes typically a few microseconds. The extra energy liberated during the crack propagation leads to surface roughening and to the emission of acoustic waves[2,14,16] and so numerous features are observed on the surface which probably result from the interaction of the crack front with elastic waves. This is illustrated in Figure 9, which shows an optical microscopy image of the cleaved surface of the sample scratched at 5 mN in Figure 7a. The surface presents river line patterns, which are usually perpendicular to the direction of the crack front[39] and have a height of a few nanometers. These ones coalesce and give rise to larger terraces of a few tens of nanometer in height.

b) For larger initial median cracks, the growth stabilises after a very fast crack initiation over a few mm and smoother crack propagation follows. Thus, surface features are observed at the beginning of the fracture, near the scratch, but optically flat mirror surfaces can be achieved further along the sample. Although not shown here, AFM scans performed on optically flat areas indicate an atomic level flatness.

c) Besides the geometry of the initial crack and depending on the relative advance of the crack front at the surface as well as in the depth of the sample, the crack tip might experience strong shear opening components (so-called Mode II and III). When not suppressed, these modes will lead to structures similar to those of Figure 9.[14] Additional effects such as the direction of the crack front inside the cleavage face have also been reported to influence the surface structure. In particular, Okui *et al.*[3] report that crack front advance in the [1$\bar{1}$0] direction (direction of the cut introduced in the sample in Fig. 6b) in the {110} plane is favourable to produce atomically flat surfaces. However, we observe that crack speed and shear stress components, which were not controlled in most experiments, play a more important factor than the in-plane anisotropy.

4.5. Summary of Section 4

It has been shown that, for a wafer without any defect, a wide zone of stresses exist around the upper clamp whereas for a wafer cracked until its middle and open two-third of its thickness, stress concentrates mainly at the crack tip. Additionally, based on fracture mechanics principles, the size and shape of the initial defect will influence the forces necessary to initiate the crack growth. By carefully controlling these parameters, it has been demonstrated that, for a material as brittle as GaAs, it is, not only, possible to avoid abrupt / unstable fracture leading to the creation of rough features on the cleaved surface, but also to control the crack propagation, even over macroscopic distance.

5. Conclusions

This paper has presented a detailed overview of the various phenomena occurring during nano-scratching and fracturing of semiconductor surfaces. The results show that scratching can be used as a paradigm tool for phase transformations in Si as well as intentional dislocation generation and, when higher forces are applied, generation of atomically sharp cracks in

GaAs and InP. These atomically sharp cracks, also called median cracks, are found to be a requisite to break reproducibly small size specimens of brittle semiconductor with typical dimensions in the mm range. Also shown are some of the basic requirements for the achievement of flat surfaces over macroscopic distance which can be summarised as a) a control of the crack speed to avoid surface roughening, which can be achieved by creating an initial median crack of sufficient depth, and b) a loading configuration that favours the Mode I opening of the crack in the prescribed fracture direction.

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