A Stochastic Perturbative Approach to Design a Defect-Aware Thresholder in the Sense Amplifier of Crossbar Memories

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The use of nanowire crossbars to build devices with large storage capabilities is a very promising architectural paradigm for forthcoming nanoscale memory devices. However, this new type of memory devices raises questions regarding how to test their correct operation. In particular, the variability affecting the decoder is expected to make very complex the test of these new devices. In this paper we present a method to simplify the test of these new devices by using a current thresholder to detect badly addressed nanowires. In the proposed method, the thresholder design is based on a stochastic and perturbative model of the current through the nanowires. Thus, the calculated thresholder parameters are robust against technology variation. As our experimental results indicate, the thresholder error probability is initially only $\sim 10^{-4}$, which can be also reduced further (up to $\sim 60\times$) by trading-off only $\sim 35\%$ area overhead in the memory.

I. Introduction

One of the most challenging issues in *Very Large Scale System Integration (VLSI)* is the continuously increasing device variability due to technological and physical limitations [5]. Circuits based on regular arrays can be more fault-tolerant, and they were suggested as the only currently realistic candidates for systems fabricated using bottom-up approaches by self-assembly of highly unreliable nanometer scale devices [12], such as molecular switches [21] and quasi one-dimensional *nanowires (NW)* [9].

These devices are suitable for ultra-high integration within a regular architecture called *crossbar* [10]. Crossbar memories can be realized in a separate part of a standard CMOS chips, where a decoder bridges the two parts having different scales [13, 16, 3]. The variability affecting the nanowires causes decoder defects, where more than one bit can be addressed simultaneously [4]. Consequently, *Pattern Sensitivity Faults (PSFs)* with no neighborhood pattern are expected to be dominant in crossbar memories. A general PSF test would be too expensive. So, we suggest to resolve the decoder-induced PSFs using a simple method based on a thresholder that detects badly addressed nanowires by comparing the current through the nanowires to fixed threshold values.

The purpose of this paper is to investigate the design aspects of a reliable current thresholder that identifies badly addressed nanowires, and to estimate the thresholder error probability. Thereby, a model for the current and the noise through the nanowire array is developed by combining a stochastic approach with a perturbative analysis.

This rest of the paper is organized in the following way. In Section 2 we review the work related to crossbar arrays, ranging from devices to architectures, and we focus on the nanowire decoder. In Section 3 we present the system architecture, and motivate the need for testing the nanowires. Section 4 describes the defect model and the requirements on the optimal thresholder. Section 5 introduces the perturbative approach. Then, in Section 6 we enhance the perturbative approach with a stochastic description, which completely quantifies the noise level and the optimization conditions for the thresholder. Finally, in Section 7, we simulate the implemented circuit, investigate the performance of the thresholder, and analyze the technological trade-offs of its design parameters that can be exploited to improve its robustness against technology variations.

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II. Related Work

Silicon Nanowires (SiNW) can be fabricated with bottom-up and top-down techniques [17, 8, 20, 19, 7, 22]. Connections between wires were demonstrated using molecular switches grafted at the wire crosspoints [21]. In [18], logic gates based on SiNW and switching crosspoints were proposed and architectural paradigms for building logic circuits was suggested in [10, 14, 11, 15]. Crossbars are also suitable for information storage, where the information is represented by the on/off state of the molecular switch grafted at the crossing of two nanowires [21].

Crossbar circuits can be fabricated as a separate part of a CMOS circuit; then a decoder is needed in order to address every nanowire and to bridge the scales between the sub-lithographic crossbar and the CMOS circuit defined at the lithography scale. Several decoder types were suggested depending on the technology. The axial [13] and radial [24] decoders were proposed for differentiated nanowires, having an in-situ defined doping profile. The mask-based [3] and random-contact [16] decoders were suggested for undifferentiated nanowires with no defined doping profile.

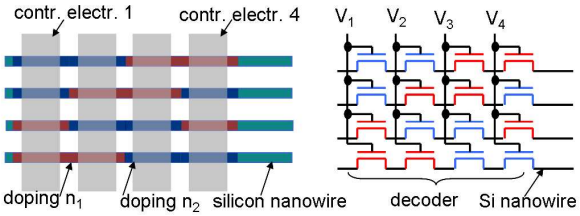

Fig. 1. Nanowire array including decoder (left) and equivalent circuit (right)

A schematic principle of an array of nanowires with a decoder [4] is illustrated in Figure 1. The alternation of regions having different doping levels or different insulator types on every nanowire defines a *pattern* of *field effect transistors (FET)* with different threshold voltages (V_T), and the *address* of the nanowire. The FET channel is the nanowire and its gate is represented by one of the M *mesowires* crossing the set of N nanowires. Thus, the decoder is formed by a set of N SiNWs carrying a series connection of M transistors each. By applying the gate voltages switching all the FETs of the same nanowire on, the latter becomes conducting and all other nanowires in the array become highly resistive. The gate electrodes are also designated by addressing or control electrode. In [4], it was shown that the high V_T variability induces a change in nanowire addresses. Some addresses can then acti-

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vate 0, 1, 2 or more nanowires instead of one single nanowire.

III. Crossbar Memory Architecture and Test

A. Architecture and Operation of Crossbar Memories

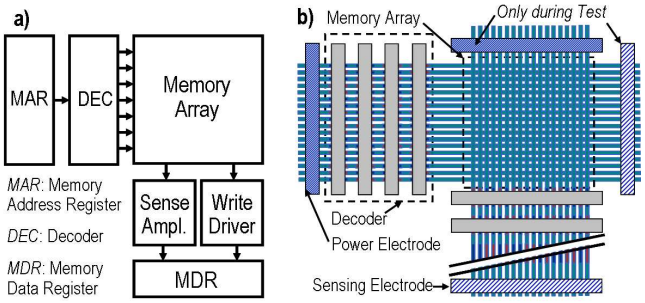

Fig. 2. Crossbar memory architecture: a) RAM architecture at the functional level, b) Sub-lithographic part of a crossbar memory

Even though there are no complete memory systems based on the crossbar architecture yet, we believe that it will have the same architecture as CMOS memories [1], which is illustrated in Fig. 2.a. Unlike conventional RAM, crossbar memories have two parts: a sub-lithographic part formed by the decoder and the memory array (Fig. 2.b) and fabricated in one of the emerging technologies described in Sec. II; and a lithographic part formed by the rest of the circuit and fabricated in CMOS technology.

The information is assumed to be stored in molecular switches grafted to every pair of crossing nanowires. In the on-state, the molecule is conducting (logic 1) and in the off-state, it is high resistive (logic 0). The writing operation is performed by, first selecting the bit to be written, and then, by applying a large positive or negative voltage at the pair of nanowires connected by the molecular switch in order to set the molecular state, *i.e.*, the bit value. On the other hand, the reading operation is current-based. In fact, if the molecule is in the off-state, then the nanowire in the lower level is almost floating [21] and no correct voltage level can be sensed. Consequently, the reading operation is performed by selecting the bit to be read, then by measuring the current through the sensing electrode (see Fig. 3.a to 3.d). Thus, the current-based read operation in crossbar memories necessitates a thresholder as a part if the sense amplifier, in order to set the limit between the logic values 0 and 1, and to translate them into logic levels that can be stored in the memory data register.

B. Testing Crossbar Memories

Many sources of variability may cause errors in the sensed signal, such as the doping level and geometry variation. In particular, we focus in this paper on defects caused by the nanowires in the memory array and in the decoder. The doping level and geometry variation in the nanowire part forming the memory array induce a change in the resistance of the nanowires and a variation of the sensed current level. In the decoder part, these sources of variability can induce a drastic change in the on-resistance of the transistors forming the decoder by modifying their threshold voltage as analyzed in detail in the following paragraphs. Also other possible defects induced by the molecular switches can theoretically accept the reliable operation of crossbar memories, but the quantification and analysis of this type of secondary defects has not been presented yet in the literature and goes beyond the scope of this paper. Nevertheless, their modeling is perfectly complementary to this work.

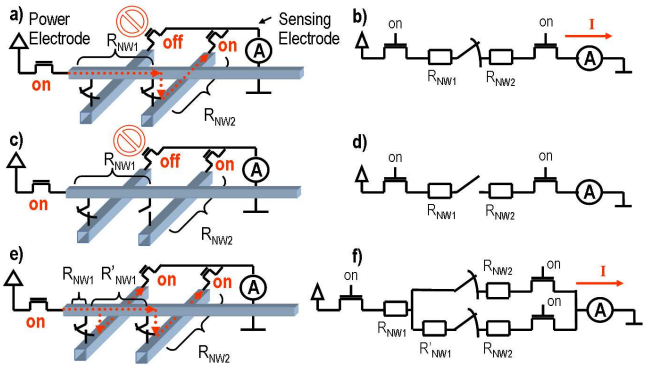

Fig. 3. Read operation in a memory with 2 bits. During correct operation, only one bit is addressed and read: a) Correct reading of '1', b) Equivalent circuit for reading '1', c) Correct reading of '0', d) Equivalent circuit for reading '0', e) Defective reading of two bits, f) Equivalent circuit for defective reading

In [4], the threshold voltage variation was shown to cause defects in the decoder in such a way that by applying an address, any number of nanowires can be activated instead of one single nanowire. Fig. 3.e and 3.f show an example of defective addressing in the second nanowire layer. Thus, the sense amplifier reads the superposition of the information stored in two bits. The thresholder cannot properly distinguish between the sensed signals resulting from the following cases: *i*) one bit with the value 1, and *ii*) the superposition of two bits whereby at least one of them has the value 1. In such a situation, the read operation of the first bit yields a result depending on the state of the second bit, which causes *coupling faults (CF)* in the memory [1]. Considering the fact that decoder defects typically make 2, 3 or more nanowires in each array active with the same address [4], the number of inter-dependant bits can be as large as 4 to 9 or even more, without necessarily having neighboring locations. This leads to the more critical pattern-sensitivity faults [1].

In order to avoid complex and exhaustive PSF test procedures on the whole memory [2], it is attemptable to resolve the PSF caused by the decoder defects, before performing the conventional memory test. The thresholder can carry out this operation by checking the addresses of all nanowires in every layer (after separating them) and keeping only the addresses that activate one single nanowire. This procedure has a linear complexity with N, the number of nanowires in a layer (where N^2 is the number of bits in the memory). While it represents an additional testing step, this testing procedure, that we call *nanowire test*, resolves the necessity of an exhaustive PSF testing of the whole memory, whose complexity is exponential with N^2. However, we expect that the molecular switches will also induce PSFs that we do not consider in this paper. Since only neighboring molecules are likely to interact with each other, one can assume neighborhood patterns for the PSFs caused by the molecules. Therefore, simplified PSF procedures having a linear complexity with N^2 can be applied [2].

IV. Defect Model and Thresholder Design

A nanowire array and the thresholder as a part of the sense amplifier are depicted in Fig. 4.a. For every address applied at the decoder, a validation signal is given by the thresholder indicating whether *i*) a single nanowire is addressed, or *ii*) no nanowire or more than one nanowire are addressed. The thresholder senses I_s, after a possible amplification, then it compares it to two reference values (I_0 and I_1 with $I_0 < I_1$). If the sensed current is smaller than I_0, then no nanowire is addressed. If the sensed current is larger than I_1, then at least two nanowires are activated with the same address. If the sensed

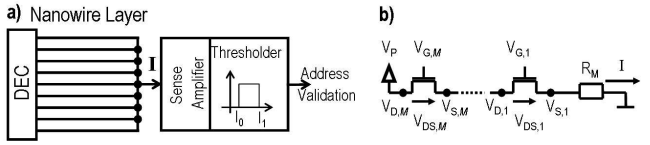

Fig. 4. Thresholder operation during the nanowire test: a) Baseline architecture, b) Equivalent circuit of one nanowire under test.

current is between the reference current levels, then only one nanowire is activated and the address is considered to be valid.

In our defect model we assume 2 sources of variability of the sensed current: *i*) Variation of the threshold voltages of the transistors in the decoder: We assume, as for conventional MOS devices [4], that $V_{\rm T}$ follows a normal distribution with known mean value $\overline{V}_{\rm T}$ and standard deviation $\sigma_{\rm T}$; *ii*)Variation of the nanowire resistance in the memory array: In the mathematical model, we assume that this resistance is fixed. Then, we investigate the impact of its variation on the results.

By assuming that the $V_{\rm T}$'s are stochastic variables and the nanowire resistance is fixed, we model $I_{\rm s}$ as a stochastic variable, whose distribution parameters depend on the nanowire resistance. Thus, the calculation of the thresholder parameters I_0 and I_1 results from a stochastic optimization. Their optimal values are obtained by maximizing the probability that a correct address is detected (P_1: the conditional probability that $I_{\rm s}$ is between I_0 and I_1 given that only one nanowire is activated), and the probabilities that a defective address is identified as such (P_0 and P_2: the conditional probability that $I_{\rm s}$ is below I_0 or beyond I_1 given that no nanowire or more than one single nanowire are activated, respectively):

$$P_0 = \Pr\{(I_{\rm s} \leq I_0) \text{ given that no NW is addressed}\}$$
$$P_1 = \Pr\{(I_0 < I_{\rm s} < I_1) \text{ given that 1 single NW is addressed}\}$$
$$P_2 = \Pr\{(I_1 \leq I_{\rm s}) \text{ given that 2 or more NWs are addressed}\}$$

Then, the probability that all three events happen simultaneously is given by: $P_0 \times P_1 \times P_2$ (assuming that the considered events are independent). Consequently, we can define the error probability of the thresholder as:

$$\epsilon = 1 - P_0 \times P_1 \times P_2 \tag{1}$$

The purpose of this work is to design the thresholder with the smallest error. Designing the thresholder means how to optimize I_0 and I_1. In the rest of the paper, we derive the analytical expressions of P_0, P_1 and P_2. We first model the stochastic distribution of the sensed signal $I_{\rm s}$ under variability conditions; then we optimize the choice of the reference currents I_0 and I_1 which minimize the thresholder error ϵ.

V. Perturbative Current Model

From the mathematical point of view, it should be possible to derive the *exact* distribution of the sensed current by considering the parameters and the $I-V$ characteristics of the circuit formed by the SiNWs. However, even the most basic $I-V$ characteristics of the transistors are not linear; thus making the derivation of an analytical expression of the distribution of the sensed current difficult. We introduce in this section our approach based on sensitivity analysis, which enables the modeling of the sensed current. We focus here on correctly addressed nanowires and we consider the impact of the variability of the $V_{{\rm T},i}$'s on the distribution of the current through these nanowires.

During the nanowire test phase, every nanowire is disconnected from the crossing layer as explained in Section III.B. It can be modeled as a wire connecting the power electrode to the sensing electrode and formed by two parts (see Figure 4.b): the decoder part that is a series of M pass transistors, and the memory part. Since the memory part is disconnected from the second nanowire layer, it is modeled as a resistive load $R_{\rm M}$.

The transistors in the decoder part of the nanowire are SiNW FETs. Their model is expected to include more scaling and coupling effects than the usual model for bulk MOS FET. We model the devices in this section in a general way as a *black-box* representing voltage-controlled current sources, *i.e.*: $I = f(V_{\rm DS}, V_{\rm GS}, V_{\rm T})$ where I is the drain-source current, $V_{\rm DS}$, $V_{\rm GS}$ and $V_{\rm T}$ are respectively the drain-to-source, gate-to-source and threshold voltages. The decoder design approaches explained in Section II are based in the simplest case on two types of transistors having two different $V_{\rm T}$'s ($V_{\rm T,Ref0}$ and $V_{\rm T,Ref1}$ such that $V_{\rm T,Ref0} < V_{\rm T,Ref1}$, and we define $\Delta V_{\rm T} = V_{\rm T,Ref1} - V_{\rm T,Ref0}$).

We consider a nanowire as modeled in Figure 4.b, where a sequence of control voltages ($V_{{\rm GS},1}$,...,$V_{{\rm GS},M}$) are applied. This sequence switches every transistor on and the M conducting transistors generate a current flow I through the nanowire. Every variation of $V_{\rm T}$ results in a variation of the current through the nanowire:

$$I = I^{\rm OP} + \delta I \tag{2}$$

Here, the signal I is linearized around the *operating point (OP)* and divided into a *large* $I^{\rm OP}$ and a *small signal* δI [6]. The large signal needs a precise device model and can be estimated with a SPICE simulator, while the small signal is easier to calculate by linearizing all the equations describing the circuit around the OP.

In the following, we derive the general expression of δI. The fixed variables are the voltage of the sensing electrode set as voltage reference, the power supply ($V_{\rm P}$) and the gate voltage ($V_{\rm G}$), both with respect to the reference. We denote by i the transistor index ($i = 1 \ldots M$). Then, the equations describing the circuit in Figure 4.b are:

$$V_{{\rm GS},i} = V_{\rm G} - R_{\rm M} \cdot I - \sum_{j=1\cdots i-1} V_{{\rm DS},j} \tag{3}$$

$$V_{\rm P} = \sum_{i=1\cdots M} V_{{\rm DS},i} + I \cdot R_{\rm M} \tag{4}$$

$$I = f(V_{{\rm DS},i}, V_{{\rm GS},i}, V_{{\rm T},i}) \;\forall\, i \tag{5}$$

Since $V_{{\rm GS},1} = V_{\rm G} - R_{\rm M} \cdot I$, we use the following convention: $\sum_{j=1\cdots 0} V_{{\rm DS},j} = 0$. The linearization of the previous equations yields to:

$$\delta \mathbf{V}_{\rm DS} = \mathbf{A}^{-1} \cdot \mathbf{B} \cdot \delta \mathbf{V}_{\rm T} \tag{6}$$

where the variational vectors are: $\delta \mathbf{V}_{\rm DS} = [\delta V_{{\rm DS},1}, \cdots, \delta V_{{\rm DS},M}]^\intercal$ and $\delta \mathbf{V}_{\rm T} = [\delta V_{{\rm T},1}, \cdots, \delta V_{{\rm T},M}]^\intercal$. The matrices $\mathbf{A}$ and $\mathbf{B}$ are given by:

$$\mathbf{A} = \begin{bmatrix} 1 + r_1 \cdot g_{{\rm DS},1} & 1 & \cdots & 1 \\ 1 - r_2 \cdot g_{{\rm m},2} & 1 + r_2 \cdot g_{{\rm DS},2} & \cdots & 1 \\ \vdots & & & \vdots \\ 1 - r_M \cdot g_{{\rm m},M} & 1 - r_M \cdot g_{{\rm m},M} & \cdots & 1 + r_M \cdot g_{{\rm DS},M} \end{bmatrix}$$

$$\mathbf{B} = \begin{bmatrix} r_1 \cdot g_{{\rm T},1} & 0 & \cdots & 0 \\ 0 & r_2 \cdot g_{{\rm T},2} & \cdots & 0 \\ \vdots & & & \vdots \\ 0 & 0 & \cdots & r_M \cdot g_{{\rm T},M} \end{bmatrix}$$

We used the following notations: $g_{{\rm DS},i} = \partial f_i / \partial V_{{\rm DS},i}$, $g_{{\rm m},i} = \partial f_i / \partial V_{{\rm GS},i}$, $g_{{\rm T},i} = \partial f_i / \partial V_{{\rm T},i}$ and $r_i = R_{{\rm M},i} || g_{{\rm m},i}^{-1}$

(parallel resistance connection). Finally, substituting Equation 6 in the linearized version of Equation 4 results in the following expression, with $\mathbf{v} = [1, \cdots, 1]^\intercal$:

$$\delta I = -1/R_{\mathrm{M}} \cdot \mathbf{v}^\intercal \cdot \mathbf{A}^{-1} \cdot \mathbf{B} \cdot \delta \mathbf{V}_{\mathrm{T}} \quad (7)$$

This perturbative approach approximates δI as a linear combination of all $\delta V_{\mathrm{T},i}$'s. This approach will be completed in the following section by a stochastic component: assuming that we have a model for the stochastic distribution of $\delta V_{\mathrm{T},i}$'s, then we can derive the distributions of δI (Equation 7) and I (Equation 2).

VI. Stochastic Current Model

In this section we model the sensed current as the sum of three components, which are analyzed separately. For each current component, a stochastic model is derived. Then, the requirements on the thresholder parameters are expressed in terms of the established stochastic distributions.

A. Components of the Sensed Signal

We divide the sensed current into a useful and a noisy part. The useful signal (I_{u}) is the current that flows through a nanowire when it is correctly addressed. On the other hand, the noise can be generated by two different processes: intrinsically (I_{i}), or defect-induced (I_{d}).

When a nanowire is not activated by the applied address, then the transistors laying in its decoder part generate a subthreshold current, which we call *intrinsic noise* of a single nanowire $I_{\mathrm{i},0}$. The total intrinsic noise is given by: $I_{\mathrm{i}} = N_{\mathrm{off}} \times I_{\mathrm{i},0}$, where N_{off} is the number of non-activated nanowires.

We consider now the case of a nanowire that is activated by the address corresponding to another nanowire. In this case, the nanowire with the valid pattern is called a *victim*, and the nanowires with the defective pattern produce a *defect-induced noise*. Their number is denoted by N_{def}. Since the total number of nanowires is N, the following equation must hold $N_{\mathrm{use}} + N_{\mathrm{off}} + N_{\mathrm{def}} = N$, where $N_{\mathrm{use}} = 0$ if no nanowire is activated by the applied code, and $N_{\mathrm{use}} = 1$ otherwise.

B. Distribution of the Useful Signal

Every V_{T} is considered as an independent and normally distributed stochastic variable with mean value $\overline{V}_{\mathrm{T}}$ and standard deviation σ_{T} [4]. For instance, if binary addresses are used, then $\overline{V}_{\mathrm{T}} = V_{\mathrm{T,Ref0}}$ holds for the transistors corresponding to the address bits '0', and $\overline{V}_{\mathrm{T}} = V_{\mathrm{T,Ref1}}$ holds for the transistors corresponding to the address bits '1'. The distribution can be noted in the following way: $V_{\mathrm{T}} \sim \mathcal{N}(\overline{V}_{\mathrm{T}}, \sigma_{\mathrm{T}}^2)$, and the same notation holds for the other (one- or multi-dimensional) stochastic variables throughout this section. If the nanowire pattern is correct, then the operating point of V_{T} coincides with its mean value. However, if a defect happens so that the bit representing V_{T} flips (for instance 1 becomes 0), then the operating point of V_{T} is shifted from the mean value of V_{T} by $-\Delta V_{\mathrm{T}}$.

We consider a defect-free nanowire generating the useful signal I_{u}. The operating points for the $V_{\mathrm{T},i}$'s are their respective mean values: $\mathbf{V}_{\mathrm{T}}^{\mathrm{OP}} = \overline{\mathbf{V}}_{\mathrm{T}}$. Given that $\delta \mathbf{V}_{\mathrm{T}} = \mathbf{V}_{\mathrm{T}} - \mathbf{V}_{\mathrm{T}}^{\mathrm{OP}}$, then $\delta \mathbf{V}_{\mathrm{T}} \sim \mathcal{N}(\mathbf{0}, \sigma_{\mathrm{T}}^2 \cdot \mathbf{v})$. The useful signal follows the distribution resulting from Equation 2. The operating point is the on-current of the transistors I_{on}, which is calculated with SPICE simulator; whereas the variable part is given by Equation 7 by applying the summation rule of independent and normally distributed variables. From the distribution of $\delta \mathbf{V}_T$ established here, it follows that: $\delta I_{\mathrm{u}} \sim \mathcal{N}(\mathbf{0}, \sigma_{\mathrm{T}}^2/R_{\mathrm{M}}^2 \cdot \|\mathbf{v}^\intercal \mathbf{A}^{-1} \mathbf{B}\|^2)$. Since $I_{\mathrm{u}} = I_{\mathrm{u}}^{\mathrm{OP}} + \delta I_{\mathrm{u}}$, I_{u} can be modeled as a normal variable following the distribution f_{u} with the following parameters:

$$\begin{aligned} I_{\mathrm{u}} &\sim \mathcal{N}(\overline{I}_{\mathrm{u}}, \sigma_{\mathrm{u}}^2) \\ \overline{I}_{\mathrm{u}} &= I_{\mathrm{on}} \\ \sigma_{\mathrm{u}} &= \sigma_{\mathrm{T}}/R_{\mathrm{M}} \cdot \|\mathbf{v}^\intercal \mathbf{A}^{-1} \mathbf{B}\| \end{aligned} \quad (8)$$

C. Distribution of the Defect Induced Noise

We consider a nanowire with a defective pattern, which can be activated by the address of another nanowire. Some of its transistors have the operating point of their V_{T} shifted by ΔV_{T}. For these transistors $\delta V_{\mathrm{T},i} \sim \mathcal{N}(\Delta V_{\mathrm{T}}, \sigma_{\mathrm{T}}^2)$ holds. For the other transistors $\delta V_{\mathrm{T},i} \sim \mathcal{N}(0, \sigma_{\mathrm{T}}^2)$ holds. We describe the series of shifts at all transistors by the vector $\mathbf{s} \in \{0,1\}^M$, where $\Delta V_{\mathrm{T}} \cdot s_i \in \{0, \Delta V_{\mathrm{T}}\}$ indicates whether a threshold voltage shift happened at the transistor i ($i = 1 \ldots M$). Then, by applying the summation rule of independent stochastic variables on Equation 7, we get the distribution of the defect-induced noise generated by one single nanowire: $\delta I_{\mathrm{d},0} \sim \mathcal{N}(-\Delta V_{\mathrm{T}}/R_M \cdot \mathbf{v}^\intercal \mathbf{A}^{-1} \mathbf{B} \cdot \mathbf{s}, \sigma_{\mathrm{T}}^2/R_M^2 \cdot \|\mathbf{v}^\intercal \mathbf{A}^{-1} \mathbf{B}\|^2)$. Here again, the operating point for $I_{\mathrm{d},0}$ is the same as before, I_{on}, since all the transistors of the decoder part of this defective nanowire are switched on. Consequently, the distribution of the defect-induced noise by one single nanowire $I_{\mathrm{d},0}$ can be expressed as follows: $\delta I_{\mathrm{d},0} \sim \mathcal{N}(I_{\mathrm{on}} - \Delta V_{\mathrm{T}}/R_M \cdot \mathbf{v}^\intercal \mathbf{A}^{-1} \mathbf{B} \cdot \mathbf{s}, \sigma_{\mathrm{T}}^2/R_M^2 \cdot \|\mathbf{v}^\intercal \mathbf{A}^{-1} \mathbf{B}\|^2)$.

The number of nanowires N_{def} that generate the defect-induced noise depends on the variability level of the technology. Every one of them is characterized by a vector $\mathbf{s}_i, i \in \{1, \ldots, N_{\mathrm{def}}\}$ and a distribution $\delta I_{\mathrm{d,i}} \sim \mathcal{N}(I_{\mathrm{on}} - \Delta V_{\mathrm{T}}/R_M \cdot \mathbf{v}^\intercal \mathbf{A}^{-1} \mathbf{B} \cdot \mathbf{s}_i, \sigma_{\mathrm{T}}^2/R_M^2 \cdot \|\mathbf{v}^\intercal \mathbf{A}^{-1} \mathbf{B}\|^2)$. Since the total defect-induced noise is equal to the sum of all defect-induced noises generated by single nanowires, the distribution of the total defect-induced noise follows the normal distribution $f_{\mathrm{D},N_{\mathrm{def}}}$ given by the following parameters:

$$\begin{aligned} I_{\mathrm{D},N_{\mathrm{def}}} &\sim \mathcal{N}(\overline{I}_{\mathrm{D},N_{\mathrm{def}}}, \sigma_{\mathrm{D},N_{\mathrm{def}}}^2) \\ \overline{I}_{\mathrm{D},N_{\mathrm{def}}} &= N_{\mathrm{def}} \cdot I_{\mathrm{on}} - \frac{\Delta V_{\mathrm{T}}}{R_M} \cdot \mathbf{v}^\intercal \mathbf{A}^{-1} \mathbf{B} \cdot \sum_{i=1 \ldots N_{\mathrm{def}}} \mathbf{s}_i \\ \sigma_{\mathrm{D},N_{\mathrm{def}}} &= \sqrt{N_{\mathrm{def}}} \cdot \sigma_{\mathrm{T}}/R_{\mathrm{M}} \cdot \|\mathbf{v}^\intercal \mathbf{A}^{-1} \mathbf{B}\| \end{aligned} \quad (9)$$

D. Distribution of the Intrinsic Noise

The intrinsic noise is generated in the subthreshold regime of the transistors forming the decoder part of the nanowire. If a nanowire that is supposed to be switched off, partially or totally turns on because of defects affecting the V_{T}, then it is considered to be generating a defect-induced noise. In contrast, if the defects shift the threshold voltages of the nanowire to higher values and make it more resistive, then the nanowire generates less intrinsic noise. In the worst case, the maximum intrinsic noise of a single nanowire $I_{i,0}$ is equal to the off-current of the transistors fabricated with the considered technology (I_{off}). As explained at the beginning of this section, the total intrinsic noise is equal to the the sum of all signals generated by the N_{off} transistors that are switched off. Thus, $I_i = N_{\mathrm{off}} \times I_{\mathrm{off}}$ is the maximum expected intrinsic noise, which is the worst-case consideration of the intrinsic noise, as a constant additive current.

E. Requirements on the Thresholder Parameters

Given the electrical expressions and the stochastic distributions of the different components of the sensed signal, it is possible now to express analytically the probabilities P_0, P_1 and P_2 (Section IV).

If no nanowire is addressed, then $N_{\text{use}} = 0, N_{\text{off}} = N, N_{\text{def}} = 0$ and $I_{\text{s}} = N \cdot I_{\text{off}}$. The probability P_0 of detecting that no nanowire is addressed, is simply equal to 1 if I_0 is set greater than $N \cdot I_{\text{off}}$, otherwise it is equal to 0. With $\delta(x)$ the Dirac distribution around 0, we obtain:

$$P_0 = \int_{-\infty}^{I_0} \delta(I - N \cdot I_{\text{off}})\, \mathrm{d}I \tag{10}$$

If we consider the case that one single nanowire is addressed, then $N_{\text{use}} = 1, N_{\text{off}} = N - 1, N_{\text{def}} = 0$ and $I_{\text{s}} = I_{\text{u}} + (N-1) \cdot I_{\text{off}}$. The additional term $(N-1) \cdot I_{\text{off}}$ shifts the mean value of I_{u} by $(N-1) \cdot I_{\text{off}}$; or equivalently, it shifts the borders of the integral P_1 by $(N-1) \cdot I_{\text{off}}$:

$$P_1 = \int_{I_0-(N-1)\cdot I_{\text{off}}}^{I_1-(N-1)\cdot I_{\text{off}}} f_{\text{u}}(I)\, \mathrm{d}I \tag{11}$$

Now, we consider the last case in which one or more nanowires are generating defect-induced noise. Here $N_{\text{use}} = 1$ and $N_{\text{off}} = N - 1 - N_{\text{def}}$ hold; where N_{def} depends on the variability level of the technology. The sensed signal is given by: $I_{\text{s}} = I_{\text{u}} + I_{\text{d}} + (N - 1 - N_{\text{def}}) \cdot I_{\text{off}}$. Let B_i be the event that exactly i nanowires are generating a defect-induced noise, $B = \cup B_i$ and $A = \{I_1 \leq I_{\text{s}}\}$. Then, by using the Bayesian relations, we obtain:

$$\begin{aligned} P_2 &= \Pr\{A|B\} \\ &= 1/\Pr\{B\} \times \sum_{i=1\ldots N_{\text{def}}} \Pr\{A|B_i\} \cdot \Pr\{B_i\} \end{aligned} \tag{12}$$

The expression $\Pr\{A|B_i\}$ represents the conditional probability that we detect the defect-induced noise generated by one or more nanowires, given the fact that there are exactly i nanowires generating this kind of noise, with $i = 1 \ldots N_{\text{def}}$. Equation sets 8 and 9 give the distributions that can be used to calculate $\Pr\{A|B_i\}$. Because of the intrinsic noise, the borders of the integral P_2 are shifted by $(N - 1 - i) \cdot I_{\text{off}}$:

$$\Pr\{A|B_i\} = \int_{I_1-(N-1-i)\cdot I_{\text{off}}}^{+\infty} (f_{\text{u}} + f_{\text{D},i})\,(I)\, \mathrm{d}I \tag{13}$$

The symbol $(f_{\text{u}} + f_{\text{D},i})$ denotes the distribution resulting from the sum of both independent and normal distributions f_{u} and $f_{\text{D},i}$ for i nanowires with defect-induced noise, which is also a normal distribution with the mean value $\overline{I}_{\text{u}} + \overline{I}_{\text{D},i}$ and the standard deviation $\sqrt{\sigma_{\text{u}}^2 + \sigma_{\text{D},i}^2}$. In order to calculate $\Pr\{B_i\}$, we refer to an algorithm presented in [4], which enumerates all possible defect scenarios for a given variability level and calculates their respective probabilities.

VII. Simulation Results

We implemented the circuit by using the bulk MOS FET model for the considered SiNW FET, as described in [23]. The linearization around the the operating point was performed in the linear region, in order to keep the power supply, as low as possible. We assumed the same bias for all transistors, *i.e.*, the same operating point. This simplifies $\mathbf{A}$ and $\mathbf{B}$ and we obtain $\mathbf{v}^\intercal \mathbf{A}^{-1}\mathbf{B} = g_{\text{m}}/(g_{\text{DS}} + M/R_{\text{M}}) \cdot \mathbf{v}^\intercal$. We also considered a reflexive code for the nanowire addressing scheme [4]. Since M transistors are used in the decoder, the vector $\mathbf{s}_i$ has in average $M/4$ entries $\neq 0$. The algorithms presented in [4] were used to verify that the likelihood that one single nanowire generates the defect-induced noise is orders of magnitude larger than the likelihood that 2 or more nanowires generate the defect-induced noise. We therefore set N_{def} to 1. This yields in average $\mathbf{v}^\intercal \mathbf{A}^{-1}\mathbf{B} \sum_{i=1}^{N_{\text{def}}} \mathbf{s}_i = (g_{\text{m}} \cdot M/4)/(g_{\text{DS}} + M/R_{\text{M}})$.

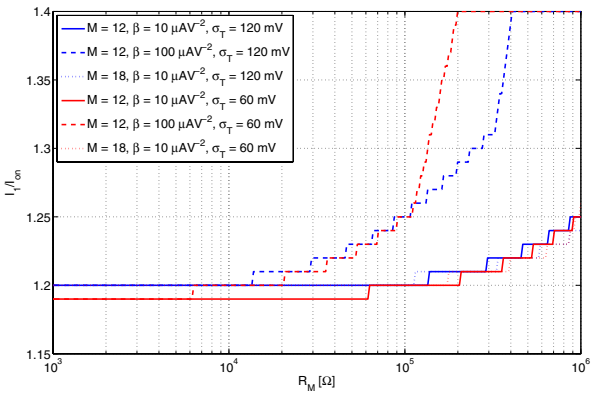

Fig. 5. Optimal value of I_1 vs. design and technology parameters

These expressions are sufficient to fully quantify the current distributions in Equations 8 and 9. We then inserted them into the probabilities of a reliable thresholder operation (Equation 10 to 13) and we optimized the values of I_0 and I_1 in these expressions in order to ultimately minimize the error probability of the thresholder (Equation 1). For the electrical parameters, we fixed V_{P} and ΔV_{T} to 0.9 V. Then, the transistor transconductance β was not fixed. Its value depends on the nanowire dimensions and the technology quality, and it was varied between 10 and 100 μAV^{-2}. Other technology parameters that were not fixed are the resistance of the nanowire in the memory part R_{M} and the variability level expressed as the standard deviation of the threshold voltage σ_{T}. The number of transistors M was left as a design parameter, because it depends on the memory size.

The thresholder parameters that we are investigating in this work are I_0 and I_1. The minimal value of I_0 is given by P_0 in Equation 1: I_0 has to be greater than $N \cdot I_{\text{off}}$ in order to insure that $P_0 = 1$. While keeping I_0 larger than this critical value, we plotted I_1 that gives the minimal thresholder error ϵ. The results are shown in Figure 5 for different technology and design parameters. The staircase shape of the plot is due to the reverse numerical calculation of the integral borders. I_1/I_{on} increases with R_{M} and β; which can be explained by the fact that the distributions of the noise and useful signal become more centred around their respective mean values, and I_1 can be relaxed (*i.e.*, larger). Among the considered technology parameters, β has the strongest influence on I_1, which is globally weak (less than 4% variation of I_1 for 10 $\times$ increase of β). The optimal value of I_1 is weakly dependent on R_{M} (less than 1% for a decade of variation of R_{M} and weak β). The dependance on R_{M} becomes noticeable when both R_{M} and β are large, which is unlikely to happen because β increases with the nanowire width; while the opposite happens to R_{M}. The dependency of I_1 on M is weaker than on R_{M} and β. Consequently, I_1 has a robust value $\sim 1.2 \times I_{\text{on}}$ that depends only on the technology by less than 4%.

Once I_1 was calculated, we fixed the value of I_0 to I_1/q for a given $q > 1$. We noticed that for $q \lesssim 1.5$, the thresholder error increased, because the thresholder range is too narrow to seperate the defect-induced noise from useful signal. For $q > 1.7$, the thresholder error remains constant. But if q becomes too large, then the intrinsic noise cannot be separated from the useful signal anymore and the thresholder error increases again. Thus, I_0 should be large enough compared to

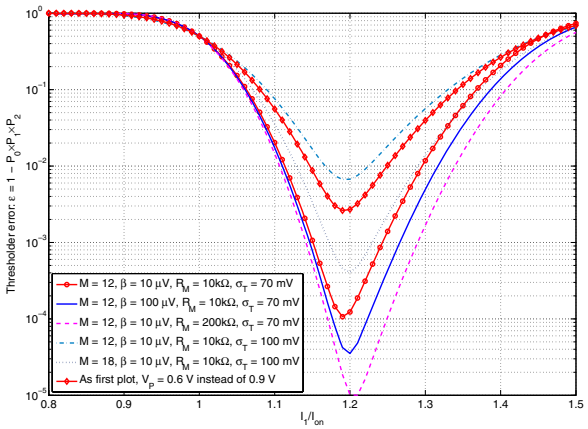

Fig. 6. Thresholder error vs. thresholder parameter I_1

$I_{\rm i}$. For a wide range of reasonable technological assumptions and memory size, q can be set to 1.8, *i.e.*, the optimal value of I_0 is $\sim\ 0.66 \times I_{\rm on}$.

By using these optimized thresholder parameters, we investigated the thresholder error under different conditions, as plotted in Figure 6. As expected, the lowest thresholder error is obtained for $I_1\ \sim\ 1.2 \times I_{\rm on}$. A typical set of technology parameters is $\beta = 10\ \mu{\rm AV}^{-2}$, $R = 10\ {\rm k}\Omega$ and $\sigma_{\rm T} = 70$ mV. For a small array with $M = 12$, the error is $\epsilon\ \sim\ 10^{-4}$. Reducing the power level from 0.9 V down to 0.6 V reduces the current level at the operating point without reducing its variable part. Thus, it increases the noise level in the sensed current, and the error probability increases by a factor of $22\times$. Consequently, the power level should be kept as high as possible under the test conditions. The variability level is the most critical parameter: increasing $\sigma_{\rm T}$ to 100 mV increases the thresholder error by a factor larger than $50\times$. Improving the transistor gain factor β by $10\times$ reduces the thresholder error by a factor of only $3\times$. A $20\times$ higher memory resistance $R_{\rm M}$ reduces the thresholder error by a factor of $10\times$. However, this is not a useful strategy, because the memory should be designed with the lowest possible $R_{\rm M}$, in order to obtain a higher level of the sensed current. In fact, our analytical model and results show that a better strategy is to increase the number of addressing wires M, which is explained in the following.

TABLE I
AREA/QUALITY TRADE-OFF: MEMORY AREA OVERHEAD AND THRESHOLDER ERROR REDUCTION BY ADDING REDUNDANCY ($M = 12$: REFERENCE)

M		12	14	16	18
Area overhead		0%	11.8%	23.6%	35.5%
Reduction of ϵ	$\sigma_{\rm T} = 80$ mV	-	3.9×	14.5×	59.2×
	$\sigma_{\rm T} = 100$ mV	-	2.5×	6.1×	15.2×

The design parameter M plays a major role not only in addressing the array, but also in improving the thresholder robustness. Increasing the number of addressing wires in the decoder (M) without changing the number of addressed nanowires adds redundancy to the decoder circuit, but it guarantees an improvement of the test quality by reducing the thresholder error. We considered the same array of nanowires having different decoder sizes (M); and we estimated the area overhead from [4] and the thresholder error. The results are summarized in Table I. For instance, accepting only $\sim 35\%$ area overhead in the decoder reduces the decoder error by a factor of $\sim\ 60\times$ for $\sigma_T = 80$ mV.

VIII. CONCLUSIONS

The nanowire test in crossbar memories is a necessary operation that enables the identification of correctly addressed nanowires. It detects the decoder-induced pattern sensitivity faults and it simplifies the subsequent conventional functional tests. A current thresholder can carry out this test. The design of the thresholder necessitates an accurate knowledge about the sensed current through the array. In this paper, we have developed a stochastic current model based on a perturbation of the signal around an operating point; then we have expressed the current distribution by means of the design and technology parameters. By minimizing the thresholder error, its parameters could be derived and the simulations showed that they were robust against technology variation. The thresholder error was shown to be dependent of the design and technology; and it was found to be as low as 10^{-4} in the typical case. The supply voltage and the variability level were shown to be fundamental parameters influencing the thresholder error. To improve the thresholder quality, the designer can increase the number of addressing electrodes: for instance, a 35% area overhead in the memory reduces the thresholder error by a factor of $60\times$. The optimized thresholder enables a reliable nanowire testing, which is not meant to replace the conventional test procedures. It should be rather carried out before other tests in order to simplify the pattern sensitivity fault test. This paper explored the mathematical aspects of the problem, and the model was restricted to the nanowire defects. The model can be enhanced in the future by including the defects at the molecular switches, which are expected to be as crucial as the nanowire defects.

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