Fabrication of Highly Ordered Vertical Nanogap Arrays and Networks on a Large Scale

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Metallic nanogap assemblies show great potential in the field of biological or chemical sensing due to their high sensitivity close to the threshold of electrical conduction. Changes in electrical properties of the gaps in presence of the detected species (induced by e.g. adsorbed bio-molecules or absorbed gases) can lead to drastic changes in electrical resistance even at low concentrations [1-3]. For sensor manufacturing on a large scale, a high reproducibility and the use of standard MEMS compatible methods are highly desirable. Existing techniques for lateral nanogap fabrication often suffer from constraints in topological and/or size control when many gaps are to be processed in parallel [1, 2]. In contrast to the lateral definition of nanogaps, vertical approaches promise to give an excellent control of the gap dimensions at a large scale by the use of standard thin film techniques. A particularly simple method makes use of the shadowing effect which occurs during evaporation on a silicon–on-insulator (SOI) stack where the top silicon layer is partially underetched by hydrofluoric acid [4].

In this project we extend this idea in a more flexible way, aiming at the realization of highly ordered metallic nanogap networks for sensing applications. The key features are arbitrary arrangements of one-dimensional nanogaps in networks on a wafer scale by solely using standard fabrication techniques. The schematic representation in figure 1 shows the working principle of such a device. Depending on the electronic state of each of the nanogaps, an electrical current will percolate through the network once a sufficiently large number of gaps are electronically active.

The primary patterns are defined by circular openings with different numbers of next neighbors. Adjacent openings can be connected by metallic stripes which include the nanogaps at each step of the circular openings. The process flow is schematically shown in figure 2. After thermal oxidation of a p-type silicon wafer, a 50 nm thick poly silicon layer is deposited by chemical vapor deposition. The poly silicon is patterned by photolithography and plasma etching using SF6 as an etching gas. The silicon oxide is isotropically etched in buffered hydrofluoric acid which produces an undercut of the poly-Si layer. Two metal layers are subsequently deposited on top of each other by evaporation followed by lift-off. Hereby, the first layer serves as a spacer to bridge a part of the distance from the silicon surface to the poly-Si layer. The second layer is the functional layer which eventually defines the opposing surfaces of the nanogaps. This two-layer approach allows keeping a constant thickness of the functional layer while controlling the size of the nanogap either by the oxide spacer or the first metal layer. The SEM image in figure 1 shows a typical square lattice whereof a single nanogap is shown in figure 3. Contact pads and electrodes with various distances are deposited by evaporation of Cr/Au through a full wafer stencil mask in order to avoid any thermal influence on the functional metal layer after deposition (see figure 4).

Due to the good control and extremely homogenous thickness of the oxide spacer, many nanogaps can be reproducibly fabricated on a full wafer.

Further work will focus on the detailed electrical characterization and use of palladium based nanogap networks as hydrogen sensors.

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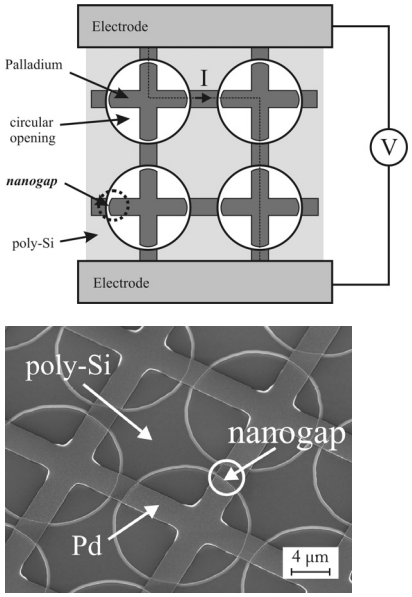

Figure 1. Schematic representation and SEM image of an ordered metallic nanogap network using a silicon oxide supported poly-Si layer with circular openings. Electric current might flow depending on the electronic state of each single nanogap.

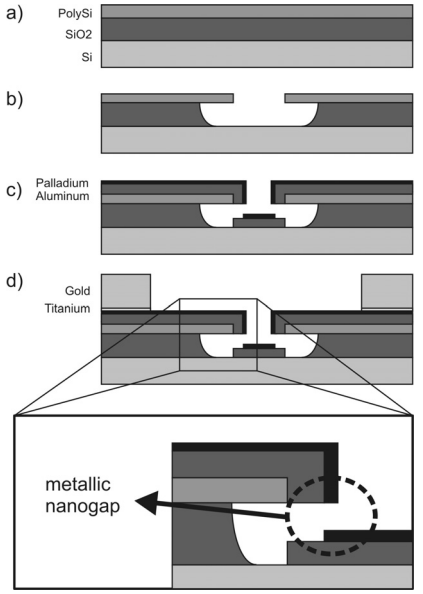

Figure 2. Process flow for nanogap network fabrication: a) thin film deposition b) BHF underetching c) Deposition of Al spacer and functional Pd layer d) Stencil deposition of Ti/Au electrodes.

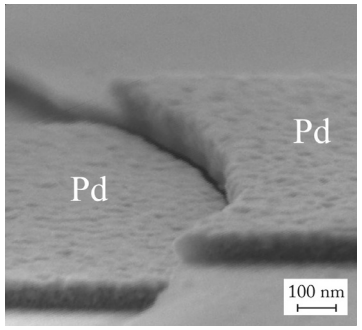

Figure 3. Close-up SEM image of a palladium nanogap.

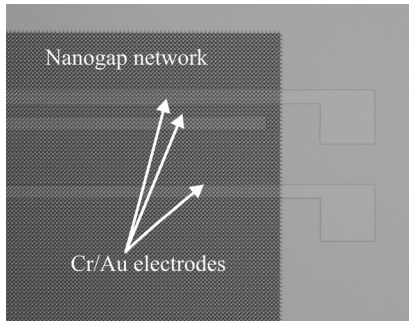

Figure 4. Final device with electrical contacts deposited by full wafer stencil lithography.