

Programmable Logic Circuits Based on Ambipolar CNFET

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ABSTRACT

Recently, it was demonstrated that the polarity of carbon nanotube field effect transistors can be electrically controlled. In this paper we show how *Programmable Logic Arrays (PLA)* can be built out of these devices, and we illustrate how they outperform usual PLA by internal signal inversion. The simulations show an area saving up to $\sim 21\%$ and decrease of the delay in PLA-based FPGA by 50%. We also show that this architecture is suitable for high-performance design tools and defect-tolerance approaches.

Categories and Subject Descriptors

B.6.1 [Logic Design]: Design Styles—*logic arrays*; B.7.1 [Integrated Circuits]: Types and Design Style—*gate arrays*

General Terms

Design, Performance

Keywords

Carbon Nanotube, CNFET, PLA, FPGA

1. INTRODUCTION

Carbon Nanotubes (CNT) are expected to be the most promising replacement for Silicon channels because of their size and electrical properties. This still immature technology is suitable for regular architectures because of the lack of controllability. It has been shown that the polarity of *CNT field effect transistors (CNFET)* can be electrically controlled [3]. These devices are called *ambipolar CNFET* and their n- or p-type behavior is controlled by an additional gate. In [4] a reconfigurable two-input logic gate based on these devices was presented. However, this approach used only two states of the device (n or p) without exploring the third (off) state. Our approach explores all three states and enables a fully regular and programmable architecture. The proposed PLA architecture is more powerful than the standard one. It has one single column per input and the polarity is generated internally; thus reducing the circuit area. The polarity of the product-terms of the implemented function can be also chosen, making this architecture suitable for the implementation of *Whirlpool PLA (WPLA)* [1], which realizes logic functions in a more compact way.

In this paper we propose the basic ambipolar CNFET cell and explain how it can implement a *generalized NOR (GNOR)* function (Section 2-3). In Section 4, we illustrate the implementation of PLA and reconfigurable interconnect within this technology. Then,

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we investigate in Section 5 the impact of the presented architecture on the area of logic circuits and the performance of *Field Programmable Gate Arrays (FPGA)*; and we present some high performance design tools which are suitable to the presented architecture.

2. AMBIPOLAR CNFET TECHNOLOGY

Ambipolar CNFET were introduced for the first time in [3], and they had one top- and one back-gate. It is possible to use two top-gates by applying the self-alignment technique [2], which results in the device depicted in Fig. 1.a with the layout shown in Fig. 1.b. The control gate CG in region A turns the device on or off, while the polarity gate PG in region B controls the type of polarity: a high (V_+) or low (V_-) PG voltage yields respectively an n- or p-type behavior, by thinning the Schottky barrier for either electrons or holes respectively. Between these two values of PG, there is a voltage $V_0 = V_{DD}/2$ (if V_{DD} is applied on the device) for which the conduction is poor and the device is always off [3]. The ambipolar CNFET symbol is shown in Fig. 1.c.

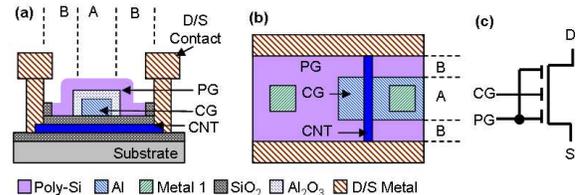


Figure 1: Ambipolar CNFET: device (a), layout (b), symbol (c)

3. AMBIPOLAR CNFET LOGIC GATES

Ambipolar CNFET can be arranged into *generalized NOR gates (GNOR)* which are more powerful and make up more compact PLA. In a GNOR cell every input has a polarity control signal. A 2-input function is given by $NOR(C_1 \odot A, C_2 \odot B)$, \odot representing EXOR. C_i is set to 0 (V_+) or 1 (V_-) to control the polarity of input i . If it is set to V_0 then the input is dropped from the function. A configured dynamic logic four-input GNOR gate is presented in Fig 2. Unlike inputs A and D, B is inverted by setting C_1, C_2 and C_4 to V_+, V_- and V_+ respectively. Input C is inhibited by setting C_3 to V_0 . As in usual dynamic logic, the transistors T_{PC} and T_{EV} are used to pre-charge and evaluate the output. They have opposite polarities: during the pre-charge phase, T_{PC} is conducting and T_{EV} is high resistive, so that Y is set high. During the evaluation phase, T_{EV} is conducting and T_{PC} is high resistive. Then, Y is set low if any one of the signals A, \bar{B} or D is high. Consequently, the configured GNOR gate in 2 performs the function $NOR(A, \bar{B}, D)$.

4. PLA ARCHITECTURE

The GNOR gate can be integrated into an array-based architecture, which is reminiscent of the regular PLA (Fig. 3 and 4). This architecture consists of a cascade of two planes, each implementing GNOR (Fig. 4). In order to avoid the use of an additional wire per CNFET for every PG signal, a charge corresponding to the voltage of the wished polarity is saved on every PG. A global signal V_{PG} connects all the polarity gates. Any transistor in position (i, j) whose polarity is to be set is selected by using the row and column

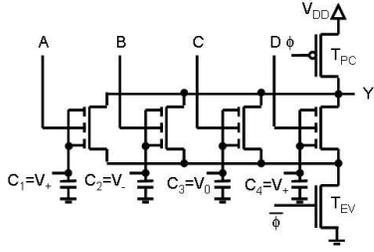


Figure 2: GNOR gate configured as $Y = \text{NOR}(A, \bar{B}, D)$

select signal $V_{\text{SelR},i}$ and $V_{\text{SelC},j}$. During the configuration phase of the PLA, every ambipolar CNFET is selected individually and the charge corresponding to its PG voltage is set. This insures an individual programming of every device.

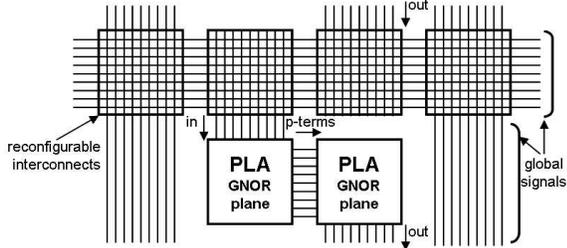


Figure 3: PLA architecture with GNOR planes

A compact interconnect array can be realized by using ambipolar CNFET: every crosspoint connects a horizontal and a vertical wire through a CNFET working as a pass transistor. All CG voltages are set at the same high level. If the PG of the CNFET is set to V_+ , then the polarity of the CNFET is n. The high level of CG makes the device conducting; then the wires are connected. If the PG of the CNFET is set to V_0 , then the device is switched off and the wires are disconnected. Interleaving PLA and interconnects (Fig. 3) enables cascades of NOR planes and realizes any logic function.

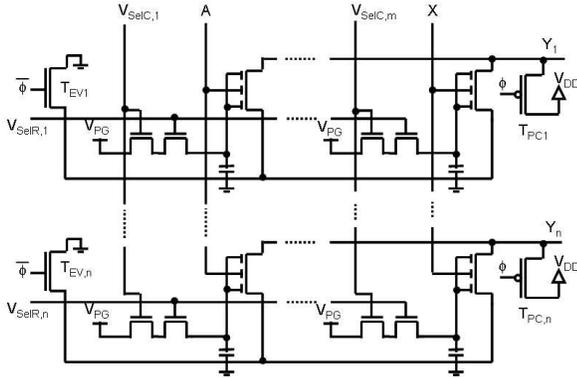


Figure 4: PLA plane with ambipolar CNFET

5. PERFORMANCE ASSESSMENT

Classical PLA planes need both polarities of input signals, whereas the use of GNOR gates prevents the replication of input columns. This powerful feature potentially reduces the size of the PLA even if the size of the basic cell is large. This area was estimated from the scaling rules suggested in [5] for CNFET. The area of Flash and EEPROM basic cells were derived from the International Technology Roadmap for Semiconductors. The area of the contacted cells with respect to the lithography resolution (L) is estimated in the first row of Table 1.

The area of the PLA implementing three functions from the MCNC suite [8] is shown in Table 1. The CNFET basic cell is 50% larger than the Flash and 40% smaller than the EEPROM basic cell. Thus, the CNFET PLA is always more compact than EEPROM PLA (up

to 68% less area). Because Flash basic cells are smaller than ambipolar CNFET cells, the CNFET implementation can only save area compared to Flash if the PLA has a large number of inputs (e.g. in max46: saving $\sim 21\%$), by taking advantage of its fewer inputs; otherwise a small area overhead (3%) can be seen.

	Flash	EEPROM	CNFET
Basic cell (L^2)	40	100	60
max46 (L^2)	34960	87400	27600
apla (L^2)	32000	80000	33000
t2 (L^2)	104000	260000	102960

Table 1: Area of logic functions in 3 technologies

For PLA-based FPGA, this reduction in area is highly desirable because it facilitates the routing of signals between the *Configurable Logic Blocs (CLB)*. Moreover the number of signals to route is reduced by almost the factor 2, because the inverted signals are not routed but generated internally. These factors boost the performance of the routing tool. Consequently, the delay, which highly depends on signal routing in FPGA, can be drastically reduced, thus increasing the frequency as shown in Table 2. To emulate the ambipolar CNFET FPGA we used a classical one with half of the area for every CLB. Both FPGA implement the same function and the standard one is full. It is noteworthy that FPGAs implement any function within a limited number of inputs, while our PLAs are minimized for any given function. We therefore expect the function implemented in a PLA-based FPGA to be split into blocks the same way standard FPGAs split large functions into different CLBs.

	Standard FPGA	CNFET FPGA
Occupied area	99%	44.9%
Frequency	154 MHz	349 MHz

Table 2: Frequency of standard FPGA and CNFET FPGA

The second advantage in using GNOR gates is the availability of the product-terms (output of first plane) with both polarities, thus allowing for a further degree of freedom in minimizing the PLA. A logic minimizer was presented in [7] and implemented in the heuristic MINI II, showing a significant area saving after logic minimization. The cascade of 4 NOR plane instead of 2 makes the implementation of WPLAs [1] with the presented architecture possible. WPLAs outperform other PLA types and a more compact implementation can be obtained by using the logic minimizer called Doppio-Espresso [1]. Finally, a fault-tolerant design approach for PLAs [6] makes use of the regular architecture and is expected to improve the yield of the unreliable devices making up the PLA.

6. CONCLUSIONS

In this work, we studied the implementation of reconfigurable logic gates based on ambipolar CNFET, yielding PLA that are more powerful than classical PLA because of an internal signal inversion. The smaller area and the lower number of wires were shown to improve the frequency in PLA-based FPGA by $\sim 2\times$. In PLA with large number of inputs, the overall size is smaller with ambipolar CNFET than with Flash and EEPROM. Thanks to the internal inversion of signals, high-performance logic minimizers and fault-tolerance approaches can be applied on the proposed PLA.

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