21.8 A 128×2 CMOS Single-Photon Streak Camera with Timing-Preserving Latchless Pipeline Readout

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Emerging imaging techniques in physics, molecular biology, and medical science are placing growing pressure on optical sensor technology. In particular, time-resolved imaging and other high-precision solutions are demanding picosecond timing accuracies and high sensitivities [1]. Recently, the introduction of monolithic CMOS single-photon avalanche diodes (SPADs) has enabled this level of performance at a fraction of the cost [2]. This trend has accelerated with the emergence of increasingly larger arrays of SPADs. In [3] a hybrid approach was adopted; by means of an *ad hoc* 3D technology, silicon SPAD arrays are connected to banks of counters implemented in CMOS. In [4] a monolithic CMOS SPAD array was proposed with random-access, pixel readout. This approach, though simple and highly timing-accurate, is limited in that only one pixel can be accessed at any time. Lately, an event-driven readout mechanism was proposed. In this approach, a pixel uses the column as a bus to transmit photon detection timing and pixel-specific ID. The bandwidth of the bus limits however, limits the saturation performance of this method [5].

In this paper we present a new method to simultaneously detect all the photons impinging upon a column while preserving their arrival times with timing accuracies comparable to random-access readout. In this approach, depicted in Fig. 21.8.1, pulses fired by individual SPADs are injected into a latchless timing-preserving delay line. To avoid time-domain aliasing, every SPAD has a gating mechanism that enables firing in a programmable time window – in our design 20 to 30ns. At the bottom of the line, the time of arrival (TOA) of each detected photon is determined in reverse order accounting for possible pixel non-firing. A pulse in position j exits the line at time $t = j\,\tau_D$ with an added term $\tau_{SPAD} + \tau_{INJ} + \mathrm{TOA(j)}$, where τ_D is the stage delay, τ_{SPAD} and τ_{INJ} are the delay of the detector and of the injection circuit, respectively. An external time discriminator is used to process TOA(j) with latency $L = N\tau_D$, where N is the number of stages. Assuming that the delays τ_D are independent identically-distributed random variables, and that jitter is not amplified by subsequent stages, the measurement uncertainty at position j becomes $\sigma^2[TOA(j)] = (N - j - 1)\,\sigma^2(\tau_D) + \sigma^2(\tau_{SPAD}) + \sigma^2(\tau_{INJ})$ with $j = [0, N\text{-}1]$. Based on performance and architectural complexity considerations, we used 16 delay lines of 8 stages each to achieve a worst-case jitter of 145ps and latency smaller than 225ns for a throughput of 40MSample/s.

The pixel implemented in this design comprises a SPAD and circuitry for pulse forming and injection. A SPAD is a pn junction biased *above* breakdown, so as to exhibit virtually infinite optical gain. In this condition, the diode operates in so-called Geiger mode. The cross-section of the junction used in this design is shown in Fig. 21.8.2; details on the physical design and optimization of the device are found in [4] and [5]. When a photon is absorbed in the multiplication region, an avalanche may be triggered by impact ionization, with a probability known as the *photon detection probability* (PDP). In this design, the avalanche is quenched passively through the non-linear resistance of transistor T_Q. The recharge time of the diode's parasitic capacitance through T_Q dominates the detection cycle time, known as *dead time*, τ_{DT}. The avalanche current is sensed and converted into a digital voltage pulse by an inverter. The L to H transition at the inverter's output pulls down node "X" through transistor T_{PD} and resistor R_{PU}, provided that gating transistor T_G is enabled by signal "GATE". The anode of the diode is intentionally set to a negative voltage V_{OP} satisfying the equation $|V_{OP}| + V_{DD} = |V_{bd}| + V_e$, where V_{bd}, V_e, and V_{DD} are the breakdown, excess bias and power supply voltage, respectively. Thermal and tunneling generation effects produce pulses even in the dark. These pulses define the *dark count rate* (DCR). Afterpulse probability was contained below 20% by sizing T_Q for a dead time of 40ns and by choosing a gating window that satisfies the inequality $\tau_G < \tau_D < \tau_{DT}$.

The pixel schematic in the latchless pipeline for time-correlated operation is depicted in Fig. 21.8.3. When there is no activity on the preceding delay line, signal "VIN_j" is at logic level L, hence the gate of source-degenerated transistor T_{PP} is L, thus the impedance at node X is dominated by the impedance at the drain of T_{PP}. In our design such impedance has been calculated to be 10kΩ and it has the function of the pull-up resistance R_{PU} of Fig. 21.8.2. When a photon is detected, a pulse is originated at this point and propagates towards the remainder of the delay line. When there is activity on the delay line, a logic transition L to H on VIN_j occurs, thus causing X to become a low impedance node. During this time any photon detected in this stage will have no effect on traveling pulses, but it will inject spurious pulses onto the line when it is at logic level L, hence the need for gated SPAD operation. To avoid ghost pulses, an appropriately sized NMOS was added to the cathode of the diode. A simplified timing diagram to operate the 8-stage delay line is shown in the inset of Fig. 21.8.3. Controls DSEL and TUNE are used for coarse- and fine-tuning of the delay line, respectively. The goal is to compensate for technological variations and temperature in a calibration loop.

The sensor is also equipped with simultaneous intensity detection based on time-uncorrelated photon counting. To implement a pitch of 25μm, a single bit counter has been added in each pixel. The counter comprises a flip-flop and a shadow latch used to read out the bit sequentially while in counting mode. Figure 21.8.4 shows a detail of the time-uncorrelated photon counting mechanism. Again, the output at the bottom of the column is in reverse order, however, in this case N = 128 was chosen for simplicity since the timing jitter of the output shift register is not critical to intensity measurement.

A micrograph of the streak camera is shown in Fig. 21.8.5. The chip was fabricated in 0.35μm CMOS technology with a total area of 4.1×1.1mm². The sensor is controlled by a logic circuit implemented in a Xilinx Spartan™ FPGA, while the time discrimination function is performed by a 6GHz LeCroy WaveMaster™ 8600A oscilloscope. To identify all the sources of time uncertainty, the timing jitter of a pipeline stage, SPAD, and injection circuit were measured separately, yielding averages of 44.5ps, 64ps, and 60.4ps, respectively. In Fig. 21.8.6 a plot is shown of the overall time uncertainty and DCR as a function of the pixel position in the array and operating biases. Coarse and fine tuning used to adjust the delay line were left unchanged for up to 10 hours of operation and the jitter was measured at regular intervals over several days. The inset of Fig. 21.8.6 shows a plot of timing uncertainty variation over time; the measured variations were within ±4ps with a temperature variation of less than ±5°C. An external feedback loop may be utilized to compensate the absolute delay for temperature and technology variations. The table of Fig. 21.8.7 lists all tested parameters relevant to the pixel detector and the overall test results for the streak camera.

Acknowledgements:
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[2] A. Rochas, "Single Photon Avalanche Diodes in CMOS technology," Ph.D. Thesis, EPFL, 2003.
[3] B. Aull et al., "Laser Radar Imager based on 3D Integration of Geiger-Mode Avalanche Photodiodes with Two SOI Timing Circuit Layers," *ISSCC Dig. Tech. Papers*, pp. 238-239, 2006.
[4] C. Niclass and E. Charbon, "A Single Photon Detector Array with 64x64 Resolution and Millimetric Depth Accuracy for 3D Imaging," *ISSCC Dig. Tech. Papers*, pp. 364-365, 2005.
[5] C. Niclass, M. Sergio, E. Charbon, "A Single Photon Avalanche Diode Array Fabricated on Deep-Submicron CMOS Technology," *Proc. Design Automation and Test in Europe*, 2006.

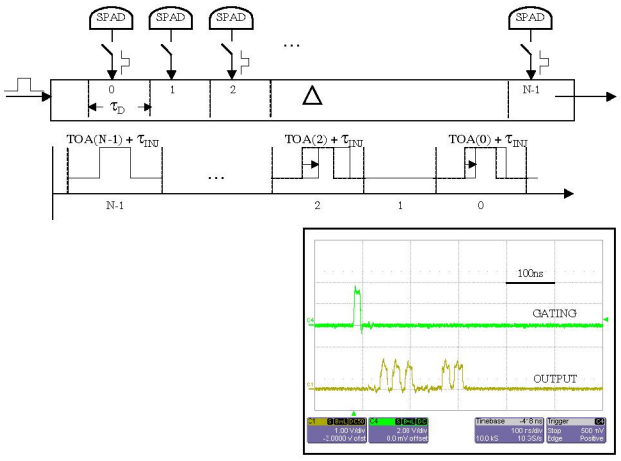

Figure 21.8.1: Readout mechanism: when photons are detected, every pixel may inject a pulse into delay line Δ. The time of arrival (TOA) of each detected photon is pipelined outside the array in reverse order starting with the (N-1)th. The absence of a pulse indicates that the corresponding SPAD did not fire. An example of the measured output is shown in the inset with respect to the gating signal.

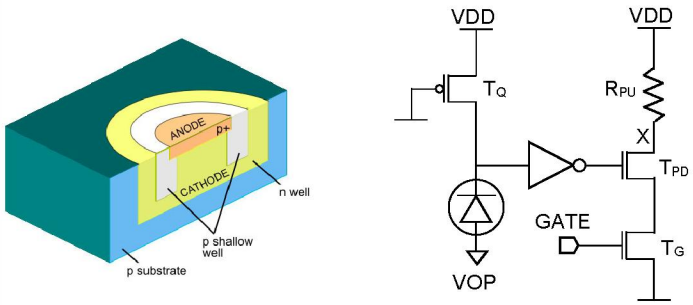

Figure 21.8.2: Cross-section of the SPAD pn junction and schematic of the quenching circuitry. The output of the inverter drives a gated pull-down circuit (transistors T_{PD}, T_G), where resistance R_{PU} acts as the pull-up.

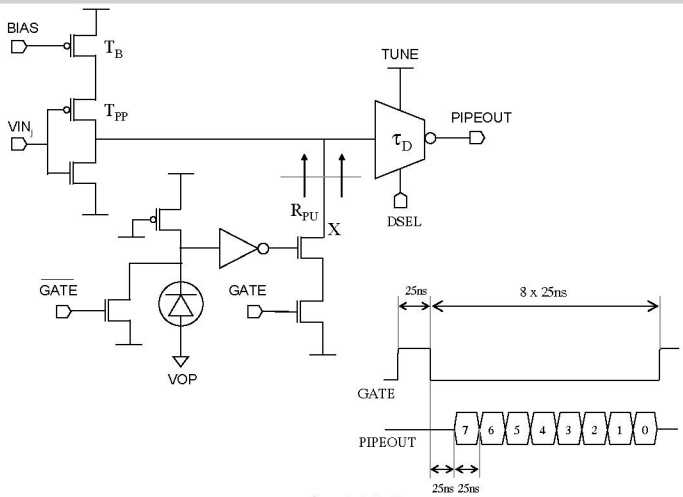

Figure 21.8.3: Simplified schematic of a pixel in the latchless pipeline for time-correlated operation. The signal BIAS controls the propagation delay from the previous pixel in the column. GATE activates the SPAD and the pull-down NMOS. DSEL and TUNE are the coarse and fine delay controls.

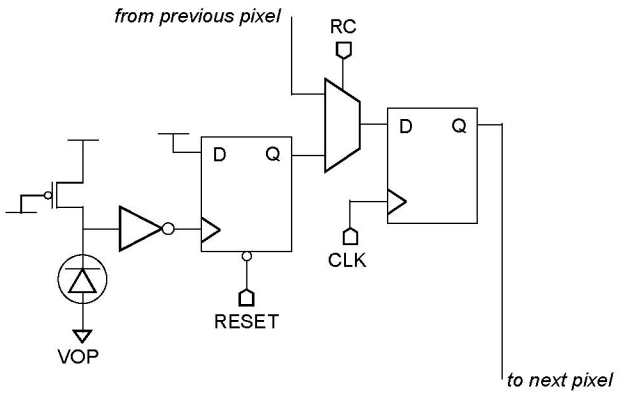

Figure 21.8.4: Detail of uncorrelated single photon counting mechanism. Global signal RESET is used to reset all the single-bit counters of the imager. RC forces the system to operate in counting or readout mode. During readout mode the shadow latches are chained into a 128b shift register. The data are reorganized externally in an FPGA.

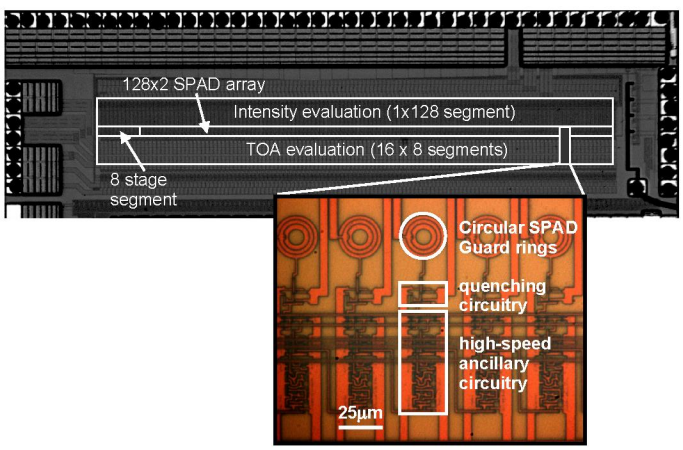

Figure 21.8.5: Micrograph of the streak camera. The inset shows a detail of a pixel. The circuit, fabricated in 0.35μm CMOS technology, has a surface of 4.1×1.1mm^2.

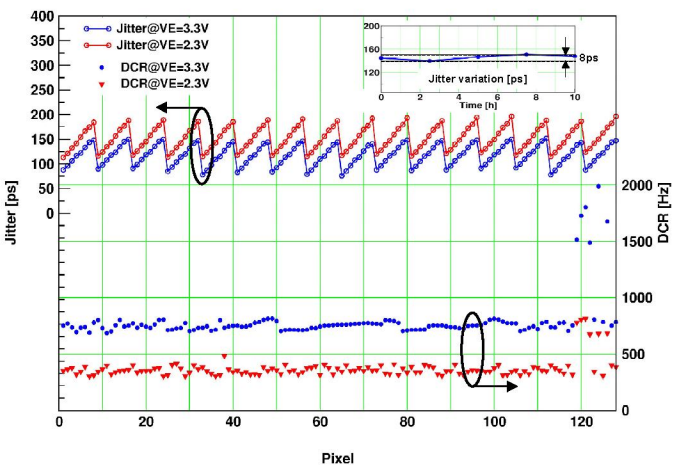

Figure 21.8.6: Absolute time uncertainty and DCR over the whole array as a function of excess bias and supply voltage at room temperature. The inset shows jitter variability over time.

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	Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Pixel	Photon detection probability	PDP			40 35	%	V_e=3.3V, λ=460nm V_e=4.0V, λ=460nm
	Sensitivity spectrum	λ	350		800	nm	
	Mean dark count rate	DCR		750		Hz	
	Fill factor	-		8.8		%	
	Jitter variation w.r.t. excess bias voltage	$\Delta\sigma(\tau_D)/\Delta V_e$			30	ps/V	V_e = 2.3V – 3.3V
Pipeline	Tuning range	τ_D	20		30	ns	
	Pipeline stage jitter	$\sigma(\tau_D)$		44.5		ps	
	jitter variation due to technological mismatch	$\Delta\sigma(\tau_D)$			5	ps	
	Jitter variation w.r.t. power supply	$\Delta\sigma(\tau_D)/\Delta$VDD			12.5	ps/V	VDD = 3.0V – 3.8V
TCSPC	Overall time uncertainty	-	88		145	ps	
	Repetition rate	-		40		MHz	
	Range	R	20		30	ns	
	Readout line length	-		8		pixels	
	Power dissipation	P_{tot}			1	mW	
Photon Counting	Integration time	-	25		10^6	ns	
	Counter resolution	-	1			bit	
	Shadow latch		1			bit	
	Readout line length	-		128		pixels	
	Counter readout clock	-	80			MHz	

Figure 21.8.7: Performance summary for the system and its components. All measurements were conducted at room temperature.

