A Single-Photon Avalanche Diode Imager for Fluorescence Lifetime Applications*

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Abstract

A 64-by-64-pixel CMOS single-photon avalanche diode (SPAD) imager for time-resolved fluorescence detection features actively quenched and reset pixels, allowing gated detection to eliminate pile-up nonlinearities common to most time-correlated single-photon counting (TCSPC) approaches. Timing information is collected using an on-chip time-to-digital converter (TDC) based on a counter and a supply-regulated delay-locked loop (DLL).

Introduction

Flourescence lifetime imaging (FLIM) has emerged as an important technique in biology[1]. In a typical time-domain measurement, fluorescent dyes are stimulated with a fast-pulsed laser and the lifetime of their emission is measured. For example, fluorescent lifetimes are sensitive to excited-state reactions such as fluorescent resonance energy transfer (FRET) which allow one to detect macromolecular associations labeled by two different fluorophores.

In most commercial systems, TCSPC is performed with laser scanning and photomultiplier-tube (PMT) detection[2], providing limited imaging frame rate. The development of arrays of SPADs in standard CMOS technologies[3] allows for TCSPC to be performed in the context of conventional wide-field microscopy with sensitivity and time resolution comparable to PMT detection. In both SPAD arrays and PMTs, timing resolution is limited by jitter (and uncalibrated TDC nonlinearities) and sensitivity by dark count rate (DCR).

This paper describes a SPAD imager specifically designed for FLIM applications and consists of an array of 64-by-64 actively quenched and reset SPAD pixels and an on-chip time-to-digital converter (TDC). A measured timing resolution of 350 ps is achieved, while timing resolutions as low as 87 ps should be possible in the current design. The dark count rate at room temperature is typically 1059 Hz with a maximum photon detection probability (PDP) of 4.7% at 440 nm. A gated-window mode allows for the elimination of pile-up nonlinearities[4] traditionally associated with TCSPC techniques.

Imager design and function

The camera, as shown schematically in Fig. 1, is implemented on a 16-mm^2 die in a high-voltage AMS 0.35-μm CMOS process. Each pixel consists of a reverse-biased p+/nwell junction SPAD with 13.5 μm^2 detection area and circuitry for active quenching and reset. The pixel is biased by setting *Vhigh* to the nominal supply voltage (V_{DD}=3.3 V) and *Vop* to a large negative voltage, typically –20.7 V. If the *EnAct* signal is low, the pixel behaves as a passively-quenched SPAD, with the resistance of its quenching load set by *Vbr*. In normal use, however, *EnAct* is held high, enabling the feedback path. When the pixel avalanches, driving its cathode low, the nFET M9 turns on and holds the cathode at ground. The pixel remains inactive until *Reset* is pulsed, at which time the cathode is pulled up quickly by pFET M8. The PDP (as determined by the bias voltage) can be varied by changing *Vhigh* and *Vop*.

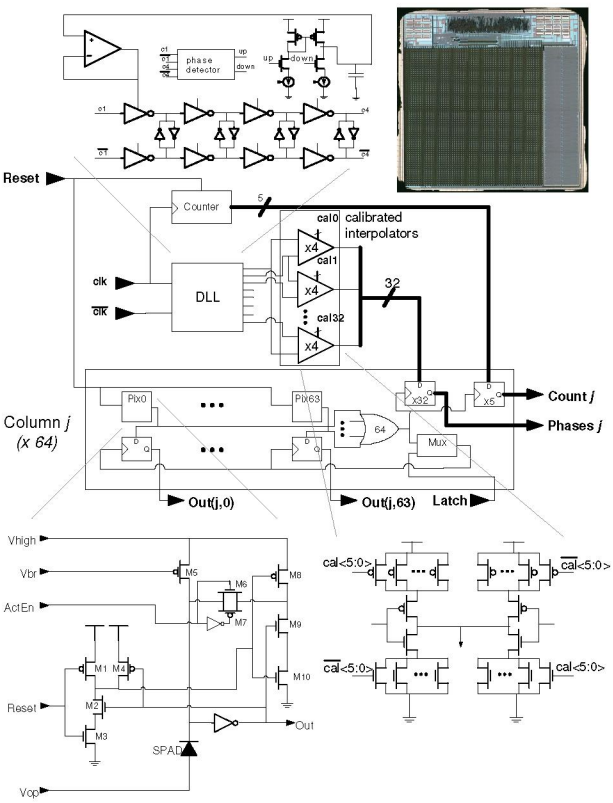

Figure 1. Die photo and circuit diagram with details of circuits of pixel, DLL, and calibrated interpolators

The TDC includes a five-bit counter (coarse timing) and a multiphase clock generator (fine timing). The multiphase clock generator consists of a supply-regulated DLL[5] (for good power-supply-noise immunity) and interpolators, generating 32 output phases. The four delay elements of the differential voltage-controlled delay line consist of supply-regulated inverters with outputs connected through a weak cross-coupled pair. The DLL also includes a digitally-calibrated charge pump, the output of which controls the supply voltages of the inverter chain through a linear regulator.

Each consecutive pair of the eight phases at the output of the DLL is sent to four identical calibrated interpolators (six-bit binary-weighted calibration), which run on the regulated supply. These allow for correcting any offsets in the charge pump and regulator and for duty-cycle correction. For a clock period T_c, this provides a timing resolution of (1/32)T_c (87 ps for T_c = 2.78 ns). In the measurements presented here, only one output from each delay element is used, providing an eight-phase clock and a timing resolution of 350 ps.

Measurement modes. The imager can measure fluorescence lifetimes in two modes, by the standard time-correlated single photon counting (TCSPC) method and with gated

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timing windows (GW). For TCSPC, a signal synchronized to the clock triggers a pulsed laser and resets the coarse five-bit counter and the pixels. When the first photon hits any pixel in one of the 64 columns, the states of the counter and the multiphase clock generator as well as the output states of all of the 64 pixels in that column are latched. The timing information and the one-hot pixel outputs are shifted off of the chip through a 64-bit bus, one bit per column. The lifetime, τ, can be computed as the negative slope of the logarithm of the probability histogram of the latched times. Because at most one hit can be detected per pixel per laser pulse, the detection of a photon at time t_i implies that no photon could have been received for this pulse prior to t_i; the result of this is a nonlinear weighting of the distribution favoring the high-intensity portion of the histogram (pile-up).[1] In conventional systems, pile-up is usually averted by using low light levels, typically such that not more than 1% of pulses yields a hit[4]. If pile-up is avoided in this way, fewer than one hit per column per laser pulse are expected. Therefore the imager only needs to accept one hit per column per pulse. This reduces the area of the design and the quantity of data produced per measurement.

The design also allows alternative methods of avoiding pile-up. Because the pixel is actively reset, we can simply delay the reset relative to the laser trigger to avoid the higher light levels at the beginning of the decay. In GW mode, a time window $[t_i, t_j]$ is defined by resetting the pixel at time t_i and latching the pixel outputs at time t_j. As long as $P(n_{ij}>1|n_{ij}>0)<<1$ where $n_{ij} = N_{ij} \cdot p$ with N_{ij} the number of photons that hit a pixel in $[t_i, t_j]$ and p the probability that the pixel converts a photon to a hit, then if $t_k - t_j = t_j - t_i$, fluorescent lifetime can be computed as[6]

$$\tau = (t_k - t_j) / \ln[P(n_{jk} > 0) - P(n_{ij} > 0)] \quad . \quad (1)$$

The great advantage of GW mode is that lifetimes can theoretically be measured for any light level as long as the window sizes are kept small enough.

Measurements

The timing and pixel characteristics of the camera are listed in Table I. The DCR is the frequency of "false" hits, the rate at which a pixel gives an output when it is not illuminated. The PDP was measured using a standard measurement setup including a monochromator, integrating sphere, and calibrated photodiode. Its maximum occurs at 440 nm.

Flourescence lifetime measurements. TCSPC measurements of the lifetimes of fluorescent quantum dots (Qdot-655, Molecular Probes) have been performed. The 360-MHz clock source is synchronized with an SRS DG535 delay generator, which triggers a gain-switched 406-nm PiLas picosecond diode laser and the imager's *Reset* signal. The data is read from the chip by an FPGA and stored in SRAM .

The imager is attached to the standard c-mount camera port of an Olympus BX51W1 microscope. Fig. 2(a) shows an image of a spot of Qdot-labelled streptavidin, immobilized on an epoxy-derivitized glass slide. Qdot density is approximately 3 x 10^{13} cm^{-2}. This image can be compared to that obtained with a Hamamatsu ORCA-ER cooled CCD camera (Fig. 2b). In these images, the quantum dots cover the lower three-quarters of the field of view. Fig. 3 shows the plots of the logarithms of the time histograms of Qdots measured with four proximate pixels. The lifetimes, given as the negative slope of this line, differ by at most 2.6%.

Table I. Characterization of imager timing and pixel.

	Timing				Pixel	
	LSB	Jitter	DNL	INL	Avg DCR	Max PDP
Value	350	< 1	1.1	1.3	1059	4.7
Units	ps	LSB	LSB	LSB	Hz	%

[1] Even if the system allows for multiple counts per laser pulse, the dead time of the detector will also cause pile-up.

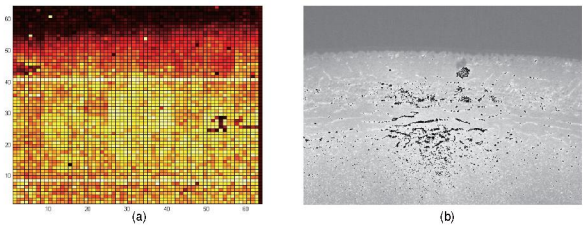

Figure 2. Microscope image of quantum dots using (a) this imager and (b) a Hamamatsu CCD camera

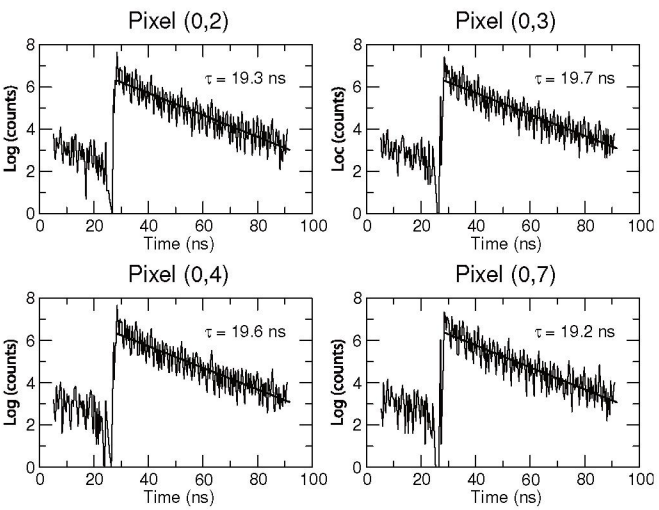

Figure 3. Simultaneous lifetime measurements of Qdots on 4 pixels

Photon detection probability. The pixel PDP is somewhat less than expected. This is because transmission-gate transistor M6 in the pixel cell clamps the cathode at –800 mV. As the cathode only resets to around 2 V, this restricts the reverse bias. This problem could easily be remedied by removing this transmission gate from the design.

Conclusions

A 4096-pixel SPAD camera for fluorescence detection has been developed. The pixels can be independently reset and latched allowing both TCSPC and gated-window-mode measurements. The imager has been demonstrated to work at 350-ps resolution, significantly shorter than the lifetime of the quantum dots measured.

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