# Breaking the Power-Delay Tradeoff: Design of Low-Power High-Speed MOS Current-Mode Logic Circuits Operating with Reduced Supply Voltage

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***Abstract*— In this paper, we study the operation of MOS current-mode logic (MCML) gates at lower-than-nominal supply voltages. We show that power can be traded for speed by reducing the supply voltage below the nominal value, while the power-delay product stays nearly constant. We propose a negative bias strategy that enables the gates to operate at maximum speed with a reduced supply voltage, thus achieving a power saving of up to 35% at no cost for speed. Comparison with CMOS logic style are presented for three different technology nodes (0.25$\mu$m, 0.18$\mu$m and 0.13$\mu$m CMOS).**

## I. Introduction

MOS Current-Mode Logic has been introduced in [1] as a design alternative to conventional CMOS logic style. Thanks to its differential nature, MCML offers considerable potential for improving the signal integrity in digital logic circuits [2]. Other advantages of MCML logic style include a reduced power consumption at very high-speed [1] and improved security in cryptography applications [3]. Moreover, MCML has proven to scale well with technology generations [4].

In this paper, we analyze MCML operation under the conditions of reduced supply voltage. Reducing the supply voltage has proven to be an effective way to reduce the power consumption in logic circuits. However, with conventional CMOS logic, the reduction in the power consumption comes at the expense of the speed performance, so that CMOS circuits are typically run at the maximum power supply voltage in order to achieve the highest speed (Fig. 1). In fact, the operation of CMOS logic is tightly related to the supply voltage, which has an impact not only on the speed and power, but also on the noise performance.

In the following sections, we show that this is not the case with MCML, where the output swing, propagation delay and hence, the performance, are mostly independant of the supply voltage. After reviewing MCML operation in section II, we analyze the effect of voltage scaling on MCML operation and performance in section III. Next, in section IV, we propose a bias strategy which allows to enhance the power-delay tradeoff by keeping the gate operating nearly at maximum speed with a reduced supply voltage. Concluding remarks follow in section V.

## II. MOS Current-Mode Logic Operation

An MCML inverter is depicted on Figure 2. It consists of one NMOS transistor, biased in the saturation region, which provides the gate with a constant tail current, one NMOS differential pair which drives the tail current to either branch according to the differential voltage at its input, and two PMOS transistors, biased in the linear region, acting as resistors to create a voltage difference at the output.

It is not our purpose here to analyse the design of MCML gates, which has been studied in details in many prior works [5], [6], but in order to point out the influence of supply voltage on MCML operation, let us briefly review the main points.

Let us assume that the voltage $V_N$ is provided such that the tail current is equal to $I_{REF}$. The output voltage swing will be given by $V_{SWING} = (R_{PMOS} \cdot I_{REF})$, where $R_{PMOS}$ is the equivalent on-resistance of the PMOS load devices, and is approximately given by [5]

$$R_{PMOS} = \left[ \mu_{eff,p} C_{OX} \frac{W_P}{L_P} \left( V_{DD} - V_P - |(V_{T,p}|) \right) \right]^{-1} \quad (1)$$

This dictates the size of the PMOS devices. NMOS differential pair size is related to the small-signal voltage gain $A_V$ and, more importantly, the noise margins $NM$ in the transfer characteristics [5]

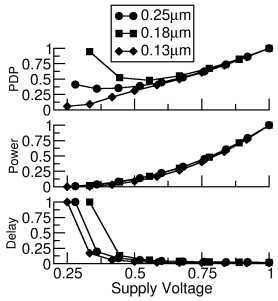
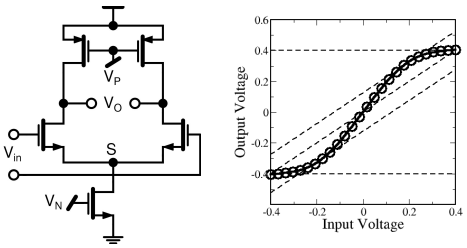



Fig. 1. Trends in the power, delay and power-delay product of a CMOS ring oscillator simulated for 3 technology nodes. All axes are normalized.




(a) (b)

Fig. 2. (a) MOS Current-Mode Logic inverter/buffer. (b) Transfer characteristic indicating the noise margins.

$$A_V = V_{SWING}\sqrt{\mu_{eff,n}C_{OX}\frac{W_N}{L_N}\frac{1}{I_{REF}}} \tag{2}$$

$$NM \cong V_{SWING}\left(1-\frac{\sqrt{2}}{A_V}\right) \tag{3}$$

Thus, the size of NMOS devices is chosen regarding noise margin considerations, according to the voltage swing and tail current of the gate. Next, the propagation delay can be modeled as

$$\tau \cong 0.69R_{PMOS}\left(C_{gd,n}+C_{db,n}+C_{gd,p}+C_{db,p}+C_L\right) \tag{4}$$

Thus, sizing down the transistors will allow reduction of the gate delay by reducing the parasitic capacitances at the output. As a result, the $V_P$ voltage sould be chosen as low as possible, to reduce the size of the PMOS devices (1). Practically, this voltage is generated on-chip by a bias circuit such as the one in Figure 3, which will compensate for any parameter variation. Proper sizing, taking into account the maximum process variations, allows to set this voltage to a value close to ground, so that we can assume $V_P = 0$ in our discussion.

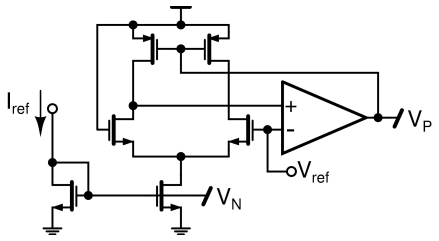



Fig. 3. Bias circuit for MCML gates. The tail current and voltage swing of a reference gate are adjusted to match the reference current and voltage which are provided externally.

## III. Voltage scaling of MCML gates

Let us now consider the effect of supply voltage on the design and performance of MCML gates. Let us assume that the gate is in steady state, that is, one input is driven at $V_{DD}$ and the other at $V_{DD}-V_{SWING}$. The NMOS with the lowest gate voltage will be turned off, and the other one will be working in saturation region. Thus, voltage $V_S$ at node $S$ is given by

$$V_S = V_{DD} - V_{GS,n}$$

where $V_{GS,n} = V_{T,n} + V_{ov}$ depends on the tail current and transistor size, and will be somewhat close to $V_{T,n}$. $V_{GS,n}$ does not depend on the supply voltage, therefore $V_S$ moves with $V_{DD}$. Since the current source transistor is operating in the saturation region, changes in voltage $V_S$ have no significant impact on the delivered tail current, on the delivered output swing, and therefore on the operation of the gate. This is the reason why MCML gates show a strong immunity to supply voltage variations.

This remains true as long as $V_S > V_{DS,sat} \cong V_N - V_{T,n}$. Figure 4 plots the tail current as a function of $V_{DD}$ for different sizes of the current source transistor and different technologies. From these plots, it is clear that in all cases, $V_{DD}$ can be reduced to about 50% of its nominal value without deteriorating the gate operation. In practice, some margin must be kept in order to allow for supply voltage variations, and a value of 60%-65% of the nominal supply voltage is more realistic, allowing to save up to 35%-40% of the power.

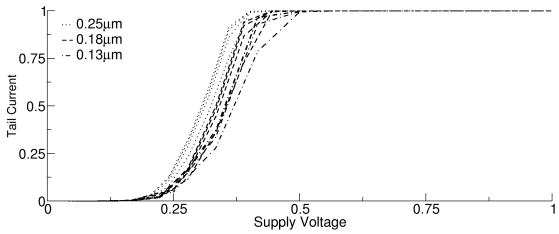
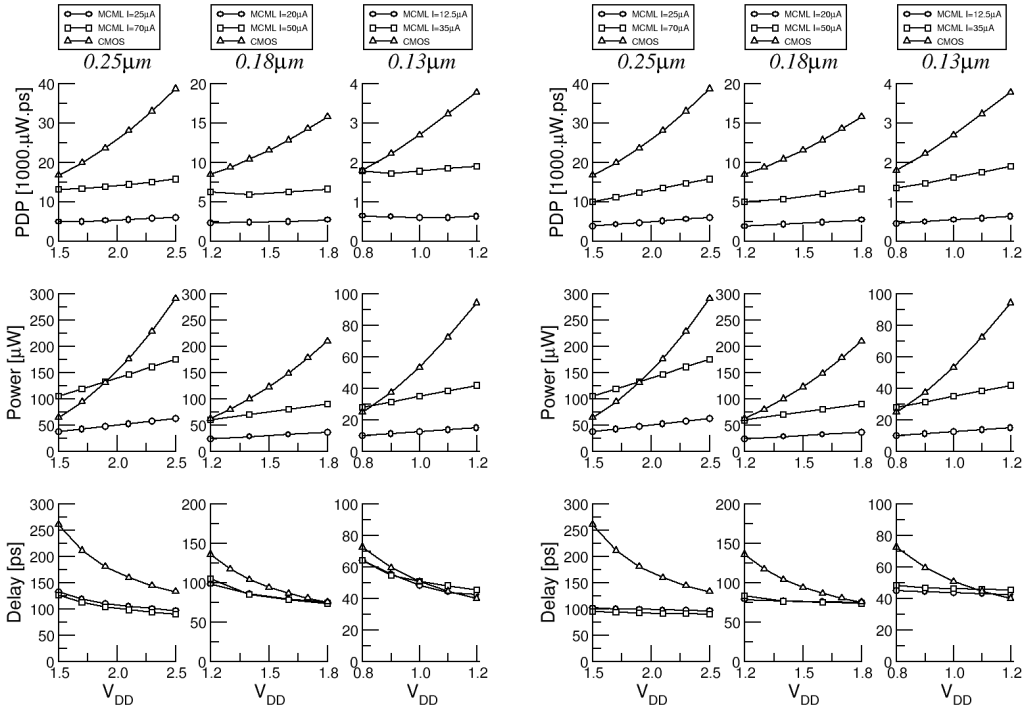



Fig. 4. Plot of the tail current versus the supply voltage, for different sizes of the current source device, at 3 different technology nodes. Both axes are normalized.

Let us now consider the impact of reducing the supply voltage, while keeping the voltage swing constant, on the transistor sizes and the gate performance. Regarding the equations (1)-(4) from previous section, we notice that $V_{DD}$ appears only in equation 1 as the source voltage of PMOS transistors. As it was mentionned previously, the voltage $V_P$ is close to zero, thus, a reduced supply voltage implies that the gate-to-source voltage of the PMOS load devices is reduced by the same amount. In order to keep the voltage swing constant, PMOS load devices need to be sized larger. This results in an increased parasitic capacitance at the output node, having a negative impact on the delay.

Another drawback of reducing the $V_{GS}$ of PMOS devices is that they become less linear. Nonlinearity in the load devices is one source of power supply noise in MCML gates [7], thus this has a negative impact on the noise performance. Finally, decreasing $V_{DD}-V_{T,p}$ also increases the impact of threshold voltage mismatch on the PMOS device on-resistance.

The previous conclusions are illustrated by the plots on Figure 5(a), which show the trends in power dissipation, delay




(a) Using positive bias voltage

(b) Using negative bias voltage

Fig. 5. Trends in the power, delay and power-delay product versus the supply voltage for a MCML ring oscillator at different tail current, for $FO_4$ load conditions and 3 different technology nodes. CMOS data for the same load conditions is included for the sake of comparison.

| | $V_{DD} = 1.2V$ | | $V_{DD} = 0.8V$ | | |
|---|---|---|---|---|---|
| | MCML | CMOS | MCML | **MCML-N** | CMOS |
| Delay $(ns)$ | 42.5 | 40.1 | 64.2 | **45.0** | 72.6 |
| Power $(\mu W)$ | 14.9 | 94.2 | 10.0 | **10.0** | 24.8 |
| PDP | 636 | 3776 | 640 | **448** | 1799 |

TABLE I

SUMMARY OF RESULTS FOR $0.13\mu m$ TECHNOLOGY (MCML-N STANDS FOR MCML WITH NEGATIVE BIAS).

| | MCML | MCML-N | CMOS |
|---|---|---|---|
| $0.25\mu m$ | 0.27 | 0.27 | 53.6 |
| $0.18\mu m$ | 0.25 | 0.25 | 56.8 |
| $0.13\mu m$ | 0.03 | 0.03 | 29.7 |

(a) Nominal $V_{DD}$

| | MCML | MCML-N | CMOS |
|---|---|---|---|
| $0.25\mu m$ | 0.32 | 0.24 | 29.5 |
| $0.18\mu m$ | 0.35 | 0.20 | 35.6 |
| $0.13\mu m$ | 0.05 | 0.03 | 14.7 |

(b) Minimum $V_{DD}$

TABLE II

COMPARISON OF SUPPLY NOISE (CURRENT RIPPLE ON THE SUPPLY LINE IN $\mu A$) FOR 15-STAGES RING OSCILLATORS.

and power-delay product of a 15-stages MCML ring oscillator as a function on the supply voltage. The ring oscillator has been chosen as test circuit, because it allows to simulate switching activity in a chain of logic gates, producing realistic results for power and noise. Data for a 15-stages CMOS ring oscillator is also included on the same plot, for the sake of comparison. It can be seen that the power and delay of MCML gates have a weak dependence on $V_{DD}$, in contrast to CMOS gates. The trends are very similar for the 3 different technologies which were used for simulation. From these plots, we conclude that reducing the supply voltage allows to trade speed for power, and we notice that the power-delay product remains nearly constant with respect to $V_{DD}$.

## IV. NEGATIVE BIAS STRAGEGY

As seen in the previous section, it is very profitable in terms of power dissipation to lower the supply voltage below its nominal value. However, because the gate-to-source voltage of PMOS devices is limited to $V_{DD}$, they need to be sized larger to get the same equivalent resistance, and the gate delay increases.

In order to avoid decreasing the gate-to-source voltage, $V_P$ can be made negative, as long as $V_{DD} - V_P$ stays lower

than the maximum gate-to-source voltage allowed by the technology, which is usually equal to the nominal supply voltage. Therefore, by using a negative voltage to bias the PMOS devices, $V_{DD}-V_P$ can be kept constant with a reduced supply voltage, circumventing the drawbacks that have been discussed previously.

This means that the bias circuitry (Fig.3) needs to be supplied with a negative voltage $V_{SS}$ in order to be able to deliver a negative voltage $V_P$. This negative voltage can be supplied off-chip, or generated on-chip using a DC-DC converter such as a charge pump. The power that needs to be delivered is very low, since it only needs to supply the bias circuitry. Therefore, area- and power- efficient DC-DC conversion can easily be achieved on-chip. A simple charge-pump circuit that provides a negative output voltage is proposed on Figure 7. Note that this circuit requires tying the NMOS body to the source, to avoid reverse-biasing the source junction. There are, however, other possible implementations when this feature is not available.

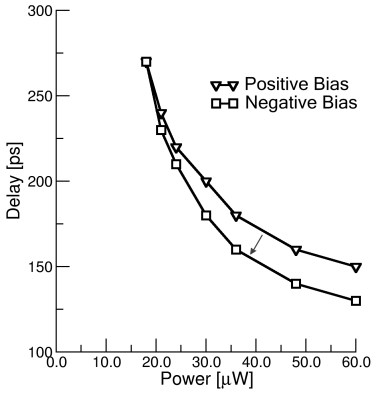
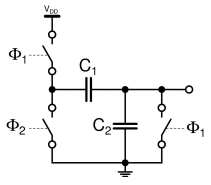
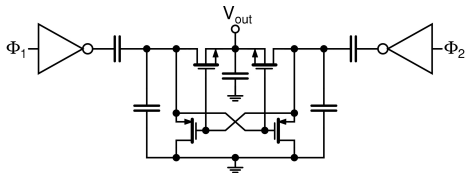



Fig. 6. Power-delay trade-off curve for positive- and negative-bias. The results are obtained from simulations in a 0.18$\mu$m CMOS technology, for $V_{DD}$=1.2V, with $FO_4$+5$fF$ load conditions




(a) Principle




(b) CMOS implementation

Fig. 7. Possible CMOS implementation of the negative voltage generation with a charge pump

Using this negative bias strategy, the simulated trends in power, delay and power-delay product are plotted on Figure 5(b). It is clear that, because the PMOS device size does not change anymore, the delay now stays constant with the varying supply voltage. Since the power decays linearly, the PDP decays in the same fashion. Thus, using this bias strategy, we can achieve up to 35%-40% reduction of the overall power dissipation in high performance MCML circuits, without paying any penalty in terms of speed reduction. The direct implication of this is seen in Fig.6, where the power-delay trade-off curve can be shifted down by applying the negative bias technique. A summary of the results is displayed in Table I for the 0.13$\mu m$ technology. It is also interesting to compare the power supply noise in the different cases. Table II summarizes the simulated peak to peak current ripple on the supply lines for the 15-stages ring oscillators, in the fanout 4 load condition. We emphasize that the noise generated by the MCML circuit is in all cases at least two orders of magnitude lower than that of the CMOS circuit. Also, as mentionned previously, using the negative bias strategy results in better noise performance at reduced supply voltage.

## V. Conclusion

The behaviour of MOS Current-Mode Logic gate under conditions of reduced power supply voltage has been investigated, and it was shown that the operating voltage can be reduced by at least 35% from its nominal value without deteriorating the gate operation. A negative bias strategy involving few additional circuitry has been proposed, which allows a significant enhancement of the power-delay tradeoff, saving up to 35% in power dissipation and power-delay product with no speed penalty. Simulations with 3 different technology nodes show that the results hold with technology scaling, and prove that MCML is competitive with CMOS for low-power design.

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