A VLSI FILTER ARCHITECTURE FOR DIGITAL HDTV CODECS

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This paper describes a compact VLSI implementation of fast pipelined two dimensional FIR filters. A polyphase architecture is presented. The filter bank make special use of coefficients which are in powers-of-two. This leads to an interesting scheme where only shift and add operations are computed.
A new design strategy has been used to speed up the algorithm, as well as a new adder. Internally, the speed achieved is around 200 MHz.

1. INTRODUCTION

Recently, several video systems were in competition, in order to determine a new standard for moving pictures (MPEGII)[0]. Many different approaches were investigated. All of them are based on algorithms performing data compression.
The efficient compression of digital TV data requires both spatial and temporal decorrelation.
The subband decomposition methods [1], and their subset, the block transform based techniques seem to perform well in reducing the spatial correlation in visual data.
Figure 1 and 2 show the CODEC in which the filter banks take place. In this system, the difference between an original image and a reconstructed image is analysed, compressed and sent through the channel.
The filters presented in this paper are analysis and synthesis filters. They are used for subband coding and also in the motion estimation system, where they prepare two low-pass filtered images for the detection of the motion vectors [2].
The architecture and the implementation of these filters. The first part explains the concept of hierarchical filtering and the choice of the coefficients. Then, the global architecture of the filter bank is described. After that, the macro-cells as well as the technology are discussed.

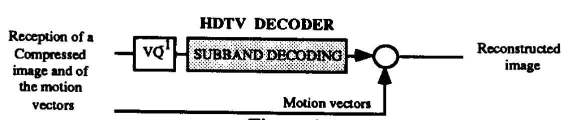

Figure 1

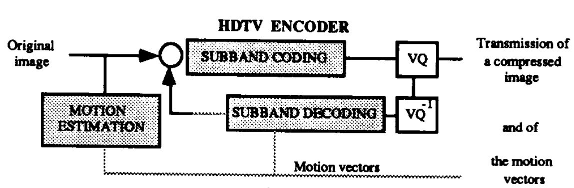

Figure 2

2. HIERARCHICAL 2-D FILTERING

The video codec presented performs a Gabor-like wavelet transform by recursive filtering. The basic structure performs a 1-D two channel frequency decomposition. The use of 1-D filtering simplifies the system and allows us to use the same filters to produce 3 levels of partitioning of an image. Figure 3 shows how an original image is high pass and low pass filtered as well as subsampled. This constitute an analysed image.

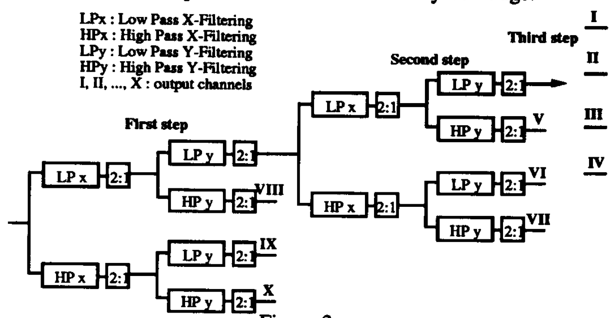

Figure 3

Beeing subsampled, the original image is transformed into another image four times smaller. The low-pass coefficients (2-D filtered) are then refiltered and subsampled in order to produce another image made with the low-passed coefficient. Finally this same operation is performed a third time. Figure 4 shows how an original image is separated in the frequency domain and which coefficients constitute the next candidate to be filtered.

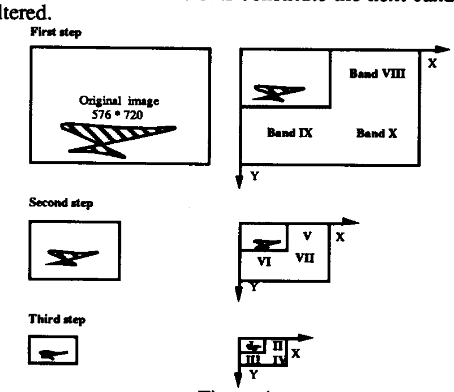

Figure 4

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The synthesis process is based on the same pyramidal principle. The ten frequency bands are reverse filtered three times through the synthesis filters and oversampled.
The use of the Gabor-like wavelet transform is motivated by the fact that Gabor functions have optimal joint localization in the spatial/spatial-frequency domain. On the other hand, according to recent experiments, the majority of the receptive field profiles of the mammalian visual system can be fit quite well by this type of functions [3].

3. THE FILTER TAPS

In data compression, filters have to meet the following requirements :
1. The filters should be as short as possible. From one hand this allows an easy implementation of the filter, and on the other hand long filters are not suitable in image compression because they create strong aliasing effects on edges.
2. The filters have to perform a good frequency partitioning.
3. It is important to maintain the phase without any significant distortion. Linear phase or zero phase filters satisfy this condition.
4. In broadcasting applications the synthesis filters with a less complexity than the analysis ones are more suitable.
5. Both the analysis and the synthesis filters should be easily implementable in real time.

Since the economical criteria has also to be satisfied, it is very important to reduce the silicon area used. Our filters are short. The coefficients are obtained using the direct substitution technique. The analysis as well as the synthesis filters are approximated by filters having coefficients in powers-of-two. Because of these approximations, the reconstructed images are not perfect. However, in all our experiments, the signal to noise ratio of the reconstructed images has been more than 46dB. This, in a large number of applications, is good enough. For applications where higher quality is required (medical), the error of reconstruction can be coded and transmitted through a separate channel.The values of the coefficients used, are reported on Table 1.

Analysis LP	Analysis HP	Synthesis LP	Synthesis HP
2^{-6}	-2^{-6}	2^{-7}	-2^{-7}
0	0	2^{-3}	2^{-3}
-2^{-3}	2^{-3}	2^{0}	-2^{0}
-2^{-7}	-2^{-7}	2^{0}	2^{0}
2^{0}	-2^{0}	2^{-3}	-2^{-3}
2^{0}	2^{0}	2^{-7}	2^{-7}
-2^{-7}	2^{-7}		
-2^{-3}	-2^{-3}		
0	0		
2^{-6}	2^{-6}		

Table 1

4. ARCHITECTURE

As shown on Figure 3, a 2-D filtering is realised. We use two 1-D filters : one for horizontal filtering, the second for vertical filtering. The structure of these two blocks is similar except that the delay Z^{-1} (which is a pel delay for the horizontal filtering) is replaced by a line delay (L^{-1}, for the vertical filtering). This implies the design of line delays which are space consuming. Because the maximum number of taps implemented in the analysis filters is 10 (6 in the synthesis filters), we need to implement 10 line delays for the vertical filtering (6 lines delay for the synthesis filters(see Figure 5)).

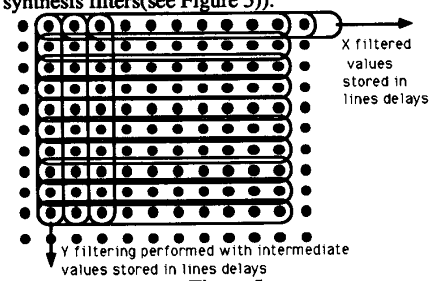


Figure 5

The size of a macro-block for 2-D filtering will depend very much on the size of the delay lines as well as on the number of taps. In this hierarchical approach, the first filtering will have the highest complexity. This is due to the size of the image : 720 by 576 luminance pels.
For the two separate FIR filters, we choosed to implement a polyphase structure. This structure is advantageous when the input data rate is high (HDTV). The subsampling is done before the filtering. This reduces the the processing speed requirements by a factor of two. The standard FIR filter is broken into two parts of half complexity plus one adder and substractor to achieve the low and high pass results (see Figure 6). Filter 1 contains the coefficients with odd indices. Filter 2 contains the coefficients with even indices.

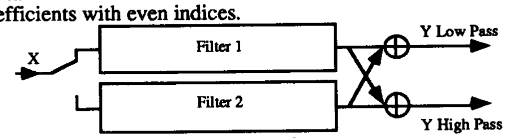
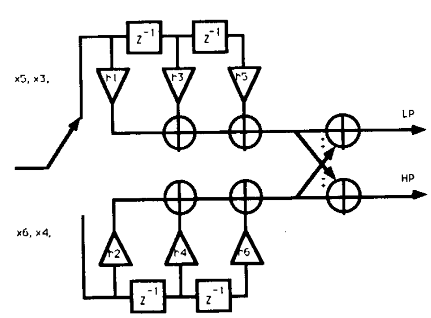


Figure 6

Since the basic FIR filters (Figure 7) use coefficients which are in powers-of-two, the multiplication can be replaced by a wired shift-add operations. We decided to implement programmable coefficients. They can have the following values : 0, 2^{-1}, 2^{-2}, 2^{-3}, ..., 2^{-7}. They are set once at the beginning of a video processing (this has been decided in order to allow a tuning of the final board).

X - Filtering



Y - Filtering

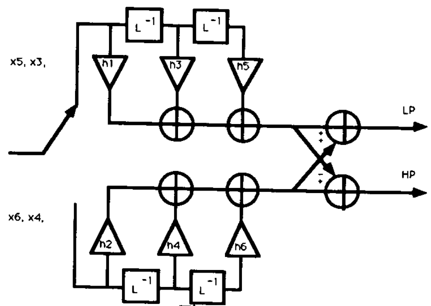


Figure 7

5. DESIGN STRATEGY

A "MIX" design strategy is presented. It is a combination of DOMINO and TSPC [4]. When a N section is in a precharge state, the following P section is in an evaluation state. Both sections are separated by the "degenerated" tristate inverter. Inside an N section, N cells can be cascaded. They are separated by a static inverter. The same process is applied to P sections. In our implementation, we decided to cascade N and P structures with only one N or P net in order to speed up the pipeline. Figure 8 shows the "MIX" design strategy. The obvious advantage is that only one clock signal is propagated on the chip and that no clock generation circuit is needed for the operative part.

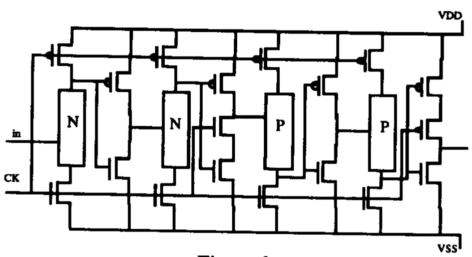


Figure 8

6. THE IMPLEMENTATION

Several basic elements are implemented. Among them, the most important elements, discussed in the following lines are the adders and the substractors.

The adders:

A new architecture has been developped for the generation of fast pipelined adders [5]. The main advantage of these adders is their speed and their regularity. They are faster than the fastest adder for a bit range smaller than 76. The obtention af any kind of adders is straightforward. They have a bit sliced structure which allows a programmability of the layout. The carry bits are generated in parallel. We use the principle of generation and propagation through the Δ operator. This operator is combined with the following recurrent formula :

$$(\partial_i, \pi_i) = (G_0, P_0) \text{ if } i = 0 \quad (1)$$

$$(\partial_i, \pi_i) = (G_i, P_i)\Delta(\partial_{i-1}, \pi_{i-1}) \text{ if } i \neq 0 \quad (2)$$

where $P_i = A_i \oplus B_i$ (3)

and $G_i = A_i B_i$ (4)

With this addition algorithm, it is possible to produce adders satisfying different trade-offs such as "number of transistors versus speed" or "speed versus area".

The substractors :

They are developped on the same algorithm just like the adders. The adders start with a first cell in which B and Bb (B bar) are used. In the substractors, B and Bb are switched in the first cell, and a slice is added on the LSB. On this slice, the inputs are forced to 1 and 0 on the right inputs [6]

The lines delays :

A cascade of TSPC latches is used.

7. THE TOOLS

Our aim was to take a system approach when developping these filters. The regularity of the layouts, the reusability of the basic elements, as well as the flexibility was taken into account.

That is why we used a CAD tool called GDT (from Mentor Graphics). Functional models were developped in M (Mentor Hardware Description Language). The graphic editor (Led) was used to provide a schematic of the filters as well as all layouts of the basic cells (AND, XOR, GP, Δ, latches, ...). Then, macrocells generators were written using the L langage.

The L language enables the layout generation of various macrocells with variable parameters.

For instance, for a line delay, the parameters are the length of the input word, the delay, a N or P structure at the beginning of the block. In the case of the adder/substractor generator, the parameters asked by the programm are : the number of input bits, the type (N or P) of the first stage, if the designer wants an adder or a substracter.

These generators allowed us to obtain automatically the layout of the basic elements of the filters.

The technology :

The basic cells were laid out with a 1,2μ CMOS process (double metal, single poly).

8. RESULTS

A functional block containing the filters for a three level pyramidal filtering in under developpement. The global estimated area is about 50mm2 for the synthesis filters and 70mm2 for the analysis ones.

Electrical simulations were carried out in ADEPT mode (SPICE like simulations with GDT). The simulated delay of the worst cell is 2,7 ns. The layouts were not optimised. All the transistors of the N or P nets have minimum dimensions.

This shows that the global filter could operate at a frequency of about 200MHz.

Table 2 shows the size of the adders and the depth of the pipeline (latency).

The area of a L^{-360} line delay is about 2mm2

bits	16	20	24
N Trans.	890	1305	1577
P Trans.	870	1187	1455
TOTAL	1760	2492	3032
l (μm) :	580	785	1190
h (μm) :	500	660	660
A(mm2) :	0.29	0.52	0.78
Latency	6	7	7

Table 2

9. CONCLUSION

For architectural reasons, two chips using a new clocking scheme are under development. One block will contain the analysis filters, the second the synthesis filters. A frequency of 200 Mhz (CMOS 1,2µ technology) is expected. This is much more than the 13,5MHz needed for the processing of the CCIR601 format. That is why these filters will be particularly interesting in many parts of the codecs fonctionning at a high bit rate and especially in HDTV.

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