

# Etching of sub-micrometer structures through Stencil

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## ABSTRACT

## INTRODUCTION

The processing techniques for micro and nano devices fabrication can be divided into two groups. On one hand, there are the techniques that allow the modification of a given substrate, e.g. ionic implantation, metallization, etching and thermal processes to either grow or deposit insulator layers. On the other hand, there are the processes that allow a pattern transfer of the designs onto the substrate. The general name for this second kind of processes would be lithography, including optical lithography, electron beam lithography (EBL), ion beam lithography (IBL), nanoimprint lithography (NIL) and stencil lithography (SL) among others. The actual fabrication of micro and nano devices consists in the pattern transfer of designs onto a substrate, which means that a combination of both types of processes must be used.

The majority of the lithographic methods mentioned before rely on the use of pre-patterned resists that selectively expose certain parts of the substrate either to a material deposition or to an etching process. Those resists are organic compounds which imply their coating, exposure, development and removal. In addition, their use also imposes certain restrictions regarding the materials and substrates to pattern. In this sense, as it is necessary to use solvents or O<sub>2</sub> plasma to remove the resists and it is necessary to place the substrate at relatively high temperatures (around 100-200°C), not all the substrates can be processed using resists. Alternatively, it is possible to use resistless process as Stencil Lithography that widen the different types substrates that can be used and leads to a reduction in the number of steps in the fabrication process flow.

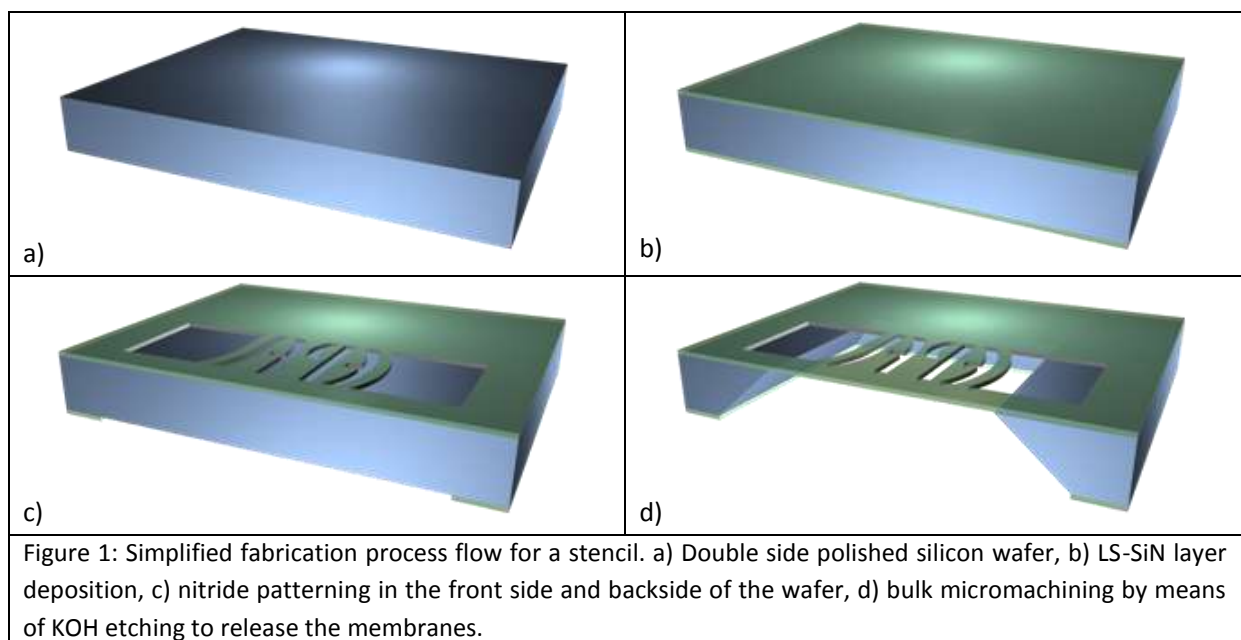
Stencil Lithography has been widely used in the last years to locally deposit metals on a substrate, providing sub-micrometer resolution [1, 2]. The deposited metals can be used either to create contacts [3], to fabricate a mechanical system [4] or to act as a mask for the posterior etching of the substrate [5, 6]. Although this technique has mainly been used for the selective deposition of metal, it has also been used to perform ionic implantation [7] and etching [8-10].

In this work, the experiments performed when using stencils as a hard mask for dry etching of thin films are presented. Therefore, the exceptional work performed by Pang et al. [11] on GaAs, has been extended into silicon, polycrystalline silicon, silicon dioxide, silicon nitride and polyimide.

## FABRICATION OF STENCILS

For this work, chip-size ( $1 \times 1 \text{ cm}^2$  or  $2 \times 2 \text{ cm}^2$ ) stencils have been used. The fabrication process flow can be found in details elsewhere [12-14]. Basically, it starts with a double sided polished Silicon wafer (100 mm in diameter) (Figure 1.a) where a layer of low stress silicon nitride (LS-SiN) is deposited (Figure 1.b). Then, the nitride layer is patterned opening some functional apertures in the front-side and windows for the bulk micromachining in the backside (Figure 1.c). Finally, the release of the membranes is made using a KOH etching (Figure 1.d). The thickness of the nitride layer is chosen depending on the final characteristics desired for the stencil, i.e. to make the membrane more stable mechanically (stiffer) it is necessary that the layer is thicker. On the other hand, when small apertures are needed, the thickness of the membrane must be reduced.

The dimensions of the different apertures in the membranes of the chips used were ranging between 200 nm and several tens of microns. In order to use these stencils as shadow masks for etching, both sides were covered by a thin Al layer (around 25 nm) that acts as a protection layer for the nitride membranes. Aluminum was chosen due to the high selectivity to the used dry etching processes. Alternatively, depending on the material to be etched and the etching parameters, other materials can be deposited to protect the stencils (e.g. amorphous silicon, aluminum nitride, aluminum oxide, etc.). This fact is itself one of the major advantages of this technique, given that the selectivity will be as high as we want it to be. With the membranes protected by this mask layer, the chips were gently placed on the wafers to be patterned and a Reactive Ion Etching was performed (Figure 2).



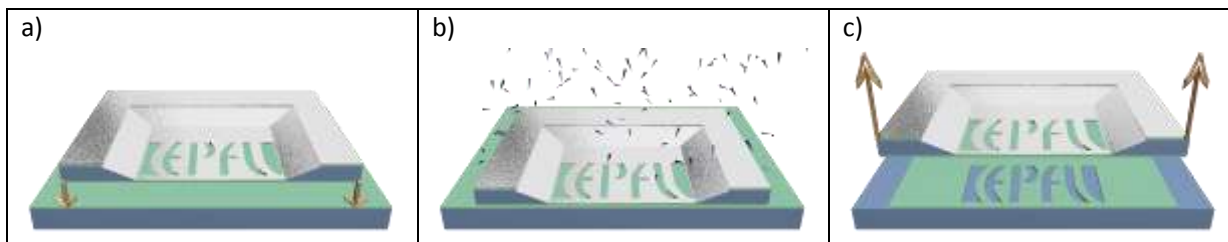


Figure 2: Schematics of the process. (a) A chip with structured membranes (SiN membranes covered by Al) is placed on a substrate (SiN). (b) The substrate is etched using RIE. (c) The chip is lifted revealing the pattern transfer into the substrate.

## ETCHING EXPERIMENTS

Different substrates were patterned using this method: crystalline and polycrystalline silicon (200 nm), thermal silicon dioxide (100 nm thick) and LS-SiN (100 nm thick) and a thin polyimide layer (500 nm). The polyimide was etched in a *STS Multiplex ICP* equipment whereas the rest of the materials were processed in a *Alcatel ICP-601E* reactor. Several etching conditions were tried in order to test the reliability and reproducibility of the experiments. In Table 1, the etching parameters that were found to be working best are included.

Substrate	Etching gases	Pressure	Platten power	Coil power	Etching rate
Si/poly-Si	100 sccm SF <sub>6</sub> 100 sccm c-C <sub>4</sub> F <sub>8</sub>	3 Pa	50 W	1800 W	1 μm/min
SiO <sub>2</sub> /LS-SiN	20 sccm C <sub>2</sub> F <sub>6</sub>	0.63 Pa	450 W	1200 W	300 nm/min (SiO <sub>2</sub> ) 200 nm/min (LS-SiN)
Polyimide	20 sccm O <sub>2</sub>	0.5 Pa	150 W	1000 W	1 μm/min

Table 1: Best etching parameters for the processing of thin films using stencil as a hard mask.

## RESULTS AND DISCUSSION

The characteristics of the different processes we tried (the etching rate (Table 1), the slope of the profiles, etc.) were found to be the same as the obtained when using a process with standard photoresist. As a typical example for the transfer of structures, Figure 3 is showing the replication of some micron sized (from 1 μm to 10 μm) structures into three different materials.

However, this technique also showed two issues of a shadow mask technique: first, when the stencil was not properly fixed on the substrate, a distortion of the patterns could be observed (Figure 4.a and b) due to the movement of the stencil during the process (mainly caused due to increase in the temperature of the stencil); and second, when a gap is present between the substrate and the stencil, there is some loss of dimensions (Figure 4.c and d).

The first of the issues is solved providing a good thermal contact between the substrate and the stencil and a large enough adhesion force to withstand the impact of ions. On the other hand, the gap will affect your pattern transfer depending on the directionality of the ions, i.e. platen power, and will affect in two ways: an effective loss of dimensions in each of the patterned structures (Figure 4.c and d) and a

superficial damage of the substrate surface (increase in roughness) (Figure 3). As a result, the best pattern transfer should be attained using the recipe with the highest platen power, and it was, given that we achieved 200 nm structures in LS-SiN (Figure 5). Another option to overcome this issue is to use a mask material on top of the substrate to be patterned. This technique has already been shown indirectly by performing a KOH etching to the LS-SiN substrates.

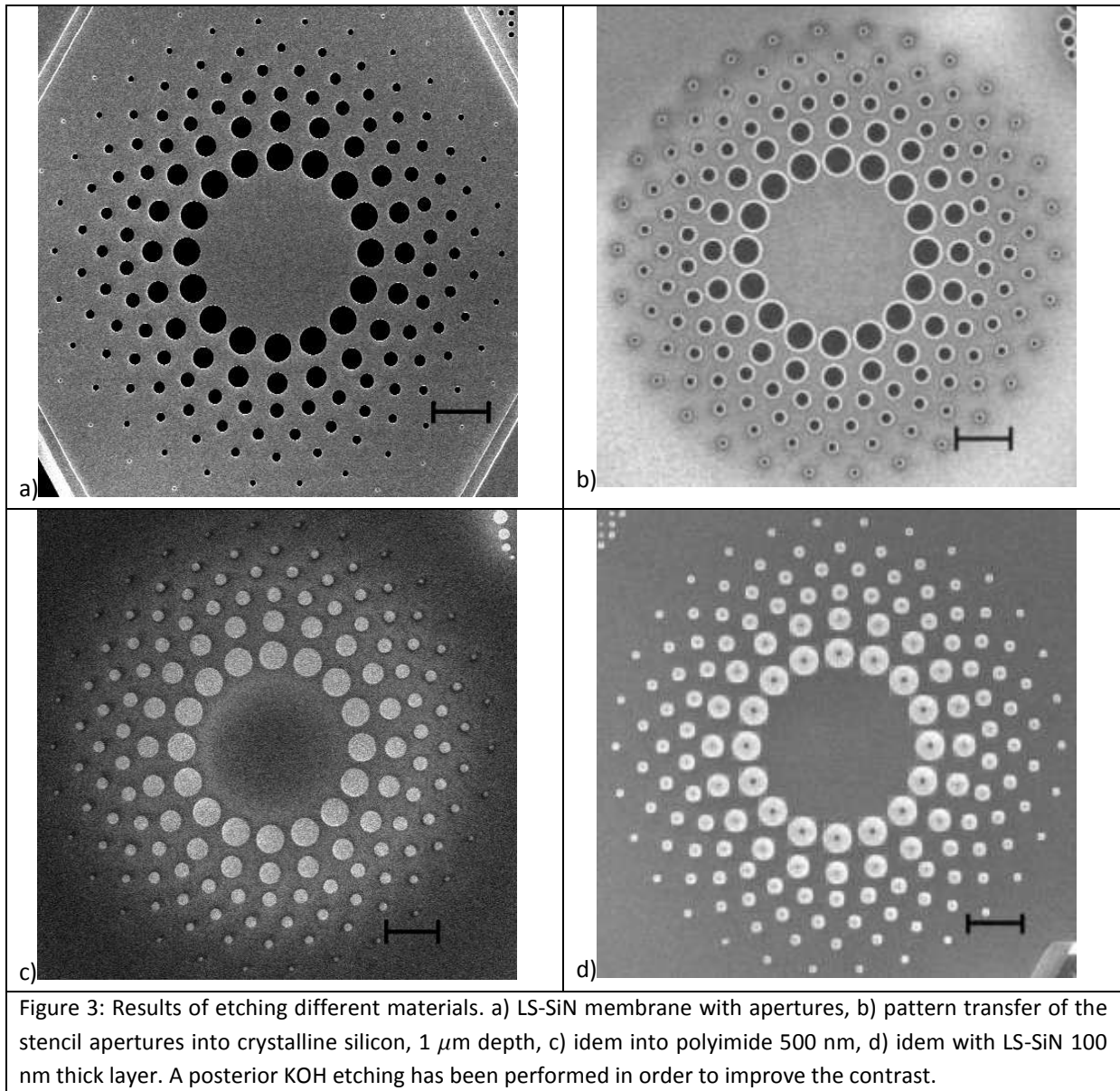


Figure 3: Results of etching different materials. a) LS-SiN membrane with apertures, b) pattern transfer of the stencil apertures into crystalline silicon, 1  $\mu\text{m}$  depth, c) idem into polyimide 500 nm, d) idem with LS-SiN 100 nm thick layer. A posterior KOH etching has been performed in order to improve the contrast.

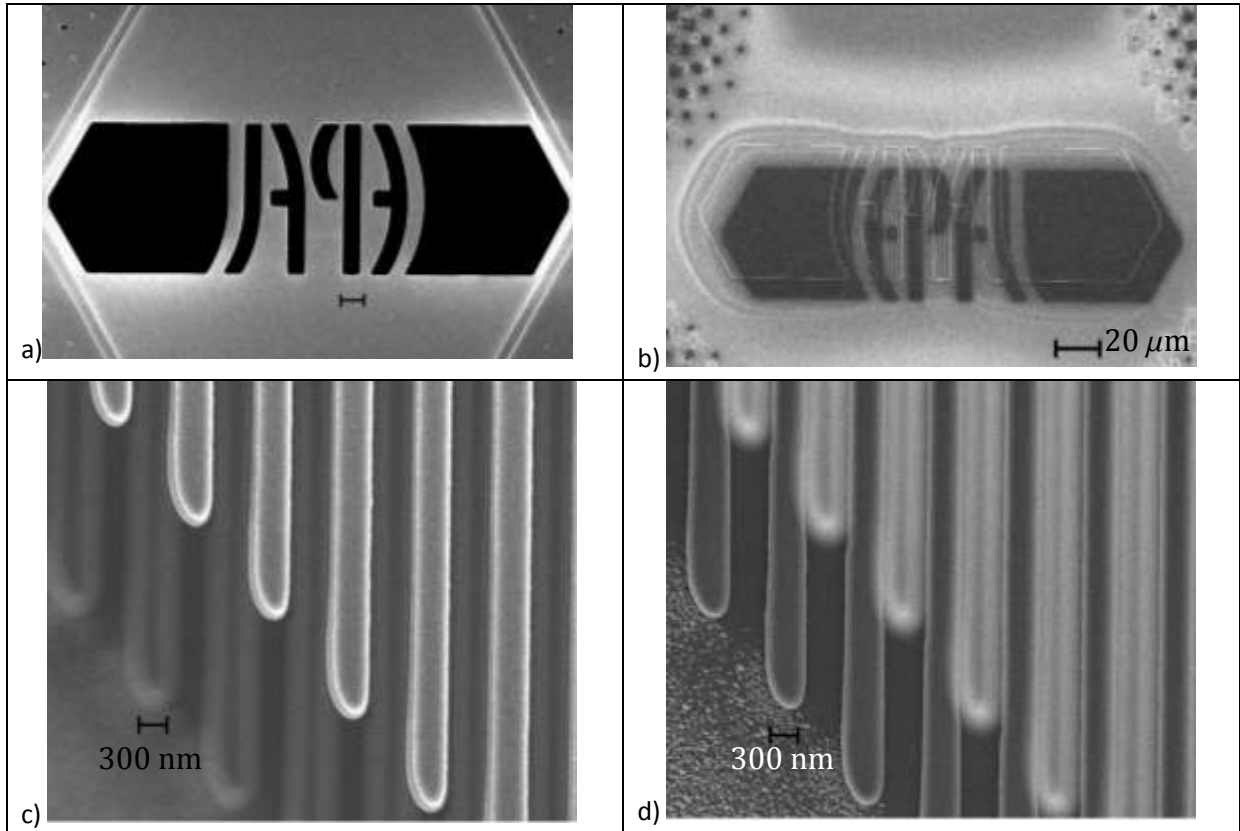


Figure 4: Main issues of this technique. a) LS-SiN membrane with apertures, b) pattern transfer of the stencil apertures into crystalline silicon with pattern distortion due to movement of the stencil during etching, c) and d) SEM pictures of a stencil and the substrate after pattern transfer. The gap can be seen as well as a loss of 50 nm in dimensions: SiN structures were 435 nm wide in the stencil and 385 nm wide in the substrate.

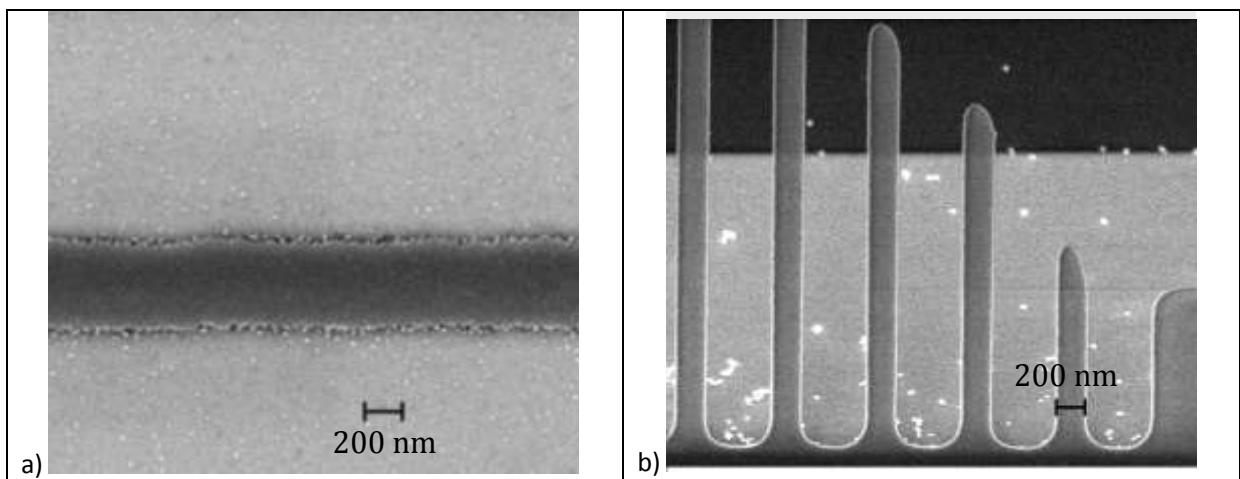


Figure 5: Minimum dimensions achieved up to date. a) 500 nm lines of a 200 nm polysilicon layer, b) 200 nm structures in a 100 nm thick LS-SiN layer.

## CONCLUSIONS

The use of stencils as hard-shadow mask for direct machining of some materials (Silicon, polysilicon, LS-SiN, SiO<sub>2</sub> and polyimide) has been shown. Two major issues have been spotted: the fixation of the stencil on the substrate and the gap between the stencil and the substrate. The effect of both issues can be minimized providing good thermal contact between the hard mask and the substrate and a high directionality of the etching ions. The smallest features attained have been 500 nm lines for a 200 nm thick polysilicon layer and 200 nm for a 100 nm thick LS-SiN layer.

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