Full wafer integration of NEMS on CMOS by nanostencil lithography

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Abstract

Wafer scale nanostencil lithography is used to define 200 nm scale mechanically resonating silicon cantilevers monolithically integrated into CMOS circuits. We demonstrate the simultaneous patterning of ~2000 nano-devices by post-processing standard CMOS wafers using one single metal evaporation, pattern transfer to silicon and subsequent etch of the sacrificial layer. Resonance frequencies around 1.5 MHz were measured in air and vacuum and tuned by applying dc voltages of 10V and 1V respectively.

Introduction

Mechanical resonators with nanometer scale dimensions have a strong interest in two areas: as high sensitivity sensors [1] and as building blocks for high frequency telecommunication systems [2]. Practical applications of mechanical resonators require on-chip signal processing, where optimal performance is achieved in the case of monolithic integration. However, combining the technology for the fabrication of nanomechanical resonators with a standard CMOS technology still remains a challenge. We present a novel wafer-scale technological process based on post-processing CMOS circuits using nanostencil lithography (nSL), a high-resolution shadow-mask technique (fig. 1). nSL directly deposits a controlled amount of material on a surface by evaporation through nanometer scale apertures in a thin membrane. It is a clean (no chemical processing is required) and parallel technique. As it will be shown, we have succeeded in the parallel definition and fabrication of multiple (~2000) silicon nanomechanical resonators at the 200 nm scale that are monolithically integrated into CMOS circuits (fig. 2).

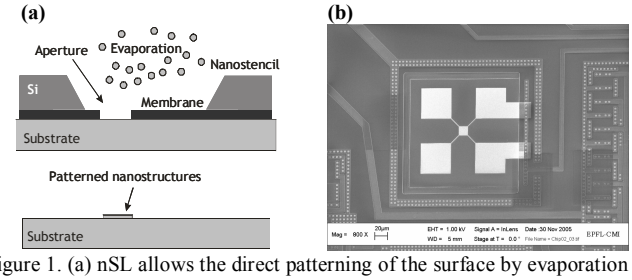

Figure 1. (a) nSL allows the direct patterning of the surface by evaporation of metal through nanometer scale holes realized in a thin membrane. (b) SEM (Scanning Electron Microscope) image of an aligned Al pattern of mechanical device (in white) deposited by nSL onto a CMOS substrate.

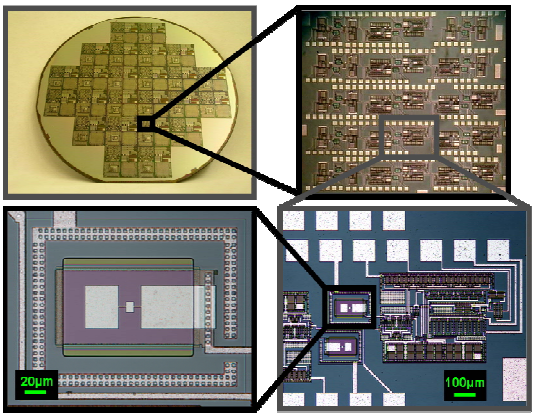

Figure 2. Full CMOS wafer (100 mm) with ~2000 nanomechanical resonators patterned by nanostencil lithography and subsequent etching, monolithically integrated with CMOS circuits. In each wafer, there are 24 CMOS/NEMS chips (7.5*7.5mm^2) containing each one 80 resonators.

A. Full-wafer nanostencil

nSL is a shadow-mask based lithography technique (fig. 1). The applications of nSL have been discussed elsewhere [3]. Full-wafer (100mm) nanostencil fabrication is based on advanced bulk and surface micromachining [4]. The stencil is a micromachined Si wafer containing hundreds of nanostencils in the form of thin (200 nm thick) free-standing silicon nitride (SiN) membranes with micro- and nano-scale apertures. This type of stencil allows local nanopatterning of a whole CMOS wafer in one deposition step (figure 2).

B. Post-processing of CMOS wafers by nanostencil

1. CMOS circuitry characteristics

CMOS circuit design

Electrostatic actuation and capacitive readout by an integrated circuit (IC) are used for detecting the oscillation of the nanomechanical resonators. Monolithic integration is optimum for 'on-chip' signal processing (amplification and conditioning) since parasitic capacitances are drastically reduced.

The resonator is electrostatically actuated by a dc+ac voltage. Its reading electrode, electrically connected to the integrated circuit input, collects a capacitive current whose one part is specifically generated by the variation of electrode-resonator capacitance due to the mechanical motion.

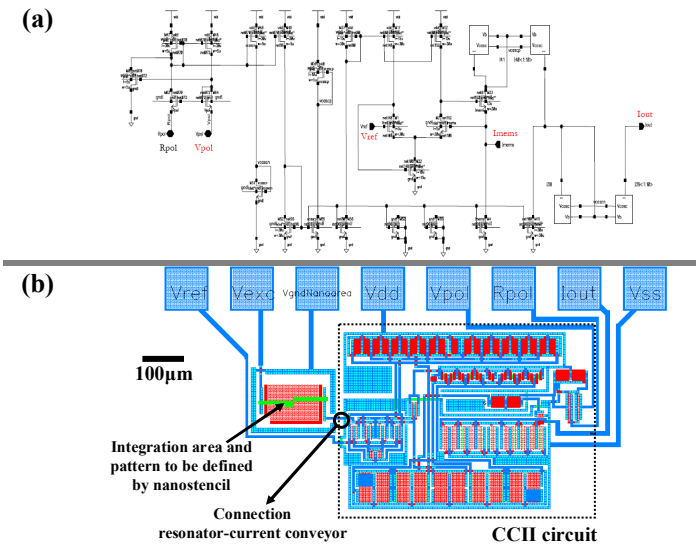

Figure 3. Schematics (a) and layout (b) of the readout CMOS circuit with the integration area

With the aim of reading out this current, the CMOS amplifier circuit of fig. 3(a) was designed based on a second generation current conveyor (CCII) [5]. Basically, the CMOS circuit ensures a constant input voltage biasing, while it amplifies the input current and converts it to an output voltage signal according to the load resistor.

The CMOS circuit layout includes an area reserved for the integration of the nanodevices (integration area, see fig.3b).

CMOS process

CMOS circuits are fabricated using an 'in house' standard two-poly mixed signal CMOS technology (CMOS *CNM25*).

2. Nanostencil lithography on CMOS wafers

The fabrication strategy is based on using existing CMOS layers as structural layer (600 nm thick polysilicon) and sacrificial layer (1 µm thick field oxide) of the resonators. This strategy simplifies the processing and facilitates the further electrical contact between the nanomechanical devices and the circuits [6].

After concluding the fabrication of the CMOS circuits, integration areas must be patterned by evaporation of 80 nm of aluminum using nSL. At this stage, two processing challenges have been addressed: (i) alignment between the CMOS wafer and the nanostencil wafer and (ii) elimination of the pattern blurring caused by the presence of a gap between the stencil and the surface of the integration area due to the CMOS wafer topography. Detailed comments on each of these issues follow.

Alignment procedure

The full-wafer nanostencil must be optically aligned to the CMOS wafer. For this purpose, a specific bond chuck was fabricated in order to be adaptable to a bond aligner (Suss

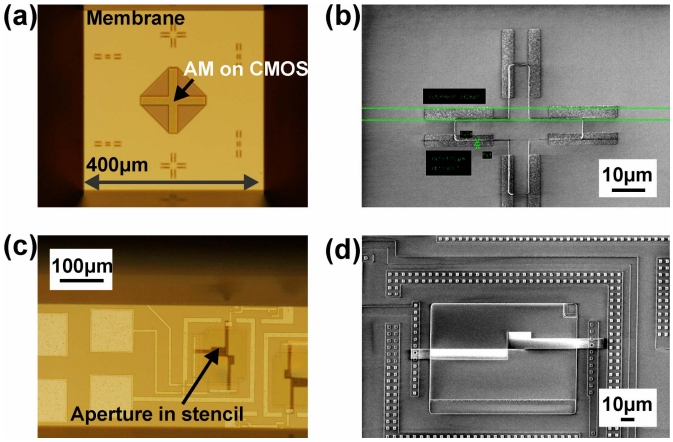

Figure 4. Images of alignment between nanostencil and CMOS wafer. (a) Optical image showing the superposed alignment marks (AM) of thin nanostencil membrane and the underneath CMOS substrate. (b) SEM image of patterned Al onto CMOS AM. Alignment across the wafer is better than 1 µm. (c) Optical image showing the wafer surface through the thin nanostencil membrane at the integration area. (d) SEM image of an integration area after Al patterning and pattern transfer to Si by RIE.

MicroTec MA/BA6), with modified software for topside alignment. It provides a thin controllable gap (down to 20 µm) during alignment procedure so that both elements can be simultaneously visualized. Then, it ensures stencil-wafer contact by mechanically clamping at three different sites. This clamping ensures a secure transportation to the deposition equipment. The entire procedure enables a placement accuracy of 1 µm (fig. 4) at wafer scale.

Blurring correction

Pattern blurring naturally occurs when using a planar stencil onto a non-flat (i.e. CMOS processed wafer) substrate: the non-zero gap (G, see fig. 5a) between the stencil and the bottom part of the surface to be structured causes a dispersion of the metal flux. This phenomenon is generally combined with material-dependent surface migration processes (see halo on fig. 5a). Consequently, patterns are widened what constitutes a major limitation in the use of nSL. Beyond the loss of nominal dimensions, the case of closely spaced patterns (i.e. with small gaps, like resonator-electrode gap) is particularly critical since trenches may remain unopened due to the halo that acts as a mask.

A corrective process [7] based on a partial dry etching of the aluminum pattern has been developed in order to eliminate the gap-induced pattern blurring. It consists on performing a controlled etching of few nanometers of the deposited Al pattern that uniformly decreases its thickness all over the sample. As the Al halo (see fig. 5) is much thinner than the rest of the pattern, it is eliminated by the partial etching. The process recipe is based on a single step of BCl_3 plasma etching (Inductively Coupled Plasma *STS Multiplex* apparatus) performed at room temperature and 1mTorr.

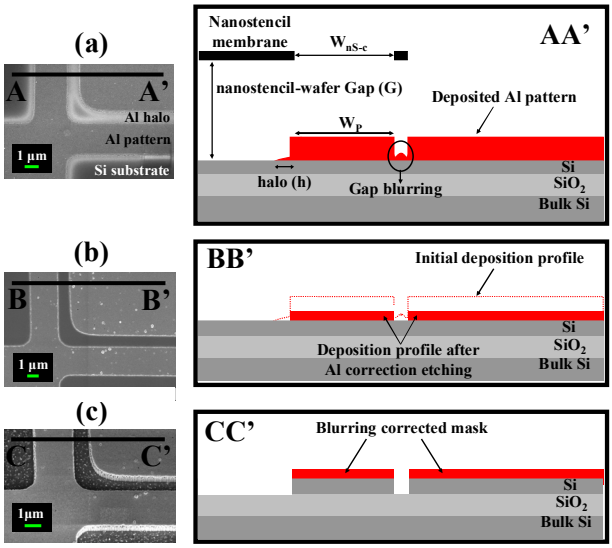

Figure 5. Strategy for blurring correction. SEM images of the Al patterned substrate and associated schematic views. (a) pattern aspect and shape after nanostencil deposition. (b) Al pattern correction by halo removal through dry etching. (c) Transfer to Si by reactive ion etching with recovered Al mask.

The recipe has been successfully implemented at 200 nm scale and across a 100 mm wafer.

Whole fabrication process

One CMOS wafer consists of ~2000 integration areas (distributed over 24 chips) for the fabrication of nanomechanical devices, of which ~ 1000 have connections to a CMOS circuit for signal amplification and interfacing.

The post-processing module leading to the fabrication of monolithically integrated nanomechanical devices starts by the alignment procedure previously discussed. Then, 80 nm thick Al is deposited by electron-beam evaporation through the stencil apertures. In this way all the sites (integration areas) are successfully patterned in one single nSL step (figure 2). Figure 6a depicts this step: the finite gap (G) separating the fabrication area from the device structural layer because of the topography of the circuit is well visible. It originates patterns blurring and subsequently, a corrective dry etching of Al (non visible on fig. 6) is performed to recover the pattern dimensions (c.f. previous section).

Pattern transfer to the 600 nm thick polysilicon structural layer is achieved by reactive ion etching (RIE) using the modified Al pattern as a mask (fig. 6b). Al is chosen as deposition material because of its very high dry etching selectivity with respect to silicon.

The subsequent photolithography process consists of making apertures on a photoresist only around the resonators so that the rest of the chip (i.e. CMOS circuitry) remains protected. Then, the field silicon oxide is locally wet etched in buffered fluorhydric (HF) acid in order to release the mechanical structures (fig. 6c).

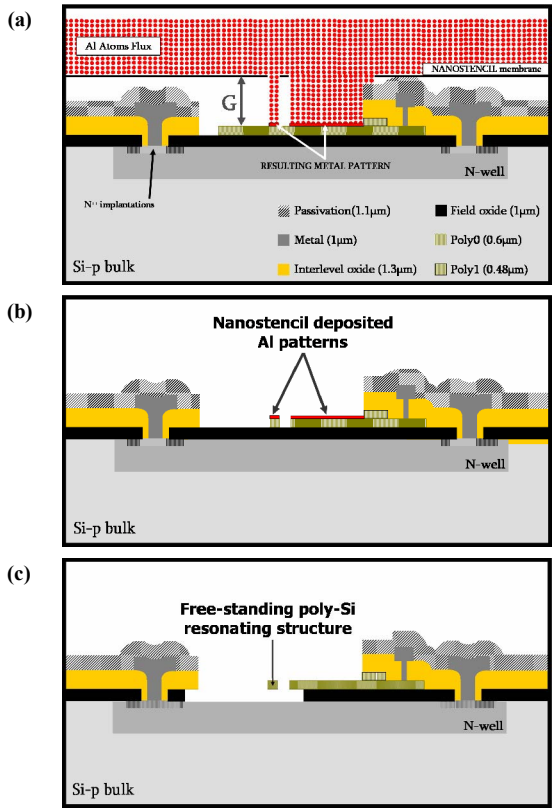

Figure 6. Profile representations of the post-processing main steps. The diagrams show the integration strategy consisting on using already existing layers of the CMOS wafer as structural (polySi) and sacrificial (field oxide) layers of the resonators. (a) Al evaporation on pre-patterned CMOS wafers through nanostencil membrane. (b) the corrected Al pattern is used as a mask for RIE of polysilicon. (c) Resonators released by wet etching with HF acid.

Mechanical structures with line widths down to 200 nm can be routinely achieved by means of the presented process sequence.

C. Electrical characterization

1. CMOS compatibility

We have investigated if nSL and its related process step (Al corrective dry etching) might modify the performance of CMOS circuitry. Specifically designed CMOS test structures were analyzed before and after the whole technological process steps and no degradation in terms of performance has been observed.

We have not found any difference in the electrical performance of the circuits before and after nSL, neither for the test circuits located far from the integration areas (IA) nor for the readout circuits located besides the IA and connected to them. This means that any spatial proximity between nanomechanical device patterned by nSL and CMOS circuitry has no incidence on device performance and therefore a high density of integration is affordable with this nanopatterning technique.

2. Nanomechanical devices characterization

Fig. 7 shows two examples of fabricated micro/nano-resonators. They have been electrically characterized through the CCII-based CMOS circuitry with a network analyzer (Agilent E5100A). Resonator actuation is made by applying a dc+ac voltage at the corresponding contact pad.

Measurements in air and vacuum have been performed on laterally vibrating cantilever beams. While the obtained quality factor is about 10 in air, it raises around 8000 in vacuum despite a relatively disordered structural material (polysilicon).

Fig. 8 is a characteristic response of cantilever beam (with typical dimensions of 14.4 µm in length, 260 nm in width and 600 nm thick) measured in a vacuum of 10^{-2} mBar. The interesting features of the spectrum are listed hereafter.

The resonance frequency can be tuned by varying the applied dc voltage [6]: it linearly decreases with the squared dc voltage (assuming dc>>ac). This so-called spring-softening effect arises from the electrostatic force acting on the parallel plate capacitor electrode/mechanical device. Interestingly, low driving voltages are enough for polarizing the devices: around 1V dc in vacuum and around 10V dc in air, added to a 0.2V ac. From this voltage dependent resonance frequency, a natural value of 1.49 MHz was extracted.

Moreover, a very interesting non-linear behavior is observable on fig. 8 on the curve corresponding to a 2V applied dc voltage. This means that the critical oscillation amplitude [8] has been exceeded and this leads to hysteretic frequency spectra that could provide novel applications like memory elements [9].

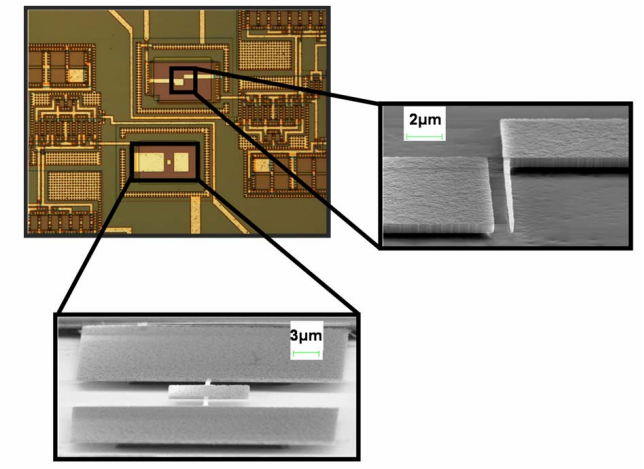

Figure 7. Examples of two types of 600 nm thick polysilicon resonators integrated with CMOS circuitry. A cantilever beam is depicted on the right: it has a width of 200 nm and the gap separating from its electrode is 800 nm wide. The bottom resonator is a torsional paddle shape structure.

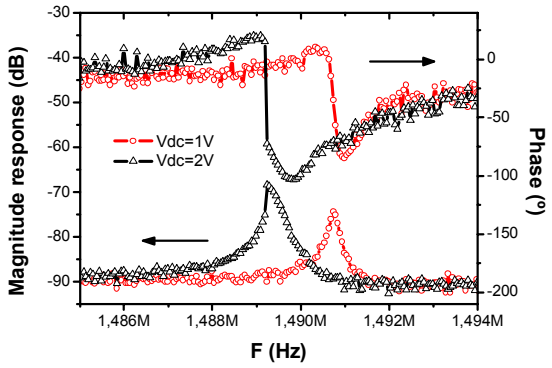

Figure 8. Resonance spectrum of the polysilicon "nano-cantilever" shown in figure 7, monolithically integrated with CMOS circuit. The measurement has been performed at a pressure of 10^{-2} mBar. The resonator is excited by ac voltage (100 mV) plus dc (1 V and 2 V). The signal is detected with a network analyzer after being amplified by the 'on-chip' circuitry. Quality factor is around 8000. The curve taken at 2V V_{DC} shows non linear behavior.

Conclusion

We have demonstrated the potential of nanostencil lithography as a parallel, straight-forward and CMOS compatible patterning technique to define devices on CMOS at the 200-nm scale. The same approach could be extended to other examples of nanodevices, such as single electron transistors (SETs) on CMOS [10], for which there is at present no affordable technological process that fulfill the requirements of high resolution processing at wafer scale and CMOS compatibility.

Acknowledgements

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References

[1] Y. T Yang, C,Callegari, X.L. Fena, K.L. Ekinci, M.L. Roukes, Nano Lett.; **6**; 583 (2006)

[2] J. Wang, Z. Ren, and C. T.-C. Nguyen, IEEE Trans. on Ultrasonics, Ferroelectrics, and Frequency Control. **51**, 1607 (2004)

[3] G.M. Kim, M.A.F. van den Boogaart, J. Brugger, Microelec. Eng., **67-68**, 609-614 (2003)

[4] M.A.F. van den Boogaart, G.M. Kim, J. Brugger, J. Vac. Sci. Technol. B 22(6), 3174 (2004)

[5] Hassanein et al., "New wide band low power CMOS Current Conveyors", Analog Integrated Circuits and Signal Processing, **40**, 91-97 (2004)

[6] J. Verd et al. IEEE J. Microelectromechanical. Systems, **14**, 508 (2006)

[7] J. Arcamone et al. "Dry-etching for the correction of gap-induced blurring and improved pattern resolution in nanostencil lithography", unpublished.

[8] R.H. Blick et al., J. Phys.: Condens. Matter, **14**, 905-945 (2002)

[9] R.L. Badzey, P. Mohanty, Nature, **437**, 995-998 (2005)

[10] K. K. Likharev. in *Nano and Giga Challenges in Microelectronics* pp. 27-68. Elsevier (2003)