COMPACT MODELING OF HIGH VOLTAGE MOSFETs

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Abstract

In the automotive industry, there is a strong trend that has increased the electronics in cars for various functions like fuel injection, electric control of doors and windows, electric chair adjustment, air conditioning etc. The 12V battery used in the present cars will not be sufficient for the increasing number of functions, as a consequence, a change towards 42V batteries will be necessary. For these automotive systems, so called smart power ICs must be used. These are the chips in which the power functionality e.g. control of motor is integrated with logic control. There is also a trend towards operation at high voltages and integrating more intelligence using a microcontroller's RAM/ROM memory and several other sensors and interfaces. The final goal is the integration of a complete system on a single chip, so called power system on chip (SoC).

The interest in accurate modeling of high voltage transistors has increased in recent years due to the compatibility of these devices with standard CMOS technology. However, existing LDMOS models are not accurate enough for this task and SPICE models are specially weak for AC performance. The limitation of these models lies in their lack of capability to physically model some of the characteristic phenomena observed in high voltage devices. The increased difficulty is related to complex 2D effects specific to asymmetric high voltage device architectures.

This thesis presents the compact modeling of high voltage devices. First, a highly scalable general high voltage MOSFET model, for the first time, is presented, which can be used for any high voltage MOSFET with extended drift region. This model includes physical effects like the quasi-saturation, impact-ionization and self-heating, and a new general model for drift resistance. The model is validated on the measured characteristics of two widely used high voltage devices in the industry i.e. LDMOS and VDMOS devices, and implemented in Verilog-A code and tested on commercial circuit simulators like SABER (Synopsys), ELDO (Mentor Graphics), Spectre (Cadence) and UltraSim (Cadence). The model exhibits excellent scalability with transistor width, drift length, number of fingers and temperature. Second, the compact modeling of lateral non-uniform doping is presented, which has great impact on the AC behavior. Third, the invalidity of Ward-Dutton charge partitioning scheme for lateral non-uniformly doped MOSFET is explained. A novel partitioning scheme is then developed and validated on the device simulation. For the first time, noise modeling of lateral non-uniformly doped MOSFET is carried out and validated on the device simulation.

Keywords: High Voltage MOSFET, DMOS, LDMOS, VDMOS, DEMOS, LAC, LAMOS, Drift, Model, DC, AC, Capacitance, EKV, HV-EKV, Partitioning, Noise, Lateral Non-uniform Doping, Scaling

Résumé

L'industrie automobile a alimenté une forte tendance d'intégrer de plus en plus de composants électroniques dans les voitures afin d'accomplir des fonctions diverses telles que le contrle de l'injection de carburant, des vitres électriques, des siges automatiques ou de la climatisation. Les batteries de 12V utilisées dans les véhicules actuels seront bientt insuffisantes pour toutes les fonctions envisagées et par conséquent l'utilisation des sources de 42V est nécessaire. Un nouveau type de circuit intégré de puissance, appelé " smart power " IC en anglais, doit tre utilisé dans lequel la fonctionnalité du contrle de la puissance sera intégrée avec celle de la logique, par exemple pour la gestion du moteur. Il existe, d'ailleurs, une tendance vers des dispositifs haute tension avec la co-intégration d'intelligence accrue, en utilisant la mémoire RAM/ROM de microcontrleurs, en parallle avec des capteurs et d'autres interfaces. Finalement, le but sera la fabrication d'un systme complet sur puce, le systme de puissance sur puce (SoC, " System on Chip ").

La compatibilité de ces composants avec la technologie standard CMOS a récemment augmenté l'intért pour une modélisation précise des transistors haute tension. Toutefois, les modles existants LDMOS ne sont pas suffisamment précis et les models SPICE s'avrent particulirement faibles quant la performance AC. La limitation des modles mentionnés se situe dans leur incapacité de modéliser physiquement des phénomnes caractéristiques observés dans les dispositifs haute tension. La difficulté principale est liée des effets bidimensionnels spécifiques aux architectures asymétriques de ces composants.

Ce travail de thse est consacré la modélisation compacte de dispositifs haute tension. Tout d'abord, un modle MOSFET général de scalabilité accrue est présenté pour la premire fois et qui peut tre utilisé pour tous les MOSFET haute tension avec une région de " drift " étendue. Le modle en question prend en compte des phénomnes physiques tels que la quasi-saturation, l'ionisation par impact, l'autoéchauffement et il introduit une nouvelle description pour la résistance de " drift ". Par ailleurs, le modle a été validé sur des caractéristiques mesurées de deux types de composants, largement répandus dans l'industrie comme le LDMOS et le VD-MOS, mis en uvre en code Verilog-A et testé sur des simulateurs commerciaux comme SABER (Synopsys), ELDO (Mentor Graphics), Spectre (Cadence) et UltraSim (Cadence). D'une part, le modle présente une scalabilité excellente avec la largeur du transistor, la longueur de " drift ", le nombre d'électrodes interdigitées et la température. D'autre part, la modélisation compacte du dopage non-uniforme latéral est présentée, qui a un impact considérable sur le comportement AC. En outre, l'invalidité de la théorie de Ward-Dutton sur la répartition des charges dans les MOSFET dopage uniforme est expliquée. Une nouvelle théorie sur cette répartition a été développée et validée par simulation numérique. Finalement, pour la premire fois, la

modélisation du bruit des MOSFET dopage latéral non-uniforme a été élaborée et vérifiée par simulation numérique.

Keywords: High Voltage MOSFET, DMOS, LDMOS, VDMOS, DEMOS, LAC, LAMOS, Drift, Model, DC, AC, Capacitance, EKV, HV-EKV, Partitioning, Noise, Lateral Non-uniform Doping, Scaling

Contents

Chapter 1

Introduction

1.1 Background

The transistor and subsequently the integrated circuits certainly qualify as two of the greatest inventions of the twentieth century. In a certain sense, all of solid-state electronics goes back to the invention by Ferdinand Braun of the solid-state rectifier in 1874 [1, 2]. That was a full 73 years before the discovery of the transistor. His work centered around the solid-state rectifier using a point contact based on lead sulfide. Of course, this configuration made for a very unstable device. In fact, after the invention of the vacuum tube, later in the century, this device very quickly became obsolete. But, later when people wanted to go to very high frequencies, and vacuum tubes would not work at the frequencies desired, the idea of the point contact rectifier made a comeback.

The theoretical development of quantum mechanics during the 1920s also played an important role in driving solid-state electronics. Without quantum mechanics, there would never have been any comprehensive understanding of solids. The understanding of the differences between metals, insulators, and semiconductors was quickly developed. The concept of electronic band structure, due to quantum mechanics, was the key to that insight. Following these advances, was the development of the quantum theory of solids led by Peierls, Wilson, Mott, Franck, and others, largely in England. These researchers added much to the understanding about electron conductivity in metals. Those days were truly the beginnings of establishing a picture of the electronic structure of metals. Metallic sodium is the simplest of all metals from an electronics point of view and was often studied in that era. A simple theory of Schottky barriers led to a crude understanding of the rectifiers discussed above, but the theory did not work quantitatively. These dedicated researchers brought the understanding forward, but semiconductors sat in the middle between the metal and the insulator, and in those days semiconductors were still a puzzle.

The continued efforts extended toward the discovery of new devices. For example, in 1926, Lilienfeld invented the concept of a field effect transistor (FET) [3]. He believed that applying a voltage to a poorly conducting material would change its conductivity and thereby achieve amplification. He patented this concept in 1926, but no one was able to do anything with it until much later.

By the late 1930s, it was beginning to be more widely accepted that there may be opportunities to create some form of solid-state devices. At this time Mervin Kelly, at Bell Labs, decided

in 1936 that he should start a solid-state device group. He challenged a number of people, Bill Shockley, Russell Ohl, Jack Scaff, and others, to begin work on solid-state devices. Kelly had a feeling that the vacuum tube was not going to be the ultimate answer to electronics. Its reliability and size were such that something needed to be done, besides making more efficient and smaller vacuum tubes. It is interesting to note that by 1938, two Germans (Pohl and Hilsch) described a solid amplifier made using potassium bromide that had three metal leads. However, this device turned out to have too low operating frequency. Also, it was not a device that could be used in any true sense for electronics. That such a device came along about the same time that Kelly created the Bell Labs solid-state group shows that other engineers were thinking along the same lines. By 1940, Russell Ohl had done a great deal of work, along with others at Bell Labs, in an attempt to understand silicon crystals. Ohl learned that depending on how you prepared single crystals of silicon, you could get either $n-$ or $p-$type silicon. What was meant by n or p type back in those days was whether it was a positive or negative rectifier. That was where the notation n or p came from. It was a question of which direction the rectification occurred; they defined these terms by that criterion. It is also interesting that a little later on, Ohl actually was able to make a sample in which the top part was a p-type region and the bottom was n type, and he found that when light was shone on it, it actually developed a voltage [4].

This was the status of solid-state electronics near the beginning of WWII, and it really did not change all that much during the war except in technology areas influenced by the work on radar. Radar requirements produced a very strong desire to fine-tune solid-state rectifiers, and this resulted in some effort to try to improve silicon and germanium materials. In this era, there was a lot of solid-state detector work done, mostly by trial and error. After WWII, the discovery of point contact transistor by Berdeen and Brattain in 1947 and the theory of the bipolar junction transistor by Shockley [5] at the Bell Telephone Laboratories [6] changed the future of microelectronics. By April 1950, Shockley et al. actually succeeded in growing the first junction npn device [7]. In fact, the device behaved essentially as predicted by Shockleys theory. Progress was supported by a series of important inventions that led to better and better devices. In fact, Shockley wrote a book titled Electrons and Holes in Semiconductors. Still it took several years before the first Si/SiO_2 MOSFET, which is now so widely used, was demonstrated by Kahng and Atalla [8, 9]. But, this turned out to be a pretty poor device. It took until the early 1970s, 15 years before planar FETs came into common use. The first integrated circuits (IC) were developed by Noyce at Fairchild Semiconductor and by Kilby at Texas Instruments. Kilby's circuits consisted of transistors fabricated using the mesa technique, where the collector contact is made to the backside of the wafer, and bonded gold wire is used for interconnect. Noyce's ICs more closely resembled present day chips because they used a planar fabrication technique developed by Hoerni at Fairchild, where oxide masking and diffusion were used to form the transistor [10].

The initial circuits were oscillators and simple digital flip-flops using two or three active devices along with passive elements, but by 1971, the technology had advanced to the stage, where the first microprocessor (Intel 4004) was fabricated with 2300 transistors. In 1965, Moore published a paper on the state of the semiconductor industry, which predicted that the number of devices in an integrated circuit would double each year [11, 12]. This prediction became the famous "Moore's Law". Today the density of transistors in a chip has crossed the billion mark.

1.2 High Voltage MOSFET models

The interest in the high voltage (HV) MOS devices has dramatically increased as these devices were integrated with the low power modules in MOS technology. Today, HV-MOS devices are extensively used in all kinds of integrated power circuits, like switch-mode power supplies and power amplifiers. In addition, Lateral double-Diffused MOSFET (LDMOS) devices processed in thin-film silicon-on-insulator (SOI) provides a new and attractive technology for smart power integrated circuits in consumer and automotive applications [13]. Optimal design of these power circuits requires HV-MOS models for circuit simulation, which describe the device characteristics accurately over a wide range of biases.

The accurate compact modeling of high voltage MOS transistors has always been a challenge in the device modeling community. This is due to the fact that the charges and field associated with the drift region and intrinsic MOS have very complex dependence on the external terminal biases owing to the asymmetric device architecture. Though many groups around the world have attempted to model the different architectures of HV-MOS transistors using different approaches, most of these are sub-circuit or macro-models. Acceptable simulation accuracy is obtained by the use of these macro-models based on conventional low voltage modules [14, 15], but these macro-models are not physical and do not take into account the special phenomena of HV devices.

The LDMOS macro model proposed by Frere et al. [15], which is being used in AMI Semiconductor (AMIS), is based on BSIM3v3.2. The model uses an adapted JFET to model the drift region and shorted PMOS transistors to model the capacitance behavior of the drift region. The drift region modeling using JFET is carried out by equations based on Schichman & Hodges [16]. The equations were implemented in Verilog-A module. The gate voltage of the JFET was tied to the intrinsic drain potential of intrinsic MOS, which provided variable threshold voltage of JFET. Two shorted PMOS transistors were used to model the gate overlap over thin and thick oxide, respectively. Even though this LDMOS model provides good behavior for both DC and AC operations, the scalability of model especially for drift length was never demonstrated.

Some other compact models have also been reported in the literature with better accuracy [17, 18, 19, 20, 21, 22, 23, 24]. Other models reported in the literature show reasonable accuracy in DC operation [17, 18, 19, 20, 22], but do not show model validity for AC operation under different biasing conditions. Although the physical LDMOS model developed by Anghel et al. demonstrated good accuracy in DC regions, it was very difficult to implement and use it for industrial purposes because of the convergence problems in the simulator. There has also been some work in the development of DMOS models using neural network based approach [25, 26]. This approach provides excellent results with speed, provided the model is trained on wide range of measurement data. The major weakness of neural network based models is that they are not scalable and can be used only for the particular device structure for which it has been trained.

The MOS model 20 (MM20) [23, 24] from NXP (earlier Philips Semiconductor) is the famous LDMOS compact model. This model has shown capability to model both DC and AC operations including quasi-saturation and self-heating effects. MM20 is a surface potential based model, whose intrinsic MOS model is similar to the MM11 or PSP [27, 28], while drift region is modeled using MM31 or MM40 [27]. MM20 model has several variations for different LDMOS structures. One model is for LDMOS with thin gate oxide all over the drift region.

Another variation of this model is for the partial gate overlap in the drift region and uses a resistance to described the non-overlapped drift region. Then there is different model for drift region with both thin and thick gate oxides. Even though all of these models have demonstrated good results for different LDMOS devices, one has to choose different model for different devices. Also none of these models take into account the lateral non-uniform doping in the intrinsic MOS, which may result in poor accuracy in the transient operations [29, 30].

Recently Hiroshima University has developed an HiSim-LDMOS model [31, 32]. This LDMOS model is the modular extension of HiSim model, which is a surface potential based model. There has been no publication of this LDMOS model yet.

Although efforts mentioned have been successful in solving some modeling problems in high voltage devices, still there are several open challenges. Following are some of the key challenges in this field, which are also the must have features of any standard high voltage model by compact modeling council (CMC):

➤ Accurate modeling of DC/AC behavior as well as the derivatives of terminal currents and node charges with respect to node voltages for all working modes (off, linear, saturation regions and reverse modes).

➤ Charge model has to be charge conservative, and intrinsic charge model has to take into account the effects of voltage drop across the source and drain resistances.

➤ Accurate modeling of drain extension (drift) region resistance including velocity saturation.

➤ Accurate modeling of gate/drain overlap region bias dependent capacitance and resistance.

➤ Accurate modeling of parasitic effects (gate, source and drain, and substrate resistances, and source/drain-body junction diodes)

➤ Accurate modeling of the 1/f, thermal, and gate induced noise.

➤ Capable of modeling accurately with power supplies up to 200 volts and temperature ranges from -50 °C to 200 °C.

➤ Capable of modeling self-heating effects accurately and efficiently, which requires scalable temperature-dependence modeling.

➤ Capable of modeling accurately quasi-saturation effects and g_m fall-off in the saturation region, namely, the channel current compressions at higher V_{GS} when V_{DS} is greater than V_{dsat}.

➤ Capable of modeling accurately C_{GD} drop at higher external V_{GS} biases.

➤ Capable of accurate modeling of the true asymmetry of the source and drain resistances and the source and drain junctions in $I - V$ and $C - V$.

➤ Capable of modeling substrate current behavior correctly including the impact ionization taking place in the drain drift extension regions.

➤ Capable of handling scalability over a wide range of geometries, biases, and temperatures with one set of global model parameter set to cover the entire device matrix provided for model extraction. Provides drain drift region length as an instance parameter.

➤ Capable of covering reverse working mode for both symmetric and asymmetric structure (i.e. when $V_{DS} < 0$)

➤ Capable of handling of p-type devices as well as n-type devices.

➤ Good convergence in reasonable scale circuit simulation.

➤ Capable of modeling accurately a wide array of HV-MOSFET process technologies and device structures, which would include LDMOS and EDMOS (Extended Drain), both symmetrical and asymmetrical, and other drain drift extension structures including, but not limited to, those of various RESURF flavors.

➤ Capable of modeling layout dependent characteristics including multi-finger device structures that have separate, merged, and shared source and drain connections, and point and wide source/drain contacts.
➤ Capable of modeling body bias dependency of DC and AC characteristics.
➤ Capable of providing optional temperature node for thermal electrical coupling simulation.
➤ Capable of modeling parasitic BJT effects.

In this thesis, a detailed analysis and modeling of high voltage MOSFETs will be presented. Some of the key challenges mentioned above will be addressed here.

1.3 Thesis Structure

This section briefly outlines the contents of the chapters.

- **Chapter 2: DC and AC behavior of High-Voltage MOSFETs**

A basic overview of the architectures of high voltage MOSFETs is presented. Impact of lateral non-uniform doping and drift region on both the DC and AC behavior is analyzed which paves the way to develop an accurate HV-MOS model [33].

- **Chapter 3: EKV-based Scalable General High Voltage MOSFET Model**

A new high voltage MOSFET model is developed in this chapter. The model uses charge based EKV model for the modeling of intrinsic MOS channel while drift region is modeled using bias dependent drift resistance. The model is validated on the AMIS I2T100 and I3T50 technologies. The scaling of the model is tested for different temperatures, drift length and number of fingers [34, 35, 36, 37].

- **Chapter 4: Compact Modeling of Lateral Non-uniform doping**

For the first time, true compact modeling of lateral non-uniform doping is presented. The impact of this model is emphasized on the capacitance behavior of high voltage MOSFETs. The model is validated on the AMIS I2T100 and I3T50 technologies especially for the AC behavior [29, 38, 39, 30].

- **Chapter 5: Partitioning Scheme and Noise Modeling in the Lateral Non-Uniformly doped MOSFET**

The invalidity of Ward-Dutton charge partitioning scheme for lateral non-uniformly doped MOSFET is explained. A novel partitioning scheme is then developed and validated on the device simulation [40, 41, 42]. For the first time, noise modeling of lateral non-uniformly doped MOSFET is carried out and validated on the device simulation [43].

Bibliography

[1] E. Braun and S. Macdonald, "Revolution in Miniature." Cambridge University Press, 1982.

[2] W. Brinkman, D. Haggan, and W. Troutman, "A history of the invention of the transistor and where it will lead us," *IEEE Journal of Solid-State Circuits*, vol. 32, no. 12, pp. 1858–1865, Dec. 1997.

[3] J. E. Lilienfield, "," *US Patent 1745175*, 1926.

[4] J. H. Scaff, H. C. Theuerer, and E. E. Schumacher, "P-type and N-type silicon and the formation of the photovoltaic barriers in silicon ingots," *Trans. A.I.M.E.*, vol. 185, p. 383388, June 1949.

[5] W. Shockley, "The Theory of p-n Junctions in Semiconductors and p-n Junction Transistors," *Bell Syst. Tech. Journal*, vol. 28, pp. 435–489, 1949.

[6] J. Bardeen and W. H. Brattain, "The transistor, a semi-conductor triode," *Phys. Rev.*, vol. 74, no. 2, pp. 230–231, Jul 1948.

[7] M. S. W. Shockley and G. K. Teal, "P-N junction transistors," *Phys. Rev.*, vol. 83, p. 151162, 1951.

[8] D. Kahng and M. M. Atalla, "Silicon-silicon dioxide field induced surface device," in *Solid State Device Research Conf.*, June 1960.

[9] D. Kahng, "A Historical Perspective on the Development of MOS Transistors and Related Devices," *IEEE Transactions on Electron Devices*, vol. 23, pp. 655–657, July 1976.

[10] G. Moore, "The Role of Fairchild in Silicon Technology in the Early days of 'Silicon Valley'," *Proceedings of the IEEE*, vol. 86, pp. 53–62, Jan 1998.

[11] ——, "Cramming More Components Onto Integrated Circuits," *Proceedings of the IEEE*, vol. 86, no. 1, pp. 82–85, Jan 1998.

[12] ——, "No exponential is forever: but 'Forever' can be delayed! [semiconductor industry]," in *IEEE International Solid-State Circuits Conference*, 2003, pp. 20–23.

[13] J. A. van der Pol, A. Ludikhuize, H. Huizing, B. van Velzen, R. Hueting, J. Mom, G. van Lijnschoten, G. Hessels, E. Hooghoudt, R. van Huizen, M. Swanenberg, J. Egbers, F. van den Elshout, J. Koning, H. Schligtenhorst, and J. Soeteman, "A-BCD: An

economic 100 V RESURF silicon-on-insulator BCD technology for consumer and automotive applications," in *IEEE International Symposium on Power Semiconductor Devices and ICs*, June 2000, p. 327330.

[14] A. Canepari, G. Bertrand, A. Giry, M. Minondo, F. Blanchet, H. Jaouen, B. Reynard, N. Jourdan, and J.-P. Chante, "LDMOS modeling for analog and RF circuit design," in *IEEE European Solid-State Device Research Conference (ESSDERC)*, Sept. 2005, pp. 469 – 472.

[15] S. Frere, P. Moens, B. Desoete, D. Wojciechowski, and A. Walton, "An improved LDMOS transistor model that accurately predicts capacitance for all bias conditions," in *Proceedings of the 2005 International Conference on Microelectronic Test Structures (ICMTS)*, April 2005, pp. 75 – 79.

[16] "Affirma spectre circuit simulator reference, product version 4.4.6," June 2000.

[17] J. Victory, J. Sanchez, T. DeMassa, and B. Welfert, "A static, physical VDMOS model based on the charge-sheet model," *IEEE Transactions Electron Devices*, vol. 43, no. 1, pp. 157 – 164, Jan. 1996.

[18] C.-Y. Tsai, D. E. Burk, and K. D. T. Ngo, "Physical Modeling of the Power VDMOST for Computer-Aided Design of Integrated Circuit," *IEEE Transactions Electron Devices*, vol. 44, no. 3, pp. 472 – 480, March 1997.

[19] N. Hefyene, C. Anghel, A. Ionescu, S. Frere, R. Gillon, M. Vermandel, B. Bakeroot, and J. Doutreloigne, "An experimental approach for bias-dependent drain series resistances evaluation in asymmetric HV MOSFETs," in *IEEE European Solid-State Device Research Conference (ESSDERC)*, Sept. 2001, pp. 403 – 406.

[20] C. Anghel, "High voltage devices for standard MOS technologies : characterisation and modelling," Ph.D. dissertation, EPFL, 2004, thesis No. 3116.

[21] N. D'Halleweyn, J. Benson, W. Redman-White, K. Mistry, and M. Swanenberg, "MOOSE: a physically based compact DC model of SOI LD MOSFETs for analogue circuit simulation," *IEEE Transactions Computer-Aided Design of Integrated Circuits and Systems*, vol. 23, no. 10, pp. 1399–1410, Oct. 2004.

[22] N. Hefyene, "Electrical characterization and modelling of lateral DMOS transistor : investigation of capacitances and hot-carrier impact," Ph.D. dissertation, EPFL, 2005, thesis No. 3200.

[23] A. Aarts, N. D'Halleweyn, and R. van Langevelde, "A surface-potential-based high-voltage compact LDMOS transistor model," *IEEE Transactions Electron Devices*, vol. 52, no. 5, pp. 999 – 1007, May 2005.

[24] A. Aarts and W. Kloosterman, "Compact modeling of high-voltage LDMOS devices including quasi-saturation," *IEEE Transactions Electron Devices*, vol. 53, no. 4, pp. 897 – 902, April 2006.

[25] S. Frere, B. Desoete, J. Rhayem, M. Anser, and A. Walton, "A neural-network-based local inverse mapping technique for building statistical DMOS models," in *IEEE European Solid-State Device Research Conference (ESSDERC)*, Sept. 2003, pp. 331– 334.

[26] R. Gillon, "Aspects of robust mixed-signal design in smart-power IC processes," in *IEEE International Symposium on Industrial Electronics (ISIE)*, vol. 2, June 2005, pp. 485– 488.

[27] "High voltage models," , http://www.nxp.com/models.

[28] G. Gildenblat, X. Li, W. Wu, H. Wang, A. Jha, R. V. Langevelde, G. Smit, A. Scholten, and D. Klaassen, "Psp: An advanced surface-potential-based mosfet model for circuit simulation," *IEEE Transactions Electron Devices*, vol. 53, no. 9, pp. 1979 – 1993, Sept. 2006.

[29] Y. S. Chauhan, F. Krummenacher, C. Anghel, R. Gillon, B. Bakeroot, M. Declercq, and A. M. Ionescu, "Analysis and Modeling of Lateral Non-Uniform Doping in High-Voltage MOSFETs," in *IEEE International Electron Devices Meeting*, Dec. 2006, pp. 8.3.1 – 8.3.4.

[30] Y. S. Chauhan, F. Krummenacher, R. Gillon, B. Bakeroot, M. Declercq, and A. M. Ionescu, "Compact Modeling of Lateral Non-uniform doping in High-Voltage MOSFETs," *IEEE Transactions on Electron Devices*, vol. 54, no. 6, pp. 1527–1539, June 2007.

[31] "Hisim-ldmos model," , http://home.hiroshima-u.ac.jp/usdl/HiSIM.html, 2006.

[32] "Model features of hisim-ldmos," , http://www.eigroup.org/cmc/minutes, 2006.

[33] Y. S. Chauhan, R. Gillon, M. Declercq, and A. M. Ionescu, "Impact of Lateral Non-uniform doping and hot carrier degradation on Capacitance behavior of High Voltage MOSFETs," in *IEEE European Solid-State Device Research Conference (ESSDERC)*, Sept. 2007.

[34] Y. S. Chauhan, C. Anghel, F. Krummenacher, R. Gillon, A. Baguenier, B. Desoete, S. Frere, A. M. Ionescu, and M. Declercq, "A Compact DC and AC Model for Circuit Simulation of High Voltage VDMOS Transistor," in *IEEE International Symposium on Quality Electronic Design (ISQED)*, March 2006, pp. 109–114.

[35] Y. S. Chauhan, C. Anghel, F. Krummenacher, A. M. Ionescu, M. Declercq, R. Gillon, S. Frere, and B. Desoete, "A Highly Scalable High Voltage MOSFET Model," in *IEEE European Solid-State Device Research Conference (ESSDERC)*, Sept. 2006, pp. 270 – 273.

[36] Y. S. Chauhan, C. Anghel, F. Krummenacher, C. Maier, R. Gillon, B. Bakeroot, B. Desoete, S. Frere, A. B. Desormeaux, A. Sharma, M. Declercq, and A. M. Ionescu, "Scalable General High Voltage MOSFET Model including Quasi-Saturation and self-heating effect," *Solid State Electronics*, vol. 50, no. 11-12, pp. 1801–1813, 2006.

[37] Y. S. Chauhan, R. Gillon, B. Bakeroot, F. Krummenacher, M. Declercq, and A. M. Ionescu, "An EKV-based High Voltage MOSFET Model with improved mobility and drift model," *Solid State Electronics*, 2007.

[38] Y. S. Chauhan, F. Krummenacher, R. Gillon, B. Bakeroot, M. Declercq, and A. M. Ionescu, "A New Charge based Compact Model for Lateral Asymmetric MOSFET and its application to High Voltage MOSFET Modeling," in *IEEE International Conference on VLSI Design and International Conference on Embedded Systems*, Jan. 2007, pp. 177 – 182.

[39] C. Anghel, Y. S. Chauhan, N. Hefyene, and A. Ionescu, "A physical analysis of HV MOSFET capacitance behaviour," in *IEEE International Symposium on Industrial Electronics (ISIE)*, vol. 2, June 2005, pp. 473 – 477.

[40] A. Aarts, R. van der Hout, J. Paasschens, A. Scholten, M. Willemsen, and D. Klaassen, "New fundamental insights into capacitance modeling of laterally nonuniform MOS devices," *IEEE Transactions Electron Devices*, vol. 53, no. 2, pp. 270 – 278, Feb. 2006.

[41] A. S. Roy, Y. S. Chauhan, C. Enz, J.-M. Sallese, A. M. Ionescu, and M. Declercq, "Partitioning Scheme in Lateral Asymmetric MOST," in *IEEE European Solid-State Device Research Conference*, Sept. 2006, pp. 307–310.

[42] A. S. Roy, C. C. Enz, and J.-M. Sallese, "Drain-Source Partitioning in MOSFET," *IEEE Transactions on Electron Devices*, June 2007.

[43] A. S. Roy, Y. S. Chauhan, C. Enz, and J.-M. Sallese, "Noise modeling in lateral asymmetric MOSFET," in *IEEE International Electron Devices Meeting (IEDM)*, Dec. 2006, pp. 191– 194.

Chapter 2

DC and AC behavior of High-Voltage MOSFETs

The interest in the high-voltage (HV) MOS devices has dramatically increased as these devices were integrated with the low power modules in MOS technology [1, 2, 3, 4, 5]. Today, HV-MOS devices are extensively used in all kinds of integrated power circuits, like switch-mode power supplies, motor drivers and, power amplifiers. In addition, LDMOS devices processed in thin-film silicon-on-insulator (SOI) provide a new and attractive technology for smart power integrated circuits in consumer and automotive applications [6]. The discussion in this chapter will be focused on different HV-MOS architectures and special effects occurring in these devices.

2.1 High Voltage MOSFET architectures

There are three different types of high-voltage devices, normally used with CMOS technology. These are Drain-Extended MOSFET [4, 5, 7, 8], Lateral double-diffused MOSFET [9, 10, 11] and Vertical double-diffused MOSFET [12, 13]. Only N-channel devices are considered here but all of them have their P-channel counterparts.

2.1.1 Drain-Extended MOSFET (DEMOS)

Modern digital VLSI circuits are presently operating at the voltage levels of 1.8 V and below. However, circuit requirements often call for design and interface with other circuits operating at 3.3/5.0 V or even higher. Example circuits are input/output interface circuits with various off-chip system components, such as power management switches that regulate power from battery or system supplies, analog input circuits conditioning transducer signals, or output analog drive functions for speakers or other actuators. System designers increasingly want all of these functions in a monolithic IC to decrease system size and increase reliability. One solution to this problem of two voltage levels on an integrated circuit is to use two gate oxides and two sets of lightly-doped drain (LDD) implants [4], but this method increases the process complexity and cost. The alternate solution is to use drain extended (DE) MOS transistors [7, 8] that can operate at much higher drain voltages without significant loss of performance and without added

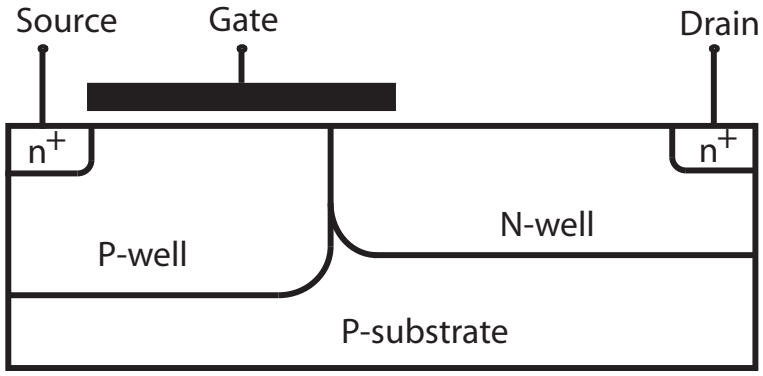


Figure 2.1: Schematic representation of the Drain-Extended MOSFET (DEMOS).

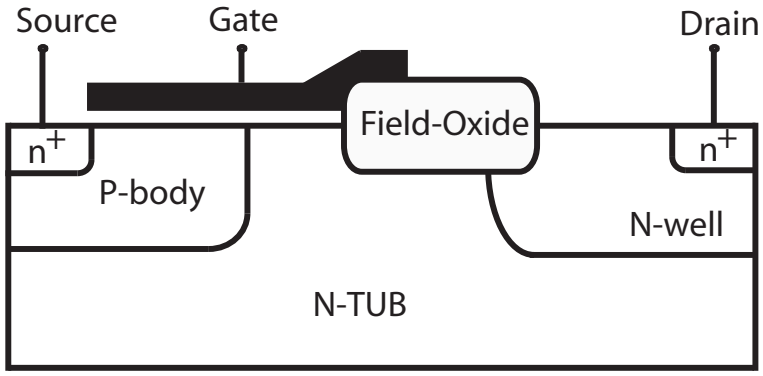


Figure 2.2: Schematic representation of the Lateral double-Diffused MOSFET (LDMOS).

process complexity. Another solution to this problem of two voltage levels on an integrated circuit that is widely used is circuit techniques such as cascading low-voltage transistors. This approach adds considerable circuit complexity and uses more power to maintain intermediate voltages for the gate drive. The use of DEMOS instead of cascaded circuits or other circuit methods offers significant die size area and power savings. It is well known that a LDD extension increases the drain breakdown voltage by reducing the electric field under the gate at the drain end of the transistor. The difficulty here has to do with achieving the goal with a higher than the very thin 4 nm oxides can normally withstand, without the luxury of a LOCOS oxide used in conventional DE style devices for the poly to terminate on. A typical twin well CMOS process, that uses p-substrate wafers, allows DE MOS transistors to be built with the n-well as the NMOS drain extension. Fig. 2.1 shows the schematic representation of N-type DEMOS device. These devices are generally used for 5V operation range especially as in input/output interfaces.

2.1.2 Lateral double-Diffused MOSFET (LDMOS)

Due to the inherent limitations of CMOS technology, DEMOS device characteristics, especially avalanche breakdown and on-resistance, are highly dependent on the n-well doping profile and surface concentration. As CMOS technology is maturing in deep-submicron lithography, other approaches were investigated in order to make available high voltage devices with

improved characteristics. The LDMOS device architecture, which actually originated from DEMOS/LDD-MOS, has much higher breakdown voltage than DEMOS architectures. Fig. 2.2 shows the schematic representation of N-type LDMOS device. The LDMOS devices are useful in high-voltage switching because of their switching speeds and relative simplicity in processing [14]. There are many variations of LDMOS devices [9, 10, 11, 15]. The device shown in Fig. 2.2 is generally used for 20-100V application e.g switch-mode power supplies and power amplifiers etc. The channel in the device is created using double diffused process and thus it has lateral non-uniform doping. The effective gate length is shorter than the physical length of the gate electrode. The drift region is lightly doped N-type whose length varies with increasing voltage blocking capability in the drain side. The maximum drain-source voltage, that can be applied, is determined by the breakdown voltage of the p-n junction, which is limited by the n layer doping, thickness and field crowding at the junction edge.

The electric field in the LDMOS near the silicon surface is considerably lower than in the conventional MOS or DEMOS. However, the maximum field still remains on the surface and avalanche breakdown may occur there [16]. The surface electric field can be reduced significantly by the use of thick oxide (as shown in Fig. 2.2) or field plate as the maximum field is now located inside the bulk. To reduce the on-resistance in LDMOS (with field plate), the length of the field plate should be as small as possible. The effect of field plate on LDMOS characteristics e.g. breakdown voltage, quasi-saturation effect has been studied in the literature in detail [17, 18, 19, 20, 21, 22]. The on-resistance of the LDMOS can also be decreased by using the ion-implantation in the drift region [23]. The field plate also shields the gate from the drain potential, thus minimizing the feedback (drain-to-gate) capacitance, which means improvement of RF signal gain. The p-n junction and the field plate form a fairly uniform field between gate and the drain, thus giving better breakdown voltage.

The LDMOS transistors fare much better at higher frequencies compared to their vertical counterpart (VDMOS) devices. The LDMOS transistors with frequencies more than 2.7GHz are already available in the market. Freescale has recently announced 3.8GHz high power LDMOS for coming WIMAX applications [24]. Since in the LDMOS design, the gate, source and drain are all on the top surface, chip size grows rapidly for high voltage handling capability above 200V.

2.1.3 Vertical double-Diffused MOSFET (VDMOS)

The growing chip size problem for higher operating voltages is addressed by the VDMOS transistor technology [25]. Fig. 2.3 shows the schematic representation of N-type VDMOS device [12, 13]. Since these devices have the drain at the back surface, a variety of junction edge termination schemes can be utilized at the perimeter of the die. However, the channel region itself is on the top surface and thus the current flow is lateral through the channel and vertical through the lightly doped drift. The channel in the device is created using double diffused process and thus it has lateral non-uniform doping. The effect of lateral non-uniform doping and lightly doped drift region on device characteristics is explained in the next section. The VDMOS design sacrifices speed for lower on-resistance and denser high-voltage layout due to large gate/drift overlap. A lower on-resistance than VDMOS is produced in VVMOS devices with similar speed as VDMOS. High speed Vertical V-groove MOS (VVMOS) devices, on the other hand, minimize gate-drain overlap at the cost of an on-resistance increase [26].

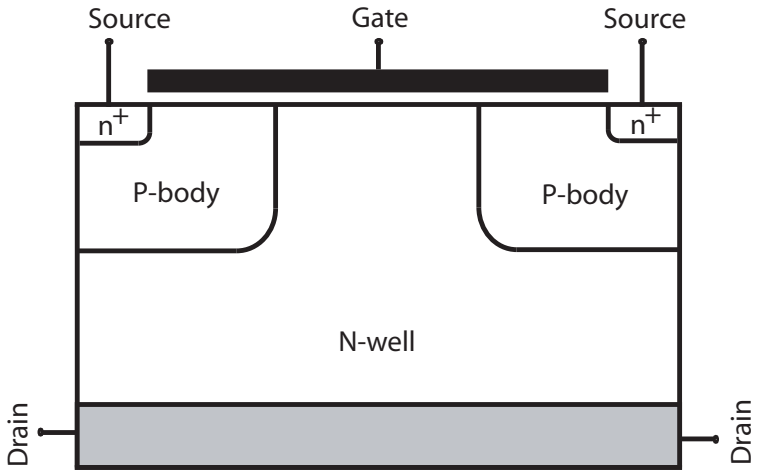


Figure 2.3: Schematic representation of the Vertical double-Diffused MOSFET (VDMOS).

2.2 DC behavior of HV-MOSFETs

The high voltage devices show some special effects due to high electric field inside the device e.g. self-heating, quasi-saturation and impact ionization effects. In fact, some of these effects (self-heating and impact ionization) are also visible in low voltage MOSFETs as electric field in these devices also becomes quite high as channel length is decreased. Even though above mentioned effects arise due to high electric fields in the device, some other special effects are also observed due to different device processes in these devices compared to conventional MOSFETs. One of the major difference in terms of device process is the lateral non-uniform doping in the channel and drift region in the drain side of HV devices. Here we will discuss the physical origin of these effects and their impact on device characteristics.

2.2.1 Quasi-Saturation Effect

The quasi-saturation effect [27, 28, 29, 30, 31] is one of the unique effect observed in HV devices other than bipolar devices [32, 33, 34, 35, 36, 37]. To explain the quasi-saturation effect, first let's discuss the saturation mechanisms in HV devices [38] using output characteristics of VDMOS transistor shown in Fig. 2.4. The current saturation on $I_{DS} - V_{DS}$ characteristics can occur due to following three mechanisms:

(a) Pinch-off in the channel: For a fixed gate voltage, if drain voltage is increased, the channel gets depleted and current saturates. This effect is called pinch-off and it is also the normal saturation mechanism in long channel MOSFETs. In HV devices, the channel pinch-off is generally observed at low V_{GS} (see $V_{GS} = 1V$ curve in Fig. 2.4).

(b) Velocity saturation in the channel: If the lateral electric field in the channel is more than certain limit called as critical field, the velocity of the electrons get saturated and thus there will be no further increase in the current for any further increase in the drain voltage. This effect is called velocity saturation, which is quite common phenomenon in short channel MOSFETs. In HV devices, this effect is generally observed for medium to high V_{GS} (see $I_{DS} - V_{DS}$ curves for $V_{GS} = 1.5, 2, 2.5, 3V$ at V_{DS}=30V in Fig. 2.4). A simple way to see this effect is that when intrinsic MOS is velocity saturated, the output characteristics become equidistant for equal

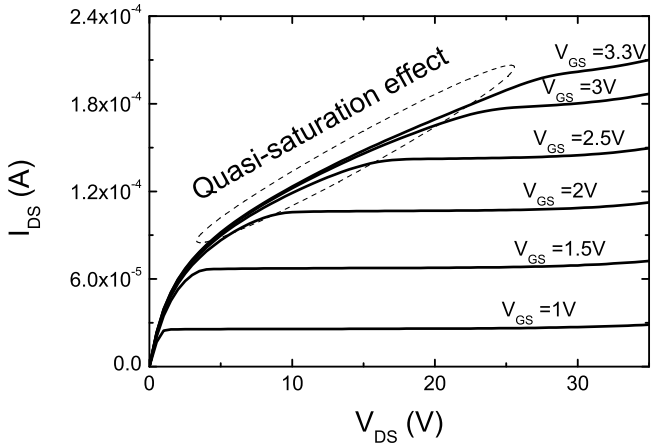


Figure 2.4: I_{DS} vs. V_{DS} from device simulation of 50V VDMOS transistor. The quasi-saturation effect is evident at higher V_{GS} for this device.

increase in V_{GS}.

(c) Velocity saturation in the drift region: Another saturation mechanism can occur due to velocity saturation in the drift while intrinsic MOS is still not saturated. Actually this cannot be called saturation as current does not get saturated. If drift is velocity saturated and intrinsic MOS is in linear region, the increase in V_{GS} does not increase current level significantly and gate bias has no or little effect (see $V_{GS} = 2, 2.5, 3, 3.3V$ in Fig. 2.4). This effect is called quasi-saturation, which is generally observed at high V_{GS}.

Note that all or any two of the three effects described above may superimpose with each other and, sometimes, they may not be separable from each other.

The quasi-saturation effect can be reduced by reducing the resistivity of the drift region and parasitic JFET in VDMOS transistor [27]. The reduction in the quasi-saturation effect increases the current carrying capability of the devices and decreases the on-resistance. One possible method of achieving this is to exploit the trench technology [39], which allows the gate to be extended down into the intercell region. Even though it reduces the quasi-saturation effect, it introduces a corner in the trench which affects the blocking capability of the device. Another method is to use the ion-implantation into the JFET structure of VDMOS, which reduces the quasi-saturation effect with little change in the blocking capability [27].

2.2.2 Self-Heating Effect

The self-heating effect (SHE) [40, 41, 42, 43, 44, 45, 46, 47] represents the heating of the device due to its internal power dissipation. This effect appears, when high levels of power are attained in the device. The dissipated heat leads to an increase in the internal temperature of the device and modifies the $I - V$ characteristics. Fig. 2.5 shows the $I_{DS} - V_{DS}$ characteristics of a 40V LDMOS transistor. The decrease in the current with increasing V_{DS} is caused by the self heating effect. As V_{DS} increases, the current starts rising. The increase in the current (I_{DS}) as well as voltage across the device (V_{DS}) increase the power dissipation ($I_{DS}V_{DS}$) inside the device. As

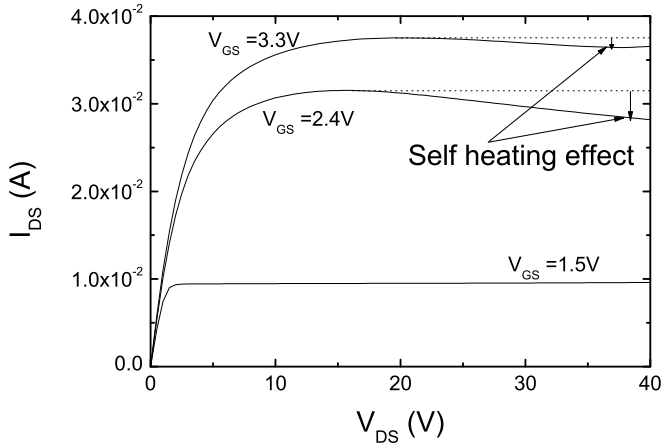


Figure 2.5: Measured I_{DS} vs. V_{DS} of 40V LDMOS transistor. The decrease in the current with increasing V_{DS} is due to self heating effect.

discussed above, the increase in power dissipation increases temperature which affects other transistor parameters (e.g. mobility, threshold voltage etc.). The rise in temperature decreases mobility due to scattering which in turn decreases the current showing negative resistance on output characteristics.

The internal temperature increase due to self heating effect influences the device characteristics mainly by affecting the mobility, threshold voltage and velocity saturation. In the literature, this effect was mainly studied on the SOI devices and the proposed models for SHE are distributed or non-distributed models. As expected, better accuracy is obtained from distributed models, which offer a larger flexibility for the current simulation. Still, the clear advantage of the non-distributed models over the distributed ones is the parameter extraction procedure, as non-distributed approach offers a simple and efficient representation of the problem. The detailed discussion of self-heating effect and its modeling has been covered in [47] and also in section 3.4.2 of chapter 3.

2.2.3 Impact Ionization Effect

Before discussing the impact ionization effect is HVMOS, lets review this effect for conventional low voltage MOSFETs [48].

The increase in the V_{DS} in the MOSFET increases the longitudinal electric field in the channel increasing from source to drain. For abrupt source and drain junctions, the peak field is at the drain-to-channel junction, and its value depends on V_{DS} and channel length L. When carriers move in the fields that exceed the value of the onset of velocity saturation, they continue to acquire kinetic energy from the field but their velocity is randomized by the excessive collisions such that their velocity along the field direction no longer increases but their kinetic energy does. Depending on the statistics of scattering, a small fraction of the overall carrier population acquires a significant amount of energy, and these are called hot carriers. Clearly, the higher the field, the higher the proportion of hot carriers. Generally, in MOSFETs, the high

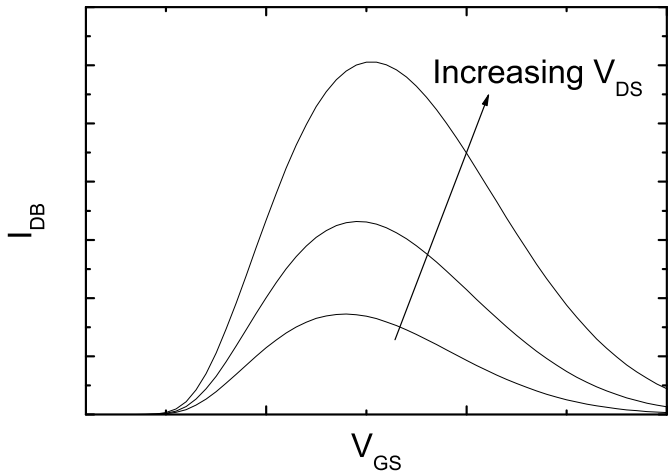


Figure 2.6: Substrate current vs. gate-source voltage, with drain-source voltage as a parameter.

fields are encountered in saturation in the pinchoff region. For large longitudinal electric field, the cool electrons are coming into the pinchoff region and are heated by the field. Some of them acquire enough energy to create impact ionization of silicon atoms, whereby new electrons and holes are created; this effect is also referred to as weak avalanche. The new electrons join the stream of channel electrons and move toward the drain. The normal depletion field in the channel pushes the holes into the substrate, where they give rise to drain-to-substrate current (I_{DB}). This current is proportional to the number of electrons available per unit time, which in turn is proportional to I_{DS}. Also, according to above discussion, I_{DB} is an increasing function of the maximum field at the drain; this field is, in turn, a function of the excess drain voltage (V'_{DS}). Fig. 2.6 shows the typical $I_{DB} - V_{GS}$ curve for MOSFET. For a given V_{DS}, when V_{GS} is increased starting from low values, I_{DS} increases, and thus I_{DB} increases too, according to above discussion. Further increase in V_{GS} increases the saturation voltage significantly, causing a strong decrease in $V_{DS} - V'_{DS}$, and thus in the maximum field at the drain. The maximum I_{DB} is observed, roughly, at $V_{GS} = V_{DS}/2$.

The impact ionization in the HVMOS device has the contributions from both the channel region and the drift region. Fig. 2.7 shows the $I_{DB} - V_{GS}$ curve for LDMOS transistor. At low current, the hot carriers are generated near the channel while at high current levels, hot carriers are generated near the drain end in the drift region. This is why there is an increase in the I_{DB} at higher V_{GS}. The impact ionization in the drift can be reduced with the field plate configuration [49]. The step drift region or deep drift design proposed in the literature also helps in the reduction of hot carriers in the drift region [49].

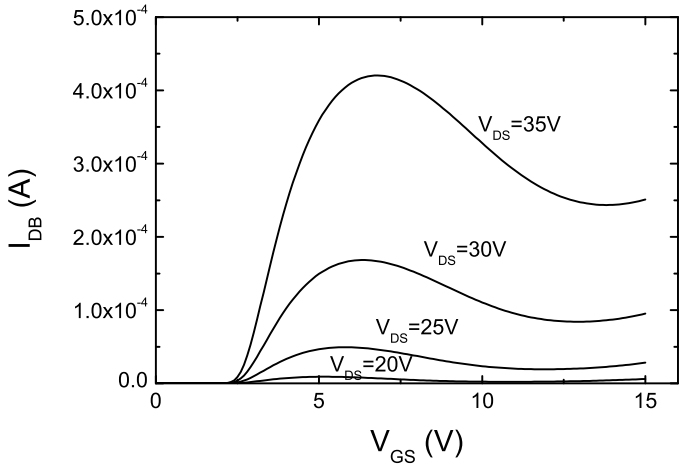


Figure 2.7: Measured substrate current vs. gate-source voltage for 40V LDMOS transistor.

2.3 AC behavior of HV-MOSFETs

The special behavior of HV-MOS e.g. LDMOS, VDMOS capacitances has been under study in research community for many years [50, 51, 52, 53, 54, 55]. In literature, generally the HV-MOS capacitances have been studied together with drift region [52, 53], which makes it difficult to separately understand and analyze the impact of lateral non-uniform doping and drift region. The unique capacitance characteristics of HV-MOS originates from the device architecture of HV-MOS. The major difference between HV-MOS and conventional MOS is the lateral non-uniform doping in the channel and the drift region, which affects the capacitances depending on the bias regime. The unique behavior of C_{GD} in high voltage devices has been analyzed in detail in the literature [50, 51, 53]. Frére et al. [50] showed that the peaks in C_{GD} are actually originating from LAMOS. Liu et al. [53] reproduced the peaks in C_{GD} of VDMOS transistor using small signal analysis. Here, the effect of lateral non-uniform doping and drift region on capacitance characteristics of HV-MOS will be separately analyzed and compared with conventional MOS characteristics [56]. To analyze the capacitance behavior of HV-MOS, we will divide the analysis in two parts - Impact of lateral non-uniform doping and drift region. For this we will have four cases as shown in Fig. 2.8: (1) Conventional MOS with uniform doping in the channel and (2) Lateral Non-uniformly doped or Lateral Asymmetric MOS (LAMOS) with lateral doping gradient in the channel, (3) Conventional MOS with uniform doping in the channel and a drift region to sustain high voltage, and (4) LAMOS with a drift region to sustain high voltage. The intrinsic drain potential in Fig. 2.8(b) will be called V_K, which is the point where channel meets the drift region.

2.3.1 Effect of Lateral Non-uniform doping

Here we will explain, how lateral non-uniform doping affects the small signal capacitance behavior of high-voltage MOSFETs. Fig. 2.8(a) shows the device architecture under study. To see the impact of lateral non-uniform doping on capacitances, let's start with C_{GD} capacitance. Fig.

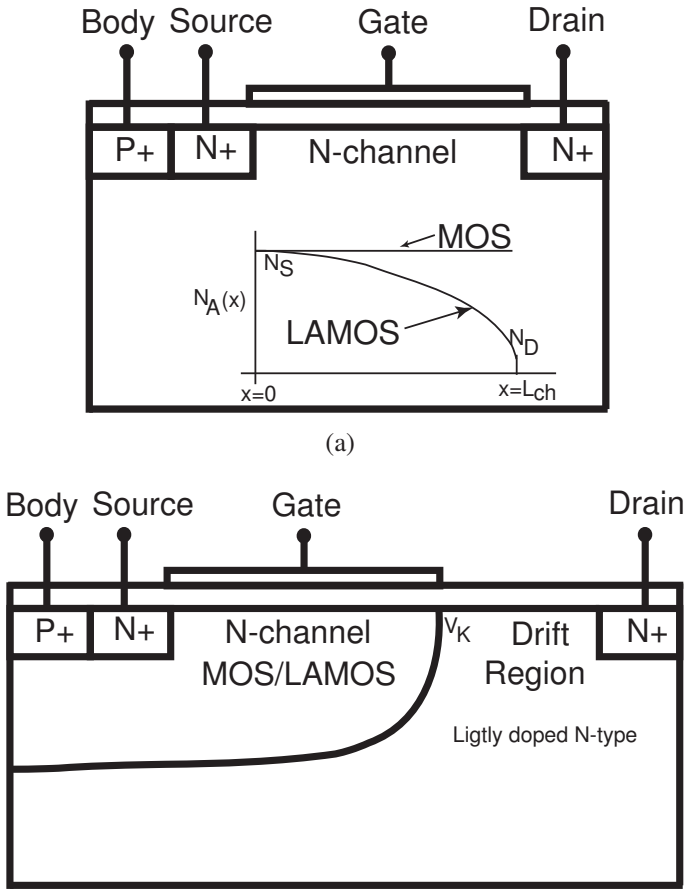


Figure 2.8: Device architectures of (L_{ch}=2μm): (a) Conventional MOSFET with uniform doping and LAMOS with lateral doping gradient in the channel. The lateral doping gradient is approximated by the complementary error function $N_A(x) = N_S.erfc[k_n(\xi)]$ [57, 58, 59], where $\xi = \frac{x}{L_{ch}}$ is the normalized position along the channel, k_n is a parameter representing the doping gradient. The doping level at the source side of the channel (N_S) is highest and decreases towards the drain in the channel region. Higher k_n means sharp decrease in the doping level from source to drain and vice-versa. (b) Conventional MOSFET with uniform doping and LAMOS with lateral doping gradient in the channel and a drift region to sustain high voltage.

2.9 shows the C_{GD} vs. V_{GS} using device simulation for different drain voltages. As expected, the C_{GD} at $V_{DS} = 0$ for conventional MOS stays low values for $V_{GS} < V_T$ (threshold voltage). As V_{GS} starts to increase beyond V_T, the C_{GD} increases sharply and saturates to $\frac{1}{2}WLC_{OX}$. The situation is completely different for LAMOS. Due to lateral non-uniform doping, the C_{GD} starts increasing as soon as V_{GS} is more than the surface inversion potential at drain side. It means that the inversion at the drain side starts at lower values of V_{GS} than source side because of the lower doping at the drain end compared to source end. As V_{GS} keeps on increasing, the inversion in the channel propagates from drain towards source and C_{GD} keeps on rising. Once V_{GS} is greater than the surface inversion potential at source side (or V_T of LAMOS), the C_{GD} starts to fall [51]. This can be explained by the fact the rise in inversion charge is exponential for $V_{GS} < V_T$ and after that rise gets slower ultimately becoming linear function of V_{GS}. In strong

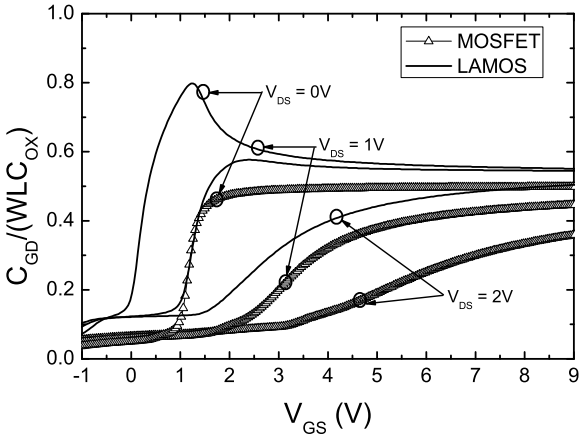


Figure 2.9: The gate-to-drain capacitance C_{GD} vs. V_{GS} for V_{DS} =0,1 and 2V. The lateral non-uniform doping in LAMOS produces peaks in C_{GD} capacitances at low drain bias.

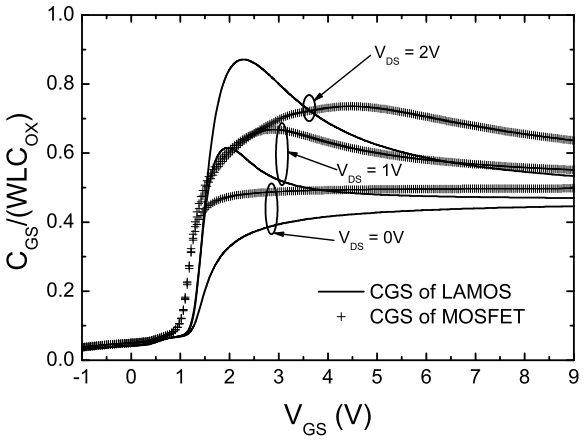


Figure 2.10: The gate-to-source capacitance C_{GS} vs. V_{GS} for V_{DS} =0,1 and 2V. The lateral non-uniform doping in LAMOS produces peaks in C_{GS} capacitances around $V_{GS} = V_T$.

inversion ($V_{GS} >> V_T$), the C_{GD} saturates to some value equal to or higher than $\frac{1}{2}WLC_{OX}$ depending on the doping gradient in the channel [58, 59]. The impact of different doping gradients on capacitances will be explained later in this section. Increasing drain voltage reduces the peak due to depletion at drain side. For sufficiently high values of drain voltages, there may not exist any peak in C_{GD} (e.g. $V_{DS} \geq 2V$ in Fig. 2.9).

Another interesting property of LAMOS capacitances is seen on C_{GS} and C_{GG} behavior as shown in Fig. 2.10 and Fig. 2.11. The C_{GS} at $V_{DS} = 0$ is similar to MOSFET (except lower values due to low doping in the drain side), where the increase in C_{GS} occurs when channel gets inverted ($V_{GS} \geq V_T$). The situation is quite different for $V_{DS} > 0$. For $V_{DS} < V_{GS} - V_{TD}$ (threshold voltage corresponding to the doping at drain), the C_{GS} is slightly higher than its value at $V_{DS} = 0$ and behaves similar to the MOS capacitance. But if $V_{DS} > V_{GS} - V_{TD}$, the

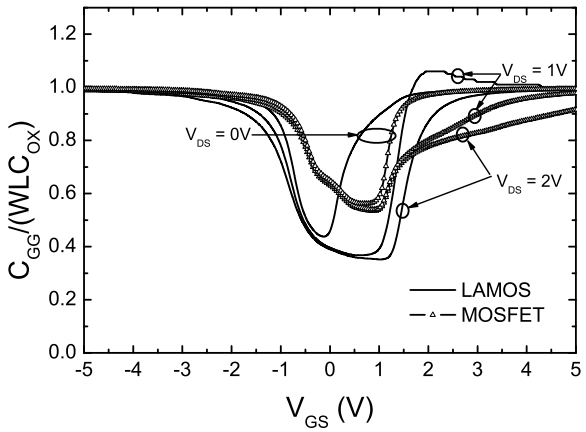


Figure 2.11: The gate-to-gate capacitance C_{GG} vs. V_{GS} for V_{DS} =0,1 and 2V. The lateral non-uniform doping in LAMOS produces peaks in C_{GG} capacitances, when V_{GS} is around threshold voltage for small nonzero V_{DS}.

drain end is depleted. For these drain voltages, as V_{GS} increases, there will be small increase in the channel charge from drain side until $V_{GS} < V_T$. At $V_{GS} = V_T$, there is sudden flow of large amount of charges from source end (the small signal resistance seen from any point in the channel towards the drain will be higher than towards the source and charges choose the least resistive path, which is source side in this case) and whole of the channel gets filled up by these charges. This sudden rise in the charge from source side gives rise to increased peaks in C_{GS} for higher drain voltages as shown in Fig. 2.10.

It is interesting to note that C_{GG} also has small peaks for V_{DS} =1V as shown in Fig. 2.11, which was also shown in [60] for nonzero small V_{DS}. These peaks in C_{GG} can be explained by the fact that for $V_{GS} \leq V_T$, the source end of the channel is still in weak inversion while drain end is in depletion. Once V_{GS} reaches close the V_T, there will be sudden flow of charge from source side giving sharp increase in C_{GG}. This is not the case with the C_{GG} of conventional MOS, where continuous supply of charge is maintained from source side due to uniform doping. Also note that for low drain voltages, there will be large supply in the charge from drain end also once it comes out of depletion which again helps in increasing the total channel charge. Note that the peak vanishes as V_{GS} increases significantly above threshold voltage as now inversion charge is being supplied from both source and drain, and now gate charge is a linear function of gate voltage. For high values of drain voltages, no peak is observed, as charges entering from source end also contributes in removing the depletion at the drain side. Hence, the peak in C_{GG} occurs for small nonzero values of V_{DS}, when V_{GS} is around threshold voltage (source end entering into strong inversion from weak/moderate inversion). Another note on the C_{GG} of LAMOS is that the dip (lowest value) is lower compared to C_{GG} of MOS. This is due to the lower doping in the drain side which produces sharper and lower dip on C_{GG}. This can also be analyzed using segmentation approach, where LAMOS channel can be divided in several smaller channel length MOS with uniform doping in each channel but varying across different MOS giving equivalent non-uniform doping also called graded channel approach [60, 61].

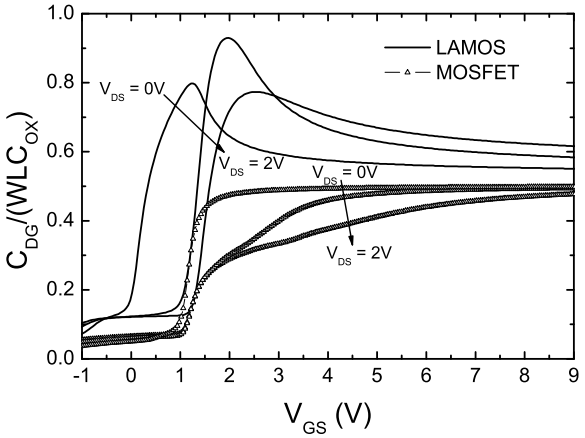
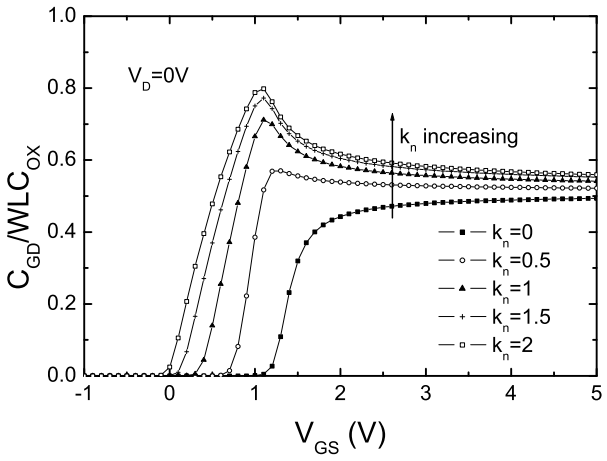


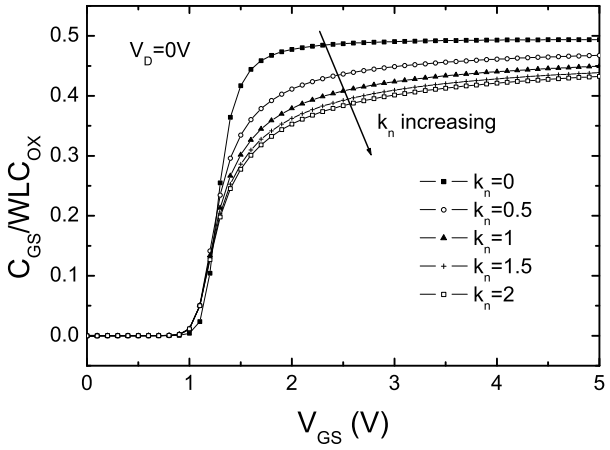
Figure 2.12: The drain-to-gate capacitance C_{DG} vs. V_{GS} for V_{DS} =0,1 and 2V. The lateral non-uniform doping in LAMOS produces peaks in C_{DG} capacitances. The peaks in the C_{DG} can be higher than WLC_{OX} depending on the doping profile and drain voltage [58]. The bias dependent partitioning scheme [62, 63] also explain these peaks.

The behavior of C_{DG} capacitances is also quite different for LAMOS [60, 64, 62, 63] as shown in Fig. 2.12. Similar to other capacitances of LAMOS, peaks are also observed on C_{DG}. The peak in C_{DG} at $V_{DS} = 0$ can be explained similar to the peak in C_{GD} at $V_{DS} = 0$. As gate voltage increases, the drain end of the channel gets inverted and C_{DG} starts increasing till source end get inverted and after that it decreases and saturates. In fact C_{GD} and C_{DG} are exactly same for $V_{DS} = 0$. But for nonzero drain voltages, C_{DG} has totally different behavior than C_{GD}. At $V_{DS} = 1V$, note that the peak increases because a change in gate voltage induces a change in the channel potential (the perturbed channel potential becomes negative), which in turn causes a change in charge distribution and the combined effect increases the peak [62, 63]. To understand why perturbed channel potential can become negative to increase the small signal charge, consider the situation, when the source end is weakly inverted and drain end is strongly inverted. In this case the transistor can be thought of a series combination of two transistors with different threshold voltages, where the one near the source is weakly inverted and near the drain end is strongly inverted. Now let Q_S and Q_D be the charge at the source and drain end of the strongly inverted transistor. The current flowing through the transistor is proportional to $Q_S^2 - Q_D^2$ [62, 63, 65, 66]. The weakly inverted transistor in series forces current to be very small, therefore $Q_S^2 \approx Q_D^2$. Now as gate voltage increases both Q_S and QD will change and we have $\delta Q_S \cdot Q_S \approx \delta Q_D \cdot Q_D$. As drain end is kept at a fixed channel potential and is in strong inversion $\delta Q_D \approx C_{OX}\delta V_{GS}$. So we have $\delta Q_S/\delta V_{GS} = (Q_D/Q_S)C_{OX}$. As $Q_D > Q_S$ in this situation (because the drain end has lower doping), we have $\delta Q_S/\delta V_{GS} > C_{OX}$, which is only possible if the channel potential goes negative and aids the gate voltage. Depending on the doping profile in the channel and drain voltage, the peak in C_{DG} may even increase above WLC_{OX} in presence of a gate voltage [62, 58].

The above analysis was made using single value of doping gradient (k_n) in the channel of LAMOS. If the value of doping gradient (k_n) is increased giving sharper doping profile



(a)



(b)

Figure 2.13: Effect of different doping gradients (k_n) on LAMOS: (a) Normalized C_{GD} and (b) normalized C_{GS} at V_{DS}=0. Note that the peak in C_{GD} increases, while C_{GS} in strong inversion decreases with increase in doping gradient. The k_n=0 corresponds to uniformly doped MOSFET.

in the channel, the peaks on C_{GD} increases and value of C_{GS} decreases in strong inversion, while the rising slope on both capacitances decreases [58] as shown in Fig. 2.13(a) and (b). The lateral doping gradient in the channel also affects DC characteristics of LAMOS. Higher doping gradient increases the saturation voltage and saturation current on the output characteristics as shown in Fig. 2.14. The prolonged linear region in the output characteristics and peaks/slopes on capacitances can be explained by the fact that doping gradient changes the surface potential required for the inversion across the channel decreasing from source to drain.

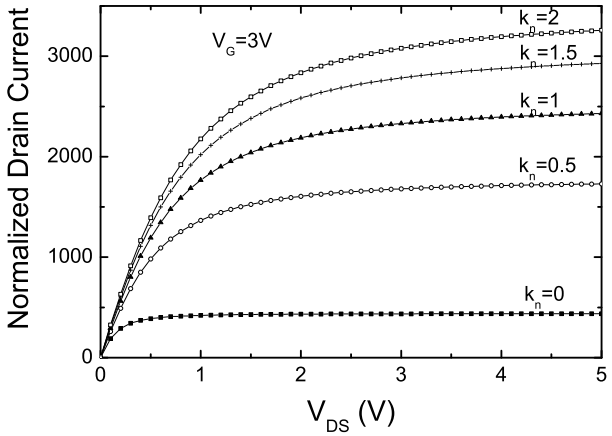


Figure 2.14: Effect of different doping gradients (k_n) on LAMOS: Normalized drain current $\frac{I_D}{2n_q\mu_0\frac{W}{L}C_{OX}U_T^2}$ at V_{GS}=3V (strong inversion). Note that the linear region extends, current as well as saturation voltage increases and R_{ON} decreases with increase in doping gradient. The k_n=0 corresponds to uniformly doped MOSFET.

2.3.2 Effect of drift region

Fig. 2.8(b) shows the device architecture under study. The effect of the drift region (without any gate overlap) is to lower the C_{GD} capacitance value in strong inversion (see LAMOS with drift region in Fig. 2.15). It is interesting to note that the C_{GD} for a conventional MOS with drift (e.g. DEMOS or LDD-MOS transistor) also shows decrease of capacitance at higher gate bias, but it should not be confused as peak in capacitance because it is always less than or equal to $\frac{1}{2}WLC_{OX}$ (see MOS with drift in Fig. 2.15). The rising part of C_{GD} is mainly given by lateral asymmetry in the channel as explained above, while the fall in C_{GD} is heavily affected by the drift region also demonstrated in Fig. 2.15. As mentioned earlier, the lateral non-uniform doping produces peaks in C_{GG} and C_{GS} around threshold voltage. The drift region gives higher peaks and also shifts the position of peaks as shown in Fig. 2.16 and Fig. 2.17 for nonzero V_{DS}. To understand it better, we can write the normalized C_{GG} expression as,

$$\begin{aligned} C_{GG} &= \frac{dQ_G(V_G,V_K,V_S,V_B)}{dV_{GS}} \\ &= \frac{\partial Q_G(V_G,V_K,V_S,V_B)}{\partial V_G} + \frac{\partial Q_G(V_{GS},V_K,V_S,V_B)}{\partial V_K}\frac{dV_K}{dV_G} \\ &= C_{GG(LAMOS)} - C_{GD(LAMOS)}\frac{dV_K}{dV_G} \end{aligned} \tag{2.1}$$

Here V_K is the intrinsic drain potential (the point where LAMOS meets drift region in high voltage devices) as shown in Fig. 2.8. If there is no drift region, then $V_K = V_D$ and second term in (4.26) vanishes as $\frac{dV_K}{dV_G} = 0$. In the presence of the drift region, V_K is not fixed and will vary to maintain a constant current from drain to source. If there is a slight positive change ∂V_G in V_G, the LAMOS current will increase. Now to increase the current in the drift region to the level of LAMOS, V_K should decrease as V_D is fixed. Larger the drift resistance, larger

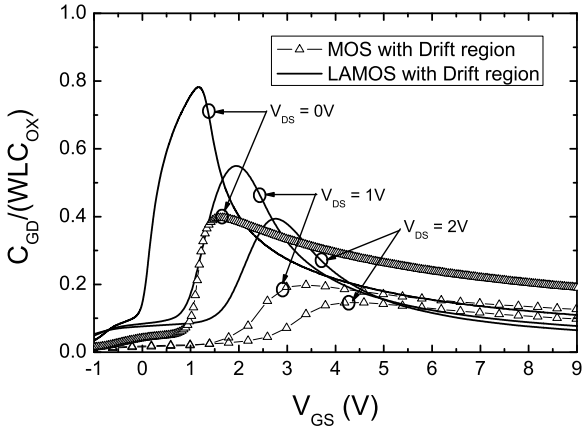


Figure 2.15: The gate-to-drain capacitance C_{GD} vs. V_{GS} for V_{DS} =0,1 and 2V. The value of C_{GD} is lowered due to drift region. Higher the value of drift resistance (quasi-saturation or current crowding effect), sharper will be the decrease in C_{GD} capacitance.

should be the drop in V_K. Thus $\frac{dV_K}{dV_G}$ will be negative for positive values of ∂V_G and from (4.26), it is evident that C_{GG} of any high voltage device would be larger than $C_{GG(LAMOS)}$ and will increase with higher drift resistance for nonzero V_{DS}. From modeling point of view, a good model for HV-MOS needs both excellent modeling of intrinsic MOS channel (which provides $C_{GG(LAMOS)}$) and drift region (which dictates derivative of V_K) [58, 54, 67].

Similarly C_{GS} can be expressed as,

$$\begin{aligned} C_{GS} &= -\frac{Q_G(V_G, V_K, V_S, V_B)}{dV_S} \\ &= -\frac{\partial Q_G(V_G, V_K, V_S, V_B)}{\partial V_S} - \frac{\partial Q_G(V_G, V_K, V_S, V_B)}{\partial V_K}\frac{dV_K}{dV_S} \\ &= C_{GS(LAMOS)} + C_{GD(LAMOS)}\frac{dV_K}{dV_S} \end{aligned} \tag{2.2}$$

If there is a slight positive change ∂V_S in V_S, the LAMOS current will decrease. Now to decrease the current in the drift region to the level of LAMOS, V_K should increase as V_D is fixed. Larger the drift resistance, larger should be the increase in V_K. Thus $\frac{dV_K}{dV_{GS}}$ will be positive for positive values of ∂V_S and from (2.2), it is evident that C_{GS} of any high voltage device would be larger than $C_{GS(LAMOS)}$ and will increase with higher drift resistance for nonzero V_{DS}.

Above analysis of capacitances did not include the drift region with gate overlap. The effect of gate overlap in the drift region is to increase the capacitances as the total gate charge increases due to the accumulation of electrons in the overlap region for positive gate voltages or vice-versa. There is also diffusion of charges from gate overlapped drift region into LAMOS in HV-MOS, which again helps in increasing the total gate charge [52].

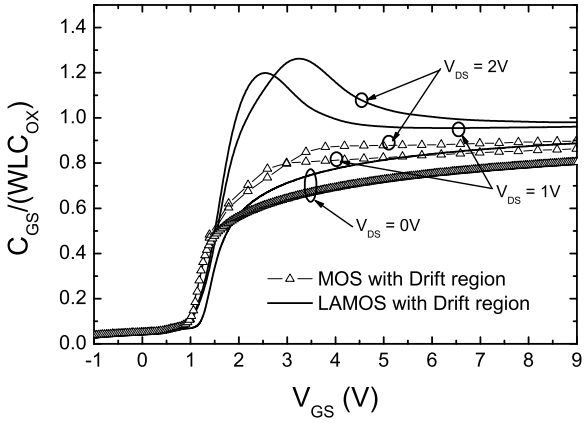


Figure 2.16: The gate-to-source capacitance C_{GS} vs. V_{GS} for V_{DS} =0,1 and 2V. The peak and value of C_{GS} is increased due to drift region. Higher the value of drift resistance (quasi-saturation or current crowding effect), sharper will be the increase in C_{GS} capacitance.

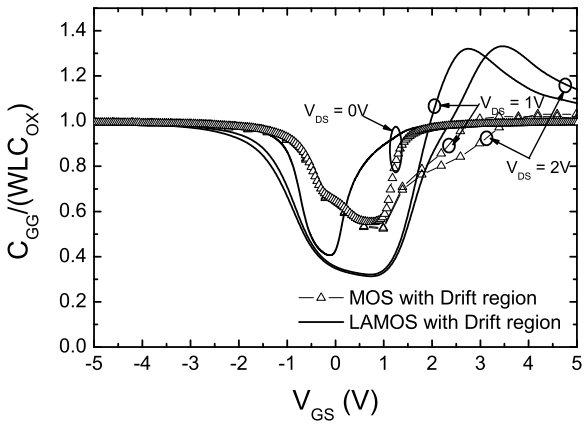


Figure 2.17: The gate-to-gate capacitance C_{GS} vs. V_{GS} for V_{DS} =0,1 and 2V. The peaks in C_{GG} is increased due to drift region. Higher the value of drift resistance (quasi-saturation or current crowding effect), sharper will be thepeaks in C_{GG} capacitance.

2.4 Conclusion

In this chapter, an overview of high voltage MOSFET architecture was presented. Three main device architectures of high-voltage devices, Drain-Extended MOSFET, Lateral double-diffused MOSFET and Vertical double-diffused MOSFET, normally used with CMOS technology, were discussed. Several advantages and disadvantages of these architectures were also pointed out. Due to several different types of asymmetric architectures, there has been no single model for these devices.

The important DC effects quasi-saturation, self-heating and impact ionization were described. The quasi-saturation effect, which originates due to velocity saturation or current crowding in the drift region has been a major problem in these devices as it gives high on resistance, which is not desired. Also modeling of this effect has been a great challenge. The self-heating effect is another unwanted effect observed in high voltage devices. The high voltage and current gives rise to high power dissipation, which in turn increases the temperature inside the device. The rise in temperature severely affects the device characteristics giving rise to negative resistance on output characteristics. The modeling of this effect has also been a problem in the past. Even today, there are no compact expressions to describe this effect in high voltage devices. The impact ionization effect occurs due to high field in the device. The impact ionization in the high voltage devices occurs at both places, the intrinsic MOS and drift region. The impact ionization in the intrinsic MOS region occurs at low to medium V_{GS} for certain V_{DS}, while impact ionization in the drift region dominates at higher gate voltages. Also the impact ionization current in the drift region does not decrease with increase in gate voltage, which is not the case in conventional MOSFET, where it decreases after giving a peak in the drain current.

An in depth study of high voltage MOSFET capacitance was carried out by separately analyzing the impact of lateral non-uniform doping and drift region. It was demonstrated that the capacitance peaks in high voltage MOSFET at low gate bias are dominated by lateral non-uniform doping while at higher gate bias, the decrease in capacitances is affected by both the lateral non-uniform doping as well as the drift region. One of the major capacitance, which gets affected by lateral non-uniform doping is the C_{GD}. The early rise in C_{GD} was explained by the early inversion at the drain side which then propagates towards source with increase in the gate voltage. It was demonstrated that the drift resistance will always decrease the capacitance value for positive gate bias in N-type DMOS and for negative gate bias in P-type DMOS. The effect of gate overlap in the drift region is to increase the capacitance due to accumulation charge for positive gate bias for N-type DMOS or vice-versa. From this study, it is clear that an accurate high voltage MOS model needs to correctly model the lateral non-uniform doping (which has been a great challenge) and drift region behavior especially for RF LDMOS, where small signal capacitances plays the main role in device performance.

Bibliography

[1] G. Dolny, O. S. Jr., B. Goldsmith, and L. Goodman, "Enhanced CMOS for analog-digital power IC applications," *IEEE Transactions on Electron Devices*, vol. 33, no. 12, pp. 1985–1991, 1986.

[2] E. Habekotti, B. Hoefflinger, W. Renker, and G. Zimmer, "A coplanar CMOS power switch," *IEEE Journal of Solid-state Circuirs*, vol. 16, no. 3, pp. 212–225, 1981.

[3] S. A. Buhler, D. L. Heald, R. R. Ronan, T. Gannon, and P. Elkins, "Integrated high voltage/low voltage MOS devices," in *IEEE International Electron Devices Meeting (IEDM)*, 1981, pp. 259–262.

[4] P. M. Santos, A. P. Casimiro, M. Lanca, and M. I. C. Simas, "High-voltage solutions in CMOS technology," *Microelectronics Journal*, vol. 33, no. 8, pp. 609–617, 2002.

[5] P. M. Santos, H. Quaresma, A. P. Silva, and M. Lanca, "High-voltage NMOS design in fully implanted twin-well CMOS," *Microelectronics Journal*, vol. 35, no. 9, pp. 723–730, 2004.

[6] J. A. van der Pol, A. Ludikhuize, H. Huizing, B. van Velzen, R. Hueting, J. Mom, G. van Lijnschoten, G. Hessels, E. Hooghoudt, R. van Huizen, M. Swanenberg, J. Egbers, F. van den Elshout, J. Koning, H. Schligtenhorst, and J. Soeteman, "A-BCD: An economic 100 V RESURF silicon-on-insulator BCD technology for consumer and automotive applications," in *IEEE International Symposium on Power Semiconductor Devices and ICs*, June 2000, p. 327330.

[7] J. Mitros, C. Y. Tsai, H. Shichijo, K. Kunz, A. Morton, D. Goodpaster, D. Mosher, and T. Efland, "High-Voltage Drain Extended MOS Transistors for 0.18 um Logic CMOS Process," in *IEEE European Solid-State Device Research Conference (ESSDERC)*, 2000, pp. 376– 379.

[8] J. Mitros, C.-Y. Tsai, H. Shichijo, M. Kunz, A. Morton, D. Goodpaster, D. Mosher, and T. Efland, "High-voltage drain extended MOS transistors for 0.18 μ m logic CMOS process," *IEEE Transactions on Electron Devices*, vol. 48, no. 8, pp. 1751–1755, 2001.

[9] L. Vestling, J. Ankarcrona, and J. Olsson, "Analysis and design of a low-voltage high-frequency LDMOS transistor," *IEEE Transactions on Electron Devices*, vol. 49, no. 6, pp. 976–980, 2002.

[10] J. Kim, S. Kim, J. Koo, and D. Kim, "p-channel LDMOS transistor using new tapered field oxidation technology," *IEE Electronics Letters*, vol. 34, no. 19, pp. 1893–1894, 1998.

[11] P. Santos, V. Costa, M. Gomes, B. Borges, and M. Lanca, "High-voltage LDMOS transistors fully compatible with a deep-submicron 0.35 μ m CMOS process," *Microelectronics Journal*, vol. 38, no. 1, pp. 35–40, 2007.

[12] K. Li, "A novel self aligned VDMOS device," in *IEEE International Conference on Solid-State and Integrated Circuit Technology*, 1995, pp. 479–481.

[13] P. Wilson, "A novel high voltage RF vertical MOSFET for high power applications," in *IEEE International Symposium on Electron Devices for Microwave and Optoelectronic Applications*, 2002, pp. 95– 100.

[14] E. Fong, D. Pitzer, and R. Zeman, "Power DMOS for high-frequency and switching applications," *IEEE Transactions on Electron Devices*, vol. 27, no. 2, pp. 322– 330, Feb. 1980.

[15] G. Cao, S. K. Manhas, E. Narayanan, M. M. D. Souza, and D. Hinchley, "Comparative study of drift region designs in RF LDMOSFETs," *IEEE Transactions on Electron Devices*, vol. 51, no. 8, pp. 1296– 1303, 2004.

[16] I. Yoshida, T. Okabe, M. Katsueda, S. Ochi, and M. Nagata, "Thermal stability and secondary breakdown in planar power MOSFET's," *IEEE Transactions on Electron Devices*, vol. 27, no. 2, pp. 395– 398, Feb. 1980.

[17] S. G. J. C. D. K. L. Liu, "Analytical Model for Surface Electrical Field of Double RESURF LDMOS with Field Plate," in *IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT)*, Oct. 2006, pp. 1324–1326.

[18] A. Shibib, S. Xu, Z. Xie, P. Gammel, M. Mastrapasqua, and I. Kizilyalli, "Control of hot carrier degradation in LDMOS devices by a dummy gate field plate: experimental demonstration," in *IEEE International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, May 2004, pp. 233– 235.

[19] Z. Hossain, T. Ishigwo, L. Tu, H. Corleto, F. Kuramae, and R. Nair, "Field-plate effects on the breakdown voltage of an integrated high-voltage LDMOS transistor," in *IEEE International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, May 2004, pp. 237– 240.

[20] I. Cortes, J. Roig, D. Flores, J. Urresti, S. Hidalgo, and J. Millan, "Degradation analysis in SOI LDMOS transistors with steep retrograde doping profile and source field plate," in *IEEE Spanish Conference on Electron Devices*, Feb. 2005, pp. 91– 96.

[21] M. N. Marbell, S. V. Cherepko, J. C. M. Hwang, M. A. Shibib, and W. R. Curtice, "Modeling and Characterization of Effects of Dummy-Gate Bias on LDMOSFETs," *IEEE Transactions on Electron Devices*, vol. 54, no. 3, pp. 580–588, Mar 2007.

[22] I. Cortes, J. Roig, D. Flores, J. Urresti, S. Hidalgo, and J. Rebollo, "A numerical study of field plate configurations in RF SOI LDMOS transistors," *Solid-State Electronics*, vol. 50, no. 2, pp. 155–163, February 2006.

[23] S. Ochi, T. Okabe, I. Yoshida, K. Yamaguchi, and M. Nagata, "Computer analysis of breakdown mechanism in planar power MOSFET's," *IEEE Transactions on Electron Devices*, vol. 27, no. 2, pp. 399– 400, Feb. 1980.

[24] "Ldmos," , http://www.microwaves101.com/encyclopedia/LDMOS.cfm, 2006.

[25] R. Coen, D. Tsang, and K. Lisiak, "A high-performance planar power MOSFET," *IEEE Transactions on Electron Devices*, vol. 27, no. 2, pp. 340– 343, Feb. 1980.

[26] W. Lane and C. Salama, "Epitaxial VVMOS power transistors," *IEEE Transactions on Electron Devices*, vol. 27, no. 2, pp. 349– 355, Feb. 1980.

[27] Z. M. LI, P. A. MAWBY, and K. BOARD, "A physical insight into the quasi-saturation effect in VDMOS power transistors," *International Journal of Electronics*, vol. 83, no. 1, pp. 13 – 22, July 1997.

[28] J. Rebollo, E. Figueras, J. Milln, E. Lora-Tamayo, and F. Serra-Mestres, "Analysis of the quasi-saturation region of high voltage VDMOS devices," *Solid-State Electronics*, vol. 30, no. 2, pp. 177–180, February 1987.

[29] C.-K. Park and K. Lee, "Experiments and 2D-simulations for quasi-saturation effect in power VDMOS transistors," in *IEEE International Symposium on Power Semiconductor Devices and ICs*, June 1990, pp. 219–224.

[30] M. N. Darwish, "Study of the quasi-saturation effect in VDMOS transistors," *IEEE Transactions on Electron Devices*, vol. 33, no. 11, pp. 1710– 1716, Nov 1986.

[31] K. H. Lou, C. M. Liu, and J. B. Kuo, "Analysis of the quasi-saturation behavior considering the drain-to-source voltage and cell-spacing effects for a vertical DMOS power transistor," *Solid-State Electronics*, vol. 36, no. 1, pp. 85–91, January 1993.

[32] B. Y. Chen and J. B. Kuo, "An accurate knee current model considering quasi-saturation for BJTs operating at high current density," *Solid-State Electronics*, vol. 38, no. 6, pp. 1282–1284, June 1995.

[33] J. S. Yuan and W. R. Eisenstadt, "Circuit modeling of collector current spreading effects in quasi-saturation for advanced bipolar transistors," *Solid-State Electronics*, vol. 31, no. 12, pp. 1725–1731, December 1988.

[34] A. W. Alden and A. R. Boothroyd, "Modelling of VHF and microwave power transistors operating in quasi-saturation," *Solid-State Electronics*, vol. 25, no. 8, pp. 723–731, August 1982.

[35] H. C. de Graaff and R. J. van der Wal, "Measurement of the onset of quasi-saturation in bipolar transistors," *Solid-State Electronics*, vol. 17, no. 11, pp. 1187–1192, Nov 1974.

[36] M. Kumar and K. N. Bhat, "Collector recombination lifetime from the quasi-saturation analysis of high-voltage bipolar transistors," *IEEE Transactions on Electron Devices*, vol. 37, no. 11, pp. 2395–2398, Nov 1990.

[37] S. Roy and M. Kumar, "Enhanced breakdown voltage, diminished quasi-saturation, and self-heating effects in SOI thin-film bipolar transistors for improved reliability: a TCAD simulation study," *IEEE Transactions on Device and Materials Reliability*, vol. 6, no. 2, pp. 306– 314, June 2006.

[38] C. Anghel, N. Hefyene, A. Ionescu, M. Vermandel, B. Bakeroot, J. Doutreloigne, R. Gillon, S. Frere, C. Maier, and Y. Mourier, "Investigations and Physical Modelling of Saturation Effects in Lateral DMOS Transistor Architectures Based on the Concept of Intrinsic Drain Voltage," in *IEEE European Solid-State Device Research Conference (ESSDERC)*, Sept. 2001, pp. 399 – 402.

[39] J. Zeng, P. A. Mawby, M. S. Towers, and K. Board, "Numerical analysis of a trench VDMOST structure with no quasi-saturation," *Solid-State Electronics*, vol. 38, no. 4, pp. 821–828, April 1995.

[40] L. Su, K. Goodson, D. Antoniadis, M. Flik, and J. Chung, "Measurement and Modeling of Self-Heating Effects in SOI NMOSFETs," in *IEEE International Electron Devices Meeting (IEDM)*, 1992, p. 357 360.

[41] G. Wachutka, "Rigorous Thermodynamic Treatment of Heat Generation and Conduction in Semiconductor Device Modelling," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 9, no. 11, p. 1141 1149, 1990.

[42] P. Mautry and J. Trager, "Investigation of Self-Heating in VLSI and ULSI MOSFETs," in *International Conference on Microelectronic Test Structures (ICMTS)*, March 1990, p. 221 226.

[43] J. Jomaah, G. Ghibaudo, and F. Balestra, "Analysis and Modeling of Self-Heating Effects in Thin-Film SOI as a Function of Temperature," *Solid-State Electronics*, vol. 38, no. 3, pp. 615–618, 1995.

[44] L. McDaid, S. Hall, P. Mellor, W. Eccleston, and J. Alderman, "Physical Origin of Negative Differential Resistance in SOI Transistors," *IEE Electronics Letters*, vol. 25, no. 13, p. 827 828, 1989.

[45] C. Anghel, N. Hefyene, R. Gillon, M. Tack, M. Declercq, and A. Ionescu, "New method for temperature-dependent thermal resistance and capacitance accurate extraction in high-voltage DMOS transistors," in *IEEE International Electron Devices Meeting (IEDM)*, Dec. 2003, pp. 5.6.1 – 5.6.4.

[46] C. Anghel, R. Gillon, and A. Ionescu, "Self-heating characterization and extraction method for thermal resistance and capacitance in HV MOSFETs," *IEEE Electron Device Lett.*, vol. 25, no. 3, pp. 141 – 143, March 2004.

[47] C. Anghel, "High voltage devices for standard MOS technologies : characterisation and modelling," Ph.D. dissertation, EPFL, 2004, thesis No. 3116.

[48] Y. Tsivids, "," in *Operation and Modeling of The MOS Transistor*. McGraw-Hill, 1999.

[49] G. Cao, S. Manhas, E. Narayanan, M. D. Souza, and D. Hinchley, "Comparative study of drift region designs in RF LDMOSFETs," *IEEE Transactions on Electron Devices*, vol. 51, no. 8, pp. 1296– 1303, Aug. 2004.

[50] S. Frére, J. Rhayem, H. Adawe, R. Gillon, M. Tack, and A. Walton, "LDMOS Capacitance Analysis versus Gate and Drain Biases, Based on Comparison between TCAD Simulations and Measurements," in *IEEE European Solid-State Device Research Conference (ESSDERC)*, Sept. 2001, pp. 219 – 222.

[51] C. Anghel, B. Bakeroot, Y. S. Chauhan, R. Gillon, C. Maier, P. Moens, J. Doutreloigne, and A. Ionescu, "New Method for Threshold Voltage Extraction of High-Voltage MOSFETs Based on Gate-to-Drain Capacitance Measurement," *IEEE Electron Device Letters*, vol. 27, no. 7, pp. 602 – 604, July 2006.

[52] C. Anghel, Y. S. Chauhan, N. Hefyene, and A. Ionescu, "A physical analysis of HV MOSFET capacitance behaviour," in *IEEE International Symposium on Industrial Electronics (ISIE)*, vol. 2, June 2005, pp. 473 – 477.

[53] C.-M. Liu and J. B. Kuo, "Quasi-saturation capacitance behavior of a DMOS device," *IEEE Transactions Electron Devices*, vol. 44, no. 7, pp. 1117 – 1123, July 1997.

[54] N. Hefyene, E. Vestiel, B. Bakeroot, C. Anghel, S. Frere, A. Ionescu, and R. Gillon, "Bias-dependent drift resistance modeling for accurate DC and AC simulation of asymmetric HV-MOSFET," in *IEEE European Solid-State Device Research Conference (ESSDERC)*, Sept. 2002, pp. 203 – 206.

[55] K. Narasimhulu, M. P. Desai, S. G. Narendra, and V. R. Rao, "The effect of lac doping on deep submicrometer transistor capacitances and its influence on device rf performance," *IEEE Transactions Electron Devices*, vol. 51, no. 9, pp. 1416 – 1423, September 2004.

[56] Y. S. Chauhan, R. Gillon, M. Declercq, and A. M. Ionescu, "Impact of Lateral Non-uniform doping and hot carrier degradation on Capacitance behavior of High Voltage MOSFETs," in *IEEE European Solid-State Device Research Conference (ESSDERC)*, Sept. 2007.

[57] Y. S. Chauhan, F. Krummenacher, R. Gillon, B. Bakeroot, M. Declercq, and A. M. Ionescu, "A New Charge based Compact Model for Lateral Asymmetric MOSFET and its application to High Voltage MOSFET Modeling," in *IEEE International Conference on VLSI Design and International Conference on Embedded Systems*, Jan. 2007, pp. 177 – 182.

[58] Y. S. Chauhan, F. Krummenacher, C. Anghel, R. Gillon, B. Bakeroot, M. Declercq, and A. M. Ionescu, "Analysis and Modeling of Lateral Non-Uniform Doping in High-Voltage MOSFETs," in *IEEE International Electron Devices Meeting*, Dec. 2006, pp. 8.3.1 – 8.3.4.

[59] Y. S. Chauhan, F. Krummenacher, R. Gillon, B. Bakeroot, M. Declercq, and A. M. Ionescu, "Compact Modeling of Lateral Non-uniform doping in High-Voltage MOSFETs," *IEEE Transactions on Electron Devices*, vol. 54, no. 6, pp. 1527–1539, June 2007.

[60] A. Aarts, R. van der Hout, J. Paasschens, A. Scholten, M. Willemsen, and D. Klaassen, "New fundamental insights into capacitance modeling of laterally nonuniform MOS devices," *IEEE Transactions Electron Devices*, vol. 53, no. 2, pp. 270 – 278, Feb. 2006.

[61] K. Dharmawardana and G. Amaratunga, "Modeling of high current density trench gate MOSFET," *IEEE Transactions on Electron Devices*, vol. 47, no. 12, pp. 2420– 2428, Dec. 2000.

[62] A. S. Roy, Y. S. Chauhan, C. Enz, J.-M. Sallese, A. M. Ionescu, and M. Declercq, "Partitioning Scheme in Lateral Asymmetric MOST," in *IEEE European Solid-State Device Research Conference*, Sept. 2006, pp. 307–310.

[63] A. S. Roy, C. C. Enz, and J.-M. Sallese, "Drain-Source Partitioning in MOSFET," *IEEE Transactions on Electron Devices*, June 2007.

[64] A. Aarts, R. van der Hout, J. Paasschens, A. Scholten, M. Willemsen, and D. Klaassen, "Capacitance modeling of laterally non-uniform MOS devices," in *IEEE International Electron Devices Meeting*, Dec. 2004, pp. 751 – 754.

[65] C. Enz, F. Krummenacher, and E. Vittoz, "An analytical MOS transistor model valid in all regions of operation and dedicated to low-voltage and low-current applications," *Journal on Analog Integrated Circuits and Signal Processing*, vol. 8, no. 1, pp. 83–114, July 1995.

[66] J. M. Sallese and A.-S. Porret, "A novel approach to charge-based non-quasi-static model of the MOS transistor valid in all modes of operation," *Solid-State Electronics*, vol. 44, no. 6, pp. 887–894, June 2000.

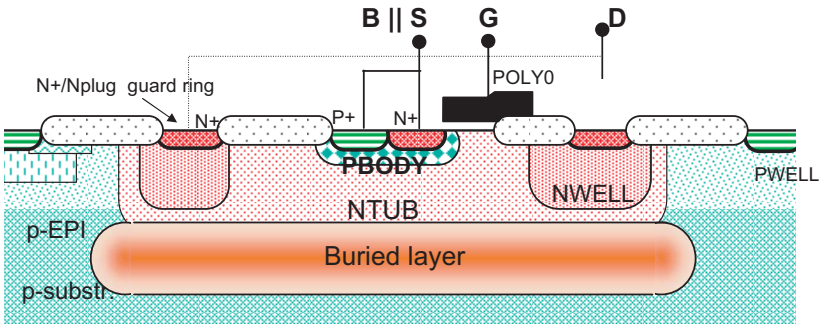
[67] Y. S. Chauhan, C. Anghel, F. Krummenacher, C. Maier, R. Gillon, B. Bakeroot, B. Desoete, S. Frere, A. B. Desormeaux, A. Sharma, M. Declercq, and A. M. Ionescu, "Scalable General High Voltage MOSFET Model including Quasi-Saturation and self-heating effect," *Solid State Electronics*, vol. 50, no. 11-12, pp. 1801–1813, 2006.

Chapter 3

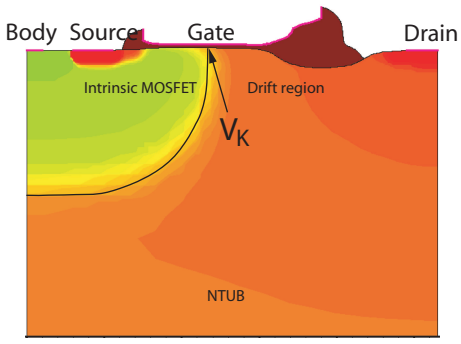
EKV-based Scalable General High Voltage MOSFET Model

The accurate compact modeling of High Voltage (HV) MOS transistors has always been a great challenge in the device modeling community. This is due to the fact that the charges and field associated with the drift region and intrinsic MOS have very complex dependence on the external terminal biases owing to the asymmetric device architecture. Though many groups around the world have attempted to model the different architectures of HV MOS transistors using different approaches, most of these are sub-circuit models. To the best of our knowledge, in the literature, there is no available compact *general* HV MOS model (i.e. a single model for any HV MOS device e.g. LDMOS and VDMOS) capable of combining the accuracy, speed, scalability for both DC and AC domains. Acceptable simulation accuracy is obtained by the use of adopted macro-models based on conventional low voltage modules [1, 2], but these macro-models are not physical and do not take into account the special phenomena of HV devices. Some compact models have also been reported in the literature with better accuracy [3, 4, 5, 6, 7, 8, 9, 10]. Halleweyen et al. [3] and Aarts et al. [8] reported surface potential based LDMOS models but only for DC operations. Previously Aarts et al. [7] reported a physical LDMOS model for both DC and AC operations, however scalability of the model has not been shown. Other models reported in the literature show reasonable accuracy in DC operation [4, 5, 6, 9, 10], but do not show model validity for AC operation under different biasing conditions and model scalability especially with temperature, drift length and number of fingers.

In this chapter, a modeling strategy for HV MOS transistors based on the scalable drift resistance [11, 12] and the use of EKV2.6 MOSFET model [13] as a core for the intrinsic MOS channel is presented [14, 15]. The strategy is optimized according to the fast convergence and good accuracy criteria. The model is stable and robust in the entire bias range useful for circuit design purpose. An important aspect of this *general* model is the scalability of the model with physical and electrical parameters along with the correct modeling of quasi-saturation and self-heating effect. The model is validated on the measured characteristics of two widely used high voltage devices in the industry i.e. LDMOS [16] and VDMOS [17] devices, and implemented on commercial circuit simulators like SABER (Synopsys), ELDO (Mentor Graphics), Spectre (Cadence) and UltraSim (Cadence). The accuracy of the model is better than 10% for DC I-V and g-V characteristics and shows good behavior for all capacitances which are unique for these devices showing peaks and shift of peaks with bias variation. Also the model exhibits excellent



(a)



(b)

Figure 3.1: (a) Schematic representation and (b) device architecture of 40V SOI-LDMOS transistor from I2T100 AMIS technology. The separation boundary between the intrinsic MOSFET and the drift region is the metallurgical junction of the PIN diode.

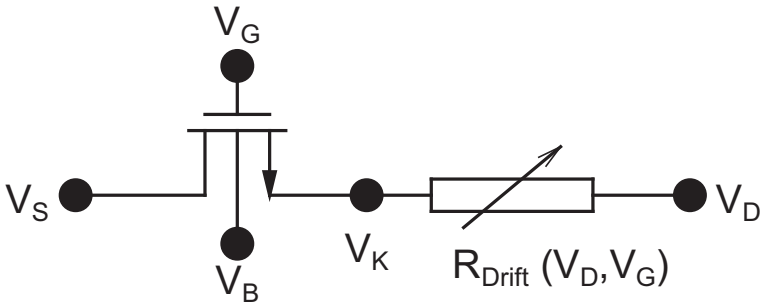


Figure 3.2: High Voltage MOSFET modeling strategy.

scalability with transistor width, drift length, number of fingers and temperature.

3.1 Behavior of surface potential in the drift region

The LDMOS device architecture under study is shown in Fig. 3.1(a). The channel of the LDMOS transistor is obtained by a double diffusion process and not by photolithographic process. Consequently, this transistor has gradual doping profile in the channel decreasing from source to the intrinsic drain (V_K) of the device. The second part of the device, i.e. the drift zone,

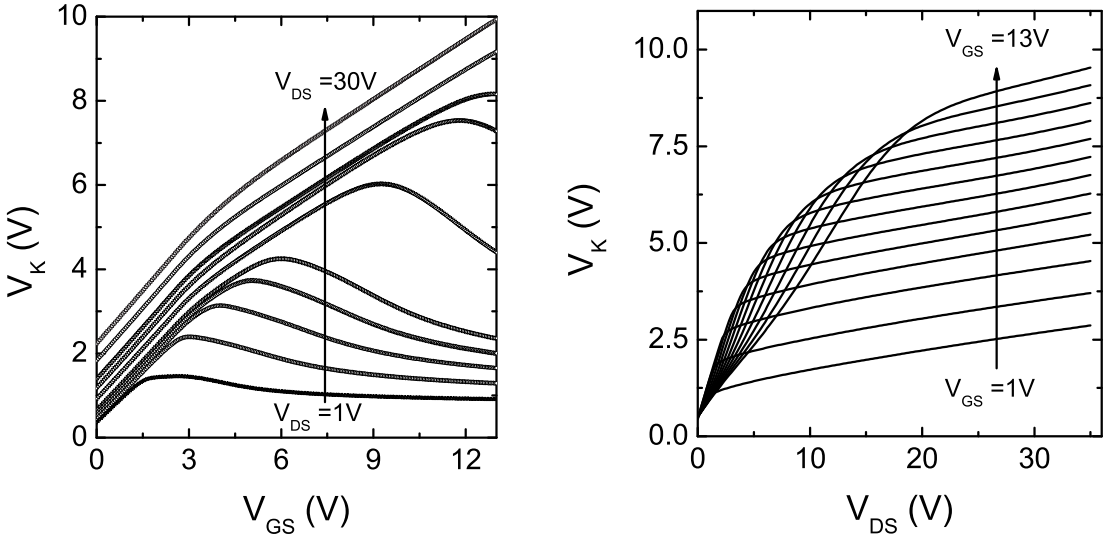
sustains the high voltage applied on the drain terminal of the device. The device presents a gate overlap over both the channel and the drift region, involving the possibility to obtain operation regions where the intrinsic channel is inverted and accumulation/depletion may exist in the drift region under gate.

Fig. 3.2 shows the modeling strategy used in this chapter. The HV MOS is divided into low voltage MOS channel and a drift region. The major issue in HV MOS modeling that make standard low-voltage MOSFET models un-applicable is the bias dependence of the drift resistance (R_{Drift}) with both gate and drain voltages. Consequently, the efforts in this chapter will be concentrated on different solutions to analytically describe the main dependencies of R_{Drift}, in all operation regimes using simple analytical expressions. The modeling of the intrinsic MOS channel is carried out using EKV model [13]. To understand the behavior of drift region, 2-D numerical device simulation is performed using ISE-DESSIS. The idea is to separate the device into physically significant regions and then to inspect and model them independently. The separation boundary between the intrinsic MOS transistor and the drift region is the metallurgical junction of the PIN diode (see V_K point in Fig. 3.1(b)). Fig. 3.3 shows the plot of V_K for different gate and drain voltages. Fig. 3.3(a) and Fig. 3.3(b) show the V_K vs. V_{GS} and V_{DS} respectively [18]. The unique behavior of V_K can be explained by considering the variation of the channel and drift resistance with bias. Initially as V_{GS} increases, most of the drain voltage drop occurs across intrinsic MOS channel as channel resistance is very high compared to drift resistance. With increasing V_{GS}, channel resistance drops sharply compared with drift resistance and at some bias condition, channel resistance becomes equal to drift resistance. This is the point, where, the peak in V_K occurs on $V_K - V_{GS}$ characteristics (see Fig. 3.3(a)). If V_{GS} keeps on increasing after this point, V_K keeps on decreasing as drift resistance now dominates compared to channel resistance. This same explanation can be easily associated with $V_K - V_{DS}$ characteristics also (Fig. 3.3(b)). Please note that the effect of drift resistance is observed in the linear region only (see Fig. 3.3(b)). There are two interesting points to note here. First, the major V_{DS} drop occurs across the drift region, which is also the desired feature. Second, the V_K behavior is quite different in the linear region while it saturates or varies slowly at higher drain voltages. This analysis also points out the importance of the modeling of the drift region in the linear region.

3.2 GENERAL DRIFT RESISTANCE MODEL

Fig. 3.4(a) and 3.4(b) show the schematics of high voltage VDMOS and LDMOS devices, respectively. Even though, here simple device architectures are shown, the model can be used, as described earlier for any HV device which uses extended drift region to handle the high voltage applied at the drain terminal e.g. LDMOS with thin or thick oxide (shown in Fig. 3.1(a)) etc.

As discussed in the previous chapter, the intrinsic drain voltage (V_K) always remains at low values for entire bias domain [18]. Based on this understanding, we consider our device divided into an intrinsic MOSFET region and a drift region, where the intrinsic transistor part is modeled by using low voltage EKV model [13] described in the next section while modeling of drift region is carried out by using bias dependent resistance explained below. The motivation to use a resistance to model the drift region is to get the fast convergence along with excellent



(a) (b)

Figure 3.3: Behavior of intrinsic drain potential (V_K) from numerical device simulation: (a) Plot of V_K vs. V_{GS}. (b) Plot of V_K vs. V_{DS}.

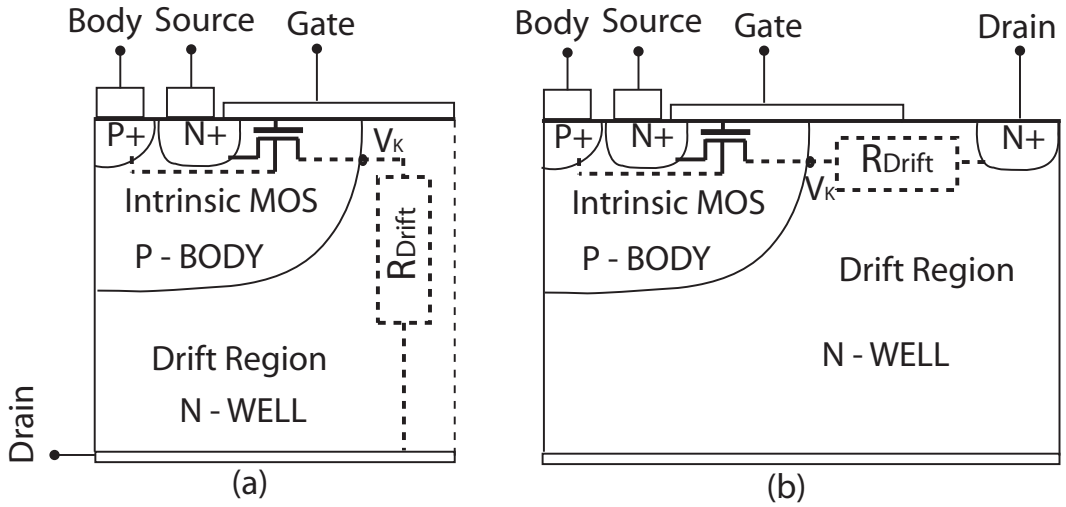


Figure 3.4: Schematic representation of high voltage (a) Vertical DMOS (VDMOS) and (b) Lateral DMOS (LDMOS) device Architecture.

accuracy. The simplest resistance expression could be a constant resistance. Fig. 3.5 shows the transfer characteristics ($I_{DS} - V_{GS}$) using constant resistance (dash lines) as drift resistance. It can be seen that the constant resistance accurately models the low drain and low to medium gate bias behavior, as at low drain bias, the intrinsic transistor drives the current while the drift region behaves like a constant resistor. Another interesting remark is that the fixed resistance cannot model the behavior of the device at low V_{DS}, when high gate voltage is applied. The explanation for this deviation comes from the accumulation charge sheet, which extends into

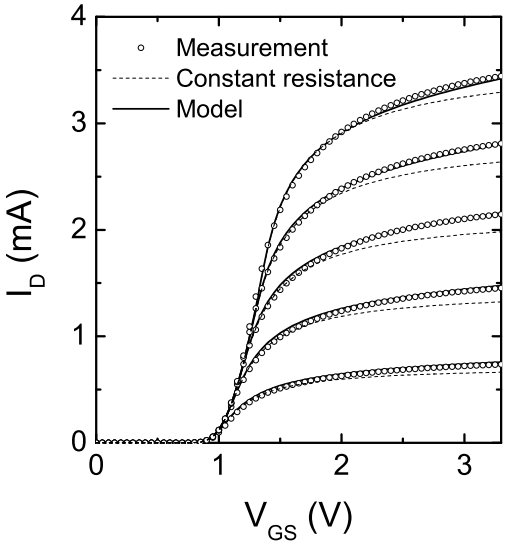


Figure 3.5: I_{DS} vs. V_{GS} for V_{DS}=0.1 to 0.5V for 50V VDMOS transistor. The constant resistance along with the accumulation charge sheet effect provides excellent accuracy at low drain bias.

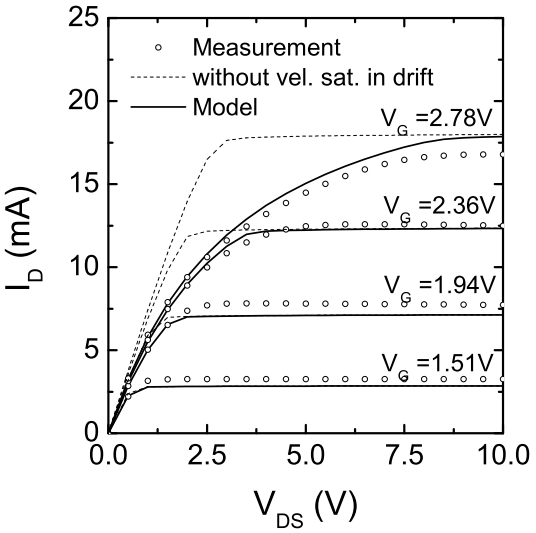


Figure 3.6: I_{DS} vs. V_{DS} for 50V VDMOS transistor. The modeling of velocity saturation effect on drift resistance provides good behavior in the linear region.

the drift region with the increase of the gate voltage and lowers the resistance of the drift part. In order to simulate the above described effect, a slight reduction of the drift resistance with the gate voltage is introduced in the model:

$$R_{Drift} = \frac{R}{1 + \theta_{Acc} \cdot |V_{GS}|} \tag{3.1}$$

where R is the constant resistance, θ_{Acc} is the gate bias modulation parameter (effect of accumulation charge sheet on R_{Drift}) and V_{GS} is the applied gate voltage. The value of R can be obtained by extracting the silicon resistivity and then calculating the global resistance function of the geometrical dimensions, if the doping concentration of the drift zone is known. The model behavior using (3.1) is shown in Fig. 3.5 by solid lines. It can be observed that the matching between the simulation and measured data is excellent. Thus, it can be concluded that (3.1) correctly reproduces the physics inside the device. Moreover, this expression proves to be highly efficient in terms of implementation as it uses the simplest representation and the minimum number of parameters for the description of the physical phenomenon at low gate and drain bias. Fig. 3.6 shows the $I_{DS} - V_{DS}$ characteristics using drift resistance derived above by dash lines. It is easily observable that even though above derived expression showed excellent characteristics at low V_{DS}, it is not working well at higher V_{DS}. It is also important to mention that once the current saturates in the intrinsic MOS transistor, the drift part has no influence on the current. Consequently, the drift part only affects the linear regime of the output characteristics. Although, this influence seems to be limited, the transition from linear to saturation is very sensitive to the drift resistance variation. The delayed transition between linear and satu-

ration regime at high gate voltages occurs due to the carrier velocity saturation in the drift and is equivalent to an increase in the resistance of the drift region. In literature, the carrier velocity saturation effect on the current is modeled using hyperbolic dependence of the electric field across the region. It means that this dependence would be linear for the resistance. Thus, in order to simulate the carrier velocity saturation dependence using the drift resistance expression, a direct dependence on the field applied in the drift region is introduced as:

$$R_{Drift} = R \cdot \left[\frac{1 + \left(\frac{V_{DS} - V_K}{VSAT * L_{DR}} \right)^{\alpha_{vsat}}}{1 + \theta_{Acc} \cdot |V_{GS}|} \right] \tag{3.2}$$

where $VSAT$ and α_{vsat} are the velocity saturation parameters. L_{DR} is the length of the drift region. The mobility is considered constant all over the current path and the electric field uniformly distributed along the length of the drift region. Solid lines in Fig. 3.6 show the drain current using (5.3), which proves that this expression takes into account major physical phenomena in the drift region.

The final expression for the drift resistance including geometry and temperature effects can be written as [11, 12]:

$$R_{Drift} = R_{Drift0} \cdot \left[\frac{1 + \left(\frac{V_{DS} - V_K}{VSAT * L_{DR}} \right)^{\alpha_{vsat}}}{1 + \theta_{Acc} \cdot |V_{GS}|} \right] \cdot \left[1 \pm (k_{rd} - 1) \cdot \left(\frac{N_F - 1}{N_F + N_{CRIT}} \right) \right] \cdot (1 + \alpha_T \cdot \Delta T) \tag{3.3}$$

where R_{Drift0} is the value of the drift resistance at low bias voltage defined as

$$R_{Drift0} = \rho_{_{Drift}} \cdot \left[\frac{L_{DR}}{(W + \Delta W) \cdot N_F} \right] \tag{3.4}$$

Where $\rho_{_{Drift}}$ is the resistivity per unit length at room temperature ($T = 300K$). W, ΔW and N_F represent the width, width offset and number of fingers respectively. N_{CRIT} and k_{rd} are the parameters for drift scaling with number of fingers. The "$+$" sign is used for drain-on-side devices while "$-$" sign is used for drain-all-around devices. α_T is the temperature coefficient of the drift region and ΔT is the difference in ambient temperature with normal room temperature ($T = 300K$).

3.3 CHARGE EVALUATION based on EKV MODEL

The main reason behind using EKV MOSFET model [13] for intrinsic channel is that EKV model has physical expression for current and charges, which are continuous from weak to moderate to strong inversion. Another important characteristic of the EKV model is that compared with other existing MOS models (e.g. BSIM), it uses less number of parameters, most of which are all physical. The intrinsic drain-to-source current (V_K to V_S in our model) in EKV model is given as

$$I_{KS} = I_S(i_f - i_r) \tag{3.5}$$

where I_S is the specific current [13] defined as

$$I_S = 2 \cdot n \cdot \beta \cdot U_T^2 \tag{3.6}$$

$$n = \frac{1}{1 - \frac{\gamma}{2 \cdot \sqrt{V_{GS} - V_T + (\frac{\gamma}{2} + \sqrt{\psi_0})^2}}} \tag{3.7}$$

$$\psi_0 = 2\phi_F + several\ U_T \tag{3.8}$$

$$\beta = \mu \cdot C_{ox} \cdot \frac{W}{L} \tag{3.9}$$

where U_T=$\frac{kT}{q}$ is the thermal voltage, n is the slope factor, V_T is the threshold voltage, γ is the body effect parameter and, C_{ox} is the oxide capacitance per unit area. The normalized forward current i_f and normalized reverse current i_r are defined as

$$i_f = \left[ln(1 + e^{\frac{v_p - v_s}{2}}) \right]^2, \tag{3.10}$$

and

$$i_r = \left[ln(1 + e^{\frac{v_p - v_k}{2}}) \right]^2, \tag{3.11}$$

where $v_p = \frac{V_P}{U_T}$, $v_s = \frac{V_S}{U_T}$, $v_k = \frac{V_K}{U_T}$ are the normalized pinch-off ($V_P = \frac{V_{GS} - V_T}{n}$), source and intrinsic drain voltage respectively [13].

The total gate charge is the sum of the charges related to intrinsic-drain (V_K), source, body and drift. The charges associated with the intrinsic MOS are directly obtained from EKV model [13].

The R_{Drift} expression (3.3) used above for current modeling does not provide the correct behavior for intrinsic drain voltage (V_K) at low-gate/high-drain biases, as this resistance in actual case should rise to Giga-ohm at low-gate/high-drain biases. The preceding statement is verified by the fact that at low gate bias, the drift region is in depletion and most of the voltage drop applied on drain terminal occurs in this region and the current is very small. But this resistance provides accurate current prediction because at low-gate/high-drain bias (intrinsic MOS in saturation), the current is well modeled by the intrinsic MOS part. The impact of the intrinsic drain potential (V_K) on AC characteristics was shown by Hefyene et al. [19, 20]. The correct V_K behavior is not only important for the peaks of capacitances which are very specific to high voltage devices, it is also extremely important for the position of the peaks with gate and drain bias. Thus it is extremely important to first obtain the correct V_K behavior with gate and drain bias. In literature, this is obtained using interpolation between V_K in the linear region and V_{Ksat} in the saturation region to limit the value of V_K to V_{Ksat} [3]. In this work, the accurate V_K value, which is used in the calculation of accumulation charge, can be obtained by backtracking of K-node charge as given below. The motivation for this strategy is to get the impact of current saturation on charge and then on V_K.

The V_K behavior which has great impact on capacitance of high voltage devices [19, 20], is obtained by backtracking of K-node charge or current backtracking [21, 14]. The normalized potential v_k is expressed as a function of v_p and q_k (normalized inversion charge density at V_K) as [21]

$$v_k = v_p - (2 \cdot q_k + \ln q_k) \tag{3.12}$$

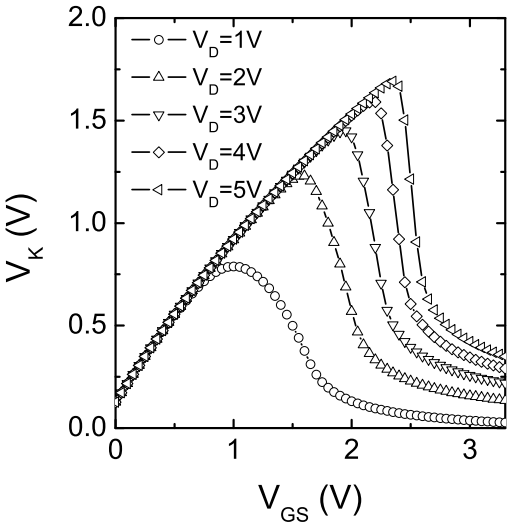


Figure 3.7: Intrinsic-drain potential V_K vs. V_{GS} for V_{DS}=1 to 5V in steps of 1V for VDMOS transistor. The decrease in V_K is caused by drift region.

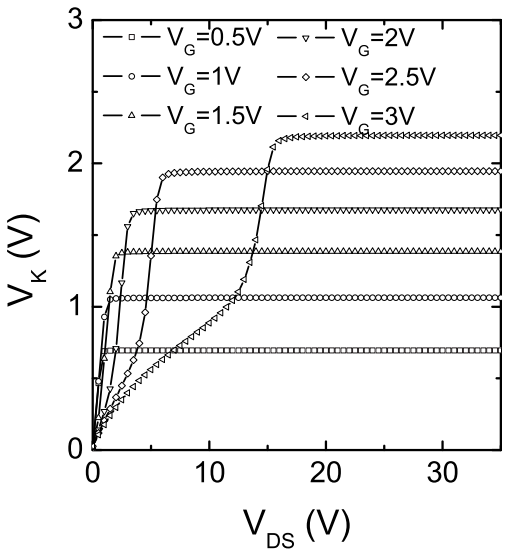


Figure 3.8: Intrinsic-drain potential V_K vs. V_{DS} for V_{GS}=0.5 to 3V in steps of 0.5V for VDMOS transistor.

where q_k is expressed as [21]

$$q_k = \sqrt{i_r + 0.25} - 0.5. \tag{3.13}$$

Thus V_K can be easily expressed as

$$V_K = U_T \cdot [v_p - \{2 \cdot (\sqrt{i_r + 0.25} - 0.5) + \ln(\sqrt{i_r + 0.25} - 0.5)\}] \tag{3.14}$$

The intrinsic drain potential (V_K) behavior obtained by this method shows excellent agreement with literature [22] (see Fig. 3.7 and 3.8).

The normalized drift accumulation charge density can be written as

$$q_{drift} = v_g - v_{fb\_drift} - \psi_{s\_drift}. \tag{3.15}$$

where v_{fb_drift} is the normalized flat-band voltage of drift region and ψ_{s_drift} is the normalized surface potential in the drift region. The total drift accumulation charge is obtained by integrating the drift charge density over the gate overlap length, assuming ψ_{s_drift} varies linearly in the drift region also validated from numerical device simulation.

Thus total gate charge can be written as,

$$Q_G = Q_S + Q_K + Q_B + Q_{Drift}, \tag{3.16}$$

where Q_S, Q_K and Q_B are the charges related to source, intrinsic drain and body node respectively, obtained from EKV MOS model [13].

The capacitances are defined using standard method as:

$$C_{ij} = \begin{cases} -\frac{\delta Q_i}{\delta V_j} & i \neq j \\ +\frac{\delta Q_i}{\delta V_j} & i = j \end{cases}$$

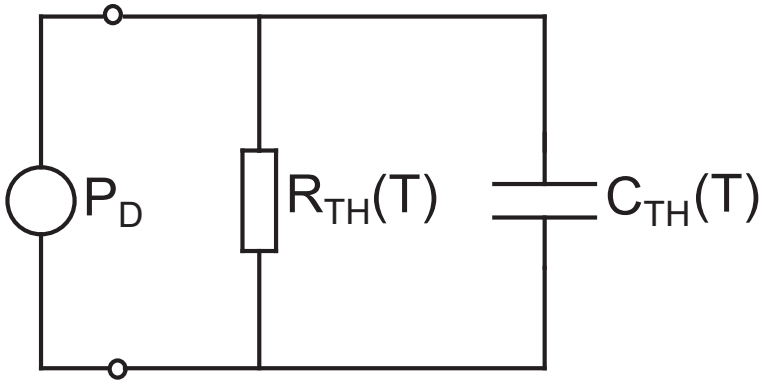


Figure 3.9: Representation of the electro-thermal circuit for self-heating effect simulation (Power dissipation $P_D = I_{DS}V_{DS}$, thermal resistance R_{TH}(T)=R_{THNOM}(1+$\alpha\Delta T$) and thermal capacitance $C_{TH} = f(R_{TH}, \tau_w)$) [23, 24].

3.4 Modeling of Quasi-Saturation and Self-Heating Effects

As discussed in the previous chapter, the high voltage devices show some special effects due to high electric field inside the device e.g. self-heating, quasi-saturation and impact ionization effects. In fact some of these effects (self-heating and impact ionization) are also visible in low voltage MOSFETs as electric field in these devices also becomes quite high as channel length is decreased. Here we will discuss, the modeling of these effects.

3.4.1 Quasi-Saturation Effect

The quasi-saturation effect is one of the unique effect observed in HV devices. This effect originates due to velocity saturation in the drift region when intrinsic MOS is still not saturated. If drift is velocity saturated and intrinsic MOS is in linear region, the increase in V_{GS} does not increase current level significantly and gate bias has small effect. As our drift resistance already includes the velocity saturation in the drift, the quasi-saturation effect is easily modeled by this model.

3.4.2 Self-Heating Effect

The self-heating effect (SHE) represents the heating of the device due to its internal power dissipation. This effect appears when high levels of power are attained in the device. The dissipated heat leads to an increase in the internal temperature of the device. The internal temperature increase influences the device characteristics mainly by affecting the mobility, threshold voltage and velocity saturation. In the literature, this effect was mainly studied on the SOI devices and the proposed models for SHE are distributed or non-distributed models. As expected, better accuracy was obtained from distributed models, which offer a larger flexibility for the current simulation. Still, the clear advantage of the non-distributed models over the distributed ones is the parameter extraction procedure, as non-distributed approach offers a simple and efficient representation of the problem. Fig. 3.9 shows the equivalent sub-circuit used for the self-heating

representation. This classical representation can be used for the DC, AC or transient simulation of the device in some critical regimes (other than analog operation).

In our model, the SHE is modeled using standard circuit shown in Fig. 3.9, where the thermal resistance (R_{TH}) and thermal capacitance (C_{TH}) varies dynamically with the device temperature [23, 24]. The extraction procedure for R_{TH} and C_{TH} has been discussed in [23, 24]. The expressions for thermal resistance and capacitance from [23, 24] are re-written here to complete this discussion.

The thermal resistance is expressed as [23, 24]

$$R_{TH} = R_{THNOM}(T_e) \cdot [1 + \alpha \cdot (T_i - T_e)] \tag{3.17}$$

where T_e, T_i are the ambient and internal device temperatures, respectively and R_{THNOM} is also considered a linear function of the ambient temperature as follows:

$$R_{THNOM}(T_e) = R_{THNOM}(300K) \cdot [1 + \alpha \cdot (T_e - 300K)] \tag{3.18}$$

One should note that in (4.12), the temperature increase, $\Delta T = T_i - T_e$, at known ambient temperature is essentially given by SHE (related to the injected electrical power P_D), and consequently, R_{THNOM} could be considered as the nominal thermal resistance at zero injected power (at given ambient temperature T_e). The thermal capacitance $C_{TH} = f(R_{TH}, \tau_w)$ and temperature coefficient of thermal resistance α are extracted from $I_{DS} - V_{DS}$ characteristics for different pulse widths τ_w [23, 24].

3.4.3 Impact Ionization Effect

When the drain bias across the device increases, the electric field in the drift region also increases as a function drain bias. In this high field zone, the longitudinal electric field varies linearly and reaches its peak value at the drain junction. The impact ionization current (or avalanche current) can be expressed as

$$I_{avl} = (M - 1) \cdot I_D \tag{3.19}$$

Where M is called as Multiplication factor. Rossel et al. [25] developed the following approximate expression for M from impact ionization integral assuming low multiplication level.

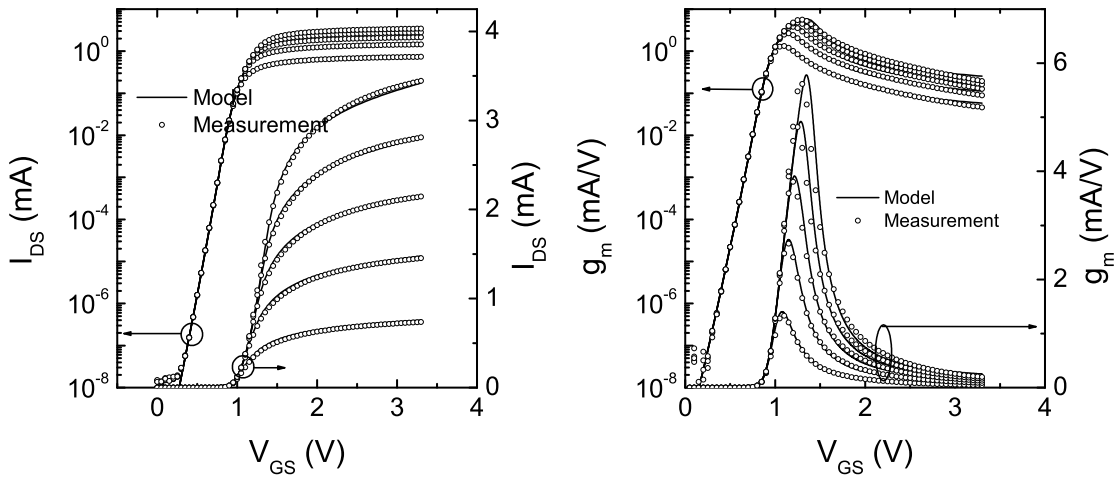
$$M - 1 \simeq 1 - \frac{1}{M} = (2.8 \cdot 10^{-73}) \cdot N_{eff}^3 \cdot V_{DS}^4 \tag{3.20}$$

In the model implementation, we combined the constant $(2.8 \cdot 10^{-73})$ with N_{eff} and used a single parameter N_{EFF}. Thus multiplication factor M can be written as:

$$M - 1 = N_{EFF}^3 \cdot V_{DS}^4 \tag{3.21}$$

3.5 MODEL VALIDATION and RESULTS

This model is calibrated on the measured characteristics of a 50V VDMOS and 40V LDMOS devices provided by AMIS and BOSCH [17, 16]. The source and body are tied to avoid parasitic bipolar transistor for all measurements.



(a) (b)

Figure 3.10: Transfer characteristics of VDMOS transistor at low drain bias for W=40μm, L=0.6μm and N_F=2 at T=30°C: (a) I_{DS}-V_{GS} for V_{DS}=0.1V-0.5V in steps of 0.1V. The current at higher V_{GS} is heavily affected by drift region. (b) g_m-V_{GS} for V_{DS}=0.1V-0.5V in steps of 0.1V. The sharp decrease in transconductance at higher gate bias can be explained by the dominance of drift resistance over channel resistance.

3.5.1 Case Study 1: VDMOS Transistor

The schematic representation of the VDMOS device (half of the device is shown as it is symmetrical along the vertical axis) under study is shown in Fig. 3.4(a). Fig. 3.10(a) shows the transfer characteristics for low drain bias, which demonstrates that the model provides accurate simulation of current and subthreshold slope. From Fig. 3.10(b), it can be observed that the model not only gives accurate values of peak in transconductance and its slope in the subthreshold regime but also predicts the correct behavior after the peak, which is very important in circuit design. Fig. 3.11 shows the transfer characteristics for medium drain bias (V_{DS}=1V to 5V in steps of 1V). The drain current at higher gate voltages is heavily affected by the drift region. Fig. 3.12 (a) and (b) show the output characteristics and output-conductance, respectively, for different gate bias which show that not only the transition from linear to saturation regime in I_{DS} is well simulated by the model, validating correct drift model, it also correctly simulates the self-heating effect in the output characteristics. The dips in output-conductance are also well predicted by the model. The first dip in $|g_{ds}|$ originates from self-heating effect, while second dip is caused by impact ionization effect. Capacitances C_{GD} and $C_{GS} + C_{GB}$ obtained using this model, are shown in Fig. 3.13 (a) and (b), respectively. The special behavior of the high voltage capacitances, i.e. the peaks [7, 20] in C_{GD} and C_{GS} are well modeled. It can be seen that all the capacitances show good trend for the entire gate and drain bias range. It should be noted that in literature very few models have been successful in modeling the correct behavior of capacitances of HV MOS devices [1, 2, 7, 11, 12]. Furthermore the accuracy on capacitances can be improved by modeling the lateral non-uniform doping in the intrinsic MOS

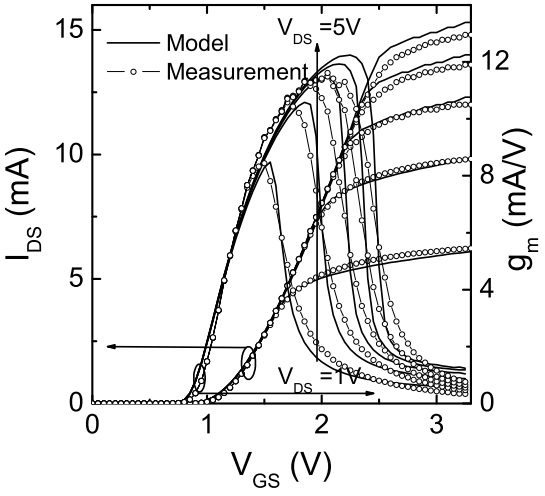
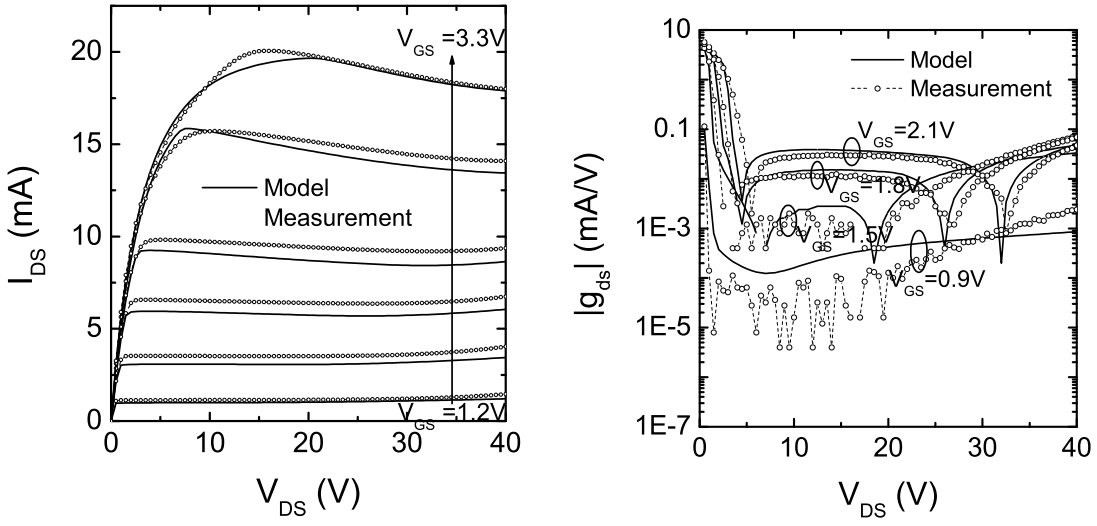
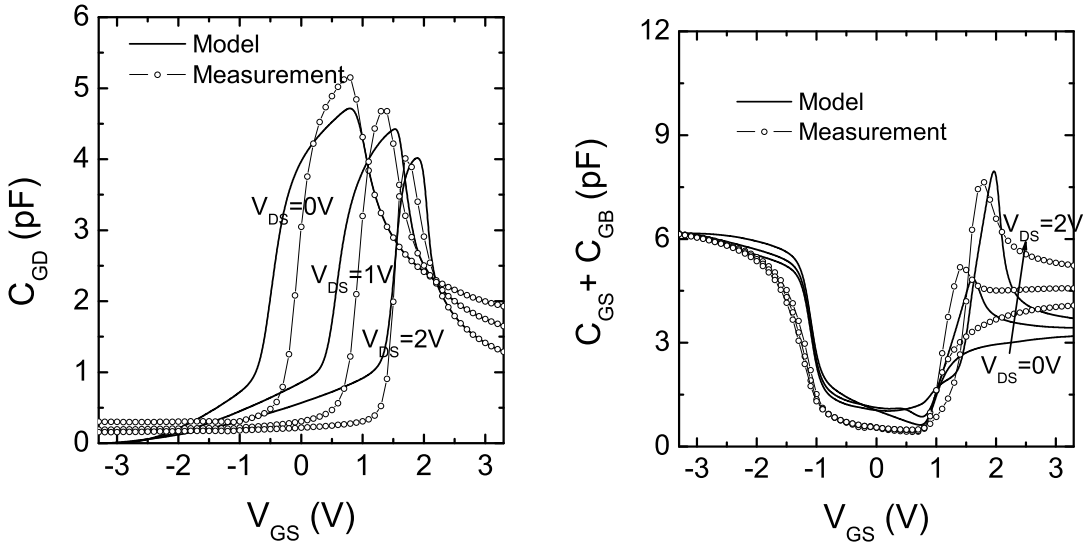


Figure 3.11: Transfer characteristics at medium drain bias for W=40μm, L=0.6μm and N_F=2 at T=30°C: I_{DS} and g_m-V_{GS} for V_{DS}= 1V-5V in steps of 1V for VDMOS transistor.



(a) (b)

Figure 3.12: Output characteristics of VDMOS transistor for W=40μm, L=0.6μm and N_F=2 at T=30°C (a) I_{DS} vs. V_{DS} for V_{GS} =1.2,1.5,1.8,2.1,2.7 and,3.3V. Note self-heating effect (decrease in I_{DS} with increase in V_{DS}) is correctly simulated. The discrepancy in the curves can be explained by the simultaneous optimization of drift resistance, self-heating effect, impact ionization effect and velocity saturation in MOSFET at high V_{DS}. (b) $|g_{ds}|$ vs. V_{DS}. Note peaks in output-conductances are correctly matched. The first dip in $|g_{ds}|$ originates from self-heating effect, while second dip is caused by impact ionization effect.

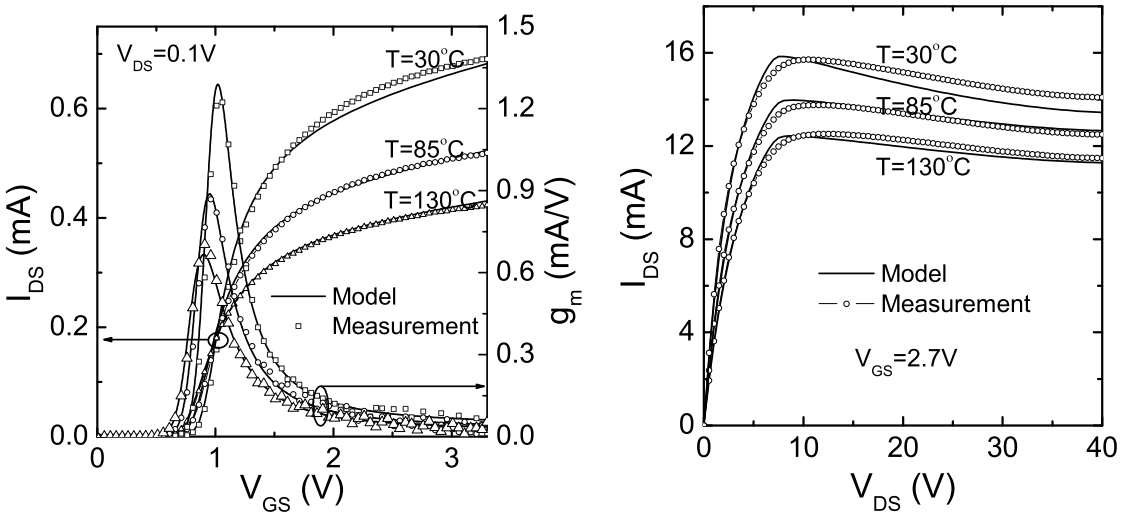


(a) (b)

Figure 3.13: (a) C_{GD} vs. V_{GS} and, (b) C_{GS}+C_{GB} vs. V_{GS} of VDMOS transistor for V_{DS}=0, 1V, and 2V. The sharp decrease in C_{GD} at higher V_{GS} is heavily affected by drift region. The discrepancy in the curves is due to assumption of constant doping in the channel and simplified drift charge evaluation. The accuracy on capacitances can be improved by modeling the lateral non-uniform doping present in the intrinsic MOS channel [20, 26, 27, 28].

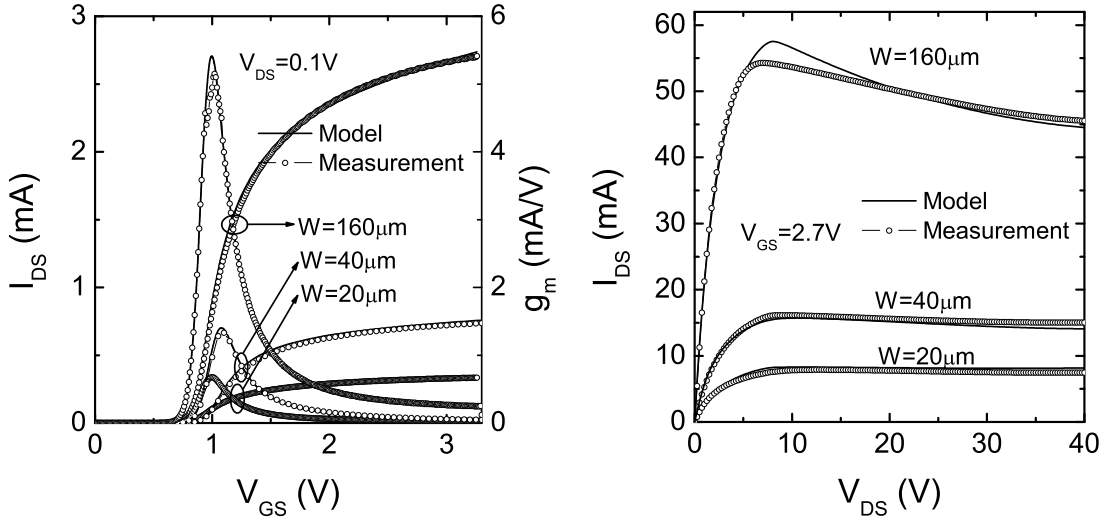
channel of high voltage devices [26, 27, 28]. The modeling of lateral non-uniform doping will be discussed in the next chapter.

Model Scalability: An important characteristic of any model is the scalability with physical and electrical parameters. Fig. 3.14 (a) shows the I_{DS} and $g_m - V_{GS}$ characteristics for different temperatures. It can be seen that the model correctly simulates the variation of drain current, transconductance and most importantly the threshold voltage shift with temperature. An important observation is that ZTC (Zero-Temperature-Coefficient) point [29, 30, 31, 32, 33] is also well modeled in Fig. 3.14 (a). Fig. 3.14 (b) shows the I_{DS}-V_{DS} curves for different temperatures, which demonstrates that the SHE is correctly modeled for entire temperature range. The scaling of the model is also tested for different device geometries. The transfer and output characteristics shown in Fig. 3.15 (a) and (b), respectively, demonstrate that the model scales well with different transistor widths. Note that the self-heating effect is more prominent for higher widths due to increased power dissipation. The variation of ON resistance (R_{ON}) with number of fingers (N_F) is modeled using k_{rd} and N_{CRIT} parameters in (3.3). Fig. 3.16 (a) shows that the R_{ON} scaling with N_F is well modeled for different widths for *drain-all-around* device. The decrease of R_{ON} with number of fingers for *drain-all-around* device is caused by current spreading at the finger edges. Fig. 3.16 (b) shows the R_{ON} scaling with N_F for *drain-on-side* device. The increase in R_{ON} with number of fingers for *drain-on-side* device is caused by the interaction of depletion regions of the neighborhood fingers. The R_{ON} scalability with temperature is shown in Fig. 3.17 for different transistor widths. It can be seen that the increase



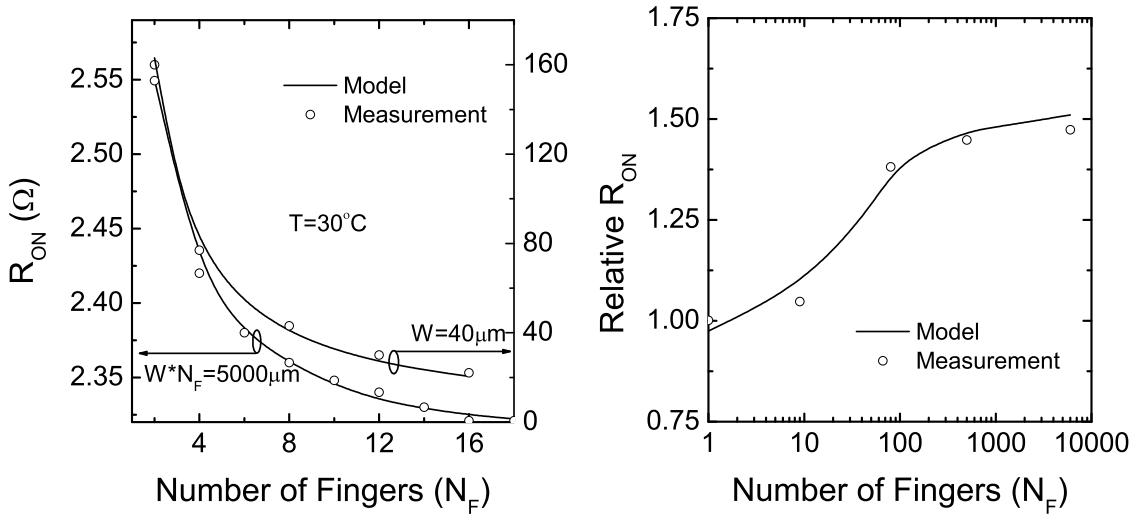
(a) (b)

Figure 3.14: Demonstration of temperature scaling of VDMOS transistor for W=40μm, L=0.6μm and N_F=2: (a) I_{DS}-V_{GS} and g_m-V_{GS} at T=30°C, 85°C and, 130°C. Note, the change in threshold voltage with temperature and peak in transconductance are correctly modeled. The ZTC-point [29, 30] is also well simulated. (b) I_{DS}-V_{DS} at T=30°C, 85°C and, 130°C. Note self-heating effect is very well modeled at different temperatures. The decrease in slope in the linear region is caused by the increase in drift resistance with temperature.



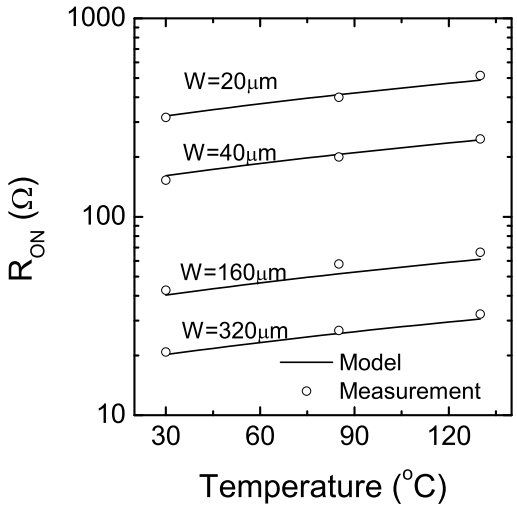
(a) (b)

Figure 3.15: Demonstration of width Scaling of VDMOS transistor for W=20μm, 40μm, 160μm, L=0.6μm and N_F=2 at T=30°C: (a) I_{DS}-V_{GS} and g_m-V_{GS} for V_{DS}=0.1V. (b) I_{DS}-V_{DS} for V_{GS}=2.7V. The self-heating effect is more prominent for higher widths due to increased power dissipation.

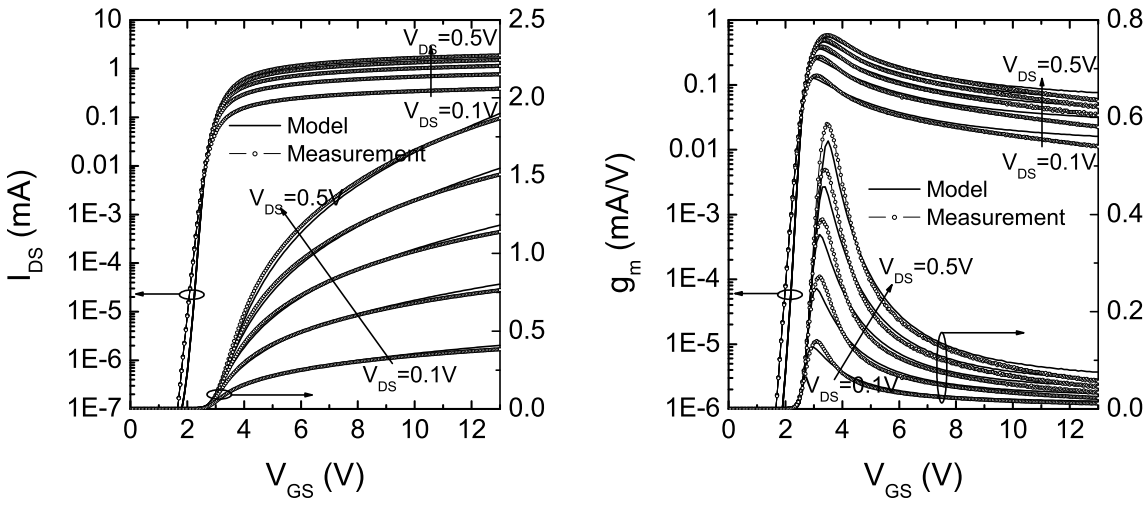


(a) (b)

Figure 3.16: (a) R_{ON} with Number of fingers (N_F) for W=40μm and $W \cdot N_F$=5000μm at V_{GS}=3.3V and V_{DS}=0.5V for *drain-all-around* VDMOS transistor at T=30°C. The decrease of R_{ON} with number of fingers for *drain-all-around* device is caused by current spreading at the finger edges. (b) Relative On-resistance $\frac{R_{ON}}{R_{ON}|_{N_F=1}}$ with Number of fingers (N_F) for *drain-on-side* VDMOS transistor. The increase in R_{ON} with number of fingers for *drain-on-side* device is caused by the interaction of depletion regions of the neighborhood fingers.



in R_{ON} with temperature is excellently modeled for different transistor widths.
Figure 3.17: R_{ON} variation with temperature for N_F=2 and W=20μm, 40μm, 160μm, 320μm for VDMOS transistor.



(a) (b)

Figure 3.18: Transfer characteristics of 40V LDMOS device (W=40μm, L=1.2μm and N_F=1 at T=30°C): (a) I_{DS}-V_{GS} and, (b) g_m-V_{GS} for V_{DS}=0.1V-0.5V in steps of 0.1V .

3.5.2 Case Study 2: LDMOS Transistor

The LDMOS devices (FND40 and FND100) used for the validation of the model are obtained from I2T100 AMIS Technology. The schematic representation of the LDMOS device under study is shown in Fig. 3.4(b) while device architecture of FND40 device is shown in Fig. 3.1. Fig. 3.18 (a) and (b) show the $I_{DS} - V_{GS}$ and $g_m - V_{GS}$ for V_{DS}=0.1V to 0.5V, respectively. Fig. 3.19 and 3.20 show the I_{DS} and $g_m - V_{GS}$ for V_{DS}=1V to 5V, and $I_{DS} - V_{DS}$ characteristics respectively for 40V LDMOS, which demonstrate that the model provides correct simulation of current and transconductance for different bias conditions. The gate-to-drain and gate-to-gate capacitance curves shown in Fig. 3.21 (a) and (b) respectively demonstrate that the model predicts correct trend for capacitances. Furthermore the accuracy on capacitances can be improved by modeling the lateral non-uniform doping in the intrinsic MOS channel of high voltage devices [26, 27, 28]. The modeling of lateral non-uniform doping will be discussed in the next chapter.

Model Scalability: An important issue in any LDMOS model is the scalability with drift length for different voltage handling capability. Fig. 3.22 (a) and (b) show the transfer and output characteristics, respectively, of a 100V LDMOS transistor (FND100 device) on the same technology (as of FND40), which demonstrates that the model scales well with drift length. It should be noted that not only the self-heating effect [24] is well modeled in Fig. 3.22 (b) but also the quasi-saturation effect observed at higher gate biases. The 100V LDMOS transistor (FND100) has longer drift length, in comparison to 40V LDMOS transistor (FND40), to handle the higher drain voltages at drain terminal. The scalability of the model is also tested for R_{ON} for different widths of LDMOS device. Fig. 3.23 shows the R_{ON} vs. V_{GS} for three different widths of 40V LDMOS device.

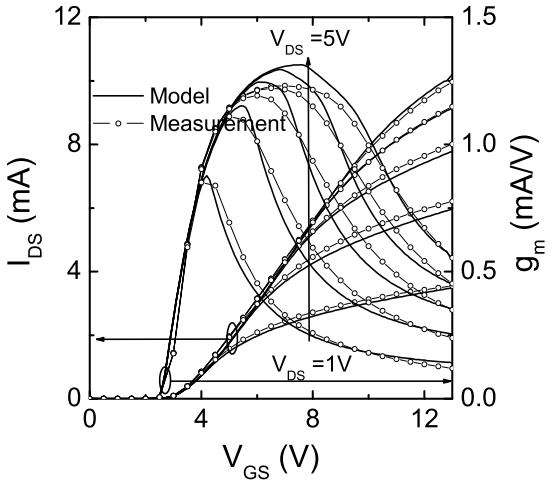


Figure 3.19: Transfer characteristics of 40V LDMOS device (W=40μm, L=1.2μm and N_F=1): I_{DS}-V_{GS} for V_{DS}=1V-5V in steps of 1V at T=30°C.

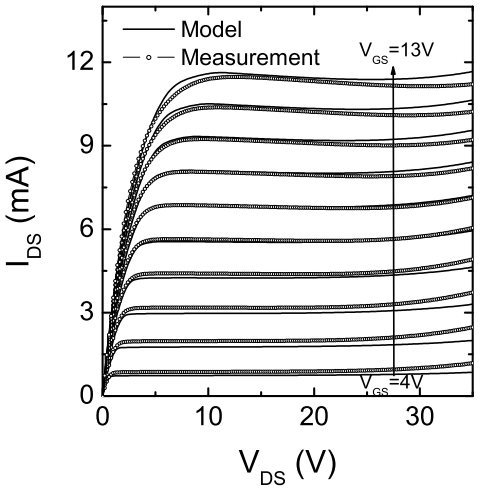
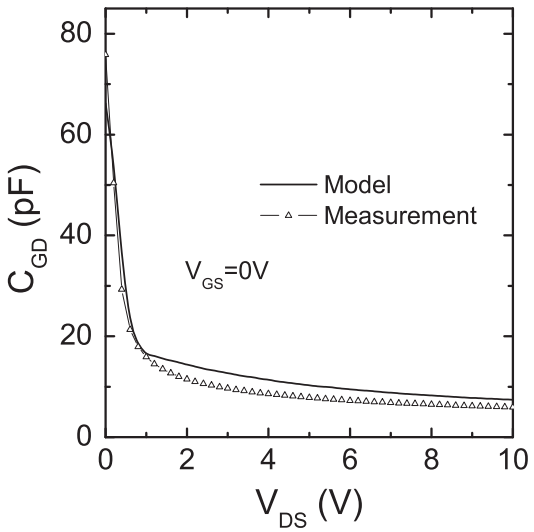
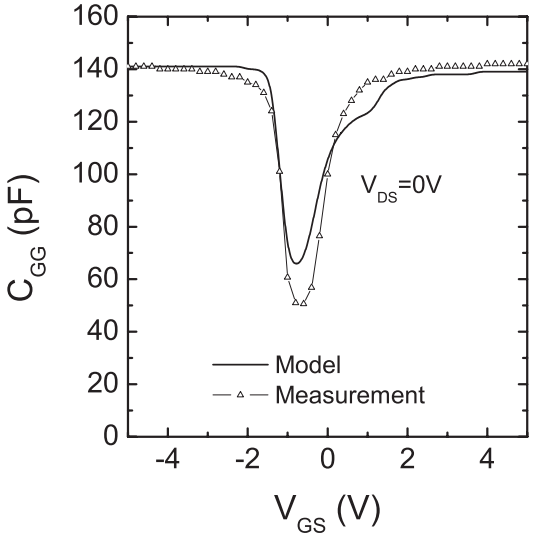


Figure 3.20: Output characteristics: I_{DS}-V_{DS} of 40V LDMOS device (W=40μm, L=1.2μm and N_F=1) at T=30°C. Note, the self-heating and impact ionization effects are correctly simulated.

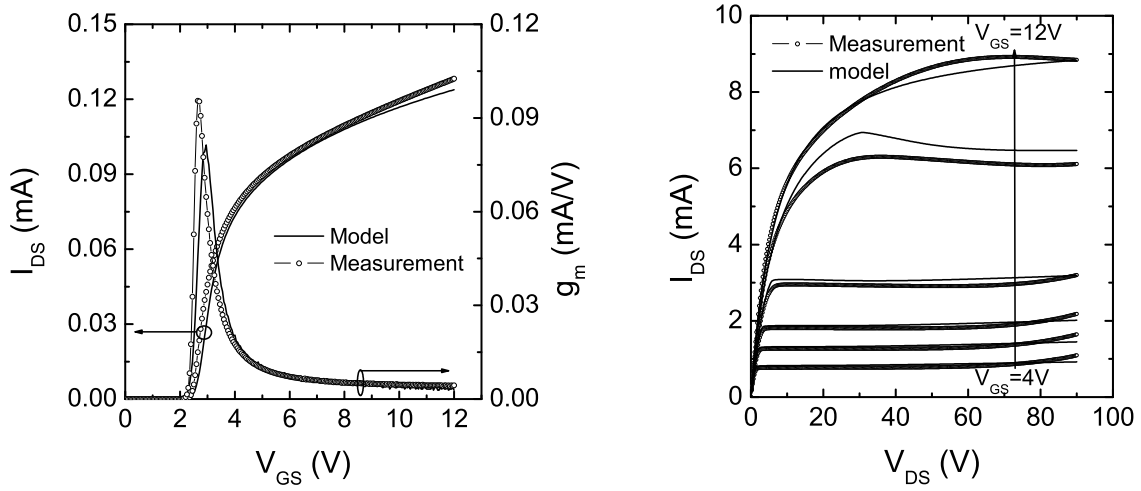


(a)



(b)

Figure 3.21: (a) Plot of C_{GD} vs. V_{DS} at V_{GS}=0V for 40V Bosch LDMOS device. (b) Plot of C_{GG} vs. V_{GS} at V_{DS}=0V for 40V Bosch LDMOS device.



(a) (b)

Figure 3.22: Drift Scaling (W=40μm, L=1.2μm and N_F=1 at T=30°C): (a) I_{DS}-V_{GS} and g_m-V_{GS} at $V_{DS} = 0.1V$, (b) I_{DS}-V_{DS} for V_{GS}=4, 4.5, 5, 6, 9 and 12V for 100V LDMOS device.

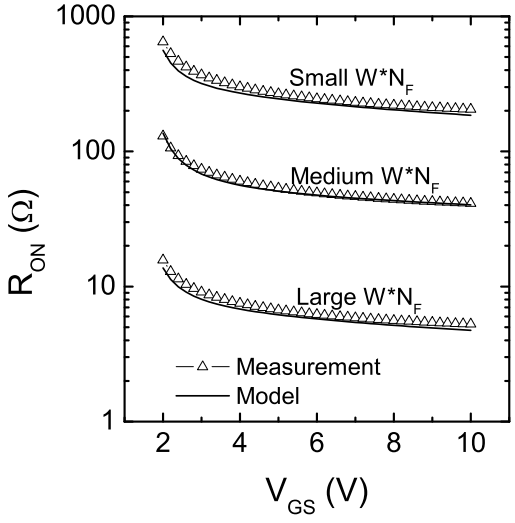


Figure 3.23: Width Scaling: R_{ON} vs. V_{GS} for three different $W * N_F$ for 40V LDMOS device at T=30°C.

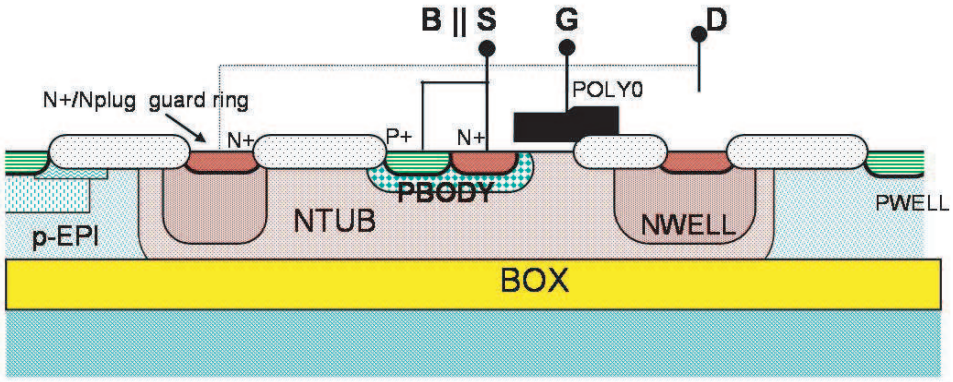
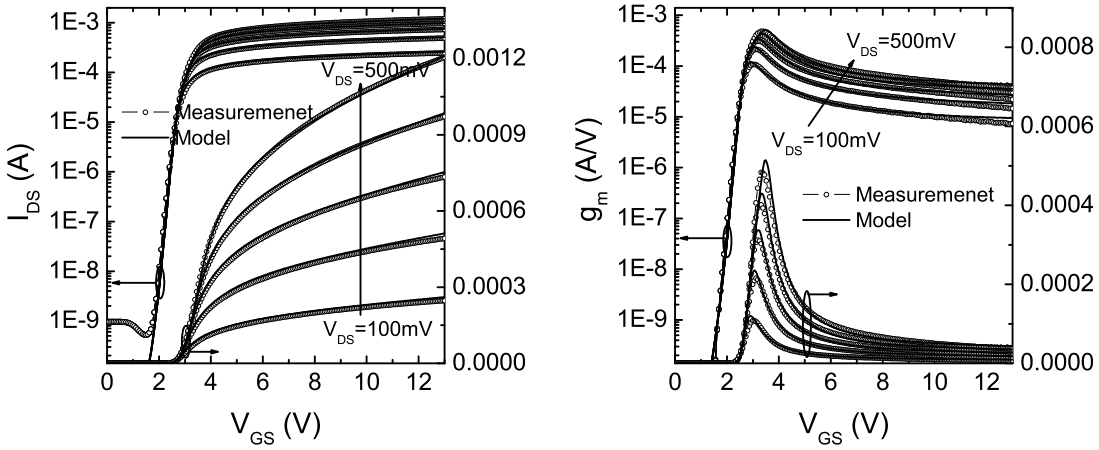


Figure 3.24: Schematic representation of 40V SOI-LDMOS transistor from I2T100 AMIS technology.



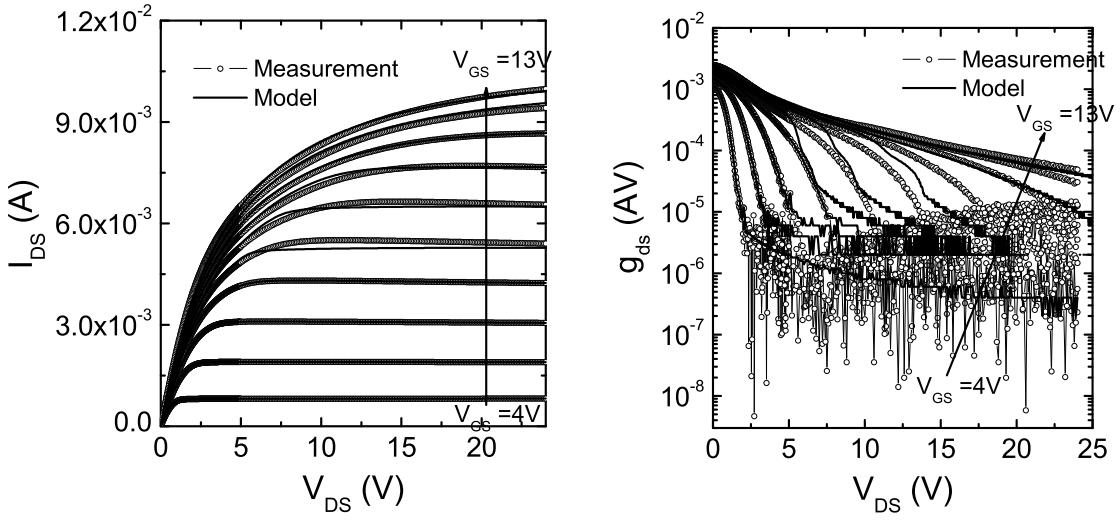
(a) (b)

Figure 3.25: Transfer characteristics of 40V SOI-LDMOS transistor from I2T100 AMIS technology (W=40μm, L=1.2μm): (a)$I_{DS} - V_{GS}$ and, (b) $g_m - V_{GS}$ for $V_{DS} = 0.1 - 0.5V$ in steps of $0.1V$. Note that, the value and position of the peaks on g_m has been modeled very well.

3.5.3 Case Study 3: SOI - LDMOS device

Fig. 3.24 shows the device architectures of SOI-LDMOS transistor [34] on AMIS technology.

The proposed model is also validated on the measured characteristics of SOI-LDMOS transistor from I2T100 AMIS technology. It should be noted that the model is same for all devices, thus showing the versatility of the model and hence called *general model*. Fig. 3.25 shows the $I_{DS} - V_{GS}$ and $g_m - V_{GS}$ characteristics for $V_{DS} = 0.1 - 0.5V$ in steps of $0.1V$. Fig. 3.26 (a) and (b) show the the output characteristics ($I_{DS} - V_{DS}$ and $g_{ds} - V_{DS}$) for $V_{GS} = 4 - 13V$. Note, significant quasi-saturation effect can be seen on the output characteristics at higher gate voltages. It can be seen that model shows good behavior across different gate and drain bias region.



(a) (b)

Figure 3.26: Output characteristics of 40V SOI-LDMOS transistor on I2T100 AMIS technology (W=40μm, L=1.2μm): (a)$I_{DS} - V_{DS}$ and, (b) $g_{ds} - V_{DS}$ for $V_{GS} = 4 - 13V$ in steps of $1V$.

Table 3.1: Main EKV Parameters

Name	Description	Units
TYPE	P-tpe/N-type	-
W	Channel Width	m
L	Channel Length	m
N_F	Number of fingers	-
COX	Oxide Capacitance	F/m^2
VT0	Long-channel Threshold Voltage	V
U0	Low Field mobility	cm^2/Vs
GAMMA	Body Effect Parameter	$\sqrt{V}$
PHI	Bulk Fermi Potential	V
E0	Mobility Reduction Coefficient	V/m
UCRIT	Longitudinal Critical Field	V/m
LAMBDA	Channel Length Modulation	-

3.6 Parameter Extraction and Model Calibration

Table 3.1, 3.2 and 3.3 show the list of main parameters used in the model. These basic parameters are used for modeling of any high voltage device at room temperature. The calibration procedure is described below and also shown in the flowchart (see Fig. 3.27). First threshold voltage and mobility is extracted using any standard extraction method [35, 36, 37, 38, 39]. Other standard EKV parameters [40] are extracted using methodology proposed in [41]. Once

Table 3.2: Drift Parameters

Name	Description	Units
L_{DR}	Drift length	m
L_{OV}	Gate overlap in the drift region	m
ρ_{Drift}	Drift resistivity	V-m/A
VSAT	Velocity saturation parameter	V/m
α_{vsat}	”	-
θ_{Acc}	Accumulation charge effect	1/V
k_{rd}	Effect of number of fingers	-
N_{CRIT}	”	-
α_T	Thermal coefficient of drift resistance	$1/K$

Table 3.3: Self-heating and impact ionization parameters

Name	Description	Units
R_{THNOM}	Thermal resistance	Ks/J
α	Temperature coefficient of R_{THNOM}	1/K
C_{TH}	Thermal capacitance	J/K
$NEFF$	Effective doping in the drift	$V^{-\frac{4}{3}}$

we have all of these parameters, $GAMMA$ and PHI are tuned for subthreshold slope on $I_{DS} - V_{GS}$ characteristics. $E0$ is tuned on $I_{DS} - V_{GS}$ characteristics in strong inversion for mobility degradation due to vertical field. $UCRIT$ and $LAMBDA$ are tuned on $I_{DS} - V_{DS}$ characteristics for velocity saturation and channel length modulation, respectively. Drift parameters $VSAT$ and α_{vsat} are fitted in the linear region of $I_{DS} - V_{DS}$ characteristics while θ_{Acc} is used to lower the drift resistance on $I_{DS} - V_{GS}$ characteristics at high V_{GS} as described earlier. k_{rd} and N_{CRIT} parameters are fitted to model the effect of number of fingers on drift resistance.

The extraction of self-heating parameters requires dedicated measurement setup. The extraction of thermal resistance and capacitance has been discussed in detail in [4, 23, 24, 42]. The impact ionization parameter N_{EFF} is used as a fitting parameter to model the impact ionization in the drift region.

Fig. 3.28 shows the worst case errors for transfer and output characteristics and also for their derivatives using proposed model on different HV-MOS architectures. The accuracy target required by the industry for high voltage models are also included in the figure [43]. It can be seen that model fulfils all the targets of the industrial model.

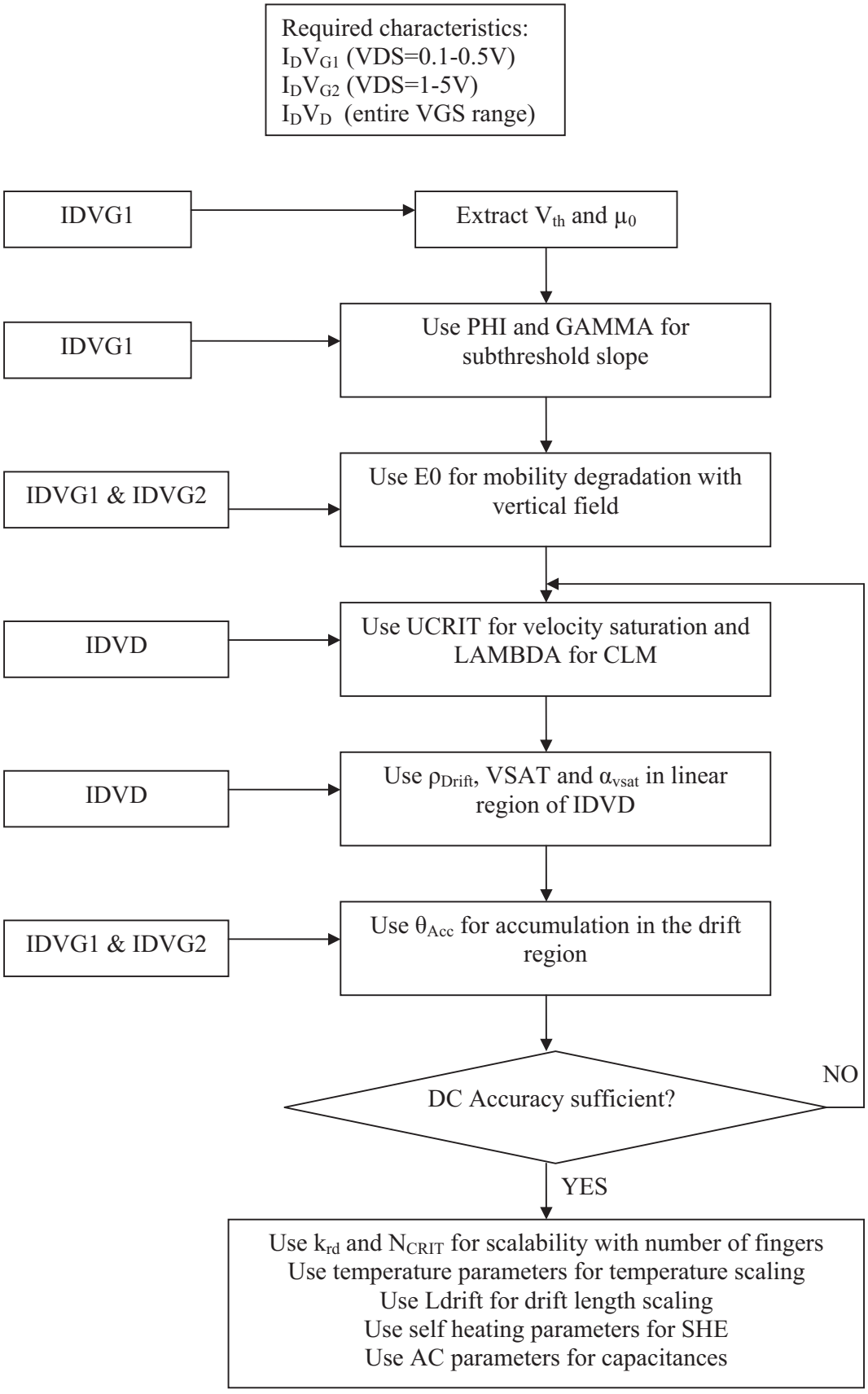


Figure 3.27: Flowchart of parameter extraction procedure.

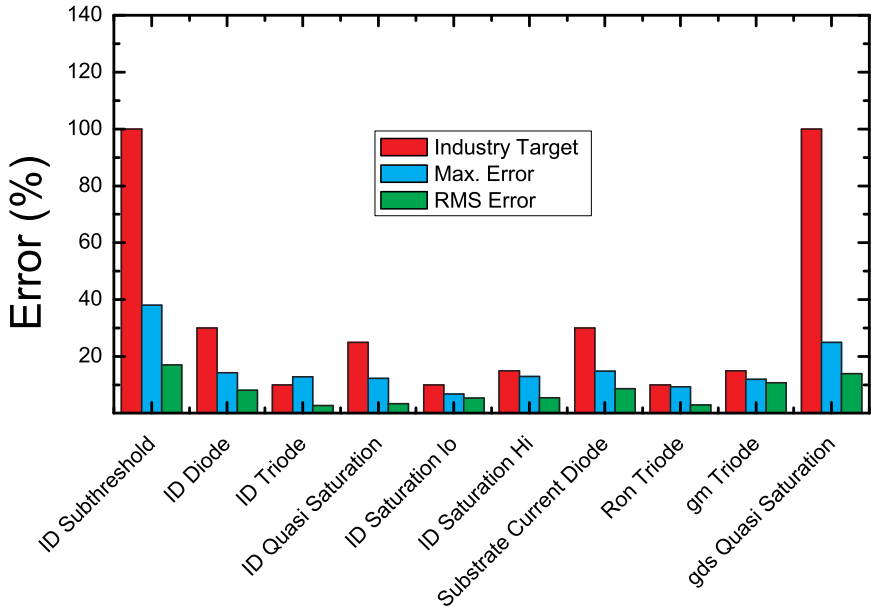


Figure 3.28: RMS and Max errors of the model.

3.7 Conclusion

A new *general* High Voltage MOSFET model based on the EKV model as a core and new bias dependent drift resistance is presented. The drift resistance includes major effects originating from the drift region like quasi-saturation and accumulation in the gate overlapped drift region. The impact ionization effect was modeled for both the regions i.e. the intrinsic MOSFET and the drift region, where impact ionization in the intrinsic MOSFET dominates at low to medium gate voltages while impact ionization at higher gate voltages is dominated by the drift region for higher drain voltages. The self heating effect was incorporated using sub-circuit approach. The thermal resistance and capacitance are dynamically varying with temperature inside the device giving better results compared to constant thermal resistance.

The model performance was demonstrated for three industrial devices: VDMOS, bulk-LDMOS and SOI-LDMOS. The model correctly reproduces the special effects of high voltage devices like the quasi-saturation and self-heating effect, and is highly scalable with all physical and electrical parameters such as transistor width, drift length, number of fingers and temperature. For the first time, the *scalability with drift length* in LDMOS transistor was demonstrated using this model. The model shows good results for entire DC bias range and good behavior for capacitances, especially the peaks and shift of these peaks with bias. The model provides excellent trade-off between speed, convergence and accuracy, being suitable for circuit simulation in any operation regime of HV MOSFETs. The model has been implemented in Verilog-A and tested on SABER (Synopsys), ELDO (Mentor Graphics) and Cadence‘s Virtuoso Spectre circuit simulator and Virtuoso UltraSim fast-Spice simulator for industrial use.

Bibliography

[1] A. Canepari, G. Bertrand, A. Giry, M. Minondo, F. Blanchet, H. Jaouen, B. Reynard, N. Jourdan, and J.-P. Chante, "LDMOS modeling for analog and RF circuit design," in *IEEE European Solid-State Device Research Conference (ESSDERC)*, Sept. 2005, pp. 469 – 472.

[2] S. Frere, P. Moens, B. Desoete, D. Wojciechowski, and A. Walton, "An improved LDMOS transistor model that accurately predicts capacitance for all bias conditions," in *Proceedings of the 2005 International Conference on Microelectronic Test Structures (ICMTS)*, April 2005, pp. 75 – 79.

[3] N. D'Halleweyn, J. Benson, W. Redman-White, K. Mistry, and M. Swanenberg, "MOOSE: a physically based compact DC model of SOI LD MOSFETs for analogue circuit simulation," *IEEE Transactions Computer-Aided Design of Integrated Circuits and Systems*, vol. 23, no. 10, pp. 1399–1410, Oct. 2004.

[4] C. Anghel, "High voltage devices for standard MOS technologies : characterisation and modelling," Ph.D. dissertation, EPFL, 2004, thesis No. 3116.

[5] N. Hefyene, C. Anghel, A. Ionescu, S. Frere, R. Gillon, M. Vermandel, B. Bakeroot, and J. Doutreloigne, "An experimental approach for bias-dependent drain series resistances evaluation in asymmetric HV MOSFETs," in *IEEE European Solid-State Device Research Conference (ESSDERC)*, Sept. 2001, pp. 403 – 406.

[6] N. Hefyene, "Electrical characterization and modelling of lateral DMOS transistor : investigation of capacitances and hot-carrier impact," Ph.D. dissertation, EPFL, 2005, thesis No. 3200.

[7] A. Aarts, N. D'Halleweyn, and R. van Langevelde, "A surface-potential-based high-voltage compact LDMOS transistor model," *IEEE Transactions Electron Devices*, vol. 52, no. 5, pp. 999 – 1007, May 2005.

[8] A. Aarts and W. Kloosterman, "Compact modeling of high-voltage LDMOS devices including quasi-saturation," *IEEE Transactions Electron Devices*, vol. 53, no. 4, pp. 897 – 902, April 2006.

[9] J. Victory, J. Sanchez, T. DeMassa, and B. Welfert, "A static, physical VDMOS model based on the charge-sheet model," *IEEE Transactions Electron Devices*, vol. 43, no. 1, pp. 157 – 164, Jan. 1996.

[10] C.-Y. Tsai, D. E. Burk, and K. D. T. Ngo, "Physical Modeling of the Power VDMOST for Computer-Aided Design of Integrated Circuit," *IEEE Transactions Electron Devices*, vol. 44, no. 3, pp. 472 – 480, March 1997.

[11] Y. S. Chauhan, C. Anghel, F. Krummenacher, R. Gillon, A. Baguenier, B. Desoete, S. Frere, A. M. Ionescu, and M. Declercq, "A Compact DC and AC Model for Circuit Simulation of High Voltage VDMOS Transistor," in *IEEE International Symposium on Quality Electronic Design (ISQED)*, March 2006, pp. 109–114.

[12] Y. S. Chauhan, C. Anghel, F. Krummenacher, A. M. Ionescu, M. Declercq, R. Gillon, S. Frere, and B. Desoete, "A Highly Scalable High Voltage MOSFET Model," in *IEEE European Solid-State Device Research Conference (ESSDERC)*, Sept. 2006, pp. 270 – 273.

[13] C. Enz, F. Krummenacher, and E. Vittoz, "An analytical MOS transistor model valid in all regions of operation and dedicated to low-voltage and low-current applications," *Journal on Analog Integrated Circuits and Signal Processing*, vol. 8, no. 1, pp. 83–114, July 1995.

[14] Y. S. Chauhan, C. Anghel, F. Krummenacher, C. Maier, R. Gillon, B. Bakeroot, B. Desoete, S. Frere, A. B. Desormeaux, A. Sharma, M. Declercq, and A. M. Ionescu, "Scalable General High Voltage MOSFET Model including Quasi-Saturation and self-heating effect," *Solid State Electronics*, vol. 50, no. 11-12, pp. 1801–1813, 2006.

[15] Y. S. Chauhan, R. Gillon, B. Bakeroot, F. Krummenacher, M. Declercq, and A. M. Ionescu, "An EKV-based High Voltage MOSFET Model with improved mobility and drift model," *Solid State Electronics*, 2007.

[16] Y. S. Chauhan, C. Anghel, F. Krummenacher, A. Ionescu, M. Declercq, R. Gillon, S. Frere, B. Desoete, B. Bakeroot, and C. Maier, "Ekv based dmos model extension for v-dmos," , http://www-g.eng.cam.ac.uk/robuspic/reports.htm, 2004-2006.

[17] ——, "Ekv based l-dmos model update including internal temperatures," , http://www-g.eng.cam.ac.uk/robuspic/reports.htm, 2004-2006.

[18] C. Anghel, N. Hefyene, A. Ionescu, M. Vermandel, B. Bakeroot, J. Doutreloigne, R. Gillon, S. Frere, C. Maier, and Y. Mourier, "Investigations and Physical Modelling of Saturation Effects in Lateral DMOS Transistor Architectures Based on the Concept of Intrinsic Drain Voltage," in *IEEE European Solid-State Device Research Conference (ESSDERC)*, Sept. 2001, pp. 399 – 402.

[19] N. Hefyene, E. Vestiel, B. Bakeroot, C. Anghel, S. Frere, A. Ionescu, and R. Gillon, "Bias-dependent drift resistance modeling for accurate DC and AC simulation of asymmetric HV-MOSFET," in *IEEE International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)*, Sept. 2002, pp. 203 – 206.

[20] C. Anghel, Y. S. Chauhan, N. Hefyene, and A. Ionescu, "A physical analysis of HV MOSFET capacitance behaviour," in *IEEE International Symposium on Industrial Electronics (ISIE)*, vol. 2, June 2005, pp. 473 – 477.

[21] J.-M. Sallese, M. Bucher, F. Krummenacher, and P. Fazan, "Inversion charge lineariazation in MOSFET modeling and rigorous derivation of the EKV compact model," *Solid-State Electronics*, vol. 46, no. 11, pp. 677–683, April 2003.

[22] C. Kreuzer, N. Krischke, and P. Nance, "Physically based description of quasi-saturation region of vertical DMOS power transistors," in *IEEE International Electron Devices Meeting (IEDM)*, Dec. 1996, pp. 489 – 492.

[23] C. Anghel, N. Hefyene, R. Gillon, M. Tack, M. Declercq, and A. Ionescu, "New method for temperature-dependent thermal resistance and capacitance accurate extraction in high-voltage DMOS transistors," in *IEEE International Electron Devices Meeting (IEDM)*, Dec. 2003, pp. 5.6.1 – 5.6.4.

[24] C. Anghel, R. Gillon, and A. Ionescu, "Self-heating characterization and extraction method for thermal resistance and capacitance in HV MOSFETs," *IEEE Electron Device Lett.*, vol. 25, no. 3, pp. 141 – 143, March 2004.

[25] P. Rossel, H. Tranduc, D. Montcoqut, G. Charitat, and I. Pages, "Avalanche characteristics of MOS transistors," in *IEEE International Conference on Microelectronics*, vol. 1, Sept. 1997, pp. 371 – 381.

[26] Y. S. Chauhan, F. Krummenacher, C. Anghel, R. Gillon, B. Bakeroot, M. Declercq, and A. M. Ionescu, "Analysis and Modeling of Lateral Non-Uniform Doping in High-Voltage MOSFETs," in *IEEE International Electron Devices Meeting*, Dec. 2006, pp. 8.3.1 – 8.3.4.

[27] Y. S. Chauhan, F. Krummenacher, R. Gillon, B. Bakeroot, M. Declercq, and A. M. Ionescu, "A New Charge based Compact Model for Lateral Asymmetric MOSFET and its application to High Voltage MOSFET Modeling," in *IEEE International Conference on VLSI Design and International Conference on Embedded Systems*, Jan. 2007, pp. 177 – 182.

[28] ——, "Compact Modeling of Lateral Non-uniform doping in High-Voltage MOSFETs," *IEEE Transactions on Electron Devices*, vol. 54, no. 6, pp. 1527–1539, June 2007.

[29] F. Heiman and H. Miiller, "Temperature dependence of n-type MOS transistors," *IEEE Transactions on Electron Devices*, vol. 12, no. 3, pp. 142– 148, Mar 1965.

[30] Z. D. Prijic, S. S. Dimitrijev, and N. D. Stojadinovic, "The determination of zero temperature coefficient point in CMOS transistors," *Microelectronics and Reliability*, vol. 32, no. 6, pp. 769–773, June 1992.

[31] I. Filanovsky and L. Najafizadeh, "Zeroing in on a zero-temperature coefficient point," in *IEEE Midwest Symposium on Circuits and Systems (MWSCAS)*, Aug. 2002, pp. I–271–4.

[32] C. H. Ling, "Observation of zero temperature coefficient of capacitance in the MOS capacitor," *Solid-State Electronics*, vol. 32, no. 11, pp. 1043–1044, November 1989.

[33] L. Najafizadeh and I. Filanovsky, "A simple voltage reference using transistor with ZTC point and PTAT current source," in *IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2004, pp. I– 909–11.

[34] F. Udrea, D. Garner, K. Sheng, A. Popescu, H. Lim, and V. Milne, "SOI power devices," *IEE Electronics & Communication Engineering Journal*, vol. 12, no. 1, pp. 27–40, 2000.

[35] C. Anghel, B. Bakeroot, Y. S. Chauhan, R. Gillon, C. Maier, P. Moens, J. Doutreloigne, and A. Ionescu, "New Method for Threshold Voltage Extraction of High-Voltage MOSFETs Based on Gate-to-Drain Capacitance Measurement," *IEEE Electron Device Letters*, vol. 27, no. 7, pp. 602 – 604, July 2006.

[36] A. Ortiz-Conde, F. G. Sanchez, A. Cerdeira, M. Estrada, D. Flandre, and J. Liou, "A procedure to extract mobility degradation, series resistance and threshold voltage of SOI MOSFETs in the saturation region," in *IEEE International Conference on Solid-State and Integrated-Circuit Technology*, Oct. 2001, pp. 887– 890.

[37] B. Cretu, T. Boutchacha, G. Ghibaudo, and F. Balestra, "New ratio method for effective channel length and threshold voltage extraction in MOS transistors," *Electronics Letters*, vol. 37, no. 11, pp. 717–719, May 2001.

[38] G. Ghibaudo, "New method for the extraction of MOSFET parameters," *Electronics Letters*, vol. 24, no. 9, pp. 543–545, Apr 1988.

[39] Y. Y. Z. Kong, F.C.J.; Yeow, "Extraction of MOSFET threshold voltage, series resistance, effective channel length, and inversion layer mobility from small-signal channel conductance measurement," *IEEE Transactions on Electron Devices*, vol. 48, no. 12, pp. 2870–2874, Dec 2001.

[40] "Ekv mos model," , http://legwww.epfl.ch/ekv.

[41] M. Bucher, C. Lallement, and C. C. Enz, "An efficient parameter extraction methodology for the EKV MOST model," in *IEEE International Conference on Microelectronic Test Structures (ICMTS)*, March 1996, pp. 145 – 150.

[42] C. Anghel, A. Ionescu, N. Hefyene, and R. Gillon, "Self-heating characterization and extraction method for thermal resistance and capacitance in high voltage MOSFETs," in *IEEE European Solid-State Device Research Conference (ESSDERC)*, Sept. 2003, pp. 449 – 452.

[43] "Robuspic (robust mixed signal design methodologies for smart power ics)," , http://www-g.eng.cam.ac.uk/robuspic, 2004-2006.

Chapter 4

Compact Modeling of Lateral Non-uniform doping

Here the detailed analysis and modeling of lateral non-uniform doping present in the intrinsic MOS channel of high voltage MOSFETs e.g. VDMOS and LDMOS is presented. It is shown that the conventional long channel MOSFET models using uniform lateral doping can never correctly model the capacitance behavior of these devices. A new analytical compact model for lateral non-uniformly doped MOSFET is developed [1, 2, 3, 4]. The intrinsic non-uniformly doped MOS model is first validated on the numerical simulation and then on measured characteristics of VDMOS and LDMOS transistors including drift region. The model shows good results in DC and, most importantly in AC regime, especially in simulating the peaks on C_{GD}, C_{GS} and C_{GG} capacitances. This new model improves the accuracy of high voltage MOS models, especially output characteristics and during transient response (i.e. amplitude and position of peaks as well as slope of capacitances).

4.1 Introduction

The lateral non-uniformly doped MOSFET or Lateral Asymmetric MOSFET (LAMOS), which has longitudinal doping variation in the channel, is the building block of many categories of high-voltage MOSFETs e.g. LDMOS and VDMOS transistors [5, 6, 7, 8, 9, 10]. The lateral asymmetric channel devices have also caught attention in deep sub-micron devices for higher performance in analog, RF and mixed signal design [11, 12, 13, 14]. In fact, lateral non-uniform doping is inherent in halo-doped nano-MOSFETs [15, 16, 17]. Recently physical modeling of LAMOS has received considerable attention as the Compact Modeling Council (CMC) [18] has started efforts to get a compact physical model for LDMOS as an industry standard model. Very few models have been reported [6, 7] in the literature for modeling of lateral non-uniform doping while majority of the models published [5, 6, 7, 19, 20, 21, 22, 23, 24, 25] use constant doping in the channel. Accurate modeling of the capacitances in high-voltage devices is a prerequisite for integrated RF design of, for instance, switched-mode power supplies and power amplifiers.

Modeling of LAMOS has been a great challenge due to the lateral doping gradient in the channel region. The main difficulty in the modeling of LAMOS arises as expressions become

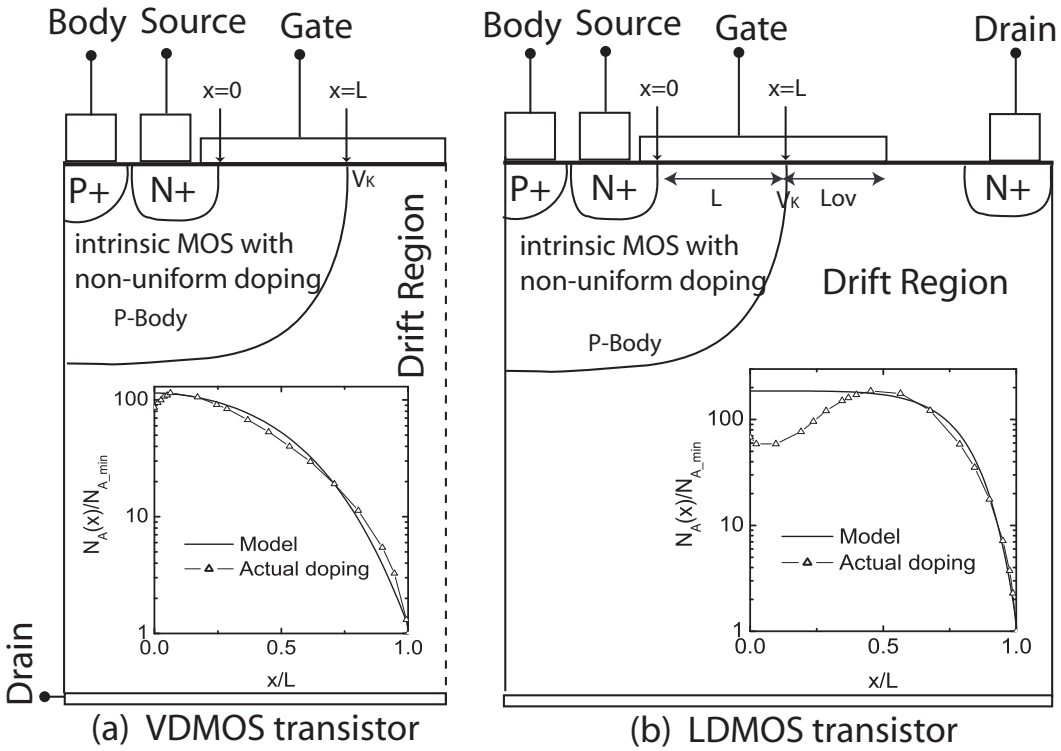


Figure 4.1: Schematic representation of VDMOS and LDMOS transistors. Note that the intrinsic MOS has a lateral doping gradient. The channel extends from x=0 to L. L_{ov} is the gate overlap in the drift region. Figures in the inset show the doping profiles normalized by $min\{N_A(x = L)\}$ in the AMI Semiconductor devices. Solid line in the doping profile represents the function $\left\{N_A(x) = N_S.erfc\left[k_n(\frac{x}{L})^a\right]\right\}$ used to model the doping in the channel. N_S is taken as highest doping in the channel, which is generally near source end of the channel. k_n and a are the parameters.

non-integrable/non-implicit due to the lateral asymmetry in the channel. In this chapter, a new compact model for LAMOS is derived in detail [1, 2, 3, 4]. Furthermore, the intrinsic LAMOS model is validated on the numerical device simulation of LAMOS structure, while the LAMOS along with the drift region is validated on the measured characteristics of LDMOS and VDMOS transistors with laterally diffused channel doping profile. The source and body are tied to avoid parasitic bipolar transistor for all measurements.

4.2 Modeling of Lateral Non-uniform doping

Fig. 4.1 shows the schematic representation of VDMOS (half of the device) and LDMOS transistors. In the inset of both figures, the lateral non-uniform doping profile of the respective devices along the channel is also shown. The doping level at the source side of the channel is highest and decreases towards the drain in the channel region. The lateral doping gradient is approximated by the complementary error function $N_A(x) = N_S.erfc[k_n(\xi)^a]$, where $\xi = \frac{x}{L}$ is the normalized position along the channel, k_n is a parameter representing the doping gradient and a is a fitting parameter. Higher k_n means sharp decrease in the doping level from source to

drain and vice-versa.

The well-known drift-diffusion current expression is given by

$$I_{DS} = I_{Drift} + I_{Diff} = \mu W \left(-Q_i \frac{d\Psi_S}{dx} + U_T \frac{dQ_i}{dx} \right) \tag{4.1}$$

where, μ, W, Q_i, and Ψ_S are the mobility, width, inversion charge, and surface potential, respectively, at any position x in the channel. The thermal voltage has been denoted by U_T. The inversion charge linearization relation between Q_i and Ψ_S using EKV formalism [26, 27] can be expressed as

$$-Q_i = n_q C_{ox}(\Psi_P - \Psi_S) \tag{4.2}$$

where slope factor n_q and pinch-off surface potential Ψ_P are defined as [26, 27]

$$n_q = 1 + \frac{\Gamma}{\sqrt{\Psi}_P + \sqrt{\Psi_P + U_T(q_s + q_d)}} \tag{4.3}$$

$$V_G - V_{FB} = \Psi_P + sign(\Psi_P)\Gamma\sqrt{U_T e^{-\frac{\Psi_P}{U_T}} + \Psi_P - U_T} \tag{4.4}$$

where C_{ox} and Γ are the oxide capacitance per unit area and body effect coefficient, respectively. The q_d and q_s are the normalized charge densities at drain and source, respectively, described later in this section. Note that the Ψ_P is a function of x now, while in a conventional long channel MOSFET, it is independent of x. The approximate solution of the transcendental equation of Ψ_P or ψ_p is given in Appendix A.

The first order mobility model can be derived as follows [28]

$$\mu = \frac{v_{drift}}{E_x} = \frac{\mu_v}{1 + \left|\frac{E_x}{E_c}\right|} = \frac{\mu_v}{1 + \left|\frac{d\Psi_S / dx}{v_{sat} / \mu_v}\right|} \tag{4.5}$$

where

$$\mu_v = \frac{v_{sat}}{E_c} = \left[\frac{1 + \left(\frac{E_{ref}}{E_{ph}}\right)^{\alpha_{ph}} + \left(\frac{E_{ref}}{E_{sr}}\right)^{\alpha_{sr}}}{1 + \left(\frac{E_{eff}}{E_{ph}}\right)^{\alpha_{ph}} + \left(\frac{E_{eff}}{E_{sr}}\right)^{\alpha_{sr}}} \right] \mu_0 = \rho_v \mu_0 \tag{4.6}$$

where v_{drift}, v_{sat}, E_x and E_c are the drift velocity, saturation velocity, longitudinal electric field and critical electric field, respectively. The mobility μ_v is a function of the vertical electric field only, through ρ_v, where ρ_v is a function of bias condition and doping level. To simplify the expressions into compact form, we will assume that ρ_v is independent of doping variation in the channel and only a function of vertical electrical field. Without loss of generality, the low field mobility μ_0 is considered constant along the channel and defined at $E_{eff} = E_{ref}$, where E_{ref} is the reference electric field. E_{ph}, α_{ph} are electric field and exponent, respectively, related to phonon scattering and E_{sr}, α_{sr} are the electric field and exponent, respectively, related to surface roughness [28]. From (5.3), (5.7) and (4.6), I_{DS} can be written as

$$I_{DS} = \frac{\mu_v}{1 + \frac{\mu_v}{v_{sat}}\left|\frac{d\Psi_s}{dx}\right|} W \left(-Q_i \frac{d\Psi_s}{dx} + U_T \frac{dQ_i}{dx} \right) \tag{4.7}$$

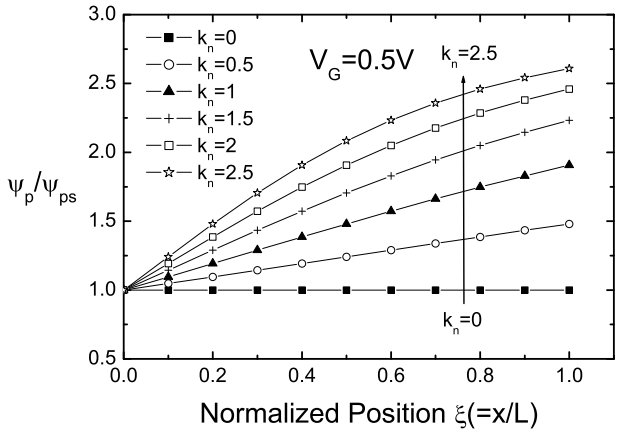


Figure 4.2: Plot of pinch off potential normalized to pinch off potential at source end ($\frac{\psi_p}{\psi_{ps}}$) vs. normalized position ($\xi = x/L$) along the channel for different values of doping gradients. The doping at the source (N_S) is taken as $5 \cdot 10^{16} cm^{-3}$. Here $k_n = 0$ refers to the case of conventional MOSFET. Note that ψ_p is almost linear along the channel for different values of k_n.

Using (4.2) and (4.6) for $\frac{d\Psi_s}{dx} > 0$, (4.7) can be rewritten as

$$\frac{dq}{d\xi} = -\frac{i_{ds} + \rho_v \left(i_{ds}\frac{\delta_{sat}}{2} - q\right)\frac{d\Psi_p}{d\xi}}{\rho_v \left(1 + 2q - \delta_{sat} i_{ds}\right)} \tag{4.8}$$

where variables and constants are normalized from EKV formalism [26, 27] as follows

$$q = \frac{-Q_i}{2n_q C_{ox} U_T}, i_{ds} = \frac{I_{DS}}{2n_q \frac{W}{L}\mu_0 C_{ox} U_T^2}, \delta_{sat} = \frac{2\mu_0 U_T}{v_{sat} L}, \psi_p = \frac{\Psi_P}{U_T}. \tag{4.9}$$

Notice that q, i_{ds}, δ_{sat}, ψ_p and ρ_v are all dimensionless quantities. The relation between normalized inversion charge density q and normalized current i_{ds} given by (4.8) cannot be solved analytically as it is a nonlinear ODE of q, where ψ_p [26, 27] is a function of normalized position ξ in the channel.

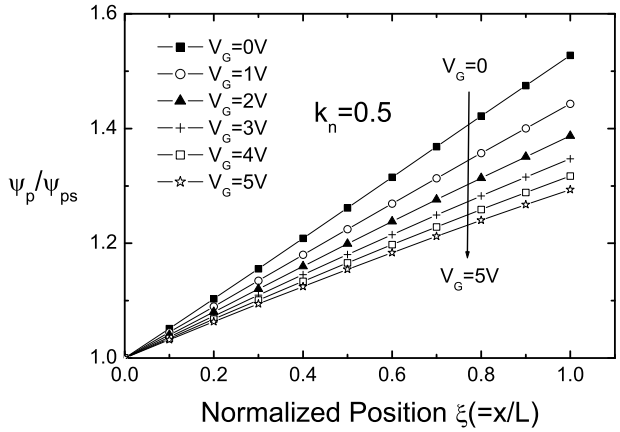
Following approximations are made to solve this differential equation (4.8).

a) The slope factor n_q is independent of position ξ. Although n_q is a function of doping through Ψ_P and Γ in (5.5), dependence of n_q on ξ is weak.

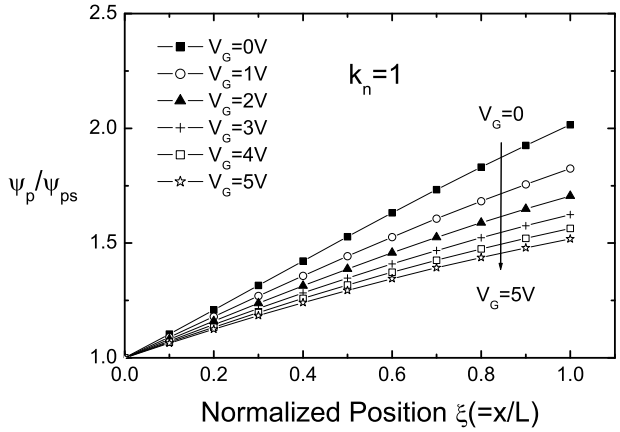
b) $\frac{d\psi_p}{d\xi}$ is assumed to be independent of ξ (i.e. $\frac{d\psi_p}{d\xi} = \Delta\psi_p$ is constant with ξ). In other words, ψ_p varies linearly with ξ. The above assumption holds very good for the entire practical range of k_n(=0-2.5) as shown in Fig. 4.2 and 4.3.

Using above approximations, (4.8) is integrated along the channel from $\xi = 0$ to $\xi = 1$, to obtain the drain to source current i_{ds} and total normalized inversion charge density q_c in the channel as

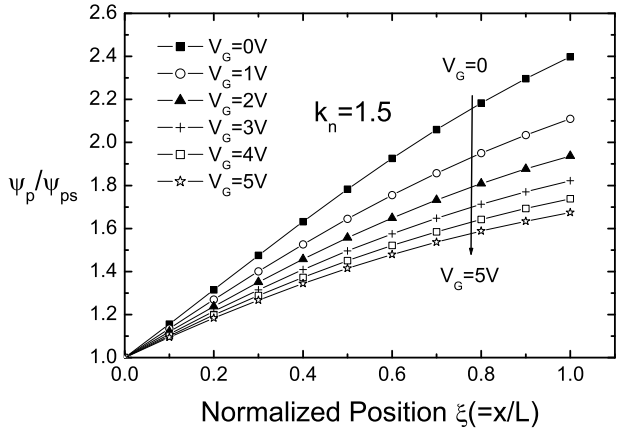
$$\Delta\psi_p = 2(q_d - q_s) + \left(1 + \frac{2i_{ds}}{\rho_v \Delta\psi_p}\right) \cdot \left[\ln\left(\frac{q_d - i_{ds}\left(\frac{1}{\rho_v \Delta\psi_p} + \frac{\delta_{sat}}{2}\right)}{q_s - i_{ds}\left(\frac{1}{\rho_v \Delta\psi_p} + \frac{\delta_{sat}}{2}\right)}\right)\right] \tag{4.10}$$



(a)



(b)



(c)

Figure 4.3: Plot of pinch off potential normalized to pinch off potential at source end ($\frac{\psi_p}{\psi_{ps}}$) vs. normalized position ($\xi = x/L$) along the channel for V_G=0 to 5V (covering weak-moderate-strong inversion) in steps of 1V for (a) k_n=0.5, (b) k_n=1, (a) k_n=1.5. The doping at the source (N_S) is taken as $5 \cdot 10^{16} cm^{-3}$. It demonstrate that the approximation $\frac{d\psi_p}{d\xi} = \Delta\psi_p$ is constant with ξ holds true for different values of doping gradients and gate biases.

$$q_c = \int_0^1 q d\xi = \frac{1}{\Delta\psi_p}\left[\left(q_d^2 - q_s^2\right) + \left(q_d - q_s\right)\left(1 - i_{ds}\delta_{sat}\right)\right] + \left[i_{ds}\left(\frac{1}{\rho_v \Delta\psi_p} + \frac{\delta_{sat}}{2}\right)\right]. \quad (4.11)$$

The normalized charge densities at drain (q_d) and source (q_s) are defined as [26]

$$2q_d + \ln(q_d) = v_p - v_d, \quad (4.12)$$

$$2q_s + \ln(q_s) = v_p - v_s. \quad (4.13)$$

where $v_d = \frac{V_D}{U_T}$, $v_s = \frac{V_S}{U_T}$ are the normalized bias voltages and v_p is the normalized pinch off voltage and defined as [26]

$$v_p = \psi_p - \psi_0, \quad (4.14)$$

where ψ_0 is the inversion surface potential and defined as [26]

$$\psi_0 = 2\phi_f + mU_T \quad (4.15)$$

Where m is few U_T or more accurate value can be obtained from [26]. The normalized bulk Fermi potential $\phi_f = ln\left(\frac{N_A}{n_i}\right)$ is assumed to be constant along the channel and taken as the value at source end i.e. $\phi_f = ln\left(\frac{N_S}{n_i}\right)$. The approximate solutions of transcendental equations of q_s or q_d is given in Appendix A.

It should be noted that the expression for current (4.10) is not an explicit function. To derive an explicit expression for current, we use interpolation between asymptotic behavior in linear and saturation region on $i_{ds} - v_{ds}$ characteristics. Using an interpolation function, i_{ds} can be written as

$$i_{ds} = g_{on}\frac{v_d - v_s}{\left[1 + \left(\frac{v_d - v_s}{v_{dsat}}\right)^n\right]^{\frac{1}{n}}} \quad (4.16)$$

where v_{dsat} is the normalized saturation voltage and can be expressed as,

$$v_{dsat} = \frac{i_{dsat}}{g_{on}}. \quad (4.17)$$

Additionally, from (4.10), the small signal conductance at $v_{ds} = 0$ is found to be,

$$g_{on} = \left.\frac{\partial i_{ds}}{\partial v_d}\right|_{v_{ds}=0.} = \left.\frac{\rho_v \Delta\psi_p q_s}{\left(1 + \frac{\delta_{sat}\rho_v\Delta\psi_p}{2}\right)\left(1 - \frac{q_s}{q_d}\right) - 2q_s ln\left(\frac{q_s}{q_d}\right)}\right|_{v_{ds}=0} \quad (4.18)$$

It should be noted that the interpolation function used in (4.16) is an infinitely differentiable mathematical smoothing function and n is an empirical fitting parameter, which can take any positive number. The larger the value of n, the more abrupt is the transition from linear to saturation on $i_{ds} - v_{ds}$ characteristics and vice-versa. The normalized saturation current i_{dsat} is evaluated iteratively from (4.10), by knowing the normalized inversion charge density at drain end of the channel in saturation ($q_{dsat} = \frac{\delta_{sat} i_{dsat}}{2}$). It is observed that within 2-3 iterations, accuracy on i_{dsat} is better than 0.01% compared with numerical solution of (4.10). Once we

know i_{ds} from (4.16), the total normalized inversion charge density q_c can be evaluated from (5.17).

The gate charge density at any position in the channel can be expressed as

$$Q'_g = C_{ox}\left(V_G - V_{FB} - \Psi_S\right). \tag{4.19}$$

The normalization of (4.19) and using (4.2) gives

$$q'_g = \frac{Q'_g}{C_{ox}U_T} = \left(v_g - v_{fb} - \psi_p + 2q\right) \tag{4.20}$$

where $v_g = \frac{V_G}{U_T}$, $v_{fb} = \frac{V_{FB}}{U_T}$ are the normalized gate and flat-band voltage, respectively. Integrating (4.20) from source to drain provides the total gate charge density in the channel as

$$q_g = v_g - \overline{v_{fb}} - \overline{\psi_p} + 2q_c \tag{4.21}$$

where $\overline{v_{fb}} = \frac{v_{fbs}+v_{fbd}}{2}$ and $\overline{\psi_p} = \frac{\psi_{ps}+\psi_{pd}}{2}$ are the arithmetic mean of the flat band voltage [29] and normalized pinch off potential, respectively, at source and drain. The final expressions for drain to source current, total inversion charge, total bulk charge and total gate charge in the LAMOS can be written as,

$$I_D = \left(2n_q\frac{W}{L}\mu_0 C_{ox}U_T^2\right) i_{ds} \tag{4.22}$$

$$Q_I = -\left(2n_q WLC_{ox}U_T\right) q_c \tag{4.23}$$

$$Q_B = -WLC_{ox}U_T\left[v_g - \overline{v_{fb}} - \overline{\psi_p} - 2\left(n_q - 1\right) q_c\right] \tag{4.24}$$

$$Q_G = WLC_{ox}U_T\left(V_{GS} - \overline{v_{fb}} - \overline{\psi_p} + 2q_c\right) \tag{4.25}$$

Even though we have obtained the expressions for Q_G and Q_B (which gives all capacitances related to gate and body node), the question which remains open is how to get the drain charge (Q_D) and source charge (Q_S), which in turn can be used for the evaluation of trans-capacitances (e.g. C_{DG}, C_{SG} etc.). Recently, it has been shown that the large signal drain and source charges do not exist for LAMOS [30, 31] and the famous Ward-Dutton charge partitioning approach [32] is not valid for LAMOS. The trans-capacitance evaluation using small signal analysis has been explained in [30, 31]. We have recently proposed a new partitioning scheme for LAMOS [33], which can be used for the evaluation of trans-capacitances. This novel development will be explained in Chapter 6.

4.3 DISCUSSION and RESULTS

4.3.1 Validation of the LAMOS model on numerical device simulation

The proposed compact model for the LAMOS device is validated on numerical device simulations performed with ISE-DESSIS. The doping level at the source end of the channel is kept at $5 \cdot 10^{16} cm^{-3}$ and value of k_n is chosen as 1.5, generally used in the 50V VDMOS devices in the industry [34, 35]. Fig. 4.4 and fig. 4.5 show the $I_{DS} - V_{GS}$ and $g_m - V_{GS}$ characteristic for V_{DS}=50mV. The model exhibits good trend for the subthreshold slope and values at higher

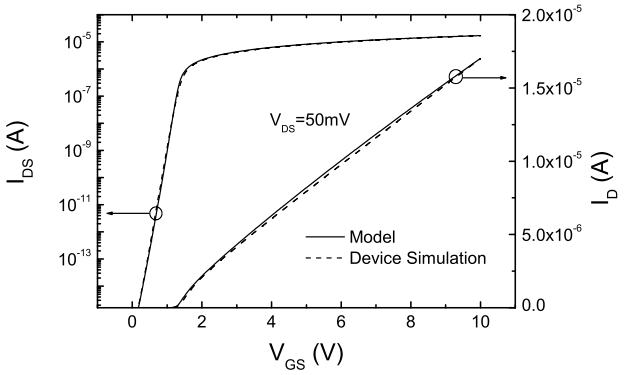


Figure 4.4: Drain current I_{DS} vs. gate voltage V_{GS} for V_{DS}=50mV on linear and logarithmic scale ($L = 2\mu m$, $N_S = 5 \cdot 10^{16} cm^{-3}$ and $k_n = 1.5$).

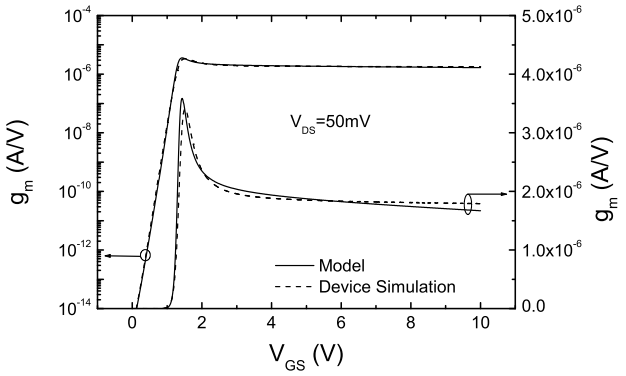


Figure 4.5: Transconductance g_m vs. gate voltage V_{GS} for V_{DS}=50mV ($L = 2\mu m$, $N_S = 5 \cdot 10^{16} cm^{-3}$ and $k_n = 1.5$).

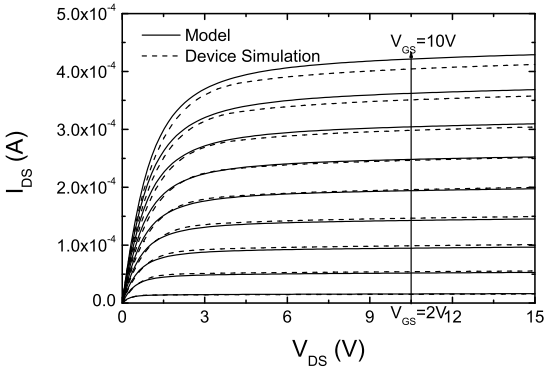


Figure 4.6: Output characteristics: drain current I_{DS} vs. drain voltage V_{DS} for V_{GS}=2-10V ($L = 2\mu m$, $N_S = 5 \cdot 10^{16} cm^{-3}$ and $k_n = 1.5$). The prolonged linear region at higher gate voltage arises due to lateral nonuniform doping.

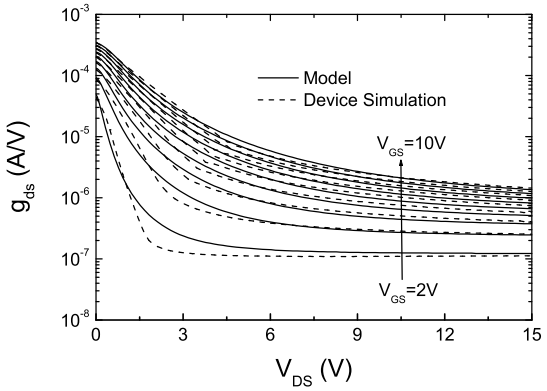


Figure 4.7: Output conductance g_{ds} vs. drain voltage V_{DS} for V_{GS}=2-10V ($L = 2\mu m$, $N_S = 5 \cdot 10^{16} cm^{-3}$ and $k_n = 1.5$).

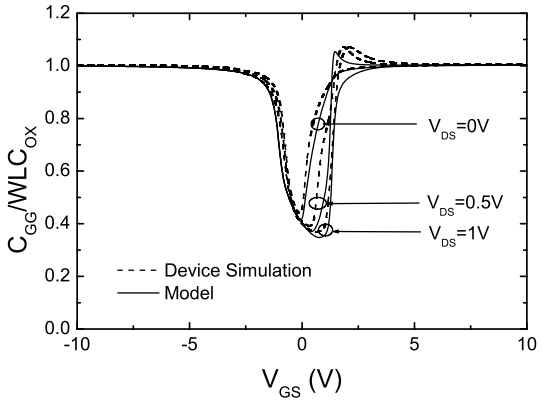


Figure 4.8: Gate-to-Gate capacitance C_{GG} vs. gate voltage V_{GS} for V_{DS}=0, 0.5 and 1V ($L = 2\mu m$, $N_S = 5 \cdot 10^{16} cm^{-3}$ and $k_n = 1.5$). Notice that peak in C_{GG} occurs, when V_{GS} is around threshold voltage. The peak in C_{GG} at low drain bias is given by lateral nonuniform doping [30].

gate bias for current and transconductance. Fig. 4.6 and 4.7 show the output characteristics ($I_{DS} - V_{DS}$) and output conductance ($g_{ds} - V_{DS}$), respectively, for V_{GS}=2-10V. It can be seen that the current as well as its slope is well simulated by the model. As mentioned in chapter 2, the prolonged linear region on output characteristics is due to lateral asymmetry in the channel. Fig. 4.8 shows the gate-to-gate capacitance C_{GG} at V_{DS}=0, 0.5 and 1V. It is interesting to note that C_{GG} has peaks at V_{DS}=0.5 and 1V, which was also shown in [30] for nonzero V_{DS}. These peaks can be explained by the fact that the drain end of the channel is in depletion while the source end of the channel is in weak/moderate inversion and source end suddenly it enters into strong inversion with slight increase in V_{GS}. Note that the peak vanishes as V_{GS} increases significantly above threshold voltage as now charge is being supplied from source. Thus, the peak in C_{GG} occurs for small nonzero values of V_{DS}, when V_{GS} is around threshold voltage (source end entering into strong inversion from weak/moderate inversion). Fig. 4.9 shows the gate-to-drain (C_{GD}) and gate-to-source (C_{GS}) capacitance at V_{DS}=0. The rising slope and value of the

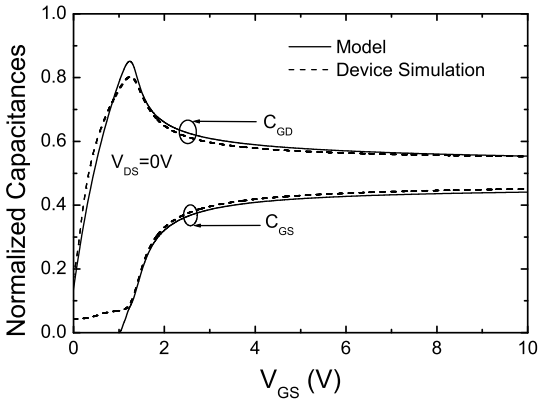


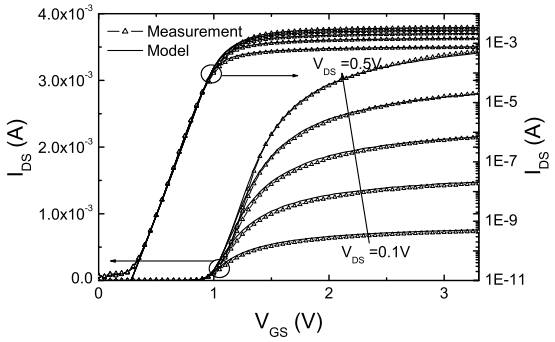
Figure 4.9: Gate-to-Drain C_{GD} and Gate-to-Source C_{GS} capacitance vs. gate voltage V_{GS} for V_{DS}=0 ($L = 2\mu m$, $N_S = 5 \cdot 10^{16} cm^{-3}$ and $k_n = 1.5$). The peak in C_{GD} is given by lateral asymmetry in the LAMOS channel [1, 36, 37, 2].

peak in C_{GD} is given by the lateral asymmetry in the LAMOS channel. The discrepancy in the capacitance behavior is due to the charge sheet approximation and the various approximations taken in the model development.

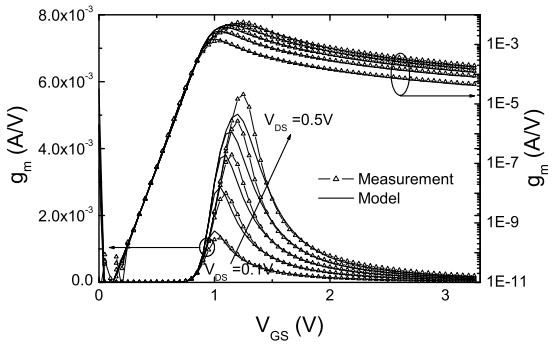
4.3.2 Model validation on the measured data of VDMOS and LDMOS

The proposed LAMOS model is also validated on the measured characteristics of 50V VDMOS and 40V LDMOS transistors obtained from AMI Semiconductor. Both devices have lateral non-uniform doping in the channel as shown in the inset of Fig. 4.1. The drift model is conveniently chosen from chapter 2 [35, 38]. The Self-heating effect is modeled in the similar way as in chapter 3 using standard thermal circuit [39, 40].

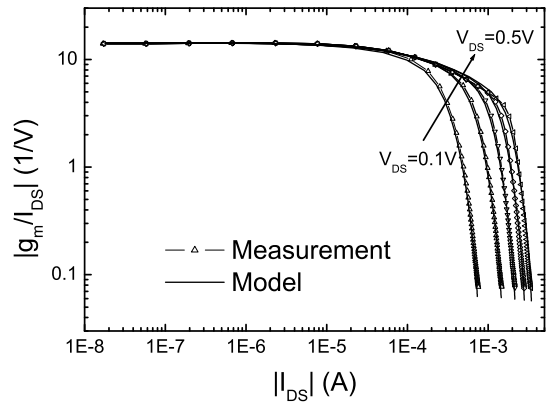
VDMOS- Fig. 4.10(a) and 4.10(b) show the transfer characteristics for low drain bias. The subthreshold current and transconductance are mainly dictated by the LAMOS while current at higher V_{GS} is also affected by drift region. It can be seen that the subthreshold slope as well as current at higher V_{GS} is excellently modeled. Fig. 4.10(c) shows the $\frac{g_m}{I_{DS}}$ vs. I_{DS} for low drain bias, which is an important parameter for analog design. Fig. 4.11 shows the drain current vs. gate bias for medium drain voltages. The drain current at higher gate bias is heavily affected by the drift region. The accuracy in g_m and $\frac{g_m}{I_{DS}}$ curves can be improved with better mobility models using more fitting parameters [42]. Fig. 4.12(a) and 4.12(b) show the output characteristics ($I_{DS} - V_{DS}$) and output conductance ($|g_{ds}| - V_{DS}$), respectively, for V_{GS}=1.4-2.78V, which demonstrates that the self-heating [39, 24, 40] as well as the impact ionization effect [43] is also well simulated. The delayed transition at higher V_{GS} from linear to saturation on $I_{DS} - V_{DS}$ characteristics owes to the lateral nonuniform doping in the channel as well as the effect of drift region. The first dip in $|g_{ds}|$ in Fig. 4.12(b) is given by the self-heating effect, while the second dip is given by the impact-ionization effect. Fig. 4.13(a), 4.13(b) and 4.13(c) show the normalized gate-to-gate capacitance (C_{GG}), gate-to-drain capacitance (C_{GD}) and gate-to-source+gate-to-body capacitance ($C_{GS} + C_{GB}$), respectively, for V_{DS}=0-5V in steps of 1V. It can be seen that the model shows good behavior for peaks as well as amplitude of peaks in



(a)



(b)



(c)

Figure 4.10: Transfer characteristics of 50V VDMOS (W=40μm, L=0.6μm at T=30°C): (a) I_{DS}-V_{GS} for V_{DS}=0.1 to 0.5V in steps of 0.1V. Note that the subthreshold slope and transition from weak to strong inversion are excellently modeled. The current at higher V_{GS}, which is heavily affected by the drift region, is also correctly modeled by the drift model [38, 41], (b) g_m-V_{GS} for V_{DS}=0.1 to 0.5V in steps of 0.1V. (c) $\frac{g_m}{I_{DS}}$ vs. I_{DS} for V_{DS}=0.1 to 0.5V in steps of 0.1V.

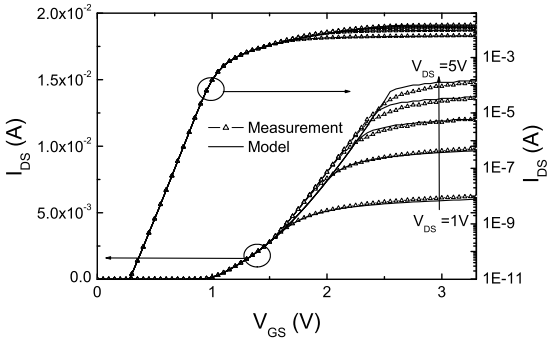


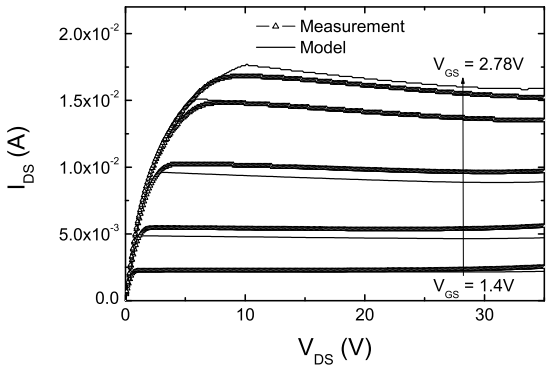
Figure 4.11: Transfer characteristics of 50V VDMOS (W=40μm, L=0.6μm at T=30°C): I_{DS}-V_{GS} for V_{DS}=1 to 5V in steps of 1V. Note that the subthreshold slope and transition from weak to strong inversion are well modeled. The current at higher V_{GS} is heavily affected by the drift region.

all capacitances, where peaks are dominated by doping gradient in the channel at low V_{DS}, and by the drift region at higher V_{DS}. The rising part of C_{GD} is mainly given by lateral asymmetry in the channel while the fall in C_{GD} is heavily affected by the drift region also demonstrated in section 2.3. As mentioned earlier in Fig. 4.8 and explained in chapter 2, the lateral non-uniform doping produces peaks in C_{GG} and C_{GS} around threshold voltage. The drift region gives higher peaks and also shifts the position of peaks as shown in 4.13(a) and 4.13(c) for nonzero V_{DS}. To understand it better, we can write the normalized C_{GG} expression as,

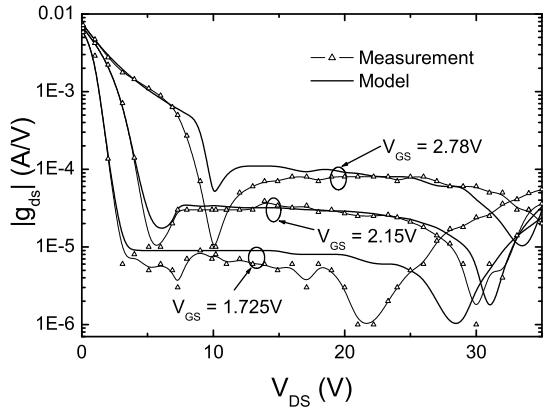
$$\begin{aligned} C_{GG} &= \frac{dQ_G(V_{GS},V_K,V_S)}{dV_{GS}} \\ &= \frac{\partial Q_G(V_{GS},V_K,V_S)}{\partial V_{GS}} + \frac{\partial Q_G(V_{GS},V_K,V_S)}{\partial V_K}\frac{dV_K}{dV_{GS}} \\ &= C_{GG(LAMOS)} - C_{GD(LAMOS)}\frac{dV_K}{dV_{GS}} \end{aligned} \tag{4.26}$$

Here V_K is the intrinsic drain potential (the point where LAMOS meets drift region in high voltage devices) shown in Fig. 4.1 [35, 38]. If there is no drift region, then $V_K = V_D$ and second term in (4.26) vanishes as $\frac{dV_K}{dV_{GS}} = 0$. In the presence of the drift region, V_K is not fixed and will vary to maintain a constant current from drain to source. If there is a slight positive change ∂V_{GS} in V_{GS}, the LAMOS current will increase. Now to increase the current in the drift region to the level of LAMOS, V_K should decrease as V_{DS} is fixed. Larger the drift resistance, larger should be the drop in V_K. Thus $\frac{dV_K}{dV_{GS}}$ will be negative for positive values of ∂V_{GS} and from (4.26), it is evident that C_{GG} of any high voltage device would be larger than C_{GG} of LAMOS and will increase with higher drift resistance for nonzero V_{DS}. Thus a good model for HV-MOS needs both excellent modeling of intrinsic MOS channel (which provides $C_{GG(LAMOS)}$) and drift region (which dictates derivative of V_K). The source of discrepancy in Fig. 4.13(a) for V_G higher than threshold voltage and high V_D is still not clear and needs more investigation on these capacitances. It could be due to the function used for the doping concentration in the LAMOS region, which is not fitting well towards source side of the device.

LDMOS- Fig. 4.14(a) and 4.14(b) show the $I_{DS} - V_{GS}$ and $g_m - V_{GS}$ for low drain bias



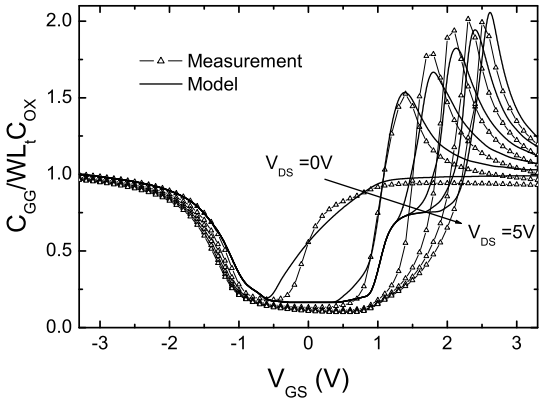
(a)



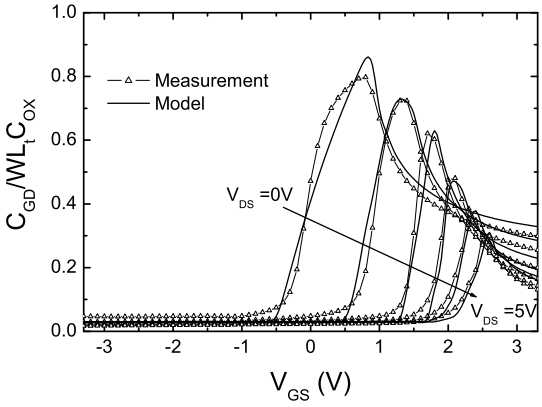
(b)

Figure 4.12: Output characteristics of 50V VDMOS (W=40μm, L=0.6μm at T=30°C): (a) Drain current I_{DS} vs. V_{DS} for V_{GS}=1.4, 1.725, 2.15, 2.58 and 2.78V. The linear region is affected by doping gradient in LAMOS channel and drift region. (b) Output conductance $|g_{ds}|$ vs. V_{DS} for three different gate voltages. The first dip in $|g_{ds}|$ is given by self-heating effect [39, 40], while second dip is given by impact-ionization effect [41].

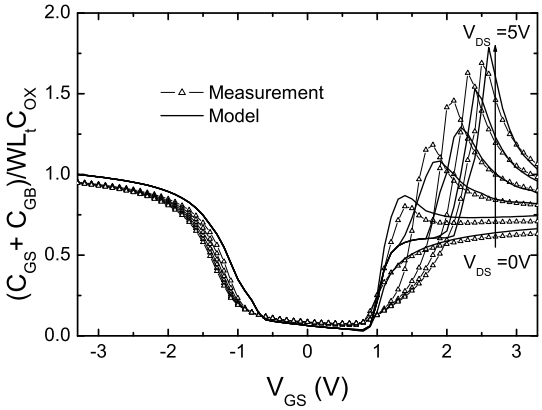
(V_{DS}=0.1 to 0.5V in steps of 0.1V). The current as well as the peaks in transconductance are very well simulated by the model, which proves correct modeling of mobility behavior with transverse field [28] and drift resistance [35, 38]. Fig. 4.14(c) shows the $\frac{g_m}{I_{DS}}$ vs. I_{DS} for V_{DS}=0.1 to 0.5V in steps of 0.1V. Fig. 4.15(a) and 4.15(b) show the transfer characteristics ($I_D - V_{GS}$) and transconductance ($g_m - V_{GS}$) for medium drain bias (V_{DS}=1 to 5V in steps of 1V). The subthreshold slope as well as value of current for higher gate bias is correctly modeled for all drain voltages. The current at higher gate and drain bias in Fig. 4.15(a) is heavily affected by the drift region. Fig. 4.16 shows the output characteristics ($I_{DS} - V_{DS}$) for V_{GS}= 4-12V in steps of 2V. The prolonged linear region on output characteristics is affected by both, the lateral non-uniform doping and the drift region. The self-heating and the impact ionization effect are also well simulated [24, 39, 40]. It should be noted that even though the DC curves can be fitted with existing low voltage MOS models with uniform doping in the



(a)

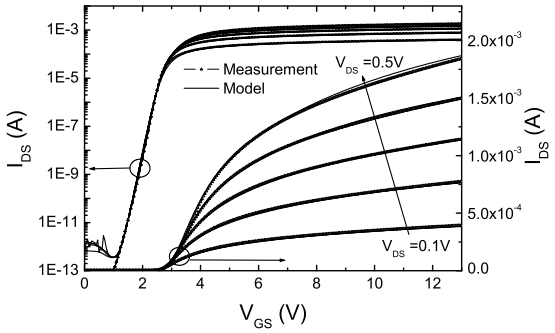


(b)

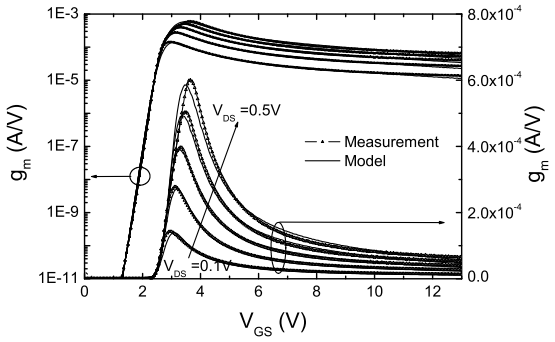


(c)

Figure 4.13: AC Characteristics of 50V VDMOS: (a) Normalized C_{GG} capacitance vs. V_{GS} for V_{DS}=0-5V in steps of 1V. The peaks in C_{GG} at low V_{DS} are dominated by doping gradient while increase in peaks with higher V_{DS} is dictated by drift region. (b) Normalized C_{GD} capacitance vs. V_{GS} for V_{DS} =0-5V. The C_{GD} peak at V_{DS}=0 is around threshold voltage due to lateral doping [36, 37, 2], but it shifts towards left with higher drift resistance (higher drift length/resistivity) or higher lateral doping gradient. (c) Normalized $C_{GS} + C_{GB}$ capacitance vs. V_{GS} for V_{DS}=0-5V. The peaks in $C_{GS} + C_{GB}$ are combined effect of both lateral doping and drift region. For capacitance normalization, $L_t = L + L_{ov}$ denotes the total gate length.



(a)



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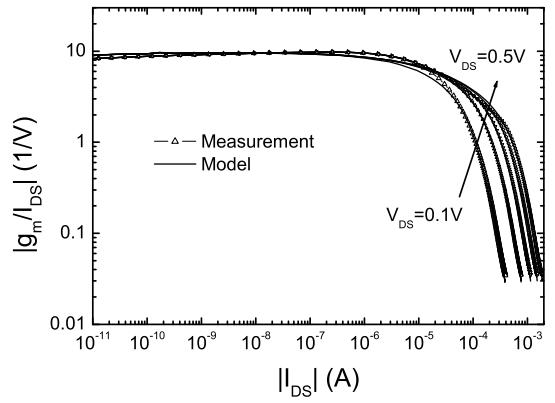
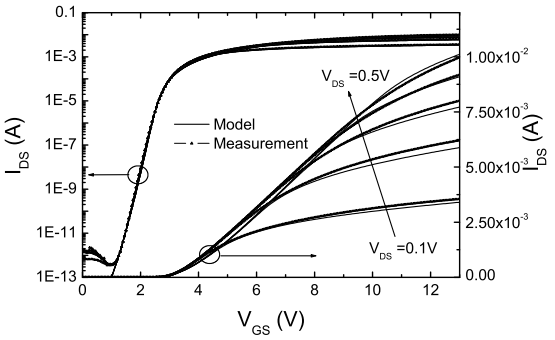
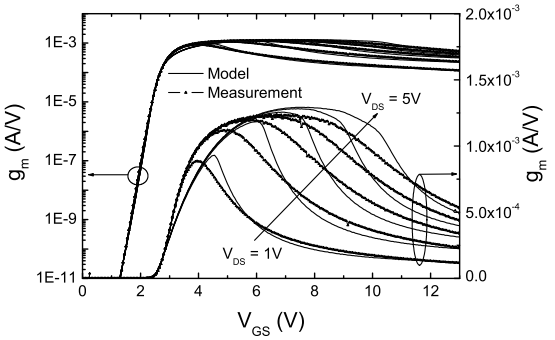


(c)

Figure 4.14: Transfer characteristics of 40V LDMOS (W=40μm, L=1.2μm at T=30°C): (a) I_{DS}-V_{GS} for V_{DS}=0.1 to 0.5V in steps of 0.1V. (b) g_m-V_{GS} for V_{DS}=0.1 to 0.5V in steps of 0.1V. (c) $\frac{g_m}{I_{DS}}$ vs. I_{DS} for V_{DS}=0.1 to 0.5V in steps of 0.1V.

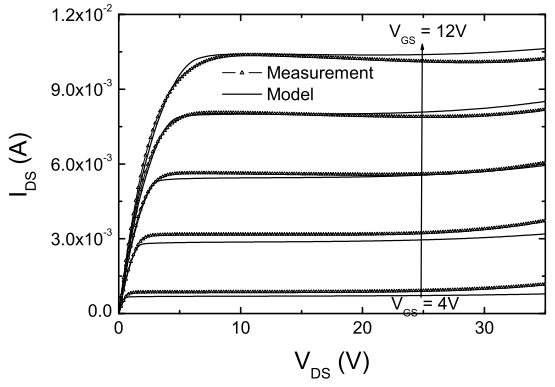


(a)



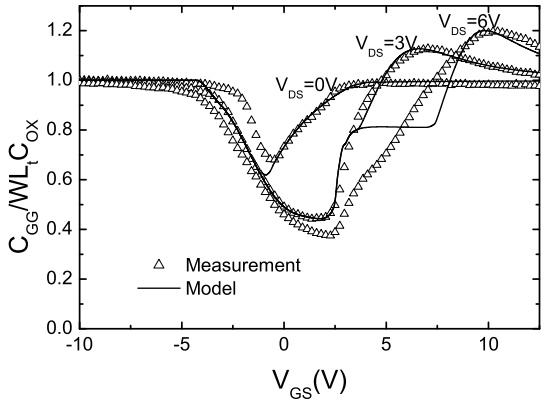
(b)

Figure 4.15: Transfer characteristics of 40V LDMOS at medium drain bias (W=40μm, L=1.2μm at T=30°C): (a) I_{DS}-V_{GS} (b) g_m-V_{GS} for V_{DS}=1 to 5V in steps of 1V. Note that the subthreshold slope and transition from weak to strong inversion are well modeled. The current at higher V_{GS} is heavily affected by the drift region.

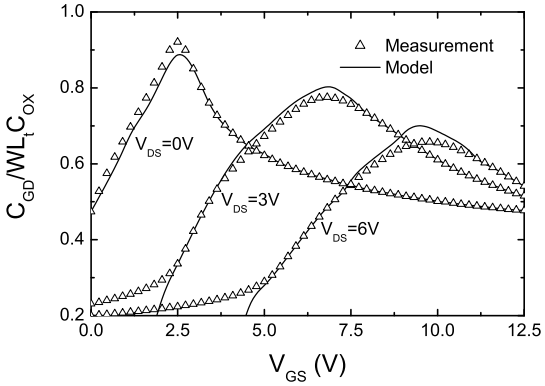


(a)

Figure 4.16: Output characteristics of 40V LDMOS (W=40μm, L=1.2μm at T=30°C): Drain current I_D vs. V_{DS} for V_{GS}=4 to 12V in steps of 2V. The linear region is affected by both the lateral non-uniform doping in the LAMOS channel and drift region.



(a)



(b)

Figure 4.17: AC characteristics of 40V LDMOS: (a) Normalized C_{GG} vs. V_{GS} for V_{DS}=0, 3 and 6V. The peak in C_{GG} at low drain bias arises due to lateral asymmetry. The peaks at higher drain and gate bias can be explained by the combined effect of lateral non-uniform doping and effect on drift region. (b) Normalized gate-to-drain capacitance (C_{GD}) vs. V_{GS} for V_{DS}=0 3 and 6V. The peak in C_{GD} at V_{DS}=0 is around threshold voltage [37, 2] while it shifts towards left with higher drift resistance (higher drift length/resistivity) or higher lateral doping gradient. For capacitance normalization, $L_t = L + L_{ov}$ denotes the total length.

channel as shown in chapter 3 [35, 38], the modeling of lateral non-uniform doping provides more physical tuning of parameters e.g. threshold voltage, body effect coefficient etc. in the model. Fig. 4.17(a) shows the $C_{GG} - V_{GS}$ for V_{DS}=0, 3 and 6V. The C_{GG} behavior at low gate bias is dominated by the lateral doping while at higher gate bias the peaks are dictated by drift region. The higher the drift resistance (large drift length or high value of drift resistivity), higher the peak in C_{GG} and vice-versa. Fig. 4.17(b) shows the $C_{GD} - V_G$ for V_{DS}=0, 3 and 6V. As mentioned earlier, the peak in C_{GD} can be explained by the lateral asymmetry present in the intrinsic MOS. The decreasing part of C_{GD} is affected by both the nonuniform doping in the channel and the drift region as explain in chapter 2. It should be noted that it is very important

to correctly model the drift region (or V_K behavior [41]) for the correct behavior after the peaks in all capacitances [44]. The peak in C_{GD} at V_{DS}=0 is around threshold voltage due to lateral doping [37, 2], but the position of the peak will shift towards left and amplitude of the peak will decrease with higher drift resistance (large drift length or high value of drift resistivity). To understand it, we can express C_{GD} of LDMOS as $C_{GD(LAMOS)}\frac{dV_K}{dV_{DS}}$, and can apply same analysis as for C_{GG} discussed above. Higher difference in doping between source and drain produces higher peaks on C_{GD}, already shown in chapter 2. The discrepancy in the results is due to the charge sheet approximation and various approximations taken in model development.

4.4 Conclusion

A *novel* charge based compact analytical model for lateral non-uniformly doped MOSFET was developed in this chapter. The model is developed using charge based EKV formalism. The major impact of the lateral non-uniform doping was seen on the capacitances, whose modeling has been a daunting task till now as expressions become non-integrable and non-implicit for current and charges. The inversion charge linearization paved the way to approximate the surface pinch-off potential across the channel. This led to develop integrable expressions for current and then charges. The inversion and gate charge in this model have clear dependence on the drain current, which is not the case in the conventional MOSFET models.

The proposed model was used for modeling of high voltage devices with a lateral doping gradient using an appropriate drift model. To the best of our knowledge, *this is the first time, the modeling of lateral non-uniform doping has been implemented in any high voltage compact model.* The model shows good behavior for all capacitances as well as for DC, when compared with device simulation and measurements. The position of the capacitance peaks as well as their amplitude are correctly simulated by the model. The major impact of the proposed model is on the accuracy improvement of high voltage MOSFET models especially during transient operations (i.e. modeling of the bias-dependent peaks and slopes of device capacitances).

Bibliography

[1] Y. S. Chauhan, F. Krummenacher, C. Anghel, R. Gillon, B. Bakeroot, M. Declercq, and A. M. Ionescu, "Analysis and Modeling of Lateral Non-Uniform Doping in High-Voltage MOSFETs," in *IEEE International Electron Devices Meeting*, Dec. 2006, pp. 8.3.1 – 8.3.4.

[2] C. Anghel, Y. S. Chauhan, N. Hefyene, and A. Ionescu, "A physical analysis of HV MOSFET capacitance behaviour," in *IEEE International Symposium on Industrial Electronics (ISIE)*, vol. 2, June 2005, pp. 473 – 477.

[3] Y. S. Chauhan, F. Krummenacher, R. Gillon, B. Bakeroot, M. Declercq, and A. M. Ionescu, "A New Charge based Compact Model for Lateral Asymmetric MOSFET and its application to High Voltage MOSFET Modeling," in *IEEE International Conference on VLSI Design and International Conference on Embedded Systems*, Jan. 2007, pp. 177 – 182.

[4] ——, "Compact Modeling of Lateral Non-uniform doping in High-Voltage MOSFETs," *IEEE Transactions on Electron Devices*, vol. 54, no. 6, pp. 1527–1539, June 2007.

[5] J. Victory, J. Sanchez, T. DeMassa, and B. Welfert, "A static, physical VDMOS model based on the charge-sheet model," *IEEE Transactions Electron Devices*, vol. 43, no. 1, pp. 157 – 164, Jan. 1996.

[6] N. D'Halleweyn, J. Benson, W. Redman-White, K. Mistry, and M. Swanenberg, "MOOSE: a physically based compact DC model of SOI LD MOSFETs for analogue circuit simulation," *IEEE Transactions Computer-Aided Design of Integrated Circuits and Systems*, vol. 23, no. 10, pp. 1399–1410, Oct. 2004.

[7] A. Aarts, N. D'Halleweyn, and R. van Langevelde, "A surface-potential-based high-voltage compact LDMOS transistor model," *IEEE Transactions Electron Devices*, vol. 52, no. 5, pp. 999 – 1007, May 2005.

[8] C. Kreuzer, N. Krischke, and P. Nance, "Physically based description of quasi-saturation region of vertical DMOS power transistors," in *IEEE International Electron Devices Meeting (IEDM)*, Dec. 1996, pp. 489 – 492.

[9] M. Trivedi and K. Shenai, "Comparison of RF performance of vertical and lateral DMOSFET," in *The 11th International Symposium on Power Semiconductor Devices and ICs*, May 1999, pp. 245 – 248.

[10] K. Pinardi, U. Heinle, S. Bengtsson, J. Olsson, and J.-P. Colinge, "High-power SOI vertical DMOS transistors with lateral drain contacts: Process developments, characterization, and modeling," *IEEE Transactions Electron Devices*, vol. 51, no. 5, pp. 790 – 796, May 2004.

[11] A. Hiroki, S. Odanaka, and A. Hori, "A High Performance 0.1μm MOSFET with Asymmetric Channel Profile," in *IEEE International Electron Devices Meeting*, Dec. 1995, pp. 17.7.1 – 17.7.4.

[12] S. Odanaka and A. Hiroki, "Potential design and transport property of 0.1-μm mosfet with asymmetric channel profile," *IEEE Transactions Electron Devices*, vol. 44, no. 4, pp. 595 – 600, April 1997.

[13] K. Narasimhulu, D. K. Sharma, and V. R. Rao, "Impact of lateral asymmetric channel doping on deep submicrometer mixed-signal device and circuit performance," *IEEE Transactions Electron Devices*, vol. 50, no. 12, pp. 2481 – 2489, December 2003.

[14] K. Narasimhulu, M. P. Desai, S. G. Narendra, and V. R. Rao, "The effect of lac doping on deep submicrometer transistor capacitances and its influence on device rf performance," *IEEE Transactions Electron Devices*, vol. 51, no. 9, pp. 1416 – 1423, September 2004.

[15] D. G. Borse, M. R. K.N., N. K. Jha, A. N. Chandorkar, J. Vasi, V. R. Rao, B. Cheng, , and J. C. S. Woo, "Optimization and realization of sub-100-nm channel length single halo p-mosfets," *IEEE Transactions Electron Devices*, vol. 49, no. 6, pp. 1077 – 1079, June 2002.

[16] N. Jha, M. Baghini, and V. Rao, "Performance and reliability of single halo deep submicron p-MOSFETs for analog applications," in *IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits*, July 2002, pp. 35 – 39.

[17] N. Jha, V. Rao, and J. Woo, "Optimization of Single Halo p-MOSFET Implant Parameters for Improved Analog Performance and Reliability," in *IEEE European Solid-State Device Research Conference*, September 2002, pp. 603 – 606.

[18] "Compact model council (CMC)," , http://www.eigroup.org/cmc/.

[19] A. Aarts and W. Kloosterman, "Compact modeling of high-voltage LDMOS devices including quasi-saturation," *IEEE Transactions Electron Devices*, vol. 53, no. 4, pp. 897 – 902, April 2006.

[20] S. Frere, P. Moens, B. Desoete, D. Wojciechowski, and A. Walton, "An improved LDMOS transistor model that accurately predicts capacitance for all bias conditions," in *Proceedings of the 2005 International Conference on Microelectronic Test Structures (ICMTS)*, April 2005, pp. 75 – 79.

[21] C.-Y. Tsai, D. E. Burk, and K. D. T. Ngo, "Physical Modeling of the Power VDMOST for Computer-Aided Design of Integrated Circuit," *IEEE Transactions Electron Devices*, vol. 44, no. 3, pp. 472 – 480, March 1997.

[22] N. Hefyene, C. Anghel, A. Ionescu, S. Frere, R. Gillon, M. Vermandel, B. Bakeroot, and J. Doutreloigne, "An experimental approach for bias-dependent drain series resistances evaluation in asymmetric HV MOSFETs," in *IEEE European Solid-State Device Research Conference (ESSDERC)*, Sept. 2001, pp. 403 – 406.

[23] A. Canepari, G. Bertrand, A. Giry, M. Minondo, F. Blanchet, H. Jaouen, B. Reynard, N. Jourdan, and J.-P. Chante, "LDMOS modeling for analog and RF circuit design," in *IEEE European Solid-State Device Research Conference (ESSDERC)*, Sept. 2005, pp. 469 – 472.

[24] C. Anghel, "High voltage devices for standard MOS technologies : characterisation and modelling," Ph.D. dissertation, EPFL, 2004, thesis No. 3116.

[25] N. Hefyene, "Electrical characterization and modelling of lateral DMOS transistor : investigation of capacitances and hot-carrier impact," Ph.D. dissertation, EPFL, 2005, thesis No. 3200.

[26] J.-M. Sallese, M. Bucher, F. Krummenacher, and P. Fazan, "Inversion charge linearization in MOSFET modeling and rigorous derivation of the EKV compact model," *Solid-State Electronics*, vol. 46, no. 11, pp. 677–683, April 2003.

[27] C. Enz, F. Krummenacher, and E. Vittoz, "An analytical MOS transistor model valid in all regions of operation and dedicated to low-voltage and low-current applications," *Journal on Analog Integrated Circuits and Signal Processing*, vol. 8, no. 1, pp. 83–114, July 1995.

[28] M. Bucher, "Analytical MOS Transistor Modelling for Analog Circuit Simulation," Ph.D. dissertation, EPFL, 1999, thesis No. 2114.

[29] R. F. Pierret, *Semiconductor Device Fundamentals*. Addision Wesley: Addision Wesley, 1996.

[30] A. Aarts, R. van der Hout, J. Paasschens, A. Scholten, M. Willemsen, and D. Klaassen, "New fundamental insights into capacitance modeling of laterally nonuniform MOS devices," *IEEE Transactions Electron Devices*, vol. 53, no. 2, pp. 270 – 278, Feb. 2006.

[31] ——, "Capacitance modeling of laterally non-uniform MOS devices," in *IEEE International Electron Devices Meeting*, Dec. 2004, pp. 751 – 754.

[32] S.-Y. O. D. Ward and R. Dutton, "Transient analysis of MOS transistors," *IEEE Transactions Electron Devices*, vol. 27, no. 8, pp. 1571 – 1578, Aug 1980.

[33] A. S. Roy, Y. S. Chauhan, C. Enz, J.-M. Sallese, A. M. Ionescu, and M. Declercq, "Partitioning Scheme in Lateral Asymmetric MOST," in *IEEE European Solid-State Device Research Conference*, Sept. 2006, pp. 307–310.

[34] Y. S. Chauhan, C. Anghel, F. Krummenacher, A. Ionescu, M. Declercq, R. Gillon, S. Frere, B. Desoete, B. Bakeroot, and C. Maier, "Ekv based dmos model extension for v-dmos," , http://www-g.eng.cam.ac.uk/robuspic/reports.htm, 2004-2006.

[35] Y. S. Chauhan, C. Anghel, F. Krummenacher, R. Gillon, A. Baguenier, B. Desoete, S. Frere, A. M. Ionescu, and M. Declercq, "A Compact DC and AC Model for Circuit Simulation of High Voltage VDMOS Transistor," in *IEEE International Symposium on Quality Electronic Design (ISQED)*, March 2006, pp. 109–114.

[36] S. Frére, J. Rhayem, H. Adawe, R. Gillon, M. Tack, and A. Walton, "LDMOS Capacitance Analysis versus Gate and Drain Biases, Based on Comparison between TCAD Simulations and Measurements," in *IEEE European Solid-State Device Research Conference (ESSDERC)*, Sept. 2001, pp. 219 – 222.

[37] C. Anghel, B. Bakeroot, Y. S. Chauhan, R. Gillon, C. Maier, P. Moens, J. Doutreloigne, and A. Ionescu, "New Method for Threshold Voltage Extraction of High-Voltage MOSFETs Based on Gate-to-Drain Capacitance Measurement," *IEEE Electron Device Letters*, vol. 27, no. 7, pp. 602 – 604, July 2006.

[38] Y. S. Chauhan, C. Anghel, F. Krummenacher, A. M. Ionescu, M. Declercq, R. Gillon, S. Frere, and B. Desoete, "A Highly Scalable High Voltage MOSFET Model," in *IEEE European Solid-State Device Research Conference (ESSDERC)*, Sept. 2006, pp. 270 – 273.

[39] C. Anghel, R. Gillon, and A. Ionescu, "Self-heating characterization and extraction method for thermal resistance and capacitance in HV MOSFETs," *IEEE Electron Device Lett.*, vol. 25, no. 3, pp. 141 – 143, March 2004.

[40] C. Anghel, N. Hefyene, R. Gillon, M. Tack, M. Declercq, and A. Ionescu, "New method for temperature-dependent thermal resistance and capacitance accurate extraction in high-voltage DMOS transistors," in *IEEE International Electron Devices Meeting (IEDM)*, Dec. 2003, pp. 5.6.1 – 5.6.4.

[41] Y. S. Chauhan, C. Anghel, F. Krummenacher, C. Maier, R. Gillon, B. Bakeroot, B. Desoete, S. Frere, A. B. Desormeaux, A. Sharma, M. Declercq, and A. M. Ionescu, "Scalable General High Voltage MOSFET Model including Quasi-Saturation and self-heating effect," *Solid State Electronics*, vol. 50, no. 11-12, pp. 1801–1813, 2006.

[42] G. Gildenblat, X. Li, W. Wu, H. Wang, A. Jha, R. V. Langevelde, G. Smit, A. Scholten, and D. Klaassen, "Psp: An advanced surface-potential-based mosfet model for circuit simulation," *IEEE Transactions Electron Devices*, vol. 53, no. 9, pp. 1979 – 1993, Sept. 2006.

[43] P. Rossel, H. Tranduc, D. Montcoqut, G. Charitat, and I. Pages, "Avalanche characteristics of MOS transistors," in *IEEE International Conference on Microelectronics*, vol. 1, Sept. 1997, pp. 371 – 381.

[44] N. Hefyene, E. Vestiel, B. Bakeroot, C. Anghel, S. Frere, A. Ionescu, and R. Gillon, "Bias-dependent drift resistance modeling for accurate DC and AC simulation of asymmetric HV-MOSFET," in *IEEE European Solid-State Device Research Conference (ESSDERC)*, Sept. 2002, pp. 203 – 206.

Chapter 5

Partitioning Scheme and Noise Modeling in the Lateral Non-Uniformly doped MOSFET

The Ward-Dutton partitioning scheme [1] is used extensively to develop transient and high frequency advanced compact models in MOSFET analysis [2]. Recently, it has been recognized that capacitance property of Lateral Non-Uniformly doped or Lateral Asymmetric MOSFET (LAMOS) [3, 4, 5, 6, 7] is fundamentally different from conventional MOSFET [6, 4] because Ward-Dutton partitioning is not applicable to this kind of devices. In this work, it will be shown that although it is not possible to guaranty a partitioning scheme for general operation of the MOSFET but it is possible to show the existence of a partitioning scheme for small-signal operation of the device in LAMOS [8]. Application of this new concept in capacitance evaluation of LAMOS considerably simplifies the existing capacitance evaluation methodology [4, 6]. This work also provides a simpler way to physically understand the unusual behavior of drain-to-gate capacitance C_{DG} in LAMOS. The proposed theory is validated by extensive numerical and device simulation. Recently generalization of this partitioning scheme including mobility degradation has also been published in the literature [9].

In the second part of this chapter, for the first time, an analytical noise modeling methodology in presence of lateral asymmetry will be presented [10]. It will be shown that noise properties of LAMOS are considerably different from the prediction of conventional Klaassen-Prins [11] based methods and at low gate voltages, they can overestimate the noise by 2-3 orders of magnitude.

5.1 Introduction

All of the advanced compact MOSFET models (PSP, MM11, HISIM, BSIM, EKV etc., see [2] and the references therein) dedicated to even sub 100 nm devices are entirely built on the Ward-Dutton partitioning [1], which was originally derived for long-channel uniformly doped MOSFET. Recently, in the pioneering work by Aarts et. al. [4], it has been recognized that the Ward-Dutton charge partitioning [1] is not applicable in LAMOS and it has been concluded that “no terminal charges exist from which the capacitances can be derived”. Therefore, [4] is

forced to solve the small-signal continuity equation under quasi-static assumption for both real and imaginary part of perturbed channel potential and calculate the capacitances from them.

Although it is not possible to guaranty a partitioning scheme for general operation of the LAMOS but it is possible to show the existence of a partitioning scheme for small-signal operation of the device in LAMOS [8]. Existence of the small signal partitioning implies that we can always define a partitioning of small-signal/perturbed charges to calculate the terminal capacitances. This alternate approach has major advantage over the existing approach as it eliminates the need of solving the continuity equation for the imaginary part of perturbed channel potential which results in a saving of one level of numerical numerical integration compared to [4]. In addition to these, it provides thorough physical insight to understand the unusual behavior of C_{DG}. This concept can also be used in the partitioning of gate tunnelling current and even noise, which are of importance in the standard CMOS devices, where, lateral asymmetry is inherent due to halo implant.

5.2 Partitioning Scheme

The current at any position x in the LAMOS/MOSFET can be written as

$$I(x) = g(x, V) \cdot \frac{dV}{dx}, \tag{5.1}$$

where $g = \mu W Q_i$ and μ, W, Q_i and V are the mobility, width, inversion charge density and channel potential respectively. Please note that in presence of velocity saturation, μ starts to depend on the electric field, so g will be a function of V and $\frac{dV}{dx}$ [12, 9] but in the present work we will consider μ to be independent of electric field. The explicit dependence of g on x implies that the doping may also vary along the channel, which is the case for a LAMOS [5, 3, 7]. Let's assume the general form of continuity equation as

$$\frac{dI}{dx} = \widehat{s}. \tag{5.2}$$

Please note that this $\widehat{s}$ expression of source term is completely general. It can be a term like $W\frac{dQ}{dt}$ (rate of change of charge per unit length) in case of a transient or term like $i_g(x)$ (gate current per unit length) in case of a gate tunnelling current. Existence of a partitioning scheme means that it is possible to decouple the current when $\widehat{s} = 0$ (we will call this current as I_0) and the effect of source term. In other words, the terminal current can be expressed as a sum of I_0 and a weighted integral of $\widehat{s}$. To see why Ward-Dutton scheme [1] fails in presence of lateral asymmetry [5, 3, 7] or mobility degradation [12], We first multiply (5.2) by x and integrate from 0 to L,

$$\int_0^L x\frac{dI}{dx}dx = \int_0^L x\widehat{s}dx \tag{5.3}$$

and integrating by parts yields

$$xI|_0^L - \int_0^L I(x)dx = \int_0^L x\widehat{s}dx \tag{5.4}$$

Substituting (5.1) in the above equation, we obtain

$$I(L) = \frac{1}{L}\int_{V_s}^{V_d} g(x,V)dV + \int_0^L \frac{x}{L}\widehat{s}dx \tag{5.5}$$

When g is a function of V only (the classical constant mobility case), the first integral depends only on the value of V at the boundaries. The point is, even if the function $V(x)$ (the channel potential distribution) changes because of the $\widehat{s}$ term, the value of the integral does not change and remains equal to the case when $\widehat{s} = 0$. In the case when $\widehat{s} = 0$, we can easily identify the integral as DC current I_0 and we get back the Ward-Dutton partitioning scheme. But when g starts to depend also on x, the situation is different. As $V(x)$ changes due to the presence of the source term in the continuity equation, the value of the integral starts to depend on the profile of V(x). Therefore, $\frac{1}{L}\int_{V_s}^{V_d} g(x,V)dV$ is different in the presence of the source term. So in the presence of lateral asymmetry,

$$I(L) \neq I_0 + \int_0^L \frac{x}{L}\widehat{s}dx \tag{5.6}$$

To extend the concept of partitioning, Let's define a quantity $\widehat{I}(x) = I(x) - I_0$. It trivially follows that $\widehat{I}(x)$ satisfies

$$\frac{d\widehat{I}(x)}{dx} = \widehat{s} \tag{5.7}$$

Let us now consider an arbitrary function $F(x) = \int_0^x f(x)dx$ and multiply (5.7) by $F(x)$ and integrate by parts from 0 to L to obtain

$$F(x)\widehat{I}(x)|_0^L - \int_0^L \widehat{I}(x)d[F(x)] = \int_0^L F(x)\widehat{s}dx \tag{5.8}$$

or

$$\Big[F(L)\widehat{I}(L) - F(0)\widehat{I}(0)\Big] - \int_0^L \widehat{I}(x)f(x)dx = \int_0^L F(x)\widehat{s}dx \tag{5.9}$$

or

$$I(L) = I_0 + \int_0^L \frac{F(x)}{F(L)}\widehat{s}dx + \frac{1}{F(L)}\int_0^L f(x)(I(x) - I_0)dx \tag{5.10}$$

Note that an existence of partitioning scheme implies that the terminal current can be expressed as a sum of I_0 and a weighted integral of $\widehat{s}$. So in order to have a partitioning scheme, the last term in (5.10) must vanish or in other words, the existence of a function such that for any given $\widehat{s}$, the following holds

$$\int_0^L f(x)I(x)dx = \int_0^L f(x)I_0dx \tag{5.11}$$

or from (5.1)

$$\int_0^L f(x)g(x,V)\cdot\frac{dV}{dx}dx = \int_0^L f(x)g\left(x,V_0\right)\cdot\frac{dV_0}{dx}dx \tag{5.12}$$

Please note that when g does not depend on x, $f(x) = 1$ trivially satisfies the above criterion and we get back the original Ward-Dutton charge partitioning. In general we can not guarantee the existence of the funtion $f(x)$ and hence the charge partitioning scheme. But we will prove

that, when $\widehat{s}$ can be considered as a small perturbation, we can always find out the function $f(x)$ for any general form of g.

As we are considering the case when $\widehat{s}$ can be treated as a small perturbation, we will start with a perturbation analysis of $I(x)$. In the subsequent analysis subscript $'0'$ will be used to denote the situation when $\widehat{s} = 0$. The perturbed current $i(x)$ can be obtained from

$$I(x) = I_0 + i(x) = g\left(x, V_0 + v\right) \frac{d(V_0 + v)}{dx} \tag{5.13}$$

where I_0 and V_0 are the unperturbed current and voltage respectively, in the channel. Taking a first order Taylor series expansion around V_0 (the unperturbed point), we obtain

$$I(x) = I_0 + i(x) = \left[g\left(x, V_0\right) + \frac{\partial g\left(x, V_0\right)}{\partial V_0} v\right] \left(\frac{dV_0}{dx} + \frac{dv}{dx}\right) \tag{5.14}$$

Neglecting second order term we obtain

$$i(x) = g\left(x, V_0\right) \frac{dv}{dx} + \frac{\partial g\left(x, V_0\right)}{\partial V_0} \frac{dV_0}{dx} v \tag{5.15}$$

To proceed further, we note that

$$\frac{dg\left(x, V_0\right)}{dx} = \frac{\partial g\left(x, V_0\right)}{\partial x} + \frac{\partial g\left(x, V_0\right)}{\partial V_0} \frac{dV_0}{dx} \tag{5.16}$$

or

$$\frac{\partial g\left(x, V_0\right)}{\partial V_0} \frac{dV_0}{dx} = \frac{dg\left(x, V_0\right)}{dx} - \frac{\partial g\left(x, V_0\right)}{\partial x} \tag{5.17}$$

Substituting (5.17) into (5.15), we obtain

$$i(x) = \left[g\left(x, V_0\right) \frac{dv}{dx} + \frac{dg\left(x, V_0\right)}{dx} v\right] - \frac{\partial g\left(x, V_0\right)}{\partial x} v \tag{5.18}$$

or

$$i(x) = \left[\frac{d[g\left(x, V_0\right) v]}{dx} - \frac{\partial g\left(x, V_0\right)}{\partial x} v\right] \tag{5.19}$$

As $i(x) = I(x) - I_0$, we seek a function from (5.10) such that

$$\int_0^L f(x) i(x) dx = 0 \tag{5.20}$$

Now from (5.19) and (5.20), if we can find a function $f(x)$ such that

$$\int_0^L f(x) \left[\frac{d\left[g(x, V_0) v\right]}{dx} - \frac{\partial g(x, V_0)}{\partial x} v\right] dx = 0 \tag{5.21}$$

for all v then we can define a partitioning scheme. Then $f(x)$ must satisfy

$$\int_0^L f(x) \frac{d\left[g(x, V_0) v\right]}{dx} dx = \int_0^L f(x) \frac{\partial g(x, V_0)}{\partial x} v dx \tag{5.22}$$

Now we integrate the LHS by parts and use the fact that v vanishes at the boundary to obtain

$$\int_0^L \left[\frac{df(x)}{dx} g(x, V_0) + f(x) \frac{\partial g(x, V_0)}{\partial x} \right] v dx = 0 \tag{5.23}$$

This criterion gives a differential equation of $f(x)$ as

$$\frac{df(x)}{dx} g(x, V_0) = -f(x) \frac{\partial g(x, V_0)}{\partial x} \tag{5.24}$$

or

$$\frac{\left[\frac{df(x)}{dx} \right]}{f(x)} = -\frac{\left[\frac{\partial g(x, V_0)}{\partial x} \right]}{g(x, V_0)} \tag{5.25}$$

which can be solved at once as

$$f(x) = \exp \left[-\int_0^x \left(\frac{\frac{\partial g(x', V_0)}{\partial x'}}{g(x', V_0)} \right) dx' \right] \tag{5.26}$$

Note that for a conventional MOSFET $\frac{\partial g(x', V_0)}{\partial x'} = 0$ and so $f(x)$ becomes 1 and we get back the original Ward-Dutton scheme. For LAMOS, the final result from (5.10) and (5.26) becomes

$$I(L) = I_0 + \int_0^L \frac{\int_0^x \exp \left[-\int_0^x \left(\frac{\frac{\partial g(x_1, V_0)}{\partial x_1}}{g(x_1, V_0)} \right) dx_1 \right] dx}{\int_0^L \exp \left[-\int_0^x \left(\frac{\frac{\partial g(x_1, V_0)}{\partial x_1}}{g(x_1, V_0)} \right) dx_1 \right] dx} \widehat{s} dx \tag{5.27}$$

5.3 APPLICATION of small signal partitioning

In this section we will show how the concept of small signal partitioning can be applied to (a) capacitance and admittance calculation in the LAMOS (b) calculation of gate tunneling current and (c) partitioning of gate tunneling noise between the source and the drain.

5.3.1 Capacitance Evaluation of LAMOS

In small signal analysis, the drain current i_d can be expressed as

$$i_d = \sum_m Y_{dk} v_k + j\omega \sum_m C_{dk} v_k \tag{5.28}$$

where v_k are the terminal small signal voltage, Y's are the admittances and C's are the capacitances.

In case of transient, the source term $\widehat{s}$ is $W \frac{dQ}{dt}$. For small signal analysis, it reduces to $W j\omega q$, where q is the perturbed inversion charge and can be expressed as

$$q(x) = \frac{\partial Q}{\partial V_G} v_g + \frac{\partial Q}{\partial V} v(x) \tag{5.29}$$

where v_g and $v(x)$ are the perturbed gate voltage and channel potential respectively. In order to obtain the terminal currents we need to solve the coupled small signal and continuity equation [4]. But thanks to the small signal partitioing , we can express the drain current as

$$i_d = i_0 + \omega W \int_0^L \frac{F(x)}{F(L)} \left[\frac{\partial Q}{\partial V_G} v_g + \frac{\partial Q}{\partial V} v(x) \right] dx \tag{5.30}$$

where i_0 is the current when $\frac{di}{dx} = 0$.

As we have already derived the partitioning scheme in the previous section, all it remains is to express $v(x)$ and i_0 in terms of perturbed terminal voltage v_g,v_s and v_d, so that (5.28) and (5.30) can be compared to derive the capacitances as well as admittances. Under quasi-static assumption (also used in [4]) $v(x)$ becomes real and equal to the value when $\frac{di}{dx} = 0$. As we are now taking variation of V_G into account, the perturbed current becomes

$$i(x) = g(x, V_0 + v, V_G + v_g) \frac{d(V_0 + v)}{dx} - g(x, V_0, V_G) \frac{dV_0}{dx} \tag{5.31}$$

or

$$i(x) = \frac{\partial g(x, V_0, V_G)}{\partial V_0} \frac{dV_0}{dx} v + g(x, V_0, V_G) \frac{dv}{dx} + \frac{\partial g(x, V_0, V_G)}{\partial V_G} \frac{dV_0}{dx} v_g \tag{5.32}$$

Using (5.17) into (5.32),

$$i(x) = \left[\frac{dg(x, V_0, V_G)}{dx} - \frac{\partial g(x, V_0, V_G)}{\partial x} \right] v + g(x, V_0, V_G) \frac{dv}{dx} + \frac{\partial g(x, V_0, V_G)}{\partial V_G} \frac{dV_0}{dx} v_g \tag{5.33}$$

or

$$i(x) = \frac{d[g(x, V_0, V_G)v]}{dx} - \frac{\partial g(x, V_0, V_G)}{\partial x} v + \frac{\partial g(x, V_0, V_G)}{\partial V_G} \frac{dV_0}{dx} v_g \tag{5.34}$$

It should be noticed that appearance of an extra v_g term does not change the partitioning function. Now under QS assumption the differential equation for $v(x)$ satisfies

$$\frac{d[g(x, V_0, V_G)v]}{dx} - \frac{\partial g(x, V_0, V_G)}{\partial x} v + \frac{\partial g(x, V_0, V_G)}{\partial V_G} \frac{dV_0}{dx} v_g = i_0 \tag{5.35}$$

where i_0 is to be determined. This ODE is solved below to obtain $v(x)$ and i_0.

The differential equation for $v(x)$ (5.35) can be rewritten as

$$\frac{d[g(x, V_0, V_G)v]}{dx} - \frac{1}{g(x, V_0, V_G)} \frac{\partial g(x, V_0, V_G)}{\partial x} [g(x, V_0, V_G)v] = i_0 - \frac{\partial g(x, V_0, V_G)}{\partial V_G} \frac{dV_0}{dx} v_g \tag{5.36}$$

We can consider this as a linear ODE with respect to $g(x, V_0, V_G)v(x)$ and can be solved using the integration factor $R(x)$ which is given by

$$R(x) = exp \left[- \int_0^x \frac{1}{g(x, V_0, V_G)} \frac{\partial g(x, V_0, V_G)}{\partial x} dx \right] \tag{5.37}$$

Multiplying (5.36) by R(x) we obtain

$$\frac{d[R(x)g(x, V_0, V_G)v(x)]}{dx} = i_0 R(x) - R(x) \frac{\partial g(x, V_0, V_G)}{\partial V_G} \frac{dV_0}{dx} v_g \tag{5.38}$$

Let's define two auxiliary variables $\lambda_v(x)$ and $\lambda_g(x)$ as

$$\lambda_v(x) = \int_0^x R(x)dx \tag{5.39}$$

$$\lambda_g(x) = \int_0^x R(x)\frac{\partial g(x, V_0, V_G)}{\partial V_G}\frac{dV_0}{dx}dx \tag{5.40}$$

Using the definition of $\lambda_v(x)$ and $\lambda_g(x)$, and integrating (5.38) from 0 to x we obtain

$$R(x)g_0(x)v(x) - g(0, V_S, V_G)v_s = i_0\lambda_v(x) - v_g\lambda_g(x) \tag{5.41}$$

where we have used the fact that $R(0) = 1$, $V_0(0) = V_S$ and $v(0) = v_s$. Now i_0 from (5.41) can be obtained using the fact that $V_0(L) = V_D$, $v(L) = v_d$ as

$$i_0 = \frac{\lambda_g(L)}{\lambda_v(L)}v_g - \frac{g(0, V_S, V_G)}{\lambda_v(L)}v_s + \frac{R(L)g(L, V_D, V_G)}{\lambda_v(L)}v_d \tag{5.42}$$

Substituting i_0 from (5.42) in (5.41), we obtain

$$v(x) = G(x)v_g + S(x)v_s + D(x)v_d \tag{5.43}$$

where $G(x)$, $S(x)$ and $D(x)$ are given by

$$G(x) = \frac{\lambda_g(L)}{\lambda_v(L)}\frac{\lambda_v(x)}{R(x)g(x, V_0, V_G)} - \frac{\lambda_g(x)}{R(x)g(x, V_0, V_G)} \tag{5.44}$$

$$S(x) = \frac{g(0, V_S, V_G)}{R(x)g(x, V_0, V_G)}(1 - \frac{\lambda_v(x)}{\lambda_v(L)}) \tag{5.45}$$

$$D(x) = \frac{\lambda_v(x)}{\lambda_v(L)}\frac{R(L)g(L, V_D, V_G)}{R(x)g(x, V_0, V_G)} \tag{5.46}$$

Now comparing (5.28) with (5.30), one can easily calculate the capacitances and admittances. For instance C_{DG} and C_{SG} can be expressed as

$$C_{DG} = W\int_0^L \frac{F(x)}{F(L)}\left[\frac{\partial Q}{\partial V_G} + \frac{\partial Q}{\partial V}G(x)\right]dx \tag{5.47}$$

$$C_{SG} = W\int_0^L \left[1 - \frac{F(x)}{F(L)}\right]\left[\frac{\partial Q}{\partial V_G} + \frac{\partial Q}{\partial V}G(x)\right]dx \tag{5.48}$$

Please note that above expressions have similar appearance as Ward-Dutton partitioning scheme where $F(x) = x$. Also by applying the concept of small signal partitioning, we have achieved a considerable simplification over the existing capacitance calculation method for LAMOS. Given the $g(x, V_0)$, development reported in [6, 4] requires 4 level of numerical integration, whereas our approach eliminates a whole level of integration with out sacrificing any accuracy.

Similarly all other capacitances associated with drain and source terminals can be expressed as

$$C_{DS} = W\int_0^L \frac{F(x)}{F(L)}\left[\frac{\partial Q}{\partial V}S(x)\right]dx \tag{5.49}$$

$$C_{DD} = W \int_0^L \frac{F(x)}{F(L)} \left[\frac{\partial Q}{\partial V} D(x)\right] dx \tag{5.50}$$

$$C_{DB} = W \int_0^L \frac{F(x)}{F(L)} \left[-\frac{\partial Q}{\partial V_G} - \frac{\partial Q}{\partial V}\left[G(x) + S(x) + D(x)\right]\right] dx \tag{5.51}$$

$$C_{SD} = W \int_0^L \left[1 - \frac{F(x)}{F(L)}\right] \left[\frac{\partial Q}{\partial V} D(x)\right] dx \tag{5.52}$$

$$C_{SS} = W \int_0^L \left[1 - \frac{F(x)}{F(L)}\right] \left[\frac{\partial Q}{\partial V} S(x)\right] dx \tag{5.53}$$

$$C_{SB} = W \int_0^L \left[1 - \frac{F(x)}{F(L)}\right] \left[-\frac{\partial Q}{\partial V_G} - \frac{\partial Q}{\partial V}\left[G(x) + S(x) + D(x)\right]\right] dx \tag{5.54}$$

Please note all the terminal voltages are defined with respect to body terminal. Thus the expressions of terminal small signal voltages in C_{DB} and C_{SB} have $v_s = v_d = v_g = -v_b$.

The admittances of LAMOS from (5.42) are given by

$$Y_{DG} = \frac{\lambda_g(L)}{\lambda_v(L)}, Y_{DS} = -\frac{g_0(0)}{\lambda_v(L)}, Y_{DD} = \frac{R(L)g_0(L)}{\lambda_v(L)}, \tag{5.55}$$

5.3.2 Partitioning of Gate Tunnelling Current

When we consider gate tunnelling current as a perturbation , we use (5.2) with $\widehat{s} = i_g(x)$, where $i_g(x)$ is the gate tunnelling current per unit length. Therefore, under the presence of a gate tunnelling current, the drain current becomes

$$I_D = I_0 + \int_0^L \frac{F(x)}{F(L)} i_g(x) dx \tag{5.56}$$

It should be noticed that as gate tunnelling current increases, it may not be possible to consider $\widehat{s}$ as a perturbation, and in presence of high gate current, there can be a significant de-biasing of channel and full solution of coupled continuity and transport equation may be needed.

5.3.3 Partitioning of Gate Tunnelling Noise

For noise partitioning, we need to relate drain current fluctuation δi_d to gate current fluctuation δi_g. Following [13], from (5.56) we obtain

$$\delta i_d = \frac{1}{F(L)} \int_0^L F(x) \delta i_g(x) dx \tag{5.57}$$

then in terms of noise

$$S_{i_d}^g = \frac{1}{F(L)^2} \int_0^L \int_0^L F(x_1) F(x_2) \overline{\delta i_g(x_1) \delta i_g(x_2)} dx_1 dx_2 \tag{5.58}$$

Assuming that the noise sources at different position are uncorrelated $\overline{\delta i_g(x_1)\delta i_g(x_2)} = S_g(x_1)\delta(x_1 - x_2)$, we finally obtain

$$S_{i_d}^g = \frac{1}{F(L)^2}\int_0^L \int_0^L F(x)^2 S_g(x)dx \tag{5.59}$$

We can split the local gate noise $S_g(x)$ into two parts as $S_g(x) = S_g^{shot}(x) + S_g^{flicker}(x)$. Now $S_g^{shot}(x)$ and $S_g^{flicker}(x)$ must have different x dependence because [13]

$$\int_0^L S_g^{shot}(x)dx \propto I_G \tag{5.60}$$

and

$$\int_0^L S_g^{flicker}(x)dx \propto I_G^2 \tag{5.61}$$

Therefore a bit detailed analysis by us clearly shows that the noise partitioning depends on the details of the noise mechanism (the $S_g(x)$ term) and will be different for shot and flicker noise, even in the conventional MOSFET.

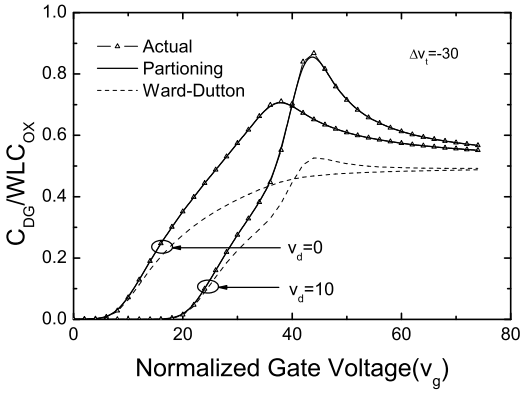
5.4 Discussion and Results

In this section, we address how a bias dependent partitioning function gives rise to peaks in C_{DG} and validates our approach by comparing our scheme with numerical and device simulation. In order to study the impact of lateral asymmetry we take a position dependent threshold voltage $V_T(x)$ as [6, 4, 14]

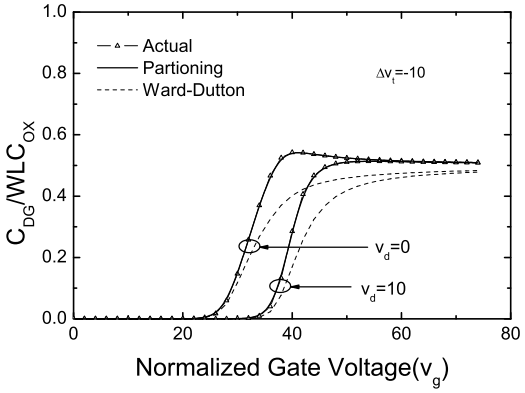
$$V_T(x) = v_{t0} \cdot U_T + \Delta v_t \cdot U_T(1 - exp(-\alpha \cdot (x/L)^2)) \tag{5.62}$$

where U_T is the thermal voltage v_{t0} is the normalized threshold voltage at the source, Δv_t is indicative of the difference between the source and drain threshold voltages and α determines the sharpness of the profile. Now we calculate the capacitances numerically as follows: we first vary any terminal voltages by δv_k and solve the small signal version of (5.2) to obtain $v(x)$ and substitute this in (5.34) to obtain the imaginary part of the current (i_y^{im}) at the source or the drain. By definition the capacitance becomes $C_{yk} = i_y^{im}/(j\omega\delta v_k)$. We will call these capacitances as actual capacitances. We also calculate the capacitances using our partitioning scheme (5.51) and (5.54) and Ward-Dutton partitioning scheme. For numerical simulation, we will take v_{t0}=40, $\alpha = 1.3$, $\Delta v_t = -10, -30$ and $v_d = 0, 10$. It has been confirmed that at low frequency, the actual capacitances are independent of the frequency, which means as expected the quasi-static assumption holds quite well.

Fig. 5.1(a) shows the plot of C_{DG} calculated by the three different methods for $\Delta v_t = -30$. As expected, our partitioning scheme and exact numerical solution show the perfect agreement and captures the peaks in C_{DG} which is a typical characteristics of LAMOS. The peak in C_{DG} can be explained by the bias dependence of partition function. First, consider the situation, when the source is in weak inversion and the drain is in strong inversion. This situation will occur because the threshold voltage at the source is greater than the threshold voltage at drain. In this case, as $g(x, V_0, V_G)$ is very small near the source, the function $f(x)$ decays off very rapidly



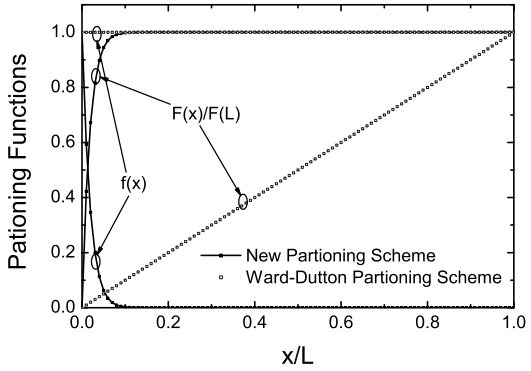
(a)



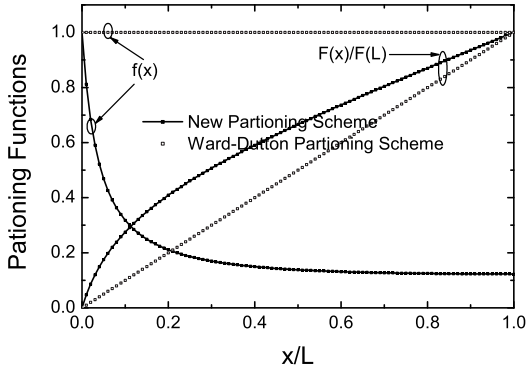
(b)

Figure 5.1: The plot of drain-to-gate capacitance C_{DG} vs v_g for (a) $\Delta v_t = -30$ and (b) $\Delta v_t = -10$. All the voltages have been normalized by thermal voltage U_T.

near the source because of the $\frac{1}{g(x,V_0,V_G)}$ term present in the exponential of $f(x)$. As a result, the partition function $F(x)$ (which is the integral of $f(x)$) remains constant almost all over the channel except a very small region near the source where it increases to take the saturation value (see Fig. 5.2(a)). Now in this situation as the gate voltage increases a part of channel gradually comes out of the weak inversion and enters the strong inversion. Therefore C_{DG} increases with gate voltage. This situation continues till the gate voltage is less than the threshold voltage of the source end. As the gate voltage exceeds the threshold voltage of the source end, the region near the source starts to enter into the strong inversion because of this the $g(x, V_0, V_G)$ starts to increase. As a result, the function $f(x)$ decays less rapidly and $F(x)$ increases continuously (see Fig. 5.2(b)). It means that the capacitance near the strongly inverted source region now gradually getting a lesser weight, as a consequence C_{DG} decreases with the gate voltage. Note that as Ward-Dutton partitioning function always take $F(x) = x$, it can never explain the sharp peak in C_{DG} curve. Also note that for $v_d = 10$, the peak increases because a change in gate voltage induces a change in the channel potential (the perturbed channel potential becomes



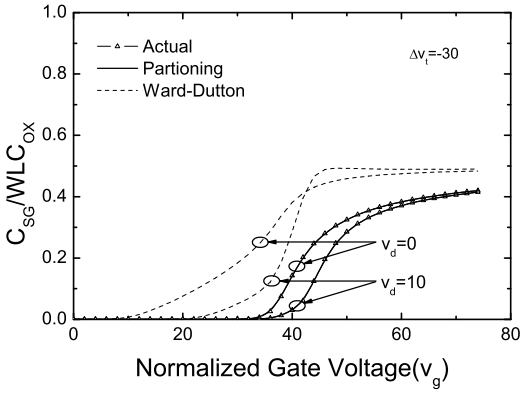
(a)



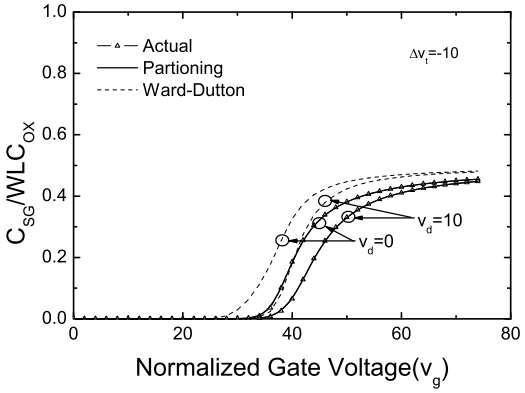
(b)

Figure 5.2: Profile of partitioning functions for (a) $v_g < v_{t0}$ and (b) $v_g > v_{t0}$. In the first case, as $g(x, V_0, V_G)$ is very small near the source, the function f(x) decays off very rapidly near the source (because of the $\frac{1}{g(x,V_0,V_G)}$ term present in the $\widehat{s}$ term). As a result, the partition function $F(x)$ (which is the integral of $f(x)$) remains constant almost all over the channel. In the second case, $f(x)$ decays less rapidly in strong inversion and thus $F(x)$ is increasing continuously from source to drain.

negative), which in turn causes a change in charge distribution and the combined effect increases the peak. To understand why perturbed channel potential can become negative to increase the small signal charge, consider the situation, when the source end is weakly inverted and drain end is strongly inverted. In this case the transistor can be thought of a series combination of two transistors with different threshold voltage, where the one near the source is weakly inverted and near the drain end is strongly inverted. Now let Q_S and Q_D be the charge at the source and drain end of the strongly inverted. The current I flowing through this transistor is proportional to $Q_S^2 - Q_D^2$. The weakly inverted transistor in series forces I to be very small, therefore $Q_S^2 \approx Q_D^2$. Now as gate voltage increases both Q_S and Q_D will increase and we have $\delta Q_S Q_S \approx \delta Q_D Q_D$. As drain end is kept at a fixed channel potential and is in strong inversion



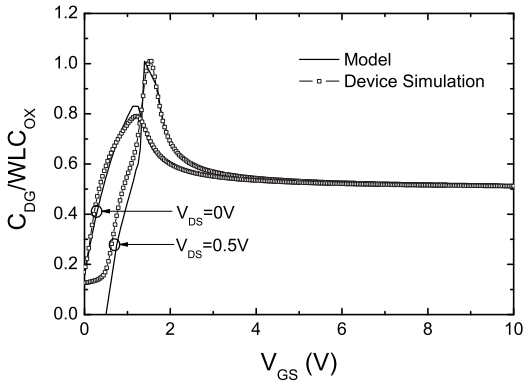
(a)



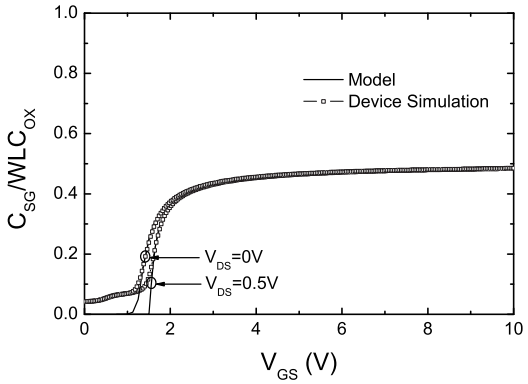
(b)

Figure 5.3: The plot of source-to-gate capacitance C_{SG} vs v_g for (a) $\Delta v_t = -30$ and (b) $\Delta v_t = -10$. All the voltages have been normalized by thermal voltage U_T.

$\delta Q_D \approx C_{ox}\delta V_G$. So we have $\delta Q_S/\delta V_G \approx (Q_D/Q_S)C_{ox}$. As $Q_D > Q_S$ in this situation (because the source end has higher doping), we have $\delta Q_S/\delta V_G > C_{ox}$, which is only possible, if the channel potential goes negative and adds in the gate voltage. Depending on the profile and drain voltage, the peak in C_{DG} vs V_{GS} curve may even increase above C_{ox} in presence of the gate voltage [5]. Fig. 5.1(b) shows the C_{DG} for $\Delta v_t = -10$. As the doping difference between the source and drain is now much less, the peak is less pronounced. From this discussion, it should be clear that if one chooses sufficiently large drain voltage to prevent the drain region entering into strong inversion before the source region, the peak in C_{DG} should disappear. Our numerical simulation $\Delta v_t = -10, v_d = 10$ represents this situation in Fig. 5.1(b). Fig. 5.3 shows the plot for C_{SG}, where our partitioning scheme and exact numerical solution also show perfect agreement. Fig. 5.4 shows a comparison with device simulation for C_{DG} and C_{SG}, where we also obtain a satisfactory agreement. The discrepancy is due to the approximations that are inherent in the expression of $g(x, V_0, V_G)$ (charge sheet approximation, inversion charge linearization etc.)



(a)



(b)

Figure 5.4: Model validation on device simulation: (a) Drain-to-gate capacitance C_{DG} vs V_{GS} for $V_{DS} = 0$ and 0.5V (b) Source-to-gate capacitance C_{SG} vs V_{GS} for $V_{DS} = 0$ and 0.5V.

Although we are able to provide a considerable simplification over the existing approach [6, 4], work needs to be done to get a more simpler approximate compact models [2] depending on specific models of $g(x, V_0, V_G)$. This new insight and a correspondence with existing Ward-Dutton partitioning may be helpful for this purpose. Even if a simplification of our exact formulation is done, the model will be a QS capacitance based model which may have some problems [15].

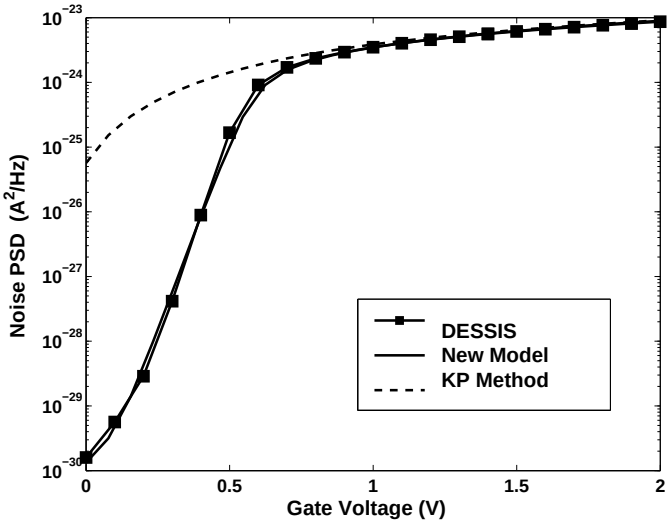


Figure 5.5: Plot of drain thermal noise power spectral density (PSD) vs. gate voltage for LAMOS at $V_{DS} = 0$. The KP method grossly overestimates the noise current especially at low gate voltages. The dotted line represents noise calculated using KP method, which is valid for conventional MOSFET and states that the drain noise current PSD is proportional to total inversion charge in the channel. We see that this approach grossly overestimates the noise current especially at low gate voltages. This suggests that the noise properties of LAMOS is considerably different from conventional MOSFET. Our proposed model correctly captures the trend and gives very good match with device simulation.

5.5 Noise Modeling in the Lateral Non-uniformly doped MOSFET

As the efforts for a compact LDMOS model [16, 17, 18, 19] for standardization is going on by the Compact Model Council (CMC) [20], the noise modeling has been set a mandatory feature for an industry standard compact model. The MOSFET noise models are either built on Klaassen-Prins (KP) [11] or some equivalent methods [21, 22, 23, 24], which are all denoted here as KP method. Fig. 5.5 shows the plot of the drain current power spectral density (PSD) in equilibrium versus the gate voltage obtained from a 2-D device noise simulation (DESSIS) and the noise PSD predicted by KP method. It shows that even in equilibrium, the KP method grossly overestimates the noise at low value of gate voltages, which reveals the importance of a new noise calculation method. Starting from a Langevin description [24], we will develop an analytical noise model for LAMOS [10, 25] and explain why the KP method fails.

5.5.1 Development of the noise model

Let's start with the basic principles of the Langevin method as shown in Fig. 5.6. The current at any position in the MOSFET channel has two components. One component is set up by the voltage perturbation caused by the noise source (which can be thought of flowing through the resistances) and other one is the noise current itself (which is represented by the noisy current source $\delta i_n(x)$). Δi_d is the total noise current flowing through the channel and is constant along

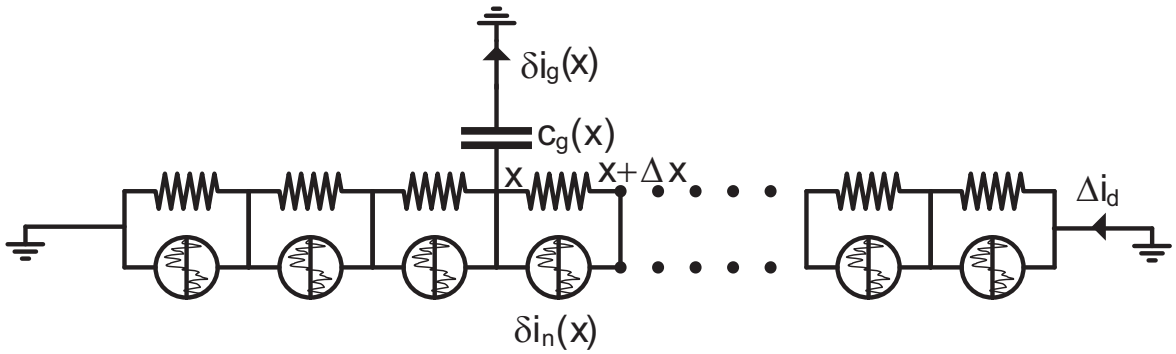


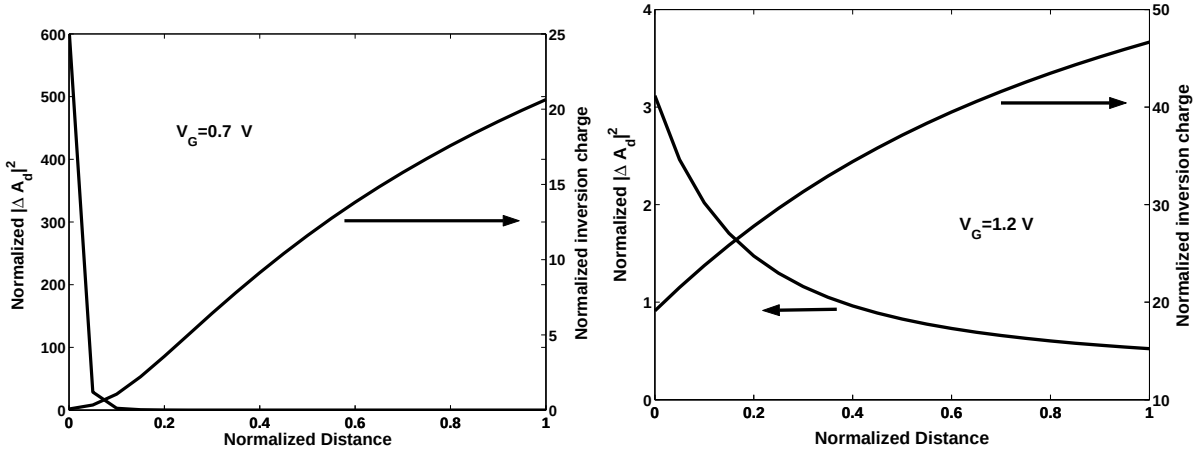
Figure 5.6: Illustration of the noise calculation by using a Langevin approach. $\delta i_n(x)$ is the noise current source, Δi_d is the terminal noise current, $\Delta i_g(x)$ is induced gate noise, which originates due to the fluctuation of channel potential across the gate capacitance $C_g(x)$. The current at any position has two components. One component is set up by the voltage perturbation caused by the noise source (which can be thought of flowing through the resistances) and other one is the noise current itself (which is represented by the noisy current source $\delta i_n(x)$). Δi_d is the total noise current flowing through the channel and is constant along the channel. The induced gate current noise $\Delta i_g(x)$ originates due to the fluctuation of channel potential across the gate capacitance $C_g(x)$ and lies in quadrature with the drain current noise.

the channel. The induced gate current noise $\Delta i_g(x)$ originates due to the fluctuation of channel potential across the gate capacitance $C_g(x)$ and lies in quadrature with the drain current noise.

The basic mathematical steps have been derived in Appendix B. Note that, to keep our analysis general, mobility degradation has also been taken into account. One of the essential steps in noise calculation is to find a proper small-signal description of the transport equation as shown in (B.2)-(B.8). One of the interesting results is (B.7), which illustrates the impact of the mobility degradation in the chain rule. Instead of trying to solve (B.8) directly, the 'trick' we apply is to rewrite (B.8) as a linear ODE with respect to the quantity $g(x, V, \frac{dV}{dx}) \cdot v$ with an integration factor $R(x)$ (see (B.9)). Using $R(x)$, we put the perturbed channel potential v inside a proper differential (B.10). Next we use the facts that total noise current Δi_d is constant along the channel and v vanishes at the boundaries to obtain drain current (B.13). Please note that when there is no lateral asymmetry, $\partial g(x, V, \frac{dV}{dx})/\partial x$ vanishes and one get back to the noise expression of [24]. In addition when there is also no mobility degradation, we get back the conventional KP equation [11]. To obtain the gate current (B.14), we apply a variant of the techniques developed in [24]. Once the current is obtained, PSDs can be easily calculated (see (B.18)-(B.22)).

5.5.2 Result and discussion

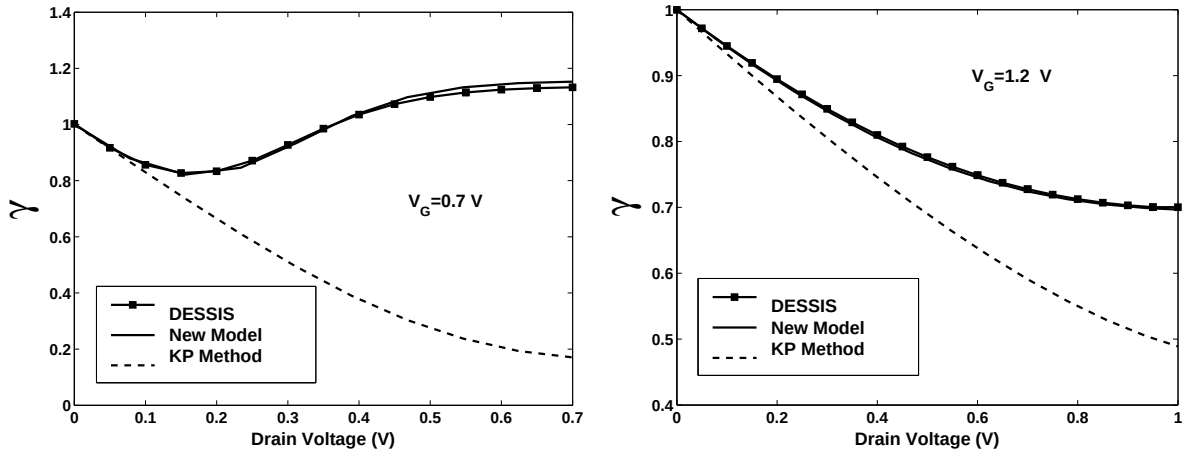
Let's first discuss, why conventional KP based methods fail for LAMOS. If we integrate (B.8) (as done in the original derivation [11]), the presence of lateral asymmetry generates an additional term, which depends on the profile of perturbed channel potential v. This fact drastically changes the so called vector impedance field (IF) [24, 26] of the device. Eq. (B.13) reveals that the contribution to the terminal drain noise from any point gets determined by the product of two terms. First one is the IF for drain, ΔA_d (see (B.16)), which represents the noise propagation



(a) (b)

Figure 5.7: Profile of squared drain IF (normalized with respect to the inverse of channel length) and inversion charge density (normalized by $C_{ox}U_T$) at $V_{DS} = 0$ (a) for low gate voltage ($V_G = 0.7$ V) and (b) for high gate voltage ($V_G = 1.2$ V). The PSD of the local noise source is proportional to the inversion charge. For normal MOSFET the normalized IF is equal to 1 but it is peaked near the source for lateral MOSFET. This considerably changes the noise behavior of LA MOSFET.

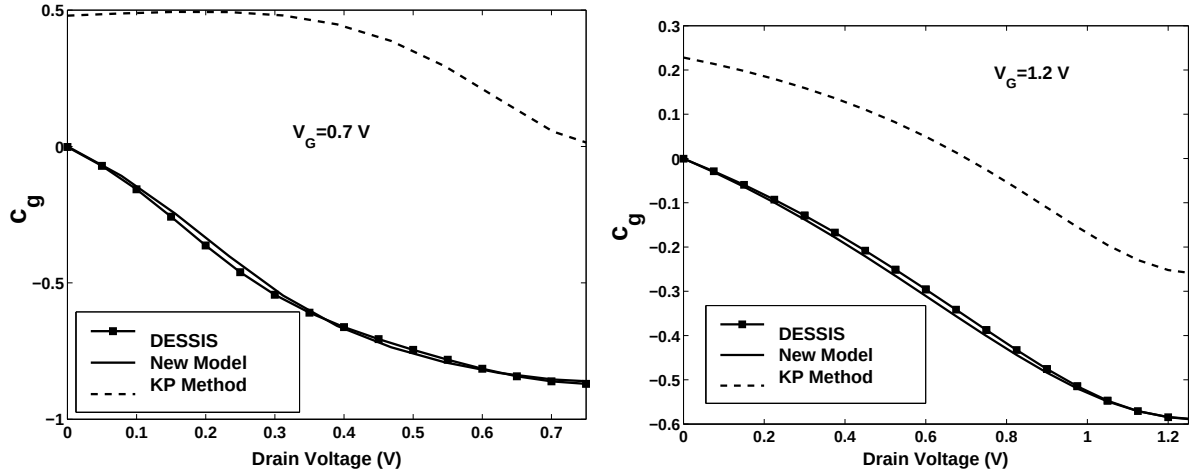
and the second term is the local noise source, whose PSD is proportional to the inversion charge (see (B.22)). Fig. 5.7 shows the plot of IF and inversion charge density versus normalized position. For a conventional MOSFET, IF is independent of position and equal to the inverse of the channel length [24, 27]. But the lateral asymmetry causes ΔA_d to highly peak near the source end and this effect is much more prominent at low gate voltages (Fig. 5.7(a)). As the source end is highly doped compared to the drain end, the inversion charge towards the drain end is much higher. These immediately reveal that KP grossly overestimates the noise current because it assigns the same weight to both strongly inverted region near the drain and weak/moderately inverted region near the source. Whereas in reality, the weak/moderately inverted region near the source gets a much higher weight and dominates the noise behavior. As the gate voltage increases, ΔA_d becomes less sharply peaked and also the difference between drain and source end charge decreases (Fig. 5.7(b)). Therefore, at high gate voltages KP can give an 'order of magnitude' kind of estimate (Fig. 5.5). The reason for the sharp peaking of the IF mathematically follows from (B.11). At low gate voltages, the value of $g(x, V, E)$ at source end will be very low, therefore the factor inside the exponential present in ΔA_d is very high, which causes this sharp peak. At higher gate voltages the value of $g(x, V, E)$ near the source is large so the exponential decays slowly. A 'crude' physical reasoning of this behavior is the following: if we lump the effect of distributed doping into two transistors, at low gate voltages the transistor near the source end will be weakly inverted and transistor near drain end will be strongly inverted. As the weakly inverted transistor has a much higher resistance and noise voltage (which, as a first order approximation, is proportional to the resistance), it follows that the noise current of the total combination will be determined by the weakly inverted transistor. In order to validate our theory, we made extensive comparison with ISE-DESIS, which calculates noise using a 2-D



(a) (b)

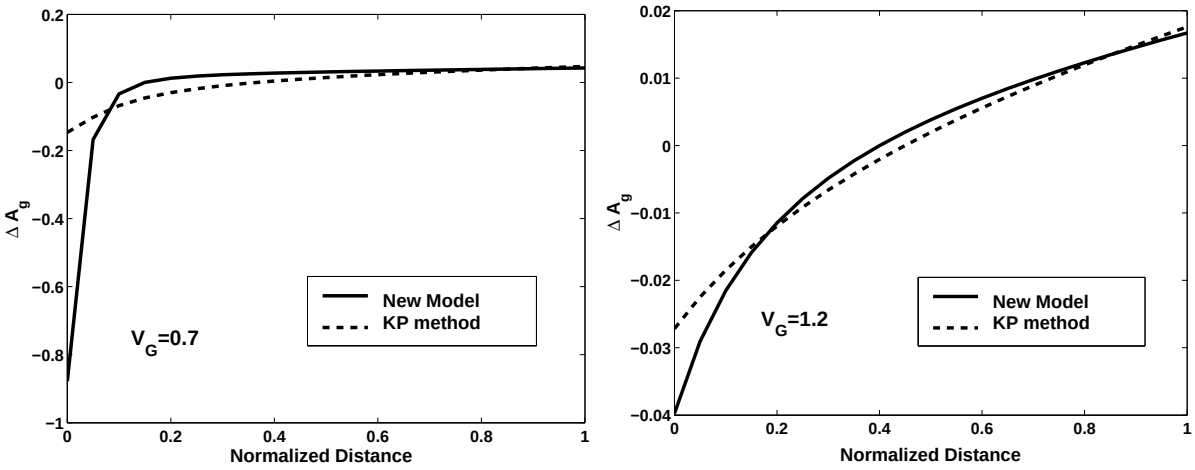
Figure 5.8: Model validation on numerical device simulation (DESSIS): Plot of γ versus drain voltage (a) at low gate voltage ($V_G = 0.7$ V) and (b) at high gate voltage ($V_G = 1.2$ V). At low gate voltage the shape can not be captured by KP method.

Greens function method. The structure simulated has a source doping of 5×10^{17} cm^{-3} and a drain doping of 1×10^{16} cm^{-3}, channel length of 2 μm, width of 1 μm, and a oxide thickness of 8 nm. Fig. 5.5 shows that our model is in close agreement with the device noise simulation in equilibrium. In order to check the bias dependence, we plot the noise factor γ (see (B.23)) as a function of drain voltage in Fig. 5.8. As an increase in drain voltage always decreases the total charge, the KP method can only predict a monotonically decreasing behavior of γ but both TCAD and our model predicts a minimum at low gate voltages (Fig. 5.8(a)) and our model satisfactorily matches the TCAD. The valley appears because the drain voltage also influences ΔA_d in a complicated way. Fig. 5.8(b) shows the same plot at high gate voltage, where we get back the expected monotonic decrease. In order to validate our induced gate noise modeling approach, we plot the correlation between drain and induced gate noise, c_g (see (B.24)), as function of drain voltage. Fig. 5.9(a) and Fig. 5.9(b) show the plots of c_g for low and high gate voltages respectively and our model again gives a very good match. Note that this term also behaves considerably different from conventional MOSFET where c_g saturates to 0.6 at weak inversion and to 0.4 at strong inversion [28, 29]. It is very interesting to note that KP based methods [24, 30, 31] for induced gate noise produces even a sign error in the correlation coefficient. This can be understood by noticing that the induced gate current changes sign as one moves from source to drain [24]. Fig. 5.10 shows the profile of IF for induced gate current ΔA_g (see (B.17)). Here also the conventional method incorrectly puts a lower weight to the source end, and as the charge is much higher near drain end, the total contribution gets dominated by the drain end. But in reality, as actual IF plots show, the gate noise gets dominated by the source end. As IF changes sign from source to drain, it is evident that KP method will cause a sign error.



(a) (b)

Figure 5.9: Model validation on numerical device simulation (DESSIS): Plot of the imaginary part of c_g versus drain voltage at (a) low gate voltage ($V_G = 0.7$ V) and (b) at high gate voltage ($V_G = 1.2$). KP method is totally incapable of predicting the behavior and even gives a wrong sign.



(a) (b)

Figure 5.10: Model validation on numerical device simulation (DESSIS): Profile of impedance field for gate current (at $V_{DS} = 0$) at (a) low gate voltage ($V_G = 0.7$ V) and (b) high gate voltage ($V_G = 1.2$ V). For gate impedance field also, KP underestimates the value at source end. As ΔA_g changes sign from source to drain, this underestimation gives a sign error in the correlation coefficient.

5.6 Conclusion

In this chapter, we discussed the *limitation of the Ward-Dutton partitioning scheme* with focus on lateral non-uniformly doped MOSFET. We showed the *existence of the small-signal partitioning scheme* for the situation when lateral asymmetry can be present in the MOSFET channel. The concept of the small signal partitioning is then successfully used to define the partitioning of perturbed charge from which the capacitances are calculated. This development provides a simple way of calculating capacitances. The proposed development was validated on the numerical device simulation and showed good results. As failure of Ward-Dutton scheme makes the concept of terminal charge invalid, the future compact modeling methodologies may undergo major changes. This new insight and a correspondence with existing Ward-Dutton partitioning will be helpful for developing simpler compact models for high voltage MOSFETs.

For the first time, *a general analytical noise modeling methodology* accounting for both lateral asymmetry and field dependent mobility was presented. This methodology is applicable to any kind of noise mechanism. The model was validated on the numerical device simulation and it was also explained why the noise properties in presence of lateral asymmetry are drastically different from conventional MOSFET.

Bibliography

[1] S.-Y. OH, D. Ward, and R. Dutton, "Transient analysis of MOS transistors ," *IEEE Transactions Electron Devices*, vol. 27, no. 8, pp. 1571–1578, Aug. 1980.

[2] J. Watts, C. McAndrew, C. Enz, C. Galup-Montoro, G. Gildenblat, C. Hu, R. van Langevelde, M. Miura-Mattausch, R. Rios, and C.-T. Sah, " Advanced Compact Models for MOSFETs ," in *Technical Proceedings of the 2005 Workshop on Compact Modeling*, May 2005, pp. 3–12.

[3] Y. S. Chauhan, F. Krummenacher, R. Gillon, B. Bakeroot, M. Declercq, and A. M. Ionescu, "A New Charge based Compact Model for Lateral Asymmetric MOSFET and its application to High Voltage MOSFET Modeling," in *IEEE International Conference on VLSI Design and International Conference on Embedded Systems*, Jan. 2007, pp. 177 – 182.

[4] A. Aarts, R. van der Hout, J. Paasschens, A. Scholten, M. Willemsen, and D. Klaassen, "New fundamental insights into capacitance modeling of laterally nonuniform MOS devices," *IEEE Transactions Electron Devices*, vol. 53, no. 2, pp. 270 – 278, Feb. 2006.

[5] Y. S. Chauhan, F. Krummenacher, C. Anghel, R. Gillon, B. Bakeroot, M. Declercq, and A. M. Ionescu, "Analysis and Modeling of Lateral Non-Uniform Doping in High-Voltage MOSFETs," in *IEEE International Electron Devices Meeting*, Dec. 2006, pp. 8.3.1 – 8.3.4.

[6] A. Aarts, R. van der Hout, J. Paasschens, A. Scholten, M. Willemsen, and D. Klaassen, "Capacitance modeling of laterally non-uniform MOS devices," in *IEEE International Electron Devices Meeting*, Dec. 2004, pp. 751 – 754.

[7] Y. S. Chauhan, F. Krummenacher, R. Gillon, B. Bakeroot, M. Declercq, and A. M. Ionescu, "Compact Modeling of Lateral Non-uniform doping in High-Voltage MOSFETs," *IEEE Transactions on Electron Devices*, vol. 54, no. 6, pp. 1527–1539, June 2007.

[8] A. S. Roy, Y. S. Chauhan, C. Enz, J.-M. Sallese, A. M. Ionescu, and M. Declercq, "Partitioning Scheme in Lateral Asymmetric MOST," in *IEEE European Solid-State Device Research Conference*, Sept. 2006, pp. 307–310.

[9] A. S. Roy, C. C. Enz, and J.-M. Sallese, "Drain-Source Partitioning in MOSFET," *IEEE Transactions on Electron Devices*, June 2007.

[10] A. S. Roy, Y. S. Chauhan, C. Enz, and J.-M. Sallese, "Noise modeling in lateral asymmetric MOSFET," in *IEEE International Electron Devices Meeting (IEDM)*, Dec. 2006, pp. 191– 194.

[11] F. M. Klaassen and J. Prins, "Thermal Noise of MOS Transistors," *Philips Res. Repts*, vol. 22, pp. 505–514, Oct. 1967.

[12] A. S. Roy, C. C. Enz, and J. M. Sallese, "Charge, current, and noise partitioning in MOSFET in the presence of mobility degradation," *IEEE Electron Device Letters*, vol. 27, no. 8, pp. 674 – 677, Aug. 2006.

[13] J. Ranuarez, M. Deen, and C.-H. Chen, "Modeling the partition of noise from the gate-tunneling current in MOSFETs," *IEEE Electron Device Letters*, vol. 26, no. 8, pp. 550–552, Aug. 2005.

[14] Y. S. Chauhan, R. Gillon, M. Declercq, and A. M. Ionescu, "Impact of Lateral Non-uniform doping and hot carrier degradation on Capacitance behavior of High Voltage MOSFETs," in *IEEE European Solid-State Device Research Conference (ESSDERC)*, Sept. 2007.

[15] P. Yang, B. D. Epler, and P. Chatterjee, "An Investigation of the Charge Conservation Problem for MOSFET Circuit Simulation," *IEEE Journal of Solid-State Circuits*, vol. 18, no. 1, pp. 128– 138, Feb 1983.

[16] L. Vestling, J. Ankarcrona, and J. Olsson, "Analysis and design of a low-voltage high-frequency LDMOS transistor," *IEEE Transactions on Electron Devices*, vol. 49, no. 6, pp. 976–980, 2002.

[17] J. Kim, S. Kim, J. Koo, and D. Kim, "p-channel LDMOS transistor using new tapered field oxidation technology," *IEE Electronics Letters*, vol. 34, no. 19, pp. 1893–1894, 1998.

[18] P. Santos, V. Costa, M. Gomes, B. Borges, and M. Lanca, "High-voltage LDMOS transistors fully compatible with a deep-submicron 0.35 μ m CMOS process," *Microelectronics Journal*, vol. 38, no. 1, pp. 35–40, 2007.

[19] G. Cao, S. K. Manhas, E. Narayanan, M. M. D. Souza, and D. Hinchley, "Comparative study of drift region designs in RF LDMOSFETs," *IEEE Transactions on Electron Devices*, vol. 51, no. 8, pp. 1296– 1303, 2004.

[20] "Compact model council (CMC)," , http://www.eigroup.org/cmc/.

[21] R. P. Jindal, "High frequency noise in fine line NMOS field effect transistors," in *IEEE International Electron Devices Meeting (IEDM)*, Dec. 1985, pp. 68– 71.

[22] C. Enz and Y. Cheng, "MOS transistor modeling for RF IC design," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 2, pp. 186–201, Feb. 2000.

[23] R. P. Jindal, "Compact Noise Models for MOSFETs," *IEEE Transactions on Electron Devices*, vol. 53, no. 9, pp. 2051– 2061, Sept. 2006.

[24] A. S. Roy, C. C. Enz, and J.-M. Sallese, "Noise Modeling Methodologies in the Presence of Mobility Degradation and Their Equivalence," *IEEE Transactions Electron Devices*, vol. 53, no. 2, pp. 348–355, Feb. 2006.

[25] E. Simoen, C. Claeys, T. Chung, D. Flandre, M. Pavanello, J. Martino, and J.-P. Raskin, "The low-frequency noise behaviour of graded-channel SOI nMOSFETs," *Solid-State Electronics*, vol. 51, no. 2, pp. 260–267, Feb. 2007.

[26] F. Bonani and G. Ghione, *Noise in Semiconductor Devices : Modeling and Simulation*. Springer, 2001.

[27] A. S. Roy and C. Enz, "Compact Modeling of Thermal Noise in the MOS Transistor," *IEEE Transactions Electron Devices*, vol. 52, no. 4, pp. 611–614, Apr. 2005.

[28] C.-H. Chen, M. J. Deen, Y. Cheng, and M. Matloubian, "Extraction of the induced gate noise, channel noise, and their correlation in submicron MOSFETs from RF noise measurements," *IEEE Transactions on Electron Devices*, vol. 48, no. 12, pp. 2884–2892, Dec. 2001.

[29] R. P. Jindal, "Effect of induced gate noise at zero drain bias in field-effect transistors," *IEEE Transactions on Electron Devices*, vol. 52, no. 3, pp. 432– 434, Mar. 2005.

[30] J. C. J. Paasschens, A. J. Scholten, and R. van Langevelde, "Generalisations of the Klaassen-Prins Equation for Calculating the Noise of Semiconductor Devices," *IEEE Transactions Electron Devices*, vol. 52, no. 11, pp. 2463– 2472, Nov. 2005.

[31] R. van Langevelde, J. Paasschens, A. Scholten, R. Havens, L. Tiemeijer, and D. Klaassen, "New compact model for induced gate current noise [MOSFET]," in *IEEE International Electron Devices Meeting (IEDM)*, Dec. 2003, pp. 36.2.1– 36.2.4.

Chapter 6

Conclusion

The major achievements of this work can be summarized as follows:

I. EKV based General High Voltage MOSFET Model

A *general* High Voltage MOSFET model based on the EKV model as a core and new bias dependent drift resistance was developed. The model performance was demonstrated for three industrial devices: VDMOS, bulk-LDMOS and SOI-LDMOS. The model correctly reproduces the special effects of high voltage devices like the quasi-saturation and self-heating effect, and is highly scalable with all physical and electrical parameters such as transistor width, drift length, number of fingers and temperature. The model shows good results for entire DC bias range and good behavior for capacitances, especially the peaks and shift of these peaks with bias. The model provides excellent trade-off between speed, convergence and accuracy, being suitable for circuit simulation in any operation regime of HV MOSFETs. The model has been implemented in Verilog-A and tested on SABER (Synopsys), ELDO (Mentor Graphics) and Cadence's Virtuoso Spectre circuit simulator and Virtuoso UltraSim fast-Spice simulator for industrial use. The model fulfils all the accuracy target required by the industry for high voltage MOSFET models.

II. Compact Modeling of Lateral Non-uniform doping

A *novel* charge based compact analytical model for lateral non-uniformly doped MOSFET was developed in this chapter. The model is developed using charge based EKV formalism. The major impact of the lateral non-uniform doping was seen on the capacitances, whose modeling has been a daunting task till now as expressions become non-integrable and non-implicit for current and charges. The inversion charge linearization paved the way to approximate the surface pinch-off potential across the channel. This led to develop integrable expressions for current and then charges. The inversion and gate charge in this model have clear dependence on the drain current, which is not the case in the conventional MOSFET models. Although this model was developed primarily for high voltage MOS devices, the lateral asymmetric channel devices have also demonstrated good behavior in deep sub-micron devices for higher performance in analog, RF and mixed signal design. In fact, lateral non-uniform doping is inherent in halo-doped nano-MOSFETs.

The proposed model was used for modeling of high voltage devices with a lateral doping gradient using an appropriate drift model. To the best of our knowledge, *this is the first time,*

the modeling of lateral non-uniform doping has been implemented in any high voltage compact model. The model shows good behavior for all capacitances as well as for DC, when compared with device simulation and measurements. The position of the capacitance peaks as well as their amplitude are correctly simulated by the model. The major impact of the proposed model is on the accuracy improvement of high voltage MOSFET models especially during transient operations (i.e. modeling of the bias-dependent peaks and slopes of device capacitances).

III. Partitioning Scheme and Noise Modeling in LAMOS

The limitation of the Ward-Dutton partitioning was explained. The existence of the small-signal partitioning scheme for the lateral non-uniformly doped MOSFET was developed. The concept of the small signal partitioning was successfully used to define the partitioning of perturbed charge from which the capacitance were calculated. This development provided a simple mean of evaluating capacitances of lateral non-uniformly doped MOSFET. It was evident, as failure of Ward-Dutton scheme makes the concept of terminal charge invalid, the future compact modeling methodologies may undergo major changes. This new insight and a correspondence with existing Ward-Dutton partitioning will be helpful for developing simpler compact models for high voltage MOSFETs. Also, for the first time, a general analytical noise modeling methodology accounting for both lateral asymmetry and field dependent mobility was presented. This methodology is applicable to any kind of noise mechanism. It was also explained why the noise properties in presence of lateral asymmetry are drastically different from conventional MOSFET.

The research work in this thesis has been successful in solving several problems related to high voltage MOS modeling. Still there are several things which should be improved or solved for a better high voltage MOS model. Following is the list of tasks which needs to be done in future to get high performance HVMOS model:

➤ Length Scaling in Lateral Non-uniformly doped transistor
➤ Noise modeling and implementation in HVMOS
➤ Simplified partitioning scheme for Lateral Non-uniformly doped transistor
➤ Charge or surface potential based modeling of drift region
➤ Accurate modeling of the overlap capacitance in the drift region

Appendix A

Solutions of transcendental equations of ψ_p, q_s and q_d

A.1 Evaluation of ψ_p

The transcendental equation for ψ_p in normalized form can be rewritten from (5.6) as

$$v_g - v_{fb} = \psi_p + sign(\psi_p)\gamma\sqrt{e^{-\psi_p} + \psi_p - 1} \tag{A.1}$$

where $\psi_p = \frac{\Psi_P}{U_T}$, $v_{fb} = \frac{V_{FB}}{U_T}$ and $\gamma = \frac{\Gamma}{U_T}$ are in the normalized forms. A simple routine for approximation of ψ_p has been developed to get the solution of this transcendental equation given below.

$$\psi_{p0} = \left[\frac{v_g - v_{fb}}{2} - 3\left(1 + \frac{\gamma}{\sqrt{2}}\right)\right] + \sqrt{\left[\frac{v_g - v_{fb}}{2} - 3\left(1 + \frac{\gamma}{\sqrt{2}}\right)\right]^2 + 6(v_g - v_{fb})} \tag{A.2}$$

Then

$$\psi_p = \begin{cases} -ln\left[1 - \psi_{p0} + \left(\frac{v_g - v_{fb} - \psi_{p0}}{\gamma}\right)^2\right], & \text{if } v_g < v_{fb}; \\ \left[\sqrt{v_g - v_{fb} - (1 - e^{-\psi_{p0}}) + \left(\frac{\gamma}{2}\right)^2} - \frac{\gamma}{2}\right]^2 + \left(1 - e^{-\psi_{p0}}\right), & \text{otherwise} \end{cases} \tag{A.3}$$

A.2 Evaluation of q $(= q_s$ or $q_d)$

The transcendental equation for q can be rewritten from (4.12) or (4.13) as

$$2q + ln(q) = v_p - v_{ch} \tag{A.4}$$

where q and v_{ch} can be "q_s and v_s" or "q_d and v_d". A simple routine for approximation of q has been developed to get the solution of this transcendental equation given below.

$$v = v_p - v_{ch} \tag{A.5}$$

if $v > -0.6$

$$\begin{aligned} q_0 &= \frac{1}{4}\left[v - 1.4 + \sqrt{v(v - 0.394036) + 9.662671}\right] \\ \delta_0 &= \frac{v - [2q_0 + ln(q_0)]}{2q_0 + 1} \\ q &= q_0\left[1 + \delta_0(1 + 0.07\delta_0)\right] \end{aligned} \tag{A.6}$$

otherwise

$$\begin{aligned} q_0 &= e^{\frac{1}{2}\left[v - 0.201491 - \sqrt{v(v + 0.402982) + 2.446562}\right]} \\ \delta_0 &= \frac{v - [2q_0 + ln(q_0)]}{2q_0 + 1} \\ q &= q_0\left[1 + \delta_0(1 + 0.483\delta_0)\right] \end{aligned}$$

Appendix B

Noise Modeling of LAMOS

The channel current can be written as

$$I(x) = g(x, V, E)E \tag{B.1}$$

where $g(x, V, E) = W\mu(x, E)Q_i(x, V)$ and $E = \frac{dV}{dx}$. Here Q_i is the inversion charge, V is the channel potential and E is the electric field at any position x in the channel. W is the width of the device. Fig. 5.6 can be mathematically represented as

$$I(x) + i_d(x) = g\left(x, V + v, \frac{d(V + v)}{dx}\right)\frac{d(V + v)}{dx} + \delta i_n(x) \tag{B.2}$$

The perturbation analysis of (B.2) in the similar way as in section 5.3.1 yields

$$i_d(x) = \left(g(x, V, E) + \frac{\partial g(x, V, E)}{\partial E}\frac{dV}{dx}\right)\frac{dv}{dx} + \left(\frac{\partial g(x, V, E)}{\partial V}\frac{dV}{dx}\right)v + \delta i_n(x) \tag{B.3}$$

The impact of lateral asymmetry and mobility degradation on $g(x, V, E)$ can be written as

$$\frac{dg(x, V, E)}{dx} = \frac{\partial g(x, V, E)}{\partial x} + \frac{\partial g(x, V, E)}{\partial V}E + \frac{\partial g(x, V, E)}{\partial E}\frac{dE}{dx} \tag{B.4}$$

It should be noted that the extra term $\frac{\partial g(x,V,E)}{\partial x}$ appears due to lateral asymmetry while $\frac{\partial g(x,V,E)}{\partial E}$ term appears due to mobility degradation. In conventional MOSFET, both of these terms would be zero.

At this point it is important to recognize that we have additional constraint on $\frac{dE}{dx}$ from the fact that $\frac{dI}{dx} = 0$. Thus, as E and $\frac{dE}{dx}$ are not independent because the unperturbed current is constant, we have from (B.1)

$$\frac{dI}{dx} = 0 = \frac{dg(x, V, E)}{dx}E + g(x, V, E)\frac{dE}{dx} \tag{B.5}$$

or

$$\frac{dE}{dx} = -\frac{\left(\frac{dg(x,V,E)}{dx}\right)E}{g(x, V, E)} \tag{B.6}$$

In the presence of mobility degradation, the "chain rule" becomes

$$\frac{dg(x,V,E)}{dx} = \frac{g(x,V,E)}{g(x,V,E) + \frac{\partial g(x,V,E)}{\partial E}E}\left(\frac{\partial g(x,V,E)}{\partial V}E + \frac{\partial g(x,V,E)}{\partial x}\right) \tag{B.7}$$

Using (B.7), the final expression of $i_d(x)$ from (B.3) can be written as

$$i_d(x) = \left[\frac{g(x,V,E) + \frac{\partial g(x,V,E)}{\partial E}E}{g(x,V,E)}\right]\frac{d}{dx}\left[g(x,V,E)v\right] - \frac{\partial g(x,V,E)}{\partial x}v + \delta i_n(x) = \Delta i_d \tag{B.8}$$

where Δi_d is the constant noise current flowing through the channel. Rearranging (B.8) as a ODE of gv

$$\frac{d}{dx}\left[g(x,V,E)v\right] - \left(\frac{\frac{\partial g(x,V,E)}{\partial x}}{g(x,V,E) + \frac{\partial g(x,V,E)}{\partial E}E}\right)\left[g(x,V,E)v\right] = \frac{g(x,V,E)}{g(x,V,E) + \frac{\partial g(x,V,E)}{\partial E}E}\left(\Delta i_d - \delta i_n(x)\right) \tag{B.9}$$

Using integration factor $R(x)$, the above ODE can be written as

$$\frac{d[R(x)g(x,V,E)v]}{dx} = f(x)\left(\Delta i_d - \delta i_n(x)\right) \tag{B.10}$$

where

$$R(x) = \exp\left[-\int_0^x \left(\frac{\frac{\partial g(x,V,E)}{\partial x}}{g(x,V,E) + \frac{\partial g(x,V,E)}{\partial E}E}\right)dx\right] \tag{B.11}$$

and

$$f(x) = \left[\frac{g(x,V,E)}{g(x,V,E) + \frac{\partial g(x,V,E)}{\partial E}E}\right]R(x) \tag{B.12}$$

As v vanishes at the 0 and L (L is the length of the device), the integration of (B.10) gives

$$\Delta i_d = \frac{\int_0^L f(x)\delta i_n(x)dx}{\int_0^L f(x)dx} \tag{B.13}$$

The expression of Induced gate noise can be written as

$$\Delta i_g = -j\omega W\frac{\int_0^L f(x)\left(\int_0^L f(x_1)(\lambda(x_1) - \lambda(x))dx_1\right)\delta i_n(x)dx}{\int_0^L f(x)dx} \tag{B.14}$$

where Δi_g is the total gate noise current (integral of $\delta i_g(x)$ in Fig. 5.6) and

$$\lambda(x) = \int_0^x \frac{\partial Q_g}{\partial V}\frac{1}{R(x)g(x,V,E)}dx \tag{B.15}$$

Q_g is the gate charge density at any position in the channel.

The impedance fields for drain and gate respectively are obtained as

$$\Delta A_d = \frac{f(x)}{\int_0^L f(x)dx} \tag{B.16}$$

$$\Delta A_g = -j\omega W \left[\frac{f(x)}{\int_0^L f(x)dx}\right] \left[\int_0^L f(x_1)(\lambda(x_1) - \lambda(x))dx_1\right] \tag{B.17}$$

The expressions of power spectral densities (PSD) are obtained as

Drain PSD:

$$S_{I_D^2} = \int_0^L |\Delta A_d|^2 S_{\delta i_n^2} dx \tag{B.18}$$

Gate PSD:

$$S_{I_G^2} = \int_0^L |\Delta A_g|^2 S_{\delta i_n^2} dx \tag{B.19}$$

Drain-Gate PSD:

$$S_{I_D I_G} = \int_0^L \Delta A_d \Delta A_g S_{\delta i_n^2} dx \tag{B.20}$$

where $S_{\delta i_n^2}$ is the power spectral density (PSD) of the elementary noise current δi_n [1]. Assuming the noise sources are spatially uncorrelated, we have

$$\overline{\delta i_n(x_1)\delta i_n(x_2)} = S_{\delta i_n^2}\delta(x_1 - x_2) \tag{B.21}$$

where the local noise PSD for thermal noise can be expressed as

$$S_{\delta i_n^2} = 4 \cdot q \cdot W \cdot Q_i \cdot D_n \cdot \Delta f \tag{B.22}$$

where D_n is the noise diffusivity [1]. For simple electron mobility model this definition of $S_{\delta i_n^2}$ reduces to the one used in [2] i.e. $S_{\delta i_n^2} = 4kT_L g \Delta f$, where T_L is the lattice temperature and k is the Boltzmann's constant. Finally the noise parameters are obtained as

$$\gamma = \frac{S_{I_D^2}}{4kT_L g_{ds0}} \tag{B.23}$$

$$c_g = \frac{S_{I_D I_G}}{\sqrt{S_{I_D^2} S_{I_G^2}}} \tag{B.24}$$

where g_{ds0} is the drain to source conductance at $V_{DS} = 0$.

Bibliography

[1] A. S. Roy and C. Enz, "Compact Modeling of Thermal Noise in the MOS Transistor," *IEEE Transactions Electron Devices*, vol. 52, no. 4, pp. 611–614, Apr. 2005.

[2] J. C. J. Paasschens, A. J. Scholten, and R. van Langevelde, "Generalisations of the Klaassen-Prins Equation for Calculating the Noise of Semiconductor Devices," *IEEE Transactions Electron Devices*, vol. 52, no. 11, pp. 2463– 2472, Nov. 2005.

Appendix C

Curriculum Vitae

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Professional Associations and Responsibilities
➢ Student Member of IEEE, USA
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➢ Reviewer of Solid State Electronics
➢ Former reviewer of IEEE International Conference on VLSI Design, India

Work Experience

EPFL, Lausanne, Switzerland	Designation: Research Engineer Duration: March, 2004 to July 2007 Responsibilities: Modeling of High Voltage MOSFETs
ST Microelectronics, Noida, India	Designation: Associate Design Engineer Duration: June, 2003 to Feb., 2004 Responsibilities: VLSI I/O Library Design and Validation on MAT10 quality
IIT Kanpur, India	Position: Teaching Assistant Duration: Aug., 2001 to Dec., 2002

Educational Qualifications

Master of Technology (M. Tech.)

Specialization	Microelectronics, VLSI and Display Technologies
Institute	Indian Institute of Technology (IIT), Kanpur, India
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Bachelor of Engineering (B. E.)

Specialization	Electronics and Telecommunication Engineering
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Year	June, 2001

Appendix D

List of Publications

Journal Publications:

1. K. Akarvardar, C. Eggimann, D. Tsamados, **Y. Chauhan**, G. C. Wan, A. M. Ionescu, R. T. Howe, and H.-S.P. Wong, "Analytical Modeling of the Suspended-Gate FET and Design Insights for Low Power Logic", accepted in IEEE Transactions on Electron Devices (TED).

2. Y. S. Chauhan, R. Gillon, B. Bakeroot, F. Krummenacher, M. Declercq, and A. M. Ionescu, "An EKV-based High Voltage MOSFET Model with improved mobility and drift model", accepted in Solid State Electronics (SSE).

3. Y. S. Chauhan, F. Krummenacher, R. Gillon, B. Bakeroot, M. Declercq, and A. M. Ionescu, "Compact Modeling of Lateral Non-uniform Doping in High-Voltage MOSFETs", IEEE Transactions on Electron Devices (TED), Vol. 54, No. 6, pp. 1527-1539, June 2007.

4. Y. S. Chauhan, C. Anghel, F. Krummenacher, C. Maier, R. Gillon, B. Bakeroot, B. Desoete, S. Frere, A. Baguenier Desormeaux, A. Sharma, M. Declercq, and A. M. Ionescu, "Scalable General High Voltage MOSFET Model inlcuding Quasi-Saturation and Self-Heating effect", Solid State Electronics (SSE), Vol. 50, Issues 11-12, pp. 1801-1813, Nov.-Dec. 2006.

5. C. Anghel, B. Bakeroot, **Y. S. Chauhan**, R. Gillon, C. Maier, P. Moens, J. Doutreloigne, and A. M. Ionescu, "New Method for Threshold Voltage Extraction of High Voltage MOSFETs based on Gate-to-Drain Capacitance Measurement", IEEE Electron Device Letters (EDL), Vol. 27, No. 7, pp. 602-604, July 2006.

Conference Publications:

1. Y. S. Chauhan, D. Tsamados, N. Abele, C. Eggimann, M. Declercq, and A. M. Ionescu, "Compact Modeling of Suspended Gate FET", accepted in IEEE International Conference on VLSI Design, Hyderabad, India, Jan. 2008.

2. Y. S. Chauhan, R. Gillon, M. Declercq, and A. M. Ionescu, "Impact of Lateral Non-uniform Doping and hot carrier degradation on Capacitance behavior of High-Voltage MOS-

FETs", IEEE European Solid-State Device Research Conference (ESSDERC), Munich, Germany, Sept. 2007.

3. D. Tsamados, **Y. S. Chauhan**, C. Eggimann, K. Akarvardar, H.S. Philip Wong, and A. M. Ionescu, "Numerical and analytical simulations of Suspended-Gate FET for ultra-low power inverters", IEEE European Solid-State Device Research Conference (ESSDERC), Munich, Germany, Sept. 2007.

4. K. Akarvardar, C. Eggimann, D. Tsamados, **Y. Chauhan**, G. C. Wan, A. M. Ionescu, and H.-S.P. Wong, "Analytical Modeling of the Suspended-Gate FET and Design Insights for Digital Logic", IEEE Device Research Conference (DRC), Bend, USA, June 2007.

5. W. Grabinski, T. Grasser, G. Gildenblat, G. Smit, M. Bucher, A. C. T. Aarts, A. Tajic, **Y. S. Chauhan**, A. Napieralski, T. A. Fjeldly, B. Iniguez, G. Iannaccone, M. Kayal, W. Posch, G. Wachutka, F. Pregaldiny, C. Lallement, L. Lemaitre, "MOS-AK: Open Compact Modeling Forum", (invited) International Workshop on Compact Modeling (IWCM), Yokohama, Japan, Jan. 2007.

6. Y. S. Chauhan, F. Krummenacher, R. Gillon, B. Bakeroot, M. Declercq, and A. M. Ionescu, "A New Charge based Compact Model for Lateral Asymmetric MOSFET and its application to High Voltage MOSFET Modeling", IEEE International Conference on VLSI Design, Bangalore, India, Jan. 2007.

7. Y. S. Chauhan, F. Krummenacher, C. Anghel, R. Gillon, B. Bakeroot, M. Declercq, and A. M. Ionescu, "Analysis and Modeling of Lateral Non-Uniform Doping in High-Voltage MOSFETs", IEEE International Electron Devices Meeting (IEDM), San Francisco, USA, Dec. 2006.

8. A. S. Roy, **Y. S. Chauhan**, C. C. Enz, J.-M. Sallesse, "Noise Modeling in Lateral Asymmetric MOSFET", IEEE International Electron Devices Meeting (IEDM), San Francisco, USA, Dec. 2006.

9. Y. S. Chauhan, C. Anghel, F. Krummenacher, A. M. Ionescu, M. Declercq, R. Gillon, S. Frere, and B. Desoete,"A Highly Scalable High Voltage MOSFET Model", IEEE European Solid-State Device Research Conference (ESSDERC), Montreux, Switzerland, Sept. 2006.

10. A. S. Roy, **Y. S. Chauhan**, J.-M. Sallesse, C. C. Enz, A. M. Ionescu, and M. Declercq, "Partitioning Scheme in the Lateral Asymmetric MOST", IEEE European Solid-State Device Research Conference (ESSDERC), Montreux, Switzerland, Sept. 2006.

11. Y. S. Chauhan, C. Anghel, F. Krummenacher, R. Gillon, A. Baguenier, B. Desoete, S. Frere, A. M. Ionescu and M. Declercq, "A Compact DC and AC Model for Circuit Simulation of High Voltage VDMOS Transistor", IEEE International Symposium on Quality Electronic Design (ISQED), San Jose, USA, March 2006.

12. C. Anghel, **Y. S. Chauhan**, N. Hefyene and A. M. Ionescu, "A Physical Analysis of High

Voltage MOSFET Capacitance Behaviour", IEEE International Symposium on Industrial Electronics (ISIE), Dubrovnik, Croatia, June 2005.

13. B. Mazhari, **Yogesh S. Chauhan**, "Design of current-Programmed amorphous-Silicon AMOLED Pixel Circuit", The 8th Asian Symposium on Information Display (ASID), China, 2003.

14. B. Mazhari, **Yogesh S. Chauhan**, "A New Negative Feedback based poly-Silicon AMOLED Pixel Circuit with Highly Linear Transfer Characteristics", 10th International Display Workshop (IDW), Fukuoka, Japan, 2003.

Invited Presentation:

1. "A Compact Model for Circuit Simulation of High Voltage Lateral & Vertical DMOS Transistors", ROBUSPIC Power Device Workshop at 18th International Symposium on Power Semiconductor Devices and ICs (ISPSD), Napoli, Italy, June 2006.

2. "The HV-EKV MOSFET Model", Compact Model Council (CMC) meeting, Boston, USA, May 2006.