Analysis and Modeling of Jitter and Frequency Tolerance in Gated Oscillator Based CDRs

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***Abstract*—This paper presents an approach to analyzing and modeling of gated-oscillator (GO) –based CDRs and predicting their performance aspects such as jitter tolerance (JTOL) and frequency tolerance (FTOL). It is shown that high JTOL of this topology in addition to their acceptable FTOL and flexible topology, have made them very suitable for short-haul multi-rate applications.**

I. INTRODUCTION

Gated-oscillator (GO) based clock and data recovery (CDR) circuits have been used widely in burst-mode applications mainly due to their fast locking time [1]. In addition to their fast locking time, GO CDRs benefit from a simple and flexible topology as well as a high jitter tolerance. These properties have made this topology very suitable for multi-channel, multi-rate CDRs for short-haul applications [2], [3].

In this article, after a brief review on GO CDR topology and its capability in implementing multi-rate data recovery systems, the main performance aspects of this topology such as jitter tolerance (JTOL) and frequency tolerance (FTOL) will be studied.

II. GO CDR

A. Topology

Figure 1 shows the topology of a GO CDR [1]. In this topology, by each transition on the received data a retiming signal (EDET) will be produced which forces the oscillator to restart its oscillation based on the timing determined by this signal. Therefore, as predicted in the timing diagram (Figure 1) synchronization of clock and data will take place at the first data transition. This topology also shows a wideband jitter transfer characteristic and any jitter on the received data will be transferred to the output without attenuation.

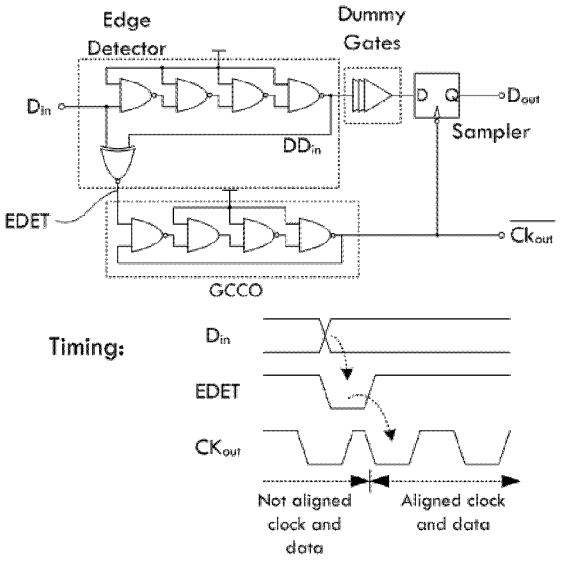


Figure 1. GO CDR topology and its operation timing diagram

As long as the pulse-width of EDET is wider than $T_{osc}/2$ (T_{osc} is the oscillation period), it can be ensured that this signal will propagate through the GO and retiming will take place effectively.

B. Multi-Rate Data Recovery

The simple and flexible topology of GO CDRs has made them very suitable for implementing multi-rate data recovery systems. As predicted in Figure 1, in conventional GO CDRs the retiming signal is applied to the first delay stage of the GO in each data transition. Therefore, the GO with oscillation period of T_{osc} will be synchronized to a data stream with time interval $T_{data} = T_{osc}$. In this case, any small difference between GO oscillation frequency ($f_{osc} = 1/T_{osc}$) and data rate ($R = 1/T_{data}$) results in incorrect sampling and hence increases the BER (bit error rate).

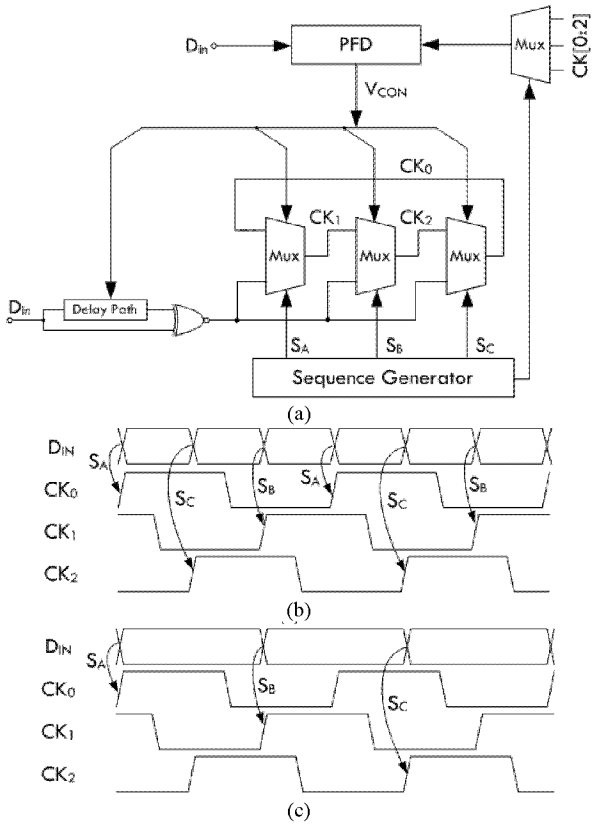


Figure 2. (a) Multi-rate GO based clock recovery topology, (b) $R/f_{osc}=1+1/3$, (c) $R/f_{osc}=1-1/3$

Figure 2a shows the modified GO topology in which the received data could be recovered correctly as while as:

$$R/f_{osc}=1\pm k/n \tag{1}$$

in which n is the number of delay stages in GO (here $n=3$), and k is an integer number ($0\le k<n$). In this topology, EDET signal could be applied to each delay stage in GO. Therefore, as long as (1) is satisfied, EDET can be applied in a predefined sequence to delay stages to keep the received data and clock synchronized. Figures 2b and 2c show two examples in which $R/f_{osc}=1+1/3$, and $R/f_{osc}=1-1/3$, respectively. In the first example, EDET signal will be applied to the delay cells by the sequence of S_A, S_C, and S_B, while for the next one the sequence has been changed to S_A, S_B, and S_C. By this approach, the time interval for applying the EDET to the GO could be adjusted by the step of T_{osc}/n.

III. Jitter Tolerance

Jitter tolerance (JTOL) is one of the most important test parameters for serial link transceivers especially in short-haul applications. This parameter is a measure of capability of a CDR in tolerating the input jitter. JTOL is usually tested by adding a sinusoidal jitter (SJ) at given frequency range to the data stream, which already includes channel jitter [4].

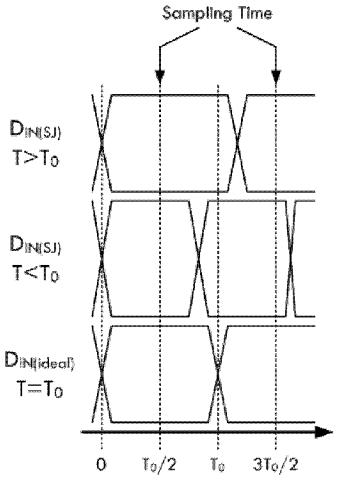


Figure 3. Sampling in presence of sinusoidal jitter (SJ) on data

The maximum jitter amplitude, which is a function of jitter frequency, at which the CDR still operates at a given BER (usually, $BER<10^{-12}$), is called jitter tolerance.

Simulation or analysis of JTOL for a non-linear system like GO CDR is a complicated task. In this section, some techniques for analysis and modeling this parameter in GO CDRs will be presented.

A. Pure Sinusoidal Input Jitter

In presence of input sinusoidal jitter on received data, the data rate will be changed as:

$$\omega(t)=\omega_0+\Delta\omega\cdot\cos\omega_j t \tag{2}$$

in which $\omega(t)$ indicates the instantaneous data frequency, ω_j is the frequency of sinusoidal jitter, ω_0 is the nominal data frequency ($\omega_0=2\pi\cdot R$), and

$$\Delta\omega=\pi\cdot UI_{pp}\cdot\omega_j \tag{3}$$

here, UI_{pp} is the peak to peak jitter amplitude [5]. Accordingly, the period of input data will be: $T_{data}=2\pi/\omega(t)$ (Figure 3). Therefore, it is possible to calculate the JTOL based on variations in data period. In presence of sinusoidal jitter, the period of data will change as:

$$T_{data}=2\pi/(\omega_0\pm\Delta\omega) \tag{4}$$

Therefore, to have a correct sampling (ignoring other types of jitter) the data edge must be within the time interval of: $T_0/2<T_{data}<3T_0/2$. Hence, concerning (5): $\Delta\omega/\omega_0<\min\{1/3,1\}$, or:

$$UI_{pp}=\omega_0/(3\pi\omega_j). \tag{5}$$

Ignoring the channel jitter, this expression indicates a very good approximation for JTOL in GO topology.

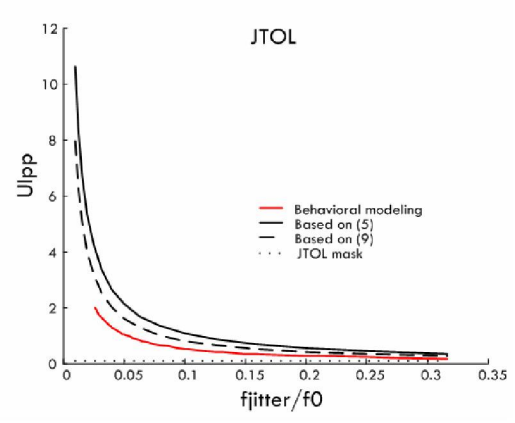


Figure 4. Modeled JTOL in presence of DJ and RJ on received data. Here, RJ=0.015UIrms (normal distribution) and DJ=0.18UIpp (uniform distribution) [4]

It is also possible to use the jitter transfer (JTRAN) function of a CDR to calculate approximately the JTOL. Based on this approach, to avoid incorrect sampling [6],

$$|\phi_{out} - \phi_{in}| \leq 0.5\,|\phi_{in}| \tag{6}$$

or approximately:

$$JTOL(s) \leq 0.5/[1 - JTRAN(s)] \tag{7}$$

In a GO CDR, the JTRAN can be approximated by a delay of $T_0/2 = T_{osc}/2$, or:

$$JTRAN(s) \approx e^{-T_0 s/2} \tag{8}$$

where $T_0 = 2\pi/\omega_0$ is the nominal data period. Therefore,

$$|JTOL(j\omega_j)| = 0.5/|1 - e^{-j\omega_j T_0/2}| = 0.125/\sin(\omega_j T_0/4) \tag{9}$$

This expression is acceptable just for small values or frequencies of jitter where the JTRAN can be approximated by (8).

The calculated JTOL based on (5) and (9) has been compared to the JTOL mask in Fig. 4. Due to the high bandwidth of a GO CDR, this topology shows a very good JTOL performance beyond the minimum requirements.

B. *Including the Channel Jitter*

To have a more practical estimation of JTOL, channel jitter must be included in calculations. Channel jitter generally includes both random (RJ) and deterministic jitter (DJ) with Gaussian and uniform distribution, respectively. In this condition,

$$BER = \max\{\int_{-\infty}^{T_0/2} P_d(\tau)\cdot d\tau,\ \int_{3T_0/2}^{+\infty} P_d(\tau)\cdot d\tau\} \tag{10}$$

in which $P_d(\cdot)$ indicates the probability of data transition. Since analytic evaluation of this expression is difficult, MATLAB simulations have been performed to evaluate the BER.

Figure 4 shows the result of MATLAB simulations. As can be seen, although the JTOL has decreased compared to (5) or (9), it is still well beyond the standard requirements.

IV. Frequency Tolerance

A. *Frequency Tolerance Estimation*

Unlike in conventional PLL-based CDRs, a frequency difference can exist between the GO CDR and the incoming data stream. In practical applications, the data rate is specified within $\pm$ 100ppm accuracy. The frequency tolerance (FTOL), defined as the maximum frequency difference at which the BER remains lower than a specified value (usually, $BER < 10^{-12}$). Ideally, when there is no jitter on data or clock, the frequency error must be smaller than

$$|f_{ck} - f_0| < f_0/2n \tag{10}$$

where $f_0 = \omega_0/2\pi$ is the nominal data frequency, $f_{ck} = 1/T_{ck}$ is oscillator frequency (sampling clock), and n indicates the number of consecutive identical digits (CID). Using 8B10B coding: $n \leq 5$, and hence based on (10): FTOL=10%. However, in practice FTOL is less than this value mainly because of jitter on sampling clock or input data (Figure 5).

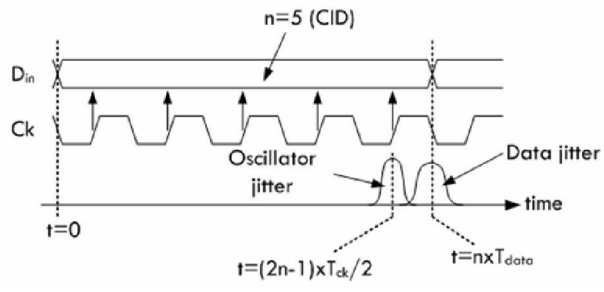


Figure 5. Sampling in presence of jitter on data and clock and also frequency error (here, n=5)

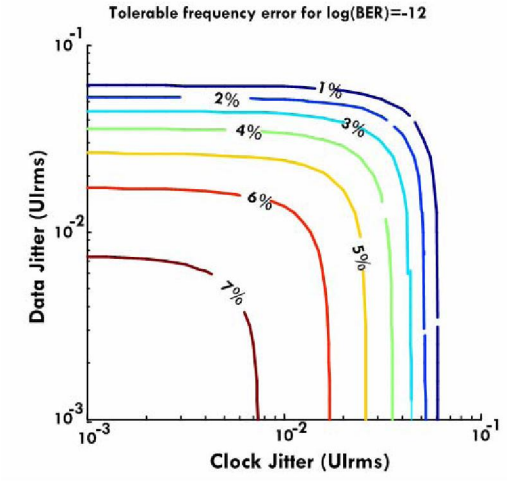
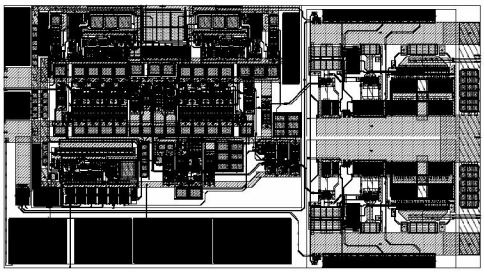
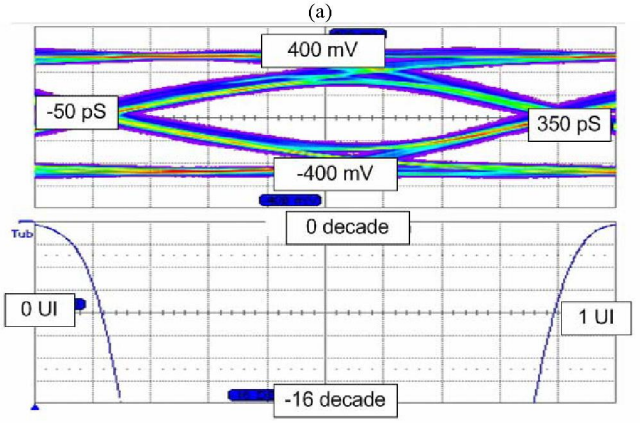


Figure 6. FTOL in presence of jitter on clock and data. Here, RJ=0.015UI_{rms} and DJ=0.35UI_{pp}.



(a)



(b)

Figure 7. (a) Mask layout of the proposed GO-based CDR used to implement an 8-channel clock and data recovery system implemented in a 0.18µm standard CMOS technology (including the two 50Ω output buffers), (b) measured eye diagram and bath tube curve showing a good eye opening

Regarding Fig. 5, the probability of incorrect sampling is:

$$BER = \int_{-\infty}^{+\infty} P_{ck}(\tau) \cdot \left(\int_{-\infty}^{\tau} P_d(\eta) \cdot d\eta \right) \cdot d\tau \qquad (11)$$

in which $P_{ck}(\cdot)$ indicates the probability of transition time of sampling clock. Figure 6 shows the achievable FTOL based on (11) in presence of random jitter on received data and recovered clock. As can be seen, an increase in clock or data jitter will lead to a degradation of FTOL.

B. Design for Acceptable FTOL

Based on this approach, to have an acceptable frequency tolerance, jitter generation in oscillator must be very small. The main source of jitter on sampling clock in this configuration is accumulated jitter during free running of gated oscillator that increases with the time interval of free running as [7]

$$\sigma_{ck} = \kappa\sqrt{\Delta T} \qquad (12)$$

in which σ_{ck} indicates the *rms* (root mean square) jitter value on clock accumulated in the time interval of ΔT, and κ is a proportionality factor which depends on topology and power consumption of delay stages and also process. Here, ΔT depends on the number of CIDs. The 8B10B encoding schemes used in short distance communications, reduces the CID to not more than 5 digits. Therefore, according to Figure 6 and using (12), to have a FTOL of about 7% to tolerate five consecutive identical bits, then $\kappa \leq 9.4\times10^{-8}$. This criterion can be used to determine the bias condition and hence the sizing of transistors in each delay cell. Frequency stability and timing jitter are the two most important specifications of the oscillator in a GO topology. Timing jitter of ring oscillators, or its frequency domain analogy phase noise, has been extensively studied in [7], [8].

V. Silicon Implementation

Exploiting the high JTOL of GO CDRs and their other specifications for short-haul application, an 8-channel clock and data recovery system based on this topology has been implemented in a standard 0.18µm CMOS technology (Figure 7a). To achieve an acceptable FTOL, bias current of transistors and so the device sizing has been chosen based on the methodology described in previous section [3]. Initial measurement results show a very stable operation and correct data retiming even in presence of frequency error (Figure 7b).

VI. Conclusion

In this article, some of the main performance aspects of GO CDRs such as JTOL and FTOL have been studied. Analyses approved by behavioral modeling show that GO CDRs show a very good JTOL makes them a good choice for short-haul applications. Meanwhile, to have an acceptable FTOL, the ring oscillator in this topology must be designed carefully to show very low jitter accumulation. A design methodology to achieve the desired jitter spec for this oscillator has been introduced, and successfully applied to the design of an 8-channel CDR circuit.

References

[1] M. Nakamura, N. Ishihara, and Y. Akazawa, "A 156 Mbps CMOS clock recovery circuit for burst-mode transmission," *IEEE Symp. On VLSI Circuits Digest of Technical Papers*, pp. 122-123, 1996.

[2] S. Kaeriyama, and M. Mizuno, "A 10Gb/s/ch 50mW 120×120µm^2 clock and data recovery circuit," *IEEE Int. Solid State Circuits Conf. (ISSCC)*, February 2003.

[3] A. Tajalli, P. Muller, M. Atarodi, and Y. Leblebici, "A multichannel 3.5mW/Gbps/channel gated oscillator based CDR in a 0.18µm digital CMOS technology," in Proc. of *European Solid-State Circuit Conf. (ESSCIRC)*, pp. 193-196, Grenoble, 2005.

[4] J. Kim, and D. –K. Jeong, "Multi-gigabit-rate clock and data recovery based in blind oversampling," *IEEE Comm. Mag.*, pp. 68-74, December 2003.

[5] L. M. De Vito, "A versatile clock recovery architecture and monolithic implementation," in *Monolithic Phase-Locked Loops and Clock Recovery Circuits, Theory and Design*, B. Razavi, Ed. New York: IEEE Press, 1996.

[6] B. Razavi, *Design of Integrated Circuits for Optical Communication Systems*, McGraw-Hill, 2003.

[7] J. A. McNeill, "Jitter in ring oscillators," *IEEE J. of Solid-State Circuits*, vol. 32, pp. 870-879, June 1997.

[8] A. Hajimiri, S. Limotyrakis, and T. H. Lee, "Jitter and phase noise in ring oscillators," *IEEE J. of Solid-State Circuits*, vol. 34, pp. 790-804, June 1999.2