COPPER/LOW-K TECHNOLOGICAL PLATFORM FOR THE FABRICATION OF HIGH QUALITY FACTOR ABOVE-IC PASSIVE DEVICES

THÈSE N^{O} 3831 (2007)

PRÉSENTÉE LE 22 JUIN 2007

PRÉSENTÉE À LA FACULTÉ DES SCIENCES ET TECHNIQUES DE L'INGÉNIEUR
Laboratoire d'électronique générale 2
SECTION DE GÉNIE ÉLECTRIQUE ET ÉLECTRONIQUE

ÉCOLE POLYTECHNIQUE FÉDÉRALE DE LAUSANNE

POUR L'OBTENTION DU GRADE DE DOCTEUR ÈS SCIENCES

PAR

Marcelo Bento PISANI

M.Sc. in Electrical Engineering, University of São Paulo, Brésil
et de nationalité brésilienne

acceptée sur proposition du jury:

Dr J.-M. Sallèse, président du jury
Prof. M. A. Ionescu, Dr C. Hibert, directeurs de thèse
Dr X. Gagnard, rapporteur
Prof. G. Piazza, rapporteur
Prof. R. Popovic, rapporteur

ÉCOLE POLYTECHNIQUE
FÉDÉRALE DE LAUSANNE

Lausanne, EPFL
2007

Copyright © 2007 by Marcelo B. Pisani

Ainda bem que você veio comigo,
Porque senão, o que seria da vida?
Nos dias frios...
(Vanessa da Mata)

Esta tese é dedicada à minha esposa Roberta Maria.

Table of Contents

Abstract ix

Version abrégée xi

List of abbreviations and acronyms xiii

List of symbols and units Xvii

Chapter 1. Introduction **1**

1.1. Organization of the thesis 2

1.2. MEMS and RF MEMS passive devices 3

1.3. Motivation and objectives 6

1.4. State-of-the-art on RF MEMS 8

1.5. Quality factor enhancement techniques 11

Chapter 2. Integrated inductors **18**

2.1. Inductors and inductance 18

2.2. Quality factor and self-resonant frequency 19

2.3. Inductance calculation 22

2.3.1. Inductance of a system of conductors 23

2.3.2. Elementary inductance calculations 24

2.3.3. Mutual inductance between current filaments 25

2.4. Spiral inductors 27

2.5. Other types of integrated inductors 30

2.6. Simplified physical model of integrated spiral inductors 31

Summary 36

Chapter 3. Copper / polyimide fabrication process **37**

3.1. Proposed process flow 37

3.2. Development of the process flow 39

3.3. Copper CMP process 41

3.4. Adhesion and diffusion issues 44

3.5. Fabrication results 45

3.5.1. Substrates used 45

3.5 2. Wafer insulation 46

3.5.3. Polyimide deposition 46

3.5.4. Polyimide hard mask deposition 49

3.5.5. Lithography 49
3.5.6. Hard mask definition 50
3.5.7. Polyimide etch 50
3.5.8. Hard mask removal 51
3.5.9. Seed layer deposition 51
3.5.10. Copper electroplating 52
3.5.11. Electroplating uniformity optimization 53
3.5.12. Copper CMP 56
3.5.13. Two metal level process 57
3.6. Process characterization test structures 59
3.6.1. Copper resistivity 59
3.6.2. Via contact resistance 60
3.7. Fabricated devices and RF performances 63
3.8. Other process developments based on this process module 69
3.9. Filter applications using high Q passive devices 70
Summary 75
Chapter 4. High Q inductors and RF packaging using quartz substrates 77
4.1. Fabrication process 78
4.2. Fabrication results 79
4.3. RF performance results 80
4.4. Functionalized quartz packaging 83
4.5. Wafer-level packaging process 84
4.6. SU-8 photolithography 85
4.7. Bonding process 87
4.8. Packaging characterization 88
4.9. Bond strength and adhesion 89
4.10. Wettability 89
Summary 90
Chapter 5. Simulation, characterization, modeling and optimization of spiral inductors 93
5.1. RF passive simulation tools 95
5.2. Measurement-based models 95
5.3. Simulation-based models 96

5.4. Analytical models 96
5.5. ADS Momentum simulations 98
5.6. HFSS simulation for a 2.5 nH inductor 100
5.7. Geometric parameter definitions 102
5.8. Inductor design space 104
5.9. Influence of the RF pads and ground rings on the RF performance of spiral inductors 105
5.10. Effect of metallization thickness and substrate resistivity 108
5.11. Physics based model for spiral inductors 109
5.11.1. Spiral losses 109
5.11.2. Current crowding effect 112
5.11.3. Coupled strip line model for spiral inductors 114
5.11.4. Comparison between the analytical model and EM simulations 123
5.11.5. Numeric optimization of inductor devices 127
Summary 129
Chapter 6. Conclusions and perspectives **131**
6.1. General conclusions 131
6.2. Perspectives for future research 133
Appendix A: Skin effect in conductors 135
A.1. Cylindrical wire 135
A.2. Infinitely long and wide rectangular stripline with finite thickness 139
A.3. Rectangular stripline 141
A.4. Fasthenry simulations and comparison between AC resistance calculation models 146
Bibliography **153**
Acknowledgments **169**
Vitae **171**

Abstract

Modern communication devices demand challenging specifications in terms of miniaturization, performance, power consumption and cost. Every new generation of radio frequency integrated circuits (RF-ICs) offer better functionality at reduced size, power consumption and cost per device and per integrated function. Passive devices (resistors, inductors, capacitors, antennas and transmission lines) represent an important part of the cost and size of RF circuits. These components have not evolved at the same level of the transistor devices, especially because their performance is strongly degenerated when they scale down in size. The low resistivity silicon used to build the transistors also imposes prohibitive levels of RF losses to these passive devices. Radio frequency microelectromechanical systems (RF MEMS) are enabling technologies capable to bring significant improvement in the electrical performances and expressive size and cost reduction of these functions, with unparallel introduction of new functionalities, unimaginable to attain when using bulky, externally connected discrete components.

High quality factor (*Q*) inductors are amongst ones of the most needed components in RF circuits and at the same time ones that are most affected by thin metallization and substrate related losses, demanding considerable research effort. This thesis presents a contribution toward the development of thick metal fabrication technologies, covering also the design, modeling and characterization of high quality factor and high self-resonant frequency (*SRF*) RF MEMS passive devices, with a special emphasis on spiral inductors. A new approach using damascene-like interconnect fabrication steps associated to low κ dielectrics (polyimide), highly-conductive thick copper electroplating, chemical mechanical polishing (CMP) and tailored substrate properties delivered quality factors in excess of 40 and self resonant frequencies in excess of 10 GHz, performances in the current state-of-the-art for integrated spiral inductors built on top of silicon wafers. Furthermore, the developed process steps are compatible with back-end processing used to fabricate modern IC interconnects and have a low thermal budget (< 250 ^{o}C), what makes it a good choice to build above-IC passives without degenerating the performance of passivated RF-CMOS circuits.

Deep reactive ion etching (DRIE) of quartz substrates was also studied for the fabrication of spiral inductors, offering excellent RF performances (*Q* exceeding 40 and SRF exceeding 7

GHz). A new doubly-functional quartz packaging concept for RF MEMS devices was developed. This technique process both sides of the packaging wafer: the top is used to embed high quality factor copper inductors while the bottom is thermo-mechanically bonded to another RF MEMS wafer, offering a semi-hermetic SU-8 epoxy-based seal. The bonding process was optimized for high yield, to be compatible with SF_6-plasma-released MEMS and to present low level of RF losses.

Band pass filters for the GSM (1.8 GHz) and WLAN (5.2 GHz) standards were fabricated and characterized by RF measurements and full wave electromagnetic simulations. Although further development is need in order to predict the frequency response accurately, insertion losses as low as 1.2 dB were demonstrated, levels that cannot be usually attained using on-chip passives.

Systematic analysis, RF measurements, electromagnetic simulations and equivalent circuit extraction were used to model the behavior of the fabricated devices and establish a methodology to deliver optimum performances for a given technological profile and specified performance targets (quality factor, inductance and frequency bandwidth). A simple yet accurate physics-based analytical model for spiral inductors was developed and proved to be accurate in terms of loss estimation for thick metal layers. This model is capable to accurately describe the frequency-dependent behavior of the device below its first resonant frequency over a large device design space. The model was validated by both measurements and full wave electromagnetic simulations and is well suited to perform numeric optimization of designs. The proposed models were also systematized in a Matlab® toolbox.

Keywords: radio frequency micro electromechanical systems (RF MEMS), high quality RF passive devices, above-IC integration, copper / low κ technology, RF passive modeling and characterization.

Version Abrégée

Les dispositifs de communication modernes ont des spécifications agressives en termes de miniaturisation, de performance, de consommation d'énergie et de coût. Chaque nouvelle génération des circuits intégrés radio (RF-ICs) offre de meilleures fonctionnalités à une petite taille, avec une faible consommation d'énergie et un coût réduit par fonction implémentée. Les dispositifs passifs (les résistances, les bobines, les condensateurs, les antennes et les lignes de transmission) représentent une partie importante du coût et de la taille des circuits RF. Ces composants n'ont pas évolués dans le même rythme des transisteurs, principalement car leur performance est fortement dégradée quand ils diminuent de taille. La faible résistivité du silicium utilisé dans la fabrication des transistors impose de forts nivaux de pertes RF aux dispositifs passifs. Les dispositifs micro électromécaniques pour la radio fréquence (RF MEMS) sont de nouvelles technologies qui ouvrent la voie pour avoir une amélioration significative de performance, avec l'introduction de nouvelles fonctionnalités inimaginables de s'obtenir par l'utilisation des composants discrets et encombrants.

Les bobines à fort facteur de qualité (*Q*) sont parmi les composants les plus attendus au même temps qu'elles sont une des plus affectées par les pertes associées aux couches métalliques minces et aux pertes RF du substrat. Cette thèse apporte des contributions vers le développement des procédés de fabrication de couches métalliques épaisses, aussi bien que pour le dessin, la modélisation et la caractérisation des dispositifs RF MEMS à fort facteur de qualité et à forte fréquence de résonance. Une attention spéciale est dédiée aux bobines en spirale.

Une approche originale utilisant la méthode damascène pour la fabrication d'interconnexions a été proposée. Le polissage chimique mécanique (CMP), l'utilisation des polymères à faible constant diélectrique (polyimide) associés aux couches épaisses en cuivre à faible résistivité et au contrôle des propriétés du substrat ont permis d'avoir des facteurs de qualité plus forts que 40 et des fréquences de résonance plus fortes que 10 GHz. Ces performances sont dans l'état de l'art pour les bobines fabriquées sur des wafers en silicium. Le procédé développé est compatible avec d'autres utilisés dans la fabrication "back-end" des interconnexions pour les CIs d'actualité, avec un petit budget thermique ($< 250\ ^{0}$C) ce qui fait de cette technique un

bon choix pour la fabrication “above-IC” des passifs sans une dégradation de la performance des circuits RF CMOS.

La gravure profonde (DRIE) des substrats en quartz a été utilisée comme technique de fabrication alternative pour les bobines en spirale, présentant d’excellents résultats pour la performance RF (Q plus fort que 40 et SRF plus forte que 7 GHz).

Un nouveau procédé d’encapsulation avec double fonction pour le wafer quartz appliqué pour les RF MEMS a été développé. Cette technique s’utilise des deux cotés du wafer : le dessus pour la fabrication de bobines et le dessous pour l’encapsulation au nivaux du wafer pour des plaquettes RF MEMS avec une protection semi hermétique basée sur la résine époxy SU-8. Le procédé de soudage a été optimisé pour avoir un rendement élevé, pour être compatible avec des dispositifs libérés par la gravure sèche basée sur le SF_6 et pour présenter des faibles pertes en RF.

Des filtres passe bande GSM (1.8 GHz) et WLAN (5.2 GHz) ont été fabriqués et caractérisés par des mesures RF et des simulations électromagnétiques. Même si une maîtrise de la réponse en fréquence est encore envisageable, des pertes d’insertion aussi faibles que 1.2 dB on été démontrées, des valeurs particuliermment difficiles à obtenir pour des filtres conçus à partir des composants passifs sur silicium.

L’analyse systématique, des mesures RF et des simulations électromagnétiques et par circuit électrique équivalents ont été utilisés pour modéliser le comportement des composants fabriqués et pour établir une méthodologie afin avoir la performance désiré en fonction des paramètres de dessin (le facteur de qualité, l’inductance et la bande de fréquence de travail). Un modèle physique simple et précis pour les bobines en spirale a été développé et validé par des mesures RF et par des simulations électromagnétiques. Les modèles proposés ont été systématisés dans une librairie de calcul pour Matlab®.

Mots-clés: systèmes microélectromécaniques pour la radio fréquence (RF MEMS), composants passifs à fort facteur de qualité, intégration “above-IC”, technologie cuivre / diélectriques à faible constante diélectrique, modélisation et caractérisation de composants RF passifs.

List of abbreviations and acronyms

1-D	one-dimensional
2-D	bi-dimensional
3-D	tri-dimensional
AC	alternate current
ADS	advanced design system (simulation program from Agilent)
Amicom	European Research Project IST-2003-507352: "European Network of Excellence on RF MEMS and RF Microsystems"
ASCII	American Standard Code for Information Interchange
ASITIC	analysis and simulation of inductors and transformers for integrated circuits
BCB	benzocyclobutene (low κ polymer)
BiCMOS	bipolar / complementary metal oxide semiconductor technology
BioMEMS	biological microelectromechanical systems
Bluetooth	short-range, low-data rate, low-cost, wireless personal area network communication standard (IEEE 802.15.1 standard, operates in the 2.4 GHz ISM frequency band)
BTA	benzotriazole ($C_6H_5N_3$)
CAD	computer aided design
CMI	Center of Micro and Nanotechnology (École Polytechnique Fédérale de Lausanne)
CMOS	complementary metal-oxide-semiconductor technology
CMP	chemical-mechanical polishing
CPS	coupled parallel striplines
CPW	coplanar waveguide
DC	direct current
DECT	digital enhanced (formerly European) cordless telecommunications (1880 – 1900 MHz in Europe, 1920 – 1930 MHz in the USA)
DMTL	distributed MEMS transmission line
DOE	design of experiments
DRIE	deep reactive ion etching
EM	electromagnetic

EPFL	École Polytechnique Fédérale de Lausanne (also Swiss Federal Institute of Technology Lausanne)
EU	European Union
FIB	focused ion beam
GaAs	gallium arsenide
GND	ground
GPIB	general propose interface bus
GPRS	general packet radio service (GSM data transfer and internet access service)
GPS	global positioning system (L1 frequency = 1575.42 MHz, L2 frequency = 1227.60 MHz)
GSG	ground, signal, ground (RF port configuration)
GSM	global system for mobile communications (0.8, 0.9 and 1.8 GHz)
HFSS	high frequency structure simulator (electromagnetic simulation tool from Ansoft Corporation)
HMDS	hexamethyldisilazane (photoresist adhesion promoter)
HR	high resistivity
HR-Si	high resistivity silicon (8 kΩ cm in this work)
IC	integrated circuit
ICP	inductively coupled plasma
IEEE	Institute of Electrical and Electronics Engineers
IMT	National Institute for Research and Development in Microtechnologies (Bucharest, Romania)
IPA	inductance per unit area [H/m^2]
IPA	isopropyl alcohol
ISM	Industrial, Scientific and Medical (various unlicensed RF frequencies, mainly in the 2400 – 2480 MHz range and its harmonics)
ISS	impedance standard substrate
IST	Information Society Technologies (EU research funded projects)
LC	inductance / capacitance
LIGA	Roentgen Litographie Galvanik Abformung (X-ray lithography, electrodeposition and molding)
LNA	low noise amplifier
LR	low resistivity (0.3 Ω cm in this work)
LTCC	low temperature co-fired ceramic

Matlab®	matrix laboratory (trademark of Mathworks Inc.)
MCM-D	multichip module deposition
MCLIN	microstrip coupled lines (ADS Libra)
MEMS	microelectromechanical systems
MIC	microwave integrated circuit
MIM	metal, insulator, metal
Mimosa	European Research project IST-2002-507045: "Microsystems platform for Mobile Services and Applications"
MLIN	microstrip line (ADS Libra)
MMIC	monolithic microwave integrated circuit
MOEMS	microoptoelectromechanical systems
OPS	oxidized porous silicon
PA	power amplifier
PC	personal computer
PECVD	plasma enhanced chemical vapor deposition
PEEC	partial element equivalent circuit
PGMEA	propylene glycol monomethyl ether acetate (SU-8 developer)
PGS	patterned ground shield
PS	porous silicon
PVC	polyvinyl chloride (also polychloroethene)
PVD	physical vapor deposition
RAM	random access memory
RCL	resistance, capacitance and inductance
RCLK	resistance, capacitance, inductance and mutual inductance
RF	radio frequency (GHz-range in this work)
RF MEMS	radio frequency microelectromechanical system
RIE	reactive ion etching
RLGC	resistance, inductance, conductance and capacitance
Si	silicon
SI	Système International (International System of Units)
SOI	silicon on insulator
SOLT	short, open, load and through
SPIE	Society of Photo-Optical Instrumentation Engineers

SPICE	simulation program with integrated circuit emphasis (University of California Berkeley, USA)
sq	square (sheet resistance measurement)
SU-8	brand name of an epoxy-based negative resist
TEM	transversal electromagnetic
TMN	tuning matching network
UMTS	universal mobile telecommunications system (2.2 GHz)
UV	ultraviolet light
UWB	ultra-wideband (bandwidth > 500 MHz or 20% of the center frequency)
VLSI	very-large scale of integration
VNA	vector network analyzer
VTTDL	variable true-time delay line
Wide-RF	European Research Project IST-2001-33286: "Innovative MEMS devices for Wideband reconfigurable RF Microsystems"
WLAN	wireless local area network (2.4 and 5.2 GHz)
WLP	wafer-level packaging

List of symbols and units

A	area [m^2]
A	arbitrary constant
ABCD	ABCD parameter matrix [1, Ω; S, 1]
A_{SPI}	spiral area [m^2]
B	magnetic flux density [T]
B	arbitrary constant
BP	back pressure [Pa or psi]
BW	frequency bandwidth [Hz]
c_n	current sheet inductance calculation coefficients [non dimensional]
C	capacitance [F]
C^*	complex (lossy) capacitance [F]
C'	capacitance per unit length [F/m]
C''	capacitance per unit area [F/m^2]
C_{INS}	insulator capacitance [F]
C_{INS}''	insulator capacitance per unit area [F/m^2]
C_P	parallel capacitance [F]
C_S	spiral capacitance [F]
C_{SUB}	substrate capacitance [F]
C_{SUB}''	substrate capacitance per unit area [F/m^2]
d	center to center distance between parallel conductors [m]
D	diameter [m]
D_{CENTER}	track center-to-center diameter of a spiral [m]
D_{IN}	internal diameter [m]
D_{OUT}	external diameter [m]
E	electric field [V/m = N/C]
E_0	electric field at the surface of a conductor [V/m]
e	natural logarithm basis ($e \cong 2.718\ 281\ 828\ 459\ 045\ 5...$)
f	frequency [Hz]
f_{CRIT}	critical frequency [Hz]
f_{QMAX}	frequency where Q_{MAX} occurs [Hz]
f_{RES}	resonance frequency, the same as SRF [Hz]

FMI	factor of merit of an inductor [Hz/m^2]
G	conductance [S]
G''	conductance per unit area [S/m^2]
GMD	geometrical mean distance [m]
GMD_{PAR}	geometrical mean distance of parallel rectangular strips [m]
G_{SUB}''	substrate conductance per unit area [S/m^2]
H	magnetic field intensity [A/m]
$H_0^{(1)}$	0-th order, 1st kind Henkel function: $H_\nu^{(1)} = J_\nu(z) + jN_\nu(z)$
HF	high frequency regime (characteristic dimensions r_0, w, $t >> \delta$)
HF	hydrofluoric acid
HS	head speed [rpm]
h	conductor thickness (in Fasthenry simulations) [m]
I	electrical current [A]
IL	insertion loss [dB]
Im	imaginary part of a complex number
IPA	inductance per unit area [H/m^2]
J	current density [A/m^2]
J_0	0-th order Bessel function: $J_\nu(z) = \sum_{m=0}^{\infty} \frac{(-1)^m (z/2)^{\nu+2m}}{m!\Gamma(\nu+m+1)}$
J_S	linear current density [A/m]
j	imaginary unit ($j = \sqrt{-1}$)
k	alternative typographic form for the dielectric constant κ [non dimensional]
k	magnetic coupling coefficient [non dimensional]
k	argument of the complete elliptic integral *K* [non dimensional]
k'	complementary argument of the complete elliptic integral *K* [non dimensional]
K(k)	first kind complete elliptic integral, $K(k) = \int_0^{\pi/2} \frac{d\varphi}{\sqrt{1-k^2 \sin^2 \varphi}}$
K'(k)	complementary first kind complete elliptic integral, *K'(k)* = *K(k')*, with $k' = \sqrt{1-k^2}$
L	inductance [H]
L^*	complex (lossy) inductance [H]
L'	inductance per unit length [H/m]
LF	low frequency regime (characteristic dimensions r_0, w, $t << \delta$)

L_{SERIES}	series inductance [H]
L_{SHUNT}	shunt inductance [H]
L_{RECT}	inductance of a rectangular stripline [H]
L_{SPI}	inductance of a spiral [H]
l	length [m]
l_{CIRC}	length of a circular spiral [m]
l_G	length of spiral gap [m]
l_{POLY}	length of a polygonal spiral [m]
ln	natural logarithm
log10	base 10 logarithm
l_{SQ}	length of a square spiral [m]
m	segment length [m]
M	mutual inductance [H]
M_{INC}	mutual inductance between 2 inclined segments [H]
M_{PAR}	mutual inductance between 2 parallel segments [H]
N	integer number
$N_\nu(z)$	Neumann function of order ν: $N_\nu(z) = \frac{\cos\nu\pi \, J_\nu(z) - J_{-\nu}(z)}{\sin\nu\pi}$
n	integer number
n	number of turns of a spiral inductor
nwinc	number of meshing cells along the width (Fasthenry)
nhinc	number of meshing cells along the thickness (Fasthenry)
N_S	number of sides per turn (polygonal spiral)
P	power [W] or [dBm]
PS	plate speed [rpm]
p	normalized frequency: $p = \sqrt{2f\sigma\mu wt} = \frac{1}{\delta}\sqrt{\frac{2wt}{\pi}}$ [non dimensional]
Q	quality factor [non dimensional]
Q_{EFF}	effective quality factor [non dimensional]
Q_{MAX}	maximum quality factor (peak value) [non dimensional]
Q_P	parallel quality factor (capacitor) [non dimensional]
Q_S	series quality factor (inductor) [non dimensional]
R	resistance [Ω]
R	spiral radius [m]

R_{CROWD}	AC resistance due to current crowding [Ω]
Re	real part of a complex number
R_F	frequency-dependent surface resistance $R_F = \sqrt{\pi f \rho \mu}$ = ρ/δ [Ω]
RR	removal rate [μm/min]
R_S	series resistance [Ω]
R_{SH}	sheet resistance [Ω / sq = Ω]
R_{SUB}	substrate resistance [Ω]
r	cylindrical radial coordinate [m]
r	rectangular conductor aspect ratio (= t / w or w / t) [non dimensional]
r_0	cylindrical wire radius [m]
rw	meshing increasing ratio along the width (non dimensional, Fasthenry)
rh	meshing increasing ratio along the thickness (non dimensional, Fasthenry)
S	S-parameter matrix [non dimensional]
s	track spacing [m]
SRF	self-resonant frequency, the same as f_{RES} [Hz]
S	scattering parameter matrix [non dimensional]
S_{11}	S_{11}-parameter data (reflection at port 1) [non dimensional]
S_{21}	S_{21}-parameter data (forward port 1-2 transmission or insertion loss) [non dimensional]
S_{12}	S_{12}-parameter data (reverse port 1-2 transmission) [non dimensional]
S_{22}	S_{22}-parameter data (reflection at port 2) [non dimensional]
T	Bessel equation parameter: $T = \sqrt{-j\omega\mu\sigma} = (1-j)/\delta$ [m^{-1}]
TCC	temperature coefficient of capacitance [K^{-1}] or [^{o}C^{-1}]
TCR	temperature coefficient of resistance [K^{-1}] or [^{o}C^{-1}]
t	thickness [m]
$\tan\delta$	loss tangent (also known as loss factor) [non dimensional]
t_{INS}	insulator thickness [m]
$t_{INS,M1}$	thickness of the insulator between the underpass and the first level of metal [m]
t_N	thickness normalized by the skin depth: $t_N = t / \delta$ [non dimensional]
t_{SUB}	substrate thickness [m]
w	track width [m]
w_N	track width normalized by the skin depth: $w_N = w / \delta$ [non dimensional]

WP	working pressure [Pa or psi]
X	reactance [Ω]
Y	conductance matrix (moduli in [S])
y_{xx}	conductance matrix coefficient (moduli in [S])
Z	complex impedance (moduli in [Ω])
Z'	impedance per unit length [Ω/m]
Z'_i	internal impedance per unit length of a conductor [Ω/m]
Z_0	real characteristic impedance [Ω]
Z_0^*	complex characteristic impedance (moduli in [Ω])
α	attenuation coefficient [Np/m] or [dB/m]
α	angle between segments [rad]
β	phase constant of a transmission line: [rad/m] or [^{0}/m]
Γ	reflection coefficient (also S_{11} or S_{22}) [non dimensional]
Γ(x)	gamma function: $\Gamma(x) = \int_0^\infty t^{x-1} e^{-t} dt$
γ	complex propagation constant = α + j β [m^{-1}]
δ	skin depth [m] = $\sqrt{\rho / \pi f \mu} = \sqrt{2 / \omega \mu \sigma}$
δ	parallel segment overlap length (for mutual inductance calculation) [m]
ε	dielectric constant [F/m]
ε^*	complex (lossy) dielectric constant = $\varepsilon - j \tan \delta$
ε_0	vacuum dielectric constant = $1/\mu_0 c_0^2 \cong 8.854\,188 \cdot 10^{-12}$ F/m
ε_{INS}	insulator dielectric constant [F/m]
ε_R	relative dielectric constant ($\varepsilon / \varepsilon_0$, non dimensional)
$\varepsilon_{R,EFF}$	effective relative dielectric constant (non dimensional)
ε_{SUB}	substrate dielectric constant [F/m]
κ	dielectric constant (alternative name to ε_R)
λ	wavelength = c / f [m]
λ_0	free space wavelength = c_0 / f [m]
μ_0	vacuum magnetic permeability = $4 \pi 10^{-7}$ H/m
μ	magnetic permeability [H/m]

μ_R	relative magnetic permeability: $\mu_R = \mu / \mu_0$ [non dimensional]
ξ	spiral geometric filling factor [non dimensional]
π	constant ≅ 3.141 592 653 589 793 1…
Σ	summation
σ	electrical conductivity [S/m]
σ_{SUB}	substrate conductance conductivity [S/m]
Φ	magnetic flux [Wb]
Φ_{ij}	magnetic flux induced in the circuit loop *j* by the current in loop *i* [Wb]
ω	angular frequency = $2 \cdot \pi \cdot f$ [rad/s]

International System of units (SI)

A	ampere – electrical current [base unit = C/s]
C	coulomb – electric charge [A·s]
dB	decibel – amplitude or power ratio defined as $20 \cdot log_{10}(U/U_{REF})$ for voltages or $10 \cdot log_{10}(P/P_{REF})$ for power
dBm	power in dB referenced to 1 mW: $P(\text{dBm}) = 10 \cdot log_{10}(P / 1\ \text{mW})$
F	farad – capacitance [$C/V = m^{-2} \cdot kg^{-1} \cdot s^4 \cdot A^2$]
GB	gigabyte – information capacity equal to $1.0 \cdot 10^6$ bytes
H	henry – inductance [$Wb/A = m^2 \cdot kg \cdot s^{-2} \cdot A^{-2}$]
Hz	hertz – frequency [s^{-1}]
kg	kilogram – mass [base unit]
m	meter – length [base unit]
mol	mol – quantity of matter [$6.022\ 141\ 5 \cdot 10^{23}$ particles]
Np	neper – amplitude ratio: 1 Np = e = 20 dB / $ln(10) \cong 8.6859$ dB
Pa	pascal – pressure [$N/m^2 = m^{-1} \cdot kg \cdot s^{-2}$]
rad	radian – angle [non dimensional]
s	second – time [base unit]
S	siemens – electrical conductivity [$A/V = \Omega^{-1} = m^{-2} \cdot kg^{-1} \cdot s^3 \cdot A^2$]
T	tesla – magnetic flux density [$Wb/m^2 = V \cdot s/m^2 = kg \cdot s^{-2} \cdot A^{-1}$]
V	volt – electric potential [$J/C = m^2 \cdot kg \cdot s^{-3} \cdot A^{-1}$]
W	watt – power [$J/s = m^2 \cdot kg \cdot s^{-3}$]

Wb	weber – magnetic induction flux [$V \cdot s = m^2 \cdot kg \cdot s^{-2} \cdot A^{-1}$]
Ω	ohm – electrical resistance [$V/A = m^2 \cdot kg \cdot s^{-3} \cdot A^{-2}$]

Non-SI units used in this work

in	length in inches: 1 in = 2.54 cm
mbar	pressure in mbar: 1 mbar = 100 Pa
psi	pressure in pounds per square inch: 1 psi = 1 lbf / in^2 = 6 894.757 29 Pa
rpm	angular velocity in revolutions per minute: 1 rpm = 2 π rad / min
sccm	flow rate in standard cubic centimeters per minute (measured at 1 atm and 0 ^{0}C): 1 sccm = 1 atm · cm^3/min @ 0 ^{o}C = $7.4358 \cdot 10^{-7}$ mol/s = $4.4780 \cdot 10^{17}$ particles / s
Torr	pressure in Torr: 1 Torr = 133.322 Pa

Physical constants

c_0	vacuum speed of light (exactly $2.99792458 \cdot 10^8$ m/s ≅ $3.0 \cdot 10^8$ m/s)
ε_0	vacuum dielectric constant = $1 / (\mu_0 c_0) = 8.85418781762 \cdot 10^{-12}$ F/m
μ_0	vacuum magnetic permeability (exactly $4 \cdot \pi \cdot 10^{-7}$ H/m ≅ $1.2566 \cdot 10^{-6}$ H/m)
η_0	vacuum characteristic impedance = $\sqrt{\mu_0 / \varepsilon_0}$ = 376.73... Ω ≅ 120 π Ω
d_{CU}	copper density = 8.920 g/cm^3
ρ_{CU}	copper resistivity (bulk value = 1.72 μΩ cm, thin film value = 2.00 μΩ cm)
ρ_{AG}	silver resistivity (bulk value = 1.62 μΩ cm)
ρ_{AU}	gold resistivity (bulk value = 2.44 μΩ cm)
ρ_{AL}	aluminum resistivity (bulk value = 2.62 μΩ cm, thin film value = 3.30 μΩ cm)
$\varepsilon_{R,OX}$	relative dielectric constant of silicon dioxide (SiO_2) = 3.9
$\varepsilon_{R,PI}$	relative dielectric constant of polyimide = 2.9
$\varepsilon_{R,SI}$	relative dielectric constant of silicon (Si) = 11.9

Chapter 1

Introduction

Microelectronic devices are miniaturized electronic components generally built in a single piece of a monocrystaline semiconductor material like silicon (Si) or gallium arsenide (GaAs). The possibility to fabricate very small components enables the integration of complex circuit functionalities in a small piece of semiconductor material at minimum cost and energy consumption per device.

An intense increase in both the degree of miniaturization and in the performance of the electronic circuits has been observed since the establishment of the microelectronic fabrication industry. A consistent increase in the number of transistors per integrated circuit has been observed every year. For each new generation of integrated circuits new and more complex functions can be integrated in a single semiconductor chip. A trend known as Moore's law, observed in 1965 by one of the co-founders of Intel Corporation and still valid today, states that the number of transistors in complex integrated circuits approximately doubles every 2 years [Moore 1965, Moore 1995].

Passive devices (resistors, capacitors, inductors and transmission lines) have been traditionally built separately from the main integrated circuit transistor functions and attached to them using special interconnection techniques. These bulky components represent a large amount of the cost of the RF circuits and the external fabrication and interconnection of these devices is a factor that adds significant volume, parasitics, weight and cost to the RF products.

Co-integration of passive devices in the same silicon substrate is desirable in order to reduce the interconnect parasitics, reduce the size and cost of the units and increase the operating frequencies of the RF circuits. The challenges following this tendency are associated to the

limited performance of these devices when built in miniaturized configurations and in proximity with high conductivity substrates. This framework introduces the need of using new materials and fabrication technologies in order to increase the electrical performance of these devices, while still keeping the process low-cost and compatible with the standard technologies used to fabricate RF CMOS circuits.

Moreover, the design of passive devices to attain a certain specification must trade-off many variables that determine the size and the performance of these devices. Careful electromagnetic optimization of the device geometry should be carried out in order to ensure that one can obtain the maximum performance that a given fabrication technology can deliver.

The aim of this thesis is to present a contribution to the study and development in the fabrication of high quality factor integrated passive devices. The development of a new fabrication technology based on the definition of thick copper layers embedded in low κ polyimide is proposed. A systematic study on the design and characterization of the fabricated devices was carried out, with special emphasis on integrated inductors used as a demonstration vehicle to probe the performance of the developed fabrication techniques.

1.1. Organization of the thesis

This first chapter of the thesis presents a general introduction to the field of MEMS and RF MEMS and a brief description of the advantages and issues related to RF MEMS fabrication technologies. The motivations and objectives of this PhD project as well as a picture of the current state-of-the-art in the field are also presented.

The chapter 2 presents the basic underlining concepts, models and equations defining passive integrated inductors, with special attention to the definition of the inductance calculation formulae and merit factors used in this research.

In the chapter 3, the fabrication technology developed in the frame of this thesis is presented in detail, describing the fabrication steps, the main issues involving the technological choices made and how they were addressed. This chapter will finally present the fabrication results obtained using the developed technology platform. An application of the high Q passive

devices developed in the frame of this thesis for the synthesis of high frequency bandpass filters is also presented.

Chapter 4 presents an alternative fabrication process based on the direct deep reactive ion-etching of insulating substrates filled with thick electroplated copper lines. An innovative double-functionalized RF packaging solution is also proposed. This solution can be used for both packaging and fabrication of high Q inductors by exploiting both sides of the capping wafer.

Chapter 5 presents the simulation tools and RF characterization methods used to predict and measure the performance of the fabricated devices. It presents and discusses the software tools used and especially developed to accomplish task. Finally, an accurate, physics-based model for spiral inductors is proposed and validated.

Finally, the chapter 6 draws up the general conclusions of this research project and point some research directions to be followed in order to continue the advancement in the field.

1.2. MEMS and RF MEMS passive devices

Micro-electro mechanical systems (MEMS) are miniaturized devices having functionality related to both the mechanical and electrical domains, presenting in general both functionalities in a single device. The term emerged to describe a class of devices that can be fabricated using adapted technologies inherited mainly from integrated circuit fabrication techniques [Madou 1997].

MEMS devices can effectively incorporate integrated circuit functions and interface these circuits with a variety of domains like fluidics and biology (microchannels, micropumps, defining the so-called Bio-MEMS field), optics (micromirrors and optical switches, defining the so called optical-MEMS or MOEMS field) and mechanical sensors and actuators (electrostatic, thermally or magnetically driven sensors and actuators).

Radio frequency micro-electro mechanical systems (RF MEMS) is the term used to describe the emerging technology of fabricating and using MEMS devices that have functionality in radio communication circuits operating in the GHz frequency range [de los Santos 1999, de

los Santos 2002, Yao 2000, Nguyen 2002, Varadan 2003]. MEMS and microelectronic fabrication techniques are enabling technologies to fabricate high quality factor passive devices (capacitors and inductors), low-loss transmission lines, RF switches, microrelays and a number of application circuits obtained by combining these basic devices in functional blocks. Emerging RF applications demand a number of passive circuit functions, including high performance switches with low insertion losses and high isolation [Rebeiz 2001], large tuning range variable capacitors [Rijks 2004], tunable inductors [Fukushige 2003], tunable filters [Brank 2001], suspended transmission lines [Pham 2001], tuning matching networks [Unlu 2006], reconfigurable antennas [Erdil 2007], variable true-time delay lines (VTTDLs) [Hung 2004, Perruisseau-Carrier 2006], antenna phased arrays [Sagkol 2002], and electromechanical filters and resonators [Nguyen 1998, Dubois 2005, Piazza 2006] as basic passive network building blocks.

Figure 1.1 shows a MEMS market forecast shared between the various families of MEMS devices available to date. The predominant products are data read / write heads, followed by micro displays, inkjet printer heads, pressure sensors and RF MEMS occupying the 5th position. Figure 1.2 shows a forecast with the sharing of the RF MEMS market in different sub-areas. This projection predicts a U$ 1.2 billion market for 2009 by having mobile telephony and consumer electronics as the major volume drivers, followed by other wireless applications. RF test and WLAN networks represent a significant percentage of this market, followed by other low volume, higher technology drivers like satellites and military applications (fig. 1.3).

These market projected figures are, of course, estimations based on the behavior and expectations of the market, and are dependent on a number of uncertain economical and technical issues that should be addressed.

From the technical point of view, the large-scale insertion of RF MEMS in mobile and consumer electronics is dependent on a number of key technological factors related to:

- How low-cost the technology would be, including the packaging issues and how this aspect impacts the cost and the performance of the devices. This topic should be addressed by searching for solutions that should be compatible with the current CMOS fabrication and packaging practices, using low bill of materials and simple and robust fabrication methods,

- The added value that RF MEMS can provide for the products in terms of new functionality, performance and energy saving,
- The reliability and long-term stability of the electrical and mechanical characteristics of these devices, especially the ones having movable mechanical parts and electrical contacts like variable capacitors and switches.

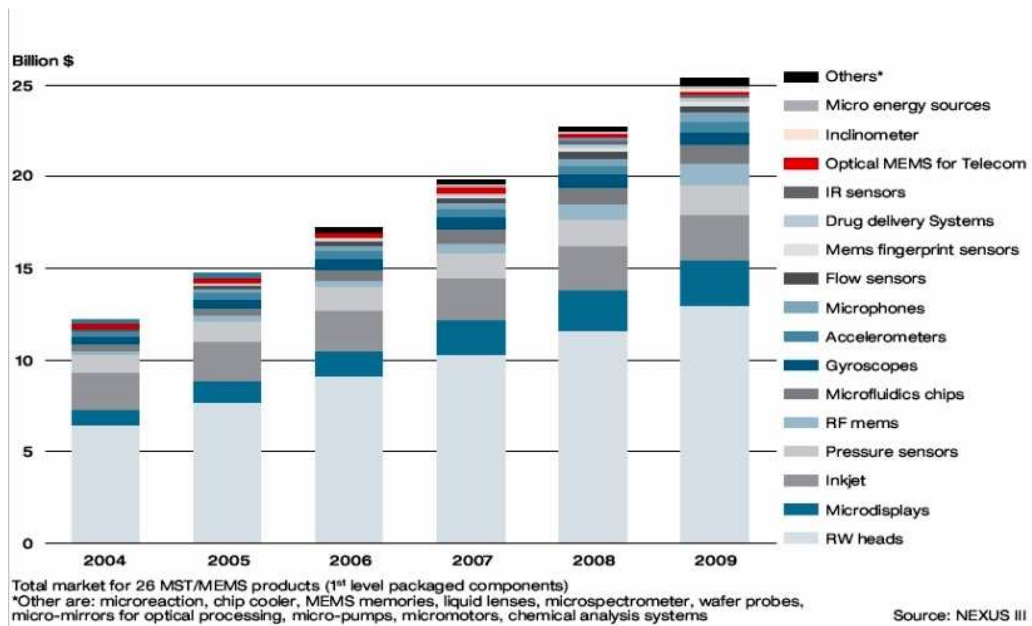


Fig. 1.1: MEMS market forecasts from 2004 to 2009 [Nexus].

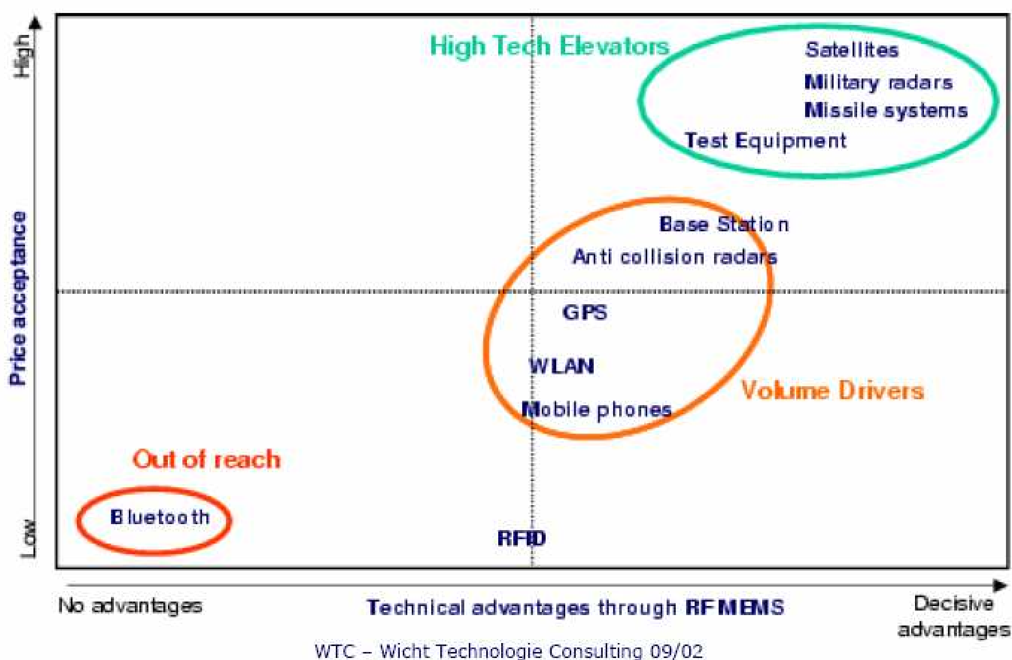


Fig. 1.2: RF MEMS technology drivers [WTC].

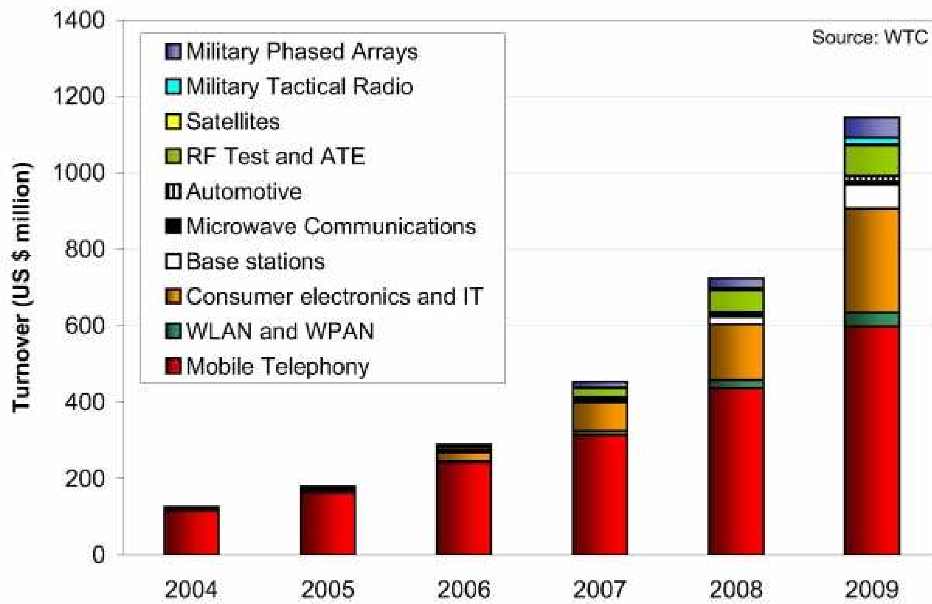


Fig. 1.3: Market forecasts for RF MEMS devices shared by different sub-applications [WTC].

1.3. Motivation and objectives

High Q passive devices, especially inductors, are desirable in order to reduce the phase noise in voltage controlled oscillators (VCOs), reduce the losses in filter and tuning matching networks (TMN) and reduce the power consumption in oscillator and power amplifier circuits (PA) [Malba 1998, Rebeiz 2003]. Table 1.1 shows how the main circuit figures of merit scale as function of the inductor quality factor (supposing that all the other parameters are kept constant).

Application	Parameters	Assumptions	Scaling with Q
Oscillators	Phase noise	LC-type resonator circuit	$1 / Q^2$
	Power consumption	For a fixed phase noise level	$1 / Q$
Amplifiers	Gain	Proportional to load impedance	Q
	Power consumption	Same gain with less transconductance for the transistor	$1 / Q$
Matching networks and filters	Insertion loss	Unloaded resonator Q sets the loss	$1 / Q$

Table 1.1: Scaling of RF circuit parameters as function of the inductor quality factor [Rebeiz 2003].

The use of MEMS devices in RF circuits is very appealing because at very high GHz frequency ranges semiconductor switches and transmission lines built on conventional silicon substrates become too lossy. Solid-state devices are also limited in terms of linearity and power handling capability, limitations that electromechanical devices are less subject to. On the other hand, there are off-chip high quality factor devices available today, but the co-integration of these devices with the IC functions is desirable in order to reduce the volume, costs and parasitics associated to the fact of having bulky components with long interconnecting lines going outside the RF circuitry core.

Additionally, the possibility of building high quality factor, tunable and switchable components will be key enabling factors for new emerging multi-GHz reconfigurable radio circuits and high performance / low power telecommunication modules by introducing new functionalities that the present day components cannot offer due to their high cost, size and impossibility of being fabricated in large numbers and co-integrated with transistors.

Passive devices have been largely studied and fabricated on GaAs and more recently on silicon-based RF technologies. RF performances on top of silicon substrates are poor in general, which poses severe limitations in the scalability and use of these technologies when co-integrated with CMOS technologies for the high GHz frequency ranges. The use of new technologies and materials associated to innovative and optimized RF designs are key points for what this thesis will propose contributions to continue the advancement in the RF silicon-based technologies.

The objective of this thesis is to contribute in the field of high quality factor RF MEMS by developing new CMOS-compatible fabrication technology platforms and by the systematic analysis on the performance limitation factors of these devices.

In order to explore all the potential of a given RF technology, numeric optimization, electromagnetic simulation and RF measurement-based models should be extensively exploited to give optimal designs in the sense that the best possible performance for a given technology profile can be delivered. This thesis make a contribution in this direction with the systematic use of modern RF simulation tools available to date, as well as applying and comparing the various models available in the literature and by extracting accurate equivalent circuit models based on S-parameter measurements.

The devices fabricated and studied in the frame of this thesis had also the objective of providing different RF MEMS related EU research projects with demonstrator prototypes. These research projects were: Wide-RF ("Innovative MEMS devices for Wideband reconfigurable RF Microsystems", project IST-2001-33286), Mimosa ("Microsystems platform for Mobile Services and Applications", project IST-2002-507045) and Amicom ("European Network of Excellence on RF MEMS and RF Microsystems", project IST-2003-507352).

1.4. State-of-the-art on RF MEMS

Integrated passive devices have been fabricated and modeled initially on top of GaAs substrates [Cauton 1968, Greenhouse 1974, Pettenpaul 1988]. The fabrication and study of spiral inductors on top of low resistivity silicon wafers has been performed essentially in the past two decades [Nguyen 1990], and started to gain more interest in the past decade [Nguyen 1998]. The first devices that appeared in this direction showed very poor RF performances, with peak quality factors that do not exceed the range of 3 – 5 and self resonance frequencies in the 1 – 3 GHz range, imposing severe limitations to the practical application of these devices [Nguyen 1990, Yue 1996].

The availability of Cu / low κ advanced interconnects in the state-of-the-art high speed CMOS processes provided an enabling way to deliver devices with significant increase in both peak quality factor (around 10) and self-resonance frequencies (around 5 GHz) [Burghartz 1996, Burghartz 1997].

In 1996, Burghartz et al. proposed to shunt layers of metal in a multilevel metallization BiCMOS process by putting traces of metal in parallel by using many vias interconnecting them. Inductors in the range of 1 to 5 nH with quality factors in the range of 5 to 20 were obtained by using this technique [Burghartz 1996b].

The obtained increase in the RF performance by using high-speed interconnects is related to the reduction in the parasitics and increase in the conductivity of the interconnects, the same driving force that is pushing the IC local interconnects for the multi-GHz frequency range, but these performances did not showed to be enough to respond the demand for high Q devices

with resonant frequencies into the 6 – 10 GHz range expected for the new emerging RF application standards (GSM, WLAN for example).

These issues have been addressed by introducing new fabrication technologies and materials and by removing the limitations imposed the lossy silicon substrate. In 1993, Chang et al. demonstrated for the first time a suspended 100 nH inductor by etching a cavity underneath the inductor and improving both gain and bandwidth of a CMOS RF amplifier [Chang 1993]. In 2000, López-Villegas et al. proposed to etch the silicon on the backside of the designed spiral inductors, demonstrating an increase in the quality factor from 3 to 30, shifting the frequency f_{QMAX} from 1.5 to 5 GHz.

In 1997, Young et al. fabricated copper solenoid inductors with conductors wrapped around a 500-µm-wide and 650-µm-high alumina core [Young 1997, Malba 1998b]. A 4.8-nH inductor with Q = 30 @ 1 GHz was demonstrated by this fabrication technique. Kim et al fabricated copper solenoid inductors with air-core instead of alumina, demonstrating inductors in the range of 1 to 20 nH with quality factors in the range of 7 to 60 [Kim 1998]. Chen et al. demonstrated in 2001 solenoid inductors made using thick SU-8 resist on top of CMOS circuits with Q_{MAX} = 20 @ 4.5 GHz and SRF > 10 GHz [Chen 2001].

In 1999, Yoon et al proposed to fabricate overhang inductor structures in order to reduce substrate related losses, placing the inductor 30 µm to 50 µm far away from the substrate [Yoon 1999]. A suspended inductor of 1.8-nH having a Q-factor of 50 at 7 GHz was demonstrated by using this technique. This same author proposed solenoid inductors fabricated on top of 10 Ω cm substrate. An inductor of 2.7 nH with a peak quality factor of 17 and self-resonant frequency of 2.4 GHz was demonstrated using this technique.

Another fabrication technique adopted in order to reduce substrate-related losses is to locally increase the resistivity of the silicon substrate underneath the inductor by providing a poor conductivity silicon material by modification of the substrate by proton ion bombardment or by the formation of porous silicon layer (PS). Hsu et al. demonstrated an increase on the peak quality factor from 8 to 18, with a shift in f_{QMAX} from 1.5 to 3.5 GHz by applying proton implantation treatment of the silicon underneath the inductors. A peak quality factor of 45 at 15 GHz with a resonant frequency of 22 GHz was demonstrated [Hsu 2002]. This process presents some issues related to the damage of the silicon by the high-energy particle

bombardment [Liao 2003]. Nam et al. demonstrated inductors fabricated on top of oxidized porous silicon (OPS): a 6.3-nH with peak Q-factor of 13.3 at 4.6 GHz and self-resonant frequency of 13.8 GHz was demonstrated [Nam 1997]. In 2003, Royet et al demonstrated Q_{MAX} = 45 @ 1 GHz and SRF of 5 GHz by using also porous silicon formation technique [Royet 2003]. In 2007, Contopanagos et al. demonstrated inductors fabricated on top of porous silicon layer using copper conductor with Q_{MAX} = 30 @ 3.5 GHz [Contopanagos 2007].

In 1999, Lee et al. as well as Kim et al. demonstrated the use of bondwires to fabricate solenoid-type inductor structures by closing large circuit loops [Lee 1999, Kim 1999]. Inductors between 2 to 6 nH with quality factors in the range of 30 to 60 were demonstrated using this fabrication technique. The problem with this approach is the difficulty to accurately control the form and size of the loops and so the final inductance value characteristics of the final device.

In 2002, Chomnawang et al. demonstrated high Q inductors using thick resist fabrication of solenoid-like inductors. A 1.8-nH inductor with Q = 40 at 10 GHz was demonstrated [Chomnawang 2002].

The use of LIGA processing enables the fabrication of thick metal structures suitable to build high Q passive devices [Bacher 1995]. In 2003, Park et al. demonstrated high current handling (> 3A) devices using nickel-iron magnetic material for the inductor core, but with very low-frequency and low quality factor (Q = 4.5 @ 50 kHz) [Park 2003]. In 2007, Lu et al. demonstrated Q_{MAX} between 60 and 90 @ 2.5 GHz and SRF between 17 and 20 GHz using very thick out-of-plane solenoid structures fabricated using LIGA process. This process uses 100 and 200 μm-thick vias [Lu 2007].

Active inductors are circuits made of a combination of transistors and other passive components to emulate the electrical behavior of passive inductors [Kaunisto 1995, Hara 1988, Hayashi 1996, Haslett 2001]. These circuits can present high Q and broadband frequency behavior at moderate to low on-wafer area consumption. The major drawback of these devices is their very poor performance in terms of phase noise and high power consumption [Craninckx 1995].

Variable inductors are highly needed to fabricate high-performance reconfigurable filters, and are probably the less developed RF MEMS device to date. The major issues associated in fabricating this kind of device is the difficulty to obtain in the same device a high inductance per area density, large range tunability, low actuation voltage or currents, high quality factor and high self-resonant frequency. No design to date can answer to all these issues simultaneously. Fukushige et al. presented an out-of-plane movable helical design with 3% of tuning range (demonstrated by the use of external actuator) and a quality factor of only 2 [Fukushige 2003]. Tassetti et al. proposed an electrostatically actuated actuator to operate the secondary of a transformer-like structure, with actuation voltages in the range of 100 V to 200 V and no reporting on the quality factor, expected to be inherently low in this kind of structure [Tassetti 2003, Tassetti 2004]. The most promising variable inductor solution proposed to date seems to associate high Q fixed devices with high-performance switches in order to build switchable banks of fixed devices, where the total inductance is defined by the series or parallel combination of individual high-performance devices. This configuration, in spite of requiring high-performance switches to be implemented, does not compromise the quality factor of the inductor in order to acquire the desired tunability. This approach also let the circuit designer free of the use of complicate feedback mechanisms or non-linear calibrations needed to precisely control the inductance value.

The current state-of-the-art results on CMOS-compatible integrated inductors has been obtained associating thick highly conductive metals, low κ polymers and high resistivity substrates, offering peak quality factors in the range of 20 – 60 and self-resonant frequency exceeding 6 GHz, reaching sometimes the range of 10 – 20 GHz [Carchon 2004].

The focus of this thesis is mainly put on spiral inductors, which are to date the devices suffering from the lower quality factor and higher substrate related losses. Finding good technological alternatives for the fabrication of inductors will set technological solutions enabling low insertion losses and high self-resonant frequencies that can be successfully applied for virtually any type of passive device.

1.5. Quality factor enhancement techniques

Many techniques have been proposed and tested in the pursuit of higher quality factor integrated inductors. These techniques can be divided basically in two major groups: design-

related and technology-related. Design-related approaches try to extract the best performance that a given technology can offer by using adapted design methodologies in order to increase the performance of the device without changing radically the way it is fabricated. These methodologies are needed when a given mature technology must be used to fabricate the devices and the designer has no choice about this point. This approach is also necessary in order to obtain the best quality factor that a given technology can offer. Technology-related approaches propose new materials and fabrication technologies in order to provide better performance and functionality by overcoming the inherent limitations of the materials and processing steps used to fabricate the device, namely the thin metal layers and substrate-related losses.

From the design point of view, in spite of being geometrically simple, inductors present many trade-offs related to the choice of the geometrical parameters.

Amongst all polygonal forms, circular spirals present a better quality factor related to a better inductance / perimeter ratio [Chaki 1995, Park 1997, Lee 2001, Aguilera 2002]. The circular design is not available in general for all the mask fabrication processes. In that case, octagonal inductors are the best compromise for the number of sides per turn when only 45^0 lines are allowed by the design rules.

Craninckx demonstrated by electromagnetic simulation that the inner segments of the spiral inductors do not contribute effectively to the total inductance of the device due to their reduced length compared to the overall spiral one [Craninckx 1997]. On the other hand, the inner segments are prone to strong magnetic field influence generated by the outer segments, and present more AC resistance per unit length than the outer ones, contributing significantly to increase the losses of the device. The conclusion of this study is that it is advisable to design "hollow spirals" having the largest possible internal diameter. The drawback of this technique is the increased on-wafer area consumption and some increase on the parasitic capacitances that scale with the total device area. In this same way of thinking, tapered spirals having narrow widths for the inner segments were proposed [López-Villegas 2000, Lin 2002]. The narrow inner tracks are less prone to AC resistance increase due to the external magnetic field generated by the outer tracks, and have also more inductance per unit length. Both effects together can compensate for the increased resistance due to the reduction in the cross section area, and these inductors can have gains in the quality factor in the order of 10 to 20%

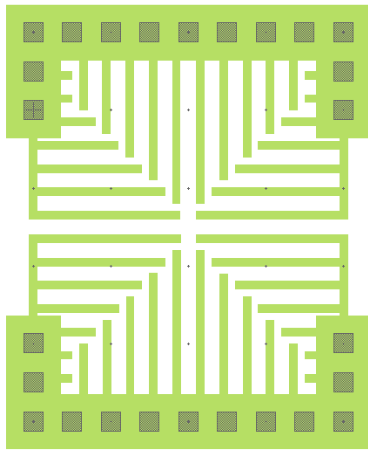
if correctly optimized. The major drawback of this technique is that an accurate modeling approach is needed in order to have the good balance with the tendency to increase the quality factor by having more resistive narrower inner tracks. For this kind of spiral, no simple rule for the track width decrease ratio as function of the geometry and inductance is clearly established. By the same way, no accurate closed-form inductance calculation formulae are available, making it difficult to build devices in an accurate predictive basis.

Differential excitation of spiral inductors showed to be less prone to substrate parasitic influence [Danesh 2002, Reiha 2003], due to the series association of parasitic capacitances when both sides of the device have potentials referenced to the ground. The result from this study suggest that moving for differential circuit architectures are beneficial and can offer up to 30% of improvement in the quality factor with respect to single ended devices build on top of low resistivity silicon substrates. A symmetrical spiral design can also help in order to flatten the frequency response of the device and have larger frequency bandwidth inductors, a feature desirable for multi standard RF circuit operation.

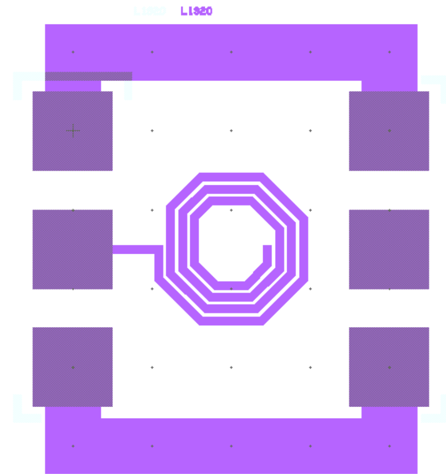
Transformer-like designs like the one proposed by Tiemeijer et al. [Tiemeijer 2001] basically put two or more spirals in parallel in order to decrease the total resistance of the inductor. This technique is effective only when the 2 spirals can be put in close proximity in order to have a high magnetic coupling coefficient that does not make the parallel inductance decrease by the same ratio of the resistance, presenting in the end a better inductance / resistance ratio and then a better quality factor. Another drawback of this type of design is that putting spirals in close proximity can increase the parasitic capacitance reducing the frequency response of the devices. The fabrication of spirals by stacking layers of metal in parallel can reduce the low frequency resistance of the spiral, presenting although a strong reduction in the self-resonant frequency due to the increase in parasitic capacitances [Koutsoyannopoulos 2000, Zolfaghari 2001].

When designing inductors on top of low resistivity substrates, the excessive losses of the substrate can be avoided by putting a conductive grid between the spiral and the substrate, made of highly-doped silicon or metal. The grid must be patterned with thin, non-closed paths in order to avoid induced losses due to eddy current and reduction of the inductance by the image currents that would be induced by a solid conductive structure. This technique is known as the patterned ground shield (PGS, fig. 1.4) [Mohan 1998, Yue 1998, Tan 2000, Ng

2001] and is effective when the resistivity of the substrate is in the order of 0.1 Ω cm or less. For higher resistivity substrates, this technique presents the drawback of increasing the parasitic coupling capacitance to the substrate, what reduces by consequence the resonant frequency of the device. Burghartz demonstrated in 1997 that the surrounding ground ring and the way it is electrically connected to the substrate also plays an important role in the quality factor of the inductors [Burghartz 1997b].



(a) Highly diffused silicon and lateral contact vias.



(b) Spiral build on metal with GSG lines contacting the underneath structure.

Fig. 1.4: The use of a patterned ground shied (a) underneath the spiral inductor (b) built on top of low resistivity substrate in order to avoid substrate eddy current losses.

Designing higher track widths reduces proportionally the low-frequency resistance of the device, but an optimum point is reach due to the decrease of inductance with the increase in the cross-sectional area as well as due to an increase of the parasitic capacitance to the substrate, proportional to the metal area. Designing with small track spacing s is usually beneficial due to the gain due to the increase of the mutual inductance term. This gain usually overcomes the drawback of having more track-to-track parasitic capacitance coupling that can potentially reduce the resonant frequency of the devices.

A summary of the studies and techniques performed to date in order design and fabricate high Q integrated inductors is schematically shown in tables 1.2 and 1.3.

Strategy	Advantages	Issues	References
Use of circular spirals	Better quality factor than square ones	Not always available in the design kit (octagonal can be a good compromise)	[Chaki 1995, Park 1997, Lee 2001, Aguilera 2002]
Use of hollow spiral designs	Avoid using low quality / inductance in the inner part of the spiral	Use of more on-wafer surface, increasing cost	[Craninckx 1997]
Tapered width spirals	Increase in *Q* for the same area of other geometries	Complicated design and optimization, gain in Q is marginal if not properly designed	[López-Villegas 2000, Lin 2002]
Symmetrical or transformer-like inductors	Increase in *Q*	Needs high coupling (lower spacing), via resistance limits the performance, needs differential excitation	[Tiemeijer 2001, Danesh 2002]
Symmetrical excitation	Increase in *Q* and *SRF* due to less substrate influence	Needs special circuit design (differential topology)	[Reiha 2003]
Increase track width	Increase *Q* in low frequencies	Large substrate parasitics and on-wafer area consumption, reduce inductance	[Aguilera 2001]
Reduce track spacing	Increase mutual coupling, reduce on-wafer area	Needs tight fabrication tolerances, increase of spiral capacitance	[Aguilera 2001]
Overall optimization for target application	Get best device for the given inductance and frequency	Needs accurate modeling tools or a large library of devices to produce measurement-based models	[Crols 1996]
Reduce track width	Increase in inductance, small footprint	Large losses due to increased line resistance	-
Stacked spirals	Increase in inductance density	Large parasitics, decreased SRF	[Koutsoyannopoulos 2000, Zolfaghari 2001, Lee 2007]

Table 1.2: Overview of design-related spiral inductor quality factor improvement strategies.

Strategy	Advantages	Issues	References
Increase the thickness of the metal	Reduce losses, increasing Q	Effective only at certain frequencies (skin depth limited), challenging etching steps or need of thick resist processing	[Massin 2002]
High conductive metals	Reduce losses, increasing Q	Needs new processing steps and materials (e.g. thick electroplating, advanced etching or CMP)	[Bahl 2001, Zu 1996, Ternent 1999, Carazzetti 2005]
Low κ polymers	Decrease parasitic capacitances, increase both Q and f_{RES}	Need of new materials and processing steps (diffusion barriers, adhesion optimization)	[Burghartz 1997, Jeong 2003]
Thick polymer under the spiral or use of multichip module deposition (MCM-D) technology	Decouple spiral performance from substrate resistivity, very good RF performances	Delaminating, need of high-quality vias or packaging-like technology to fabricate the devices	[Arnold 1992, Baringer 1993, Beyne 1995, Shimoto 1995, Samber 1998, Pieters 1998, Pieters 2001, Carchon 2004]
High resistivity substrates	Eliminate killing substrate parasitics	Makes the process less compatible with standard CMOS	[Benaissa 2003, Spirito 2005]
Backside etching	Eliminate killing substrate parasitics using low resistivity substrates	Complicated fabrication steps, stress related issues for thick metals, fragile structures	[Ozgur 1999, López-Villegas 2000]
Front side etching	Eliminate killing substrate parasitics when using low resistivity substrates	Complicated fabrication, stress related issues with thick metals	[Lakdawala 2002]
Free standing structures	Less prone to substrate losses, enable the fabrication of tunable devices, introducing new functionality	Stress related issues, tunable L has very low Q and bandwidth and usually need very high actuation voltage	[Syms 1993, Yoon 1999, Jiang 2000, Dahlmann 2001, Dahlmann 2002, Zou 2003]
Solenoid-like structures	Good inductance density, very high Q reported	Can be subject to killing via resistance, needs thick metal and sacrificial layers to have good inductance density (large loops)	[Edelstein 1998, Chomnawang 2002, Weon 2005, Lu 2007]

Use of patterned ground shields (PGS) and substrate taps	Increase Q by eliminating some substrate parasitics, simpler modeling	Works only in low resistivity substrates, marginal gain on Q	[Mohan 1998, Yue 1998, Burghartz 1997b, Tan 2000, Ng 2001]
Local increase of substrate resistivity	Eliminate substrate parasitics in low resistivity CMOS	Exotic fabrication process, ion bombardment induced defects	[Yu 2000, Hsu 2002, Chan 2003, Royet 2003, Contopanagos 2007]

Table 1.3: Overview of technological-related spiral inductor quality factor improvement strategies.

The main contributions of this thesis that will be presented in the following chapters are related to both technology and design-related topics by:

1) Developing new fabrication technologies, using highly conductive thick metals, low κ polymers and high resistivity or insulating substrates, and
2) Studying and optimizing the spiral inductor designs by measurement, simulation and accurate physics-based model for the fabricated devices.

Chapter 2

Integrated Inductors

2.1. Inductors and inductance

Inductors are used in a number of RF circuits, including LC resonant tanks in oscillators, RF chokes, filters and as tuning / impedance transformation elements in amplifier and tuning matching networks.

An inductor is a passive device for which the main function is to store electrical energy in the magnetic field. The main property of an inductor is its inductance *L*, defined as the ratio of produced magnetic flux linkage for a given applied current:

$$L = \frac{\Phi}{I} \qquad \text{(eq. 2.1)},$$

where Φ if the magnetic flux induction measured in [Wb] = [V s] and *I* the applied current in [A]. In the SI units, the inductance is measured in henry, 1 H = 1 Wb/A. This equation defines the self-inductance of a circuit, in a sense that it relates the current and the flux inside a closed-loop circuit.

The dynamic *I-V* behavior of an inductor when a time varying current is applied is obtained using the Faraday induction law that states that a variable magnetic flux $\Phi(t)$ produces an induced voltage $V = - d\Phi(t) / dt$ on the inductor terminals. For a sinusoidal time-varying current with angular frequency ω, the time varying current is expressed as:

$$i(t) = I_0 \sin(\omega t) \qquad \text{(eq. 2.2)}.$$

The magnetic flux linkage and voltage can be written as:

$$\Phi(t) = L\, i(t) \qquad \text{(eq. 2.3),}$$

$$V(t) = L\frac{dI(t)}{dt} = \omega L I_0 \cos(\omega t) \qquad \text{(eq. 2.4).}$$

In terms of Fresnel complex phasor representation, the relation between the phasors $\hat{V}$ and $\hat{I}$ defines the complex impedance $\hat{Z}$ of an inductor:

$$\hat{Z} = \frac{\hat{V}}{\hat{I}} = j\omega L \qquad \text{(eq. 2.5),}$$

where ωL is the voltage / current amplitude ratio (inductive reactance) and $j = \sqrt{-1} = e^{j\pi/2}$ defines the $\pi/2$ phase difference between the voltage (eq. 2.4) and current (eq. 2.2) signals.

2.2. Quality factor and self-resonant frequency

Practical inductors are made of finite conductivity wires that offer some resistance to the passage of the current, modifying the eq. 2.5 for the impedance to:

$$Z = R_S + j\omega L \qquad \text{(eq. 2.6),}$$

where R_S represents the series resistance of the inductor. A measure of how good an inductor is can be expressed by its quality factor Q defined as:

$$Q = \frac{\mathrm{Im}(Z)}{\mathrm{Re}(Z)} = \frac{\omega L}{R_S} \qquad \text{(eq. 2.7).}$$

Q defines a merit factor in the sense that the bigger the quality factor is, the better an inductor will be, presenting lower losses. More specifically, the quality factor can be defined as the

ratio between the peak stored magnetic energy divided by the energy dissipated per cycle in the device. This definition gives eq. 2.7 as result.

Practical inductors have also stray capacitances that appear in parallel with the device in a first order model show in fig. 2.1.

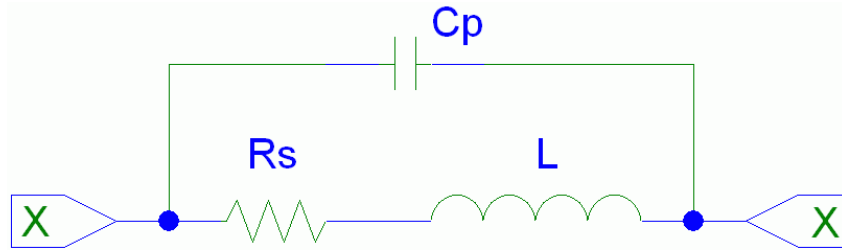


Fig. 2.1: First order RLC model of an inductor. R_S accounts for the series resistance and C_P for the stray parallel capacitance and L for the inductance.

In this case, the definition using the real / imaginary impedance relation is still used and the following expressions hold for the impedance and quality factor:

$$Z = \frac{R_S}{(1-\omega^2 LC_P)+(\omega R_S C_P)^2} + j\frac{\omega L(1-\omega^2 LC_P - R_S{}^2 C_P / L)}{(1-\omega^2 LC)+(\omega R_S C_P)^2} \quad \text{(eq. 2.8)},$$

$$Q = \frac{\mathrm{Im}(Z)}{\mathrm{Re}(Z)} = \frac{\omega L(1-\omega^2 LC_P - R_S{}^2 C_P / L)}{R_S} \quad \text{(eq.2.9)}.$$

The circuit of fig. 2.1 presents a self-resonance at:

$$\omega_{RES} = \sqrt{\frac{1}{LC_P} - \left(\frac{R_S}{L}\right)^2} \quad \text{(eq.2.10)},$$

at which the quality factor (eq. 2.9) equals zero. At this frequency, the imaginary part of the impedance goes to zero and beyond this frequency the parasitic capacitance dominates the electrical behavior and the device does not work as a lumped inductor anymore.

This definition of quality factor is appropriate for devices working at low frequencies or far below the self-resonant frequency, when the device is used as a pure inductive one. For

devices working in resonant circuits, the capacitance C_P can be included as part of the resonant circuit and a more convenient definition is used [Bahl 2001, O98]:

$$Q = \frac{f_{RES}}{BW} \quad \text{(eq.2.11)},$$

where f_{RES} is the desired resonant frequency obtained by peaking the impedance value when an ideal capacitor is put in parallel with the inductor, and BW is the 3-dB frequency bandwidth (where the impedance amplitude falls to $1/\sqrt{2}$ of its maximum value).

Another definition of quality factor useful for distributed resonators is [O98]:

$$Q = \frac{f_{RES}}{2}\left[\frac{d\varphi}{df}\right]_{f=f_{RES}} \quad \text{(eq.2.12)},$$

that measures the stability of the phase at the resonant frequency. The resonance frequency is obtained by setting the parallel capacitance to a value that makes the impedance to be maximized at the frequency f_{RES} that is the frequency of operation of the inductor in this case.

The quality factor at a given operating frequency is the main merit factor used to rank an inductor, but when the device is aimed to be used at different frequencies or in a large frequency range and other factors like wafer surface should be taken into account, another merit factors can be defined to fit the desired design criteria. Of particular interest, is the one defined in [Bahl 2001]:

$$FMI = \left[\frac{Q_{EFF} \cdot f_{RES}}{A_{SPI}}\right]_{L_{EFF}, f} \quad \text{(eq.2.13)},$$

where Q_{EFF} and L_{EFF} are the effective quality factor and inductance at the desired working frequency f, f_{RES} is the self-resonant frequency of the device and A_{SPI} is the device area. This merit factor gives best ranking for small footprint, broadband devices, having the maximum quality factor at the desired operating frequency.

For applications where the quality factor is not the first concern (high impedance RF chocks for example), one can suggest using the inductance per unit area, *IPA* as merit factor:

$$IPA = \frac{L}{A_{SPI}} \qquad \text{(eq.2.14)},$$

which will best rank devices with large inductance and small footprint devices.

2.3. Inductance calculation

The procedure to calculate the inductance of an inductor consists in evaluating eq. 2.1 as function of the geometry and properties of the magnetic circuit of a device. For inductors made of non-magnetic materials, the inductance is an exclusive function of the geometric configuration of the conductors from what the inductor is made of. Eq. 2.1 defines the self-inductance in a sense that it relates the linkage magnetic flux and the current inside a closed loop-circuit. When two or more neighbor circuits interact magnetically, the magnetic flux in one circuit induces a voltage into the other circuit and vice-versa. The constant defining this inter-circuit magnetic flux linkage as function of the current defines the mutual inductance *M*:

$$M_{ij} = \frac{\Phi_{ij}}{I_i} \qquad \text{(eq.2.15)},$$

where Φij is the magnetic flux induced in the circuit loop *j* by the current *Ii* applied to the *i-th* circuit.

The mutual inductance between two circuits can be calculated using the Neumann formula [Grover 1962]:

$$M = \frac{\mu}{4\pi} \iint \frac{\cos(\theta)}{r} dl_1 dl_2 \qquad \text{(eq.2.16)},$$

where dl_1 is a length element in the circuit 1, dl_2 is a length element in the circuit 2, *r* the distance vector between the two elements and θ the angle between them. [Grover 1962]

proposes analytical and approximated solutions for the self and mutual inductances of various elementary and complex geometries of conductors and system of conductors.

2.3.1. Inductance of a system of conductors

For a system of conductors in series (carrying the same current), the total inductance can be calculated as [Ruehli 1972, Niknejad 2000]:

$$L_{SERIES} = \sum_{\substack{i=1 \\ j=1}}^{N} M_{ij} = \sum_{i=1}^{N} L_i + 2\sum_{\substack{i=1 \\ j=i+1}}^{N} M_{ij} \quad \text{(eq.2.17)},$$

where $M_{ij} = M_{ji}$ is the mutual inductance between 2 subcircuits and $L_i = M_{ii}$ is the self-inductance of each subcircuit. The elements M_{ij} composes the inductance matrix, and characterizes completely the inductive behavior of any complex system of conductors. If two parallel conductors have the current flowing in the same directions, $M_{ij} > 0$. When the currents flow in the opposite direction, $M_{ij} < 0$. In order to maximize the inductance, one should look for geometries that maximize the positive mutual inductance term.

For N segments connected in parallel (having the same potential), the total inductance can be calculated as [Ruehli 1972]:

$$L_{SHUNT} = \frac{1}{\sum_{i=1, j=1}^{N} K_{ij}} \quad \text{(eq.2.18)},$$

where K is the reluctance matrix, defined as the inverse of the inductance matrix:

$$K = M^{-1} \quad \text{(eq.2.19)}.$$

One can note that, for a group of parallel connected inductors without magnetic coupling the inductance matrix is diagonal and eqs. 2.17 and 2.18 give the well known series and parallel equivalent inductance formulae for non-coupled inductors.

2.3.2 Elementary inductance calculations

The most elementary inductive element used in IC interconnects is a rectangular stripe line. Although getting exact solutions as function of both geometry [Hoer 1965, Wu 1992] and frequency [Djordjevic 1994, Schnieder 2001] is possible, the proposed solutions are cumbersome and do not provide much insight for hand calculations and optimizations. One accurate solution for the low frequency inductance as function of the geometry of the stripline to the 4th order expansion is given by [Mohan 1999b]:

$$L_{RECT} = \frac{\mu l}{2}\left[\ln\frac{2l}{w+t} + 0.5 + \frac{\sqrt{w^2+t^2+0.46\,tw}}{3\,l} - \frac{\left(w^2+t^2\right)^2}{24\,l^2}\right] \qquad \text{(eq.2.20)},$$

where μ is the magnetic constant of the medium, l is the stripe length, w is the stripe width and t is the stripe thickness. Figure 2.2 shows the design curves for the inductance of striplines having a fixed thickness t = 5 μm and different line widths and lengths.

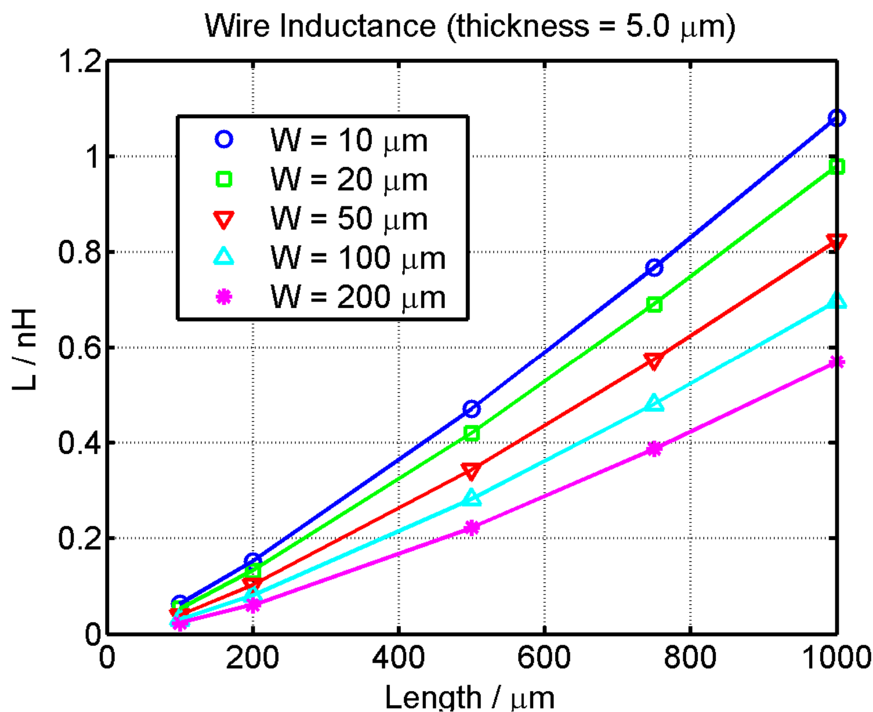


Fig. 2.2: Design curves for the inductance of striplines of different widths (10 to 200 μm) and fixed thickness t = 5 μm.

In most of the practical cases, the length of the line is much larger than both the width and thickness ($l >> w+t$), and the eq. 2.20 simplifies to:

$$L_{RECT} = \frac{\mu l}{2}\left(\ln\frac{2l}{w+t} - 0.5\right) \quad \text{(eq.2.21).}$$

2.3.3. Mutual inductance between current filaments

The starting basis for the calculation for the mutual inductance between striplines is the mutual inductance between 2 filament currents (with no width or thickness). This process involves evaluating eq. 2.16 for a couple of straight lines (fig. 2.3).

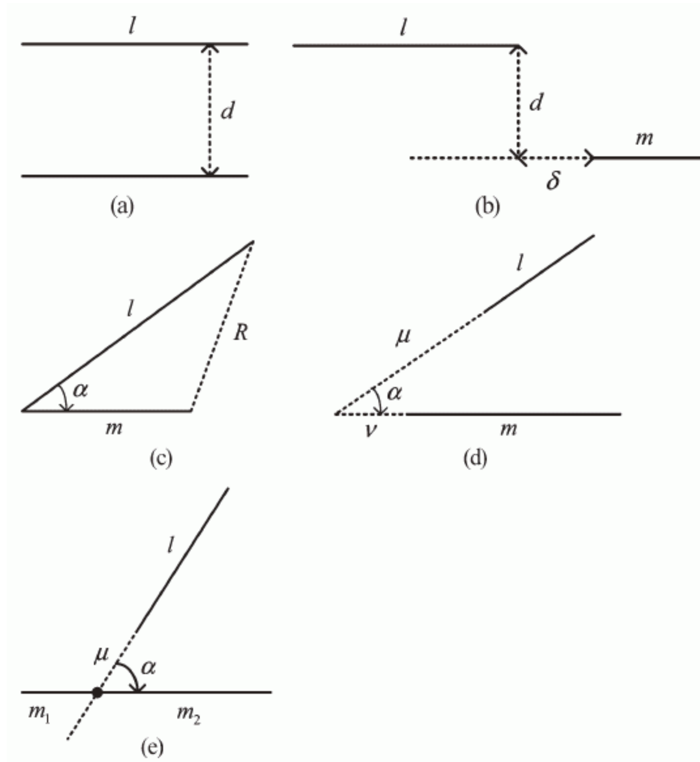


Fig. 2.3: Different geometrical configurations considered for mutual inductance calculation of 2 current filaments (eq. 2.22 to 2.26).

For 2 parallel overlapping lines of equal length (fig. 2.3a), the mutual inductance is given by:

$$M_{PAR}(l) = 2l\left[\ln\left(\frac{l}{d} + \sqrt{1+\frac{l^2}{d^2}}\right) - \sqrt{1+\frac{d^2}{l^2}} + \frac{d}{l}\right] \quad \text{(eq.2.22).}$$

If the segments are parallel but not of equal length (fig. 2.3b), the mutual inductance can be evaluated by computing the differences due to the missing segment areas and using addictiveness property as [Chen 2006]:

$$M_{PAR}(l,m) = \frac{1}{2}\left[M_{PAR}(l+m+\delta) + M_{PAR}(\delta) - M_{PAR}(l+\delta) - M_{PAR}(m+\delta)\right] \quad \text{(eq.2.23).}$$

If the 2 segments forms an angle α and have their extremities at a distance *R*, the mutual inductance term is evaluated as:

$$M_{INC}(l,m) = \cos(\alpha)\left[l.\ln\left(\frac{l+m+R}{l-m+R}\right) + m.\ln\left(\frac{l+m+R}{m-l+R}\right)\right] \quad \text{(eq.2.24).}$$

When the segments form an angle α and do not join, the following expressions hold respectively for figs. 2.3d and 2.3e:

$$M_{INC,2}(l,m) = M_{INC}(\mu+l,\nu+m) + M_{INC}(\mu+l,\nu) - M_{INC}(\mu+l,\nu) - M_{INC}(\nu+m,\mu) \quad \text{(eq.2.25),}$$

and

$$M_{INC,3}(l,m) = M_{INC}(m_1,\mu+l) + M_{INC}(m_2,\mu+l) - M_{INC}(m_1,\mu) - M_{INC}(m_2,\mu) \quad \text{(eq.2.26).}$$

These expressions can be used when the wire width is very small compared to the other distances, which can fail in dense IC interconnects. In that case these expressions are still used by replacing the 2 wires by 2 equivalent thin wires separated by a distance that would give the same resulting mutual inductance. This distance is defined as the geometric mean of all the possible distances between the segments. For 2 planar figures, the geometrical mean distance *GMD* [Grover 1962, Greenhouse 1974] can be evaluated as:

$$\ln GMD = \frac{1}{A_1A_2}\iint_1\iint_2 \ln(r)\, dx_1dy_1\, dx_2dy_2 \quad \text{(eq.2.27),}$$

where A_1 is the area of the first figure, A_2 is the area of the second one, $dx_1.dy_1$ is a surface element in the figure 1 and $dx_2 \cdot dy_2$ a surface element in the figure 2. In general, the *GMD* distance is slightly smaller than the center-to-center distances between the lines, but using the

center-to-center distance instead of *GMD* is an approximation that can be used without major loss in precision.

For 2 thin parallel wires ($t << w$), *GMD* can be calculated as:

$$\ln(GMD_{PAR}) = \ln(d) - \frac{w^2}{12\,d^2} - \frac{w^4}{60\,d^4} - \frac{w^6}{168\,d^6} - \frac{w^8}{360\,d^8} - \frac{w^{10}}{660 d^{10}} \cdots \qquad \text{(eq.2.28).}$$

An exact solution for the *GMD* value of parallel rectangular strips is cumbersome and discussed in detail in the literature [Weeks 1979, Antonini 1999]. As a numeric example, 2 parallel rectangular strips having w = 20 µm, spaced by s = 5 µm and having 5 µm of thickness have a center to center distance of $w + s$ = 25 µm. Thin film approximation (eq. 2.28) gives *GMD* = 23.49 µm. The complete solution gives 23.61 µm. In this typical example, taking the center-to-center distance resulted in an overestimation of about 6% in the value of *GMD*. The mutual inductance is proportional to *ln*(*GMD*), resulting in overestimation of only about 2% in the value of *M*.

2.4. Spiral inductors

Spiral inductors, like the ones seen in fig. 2.4, are common geometries used to fabricate inductors in planar technologies. They present the advantages of having the best possible inductance density for a planar geometric figure and a geometry simple to fabricate. Common geometries are squares, rectangles, octagons, N-sided polygons and circular spirals.

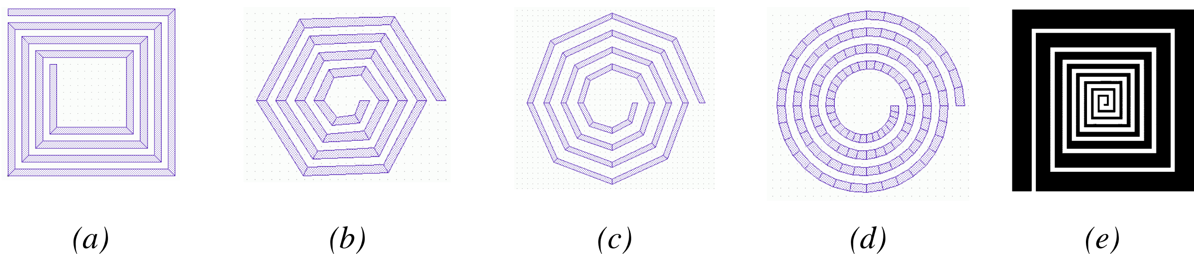


Fig. 2.4: Different spiral inductor geometries (a) squared, (b) hexagonal, (c) octagonal, (d) circular, (e) tapered [López-Villegas 2000].

Circular spirals have the best inductance density per unit of area and the best quality factor amongst all the possible planar geometries, but since circular wiring is not available in many

design and fabrication tools, octagonal geometries are presented as a good compromise between having a simple feasible geometry and good RF performances. Circular geometries sometimes poses electromagnetic simulation difficulties due to the need of exaggerated number of rectangular or triangular meshing cells needed to represent the geometry in design and simulation tools that do not have suitable curved objects as meshing discretization elements.

Some studies have demonstrated that the use of a variable width tracks, with narrower tracks for the inner segments (fig. 2.4e) can increase the quality factor [López-Villegas 2000, Lin 2002]. This type of spiral is known as “tapered width” inductor.

The main geometric parameters that characterize a spiral inductor are: its external diameter D_{OUT} (measured from the 2 outmost conductor distances), the wiring width w, the track-to-track distance (or spacing) s and the number of turns n. The thickness of the conductor winding plays a minor role in the value of the inductance, and is neglected in most of practical formulae, although thick metal spirals needs special correction for the inductance and loss calculation as discussed further.

Many studies proposed different formulae to calculate the inductance of spirals as function of their geometrical parameters [Wheeler 1928, Bahl 1998, Crols 1996, Ronkainen 1997, Bryan 1995, Voorman 1993, Dill 1964, Grover 1962]. Greenhouse method is also frequently used, although being a cumbersome method that does not give closed formulae for all types of spirals [Greenhouse 1974]. All of these methods consist in different analytical or approximated solutions to the eqs. 2.15 and 2.16. One of the most practical and accurate formulae available to date are presented in [Mohan 1999] and were used in this work to estimate the inductance of planar spiral inductors:

$$L_{SPI} = \frac{\mu n^2 D_{AVG} c_1}{2}\left[\ln\left(\frac{c_2}{\xi}\right) + c_3\xi + c_4\xi^2\right] \qquad \text{(eq.2.29)},$$

where μ is the magnetic constant of the medium, n is the number of turns, D_{AVG} is the average diameter of the spiral, c_1, c_2, c_3 and c_4 constants for a given spiral geometry (given in table

2.1) and ξ a geometric factor describing how dense the spiral design is. The definitions of D_{AVG} and ξ as function of the internal and external diameters are:

$$D_{AVG} = \frac{D_{OUT} + D_{IN}}{2} \quad \text{(eq.2.30)},$$

and

$$\xi = \frac{D_{OUT} - D_{IN}}{D_{OUT} + D_{IN}} \quad \text{(eq.2.31)},$$

where D_{OUT} is the external diameter (measured from the outmost extremity of the external conductors) and D_{IN} the internal diameter (measured from the innermost extremities of the internal conductors) of the spiral.

Geometry	c_1	c_2	c_3	c_4
Square	1.27	2.07	0.18	0.13
Hexagon	1.09	2.23	0.00	0.17
Octagon	1.07	2.29	0.00	0.19
Circle	1.00	2.46	0.00	0.20

Table 2.1: Values of the coefficients c_1, c_2, c_3 and c_4 for the inductance calculation of planar spiral inductance using eq. 2.2.

These formulae are based on fitting current sheet approximations over a large design space of thin film inductors (thickness around 1.0 μm) [Mohan 1999b]. They give accurate results (5%) in the range of 2 to 50 nH and acceptable results in the range of 1 to 100 nH (10 – 20%). Further corrections are necessary to design small footprint or sub-nH inductors as well as thick metal inductors (these expressions do not show thickness dependency of the inductance, causing some overestimation for thick metal inductors).

Typical inductance values for integrated spiral inductors are in the range of 1 to 100 nH, with external diameters varying typically from 50 to 1000 μm. Applications in the frequency ranges above 10 GHz can demand values in the 0.1 – 1 nH range. In that case, special care should be taken in modeling the parasitics and corrections should be applied to eq. 2.29 [Biondi 2005].

Fig. 2.5 shows the design curves for the maximum inductance one can obtain for an octagonal spiral inductor having D_{OUT} = 250 μm, track widths between 5 and 40 μm and s / w ratios between 0.1 and 1.0 (typical design values for spiral inductors). It should be noted that spiral inductors, although of simple realization, consume a lot of on-wafer surface, and careful optimization to have the best size / inductance and inductance / quality factor ratio should be carried out. This optimization should consider a given inductance value, frequency of operation and the technology profile used to fabricate the inductors.

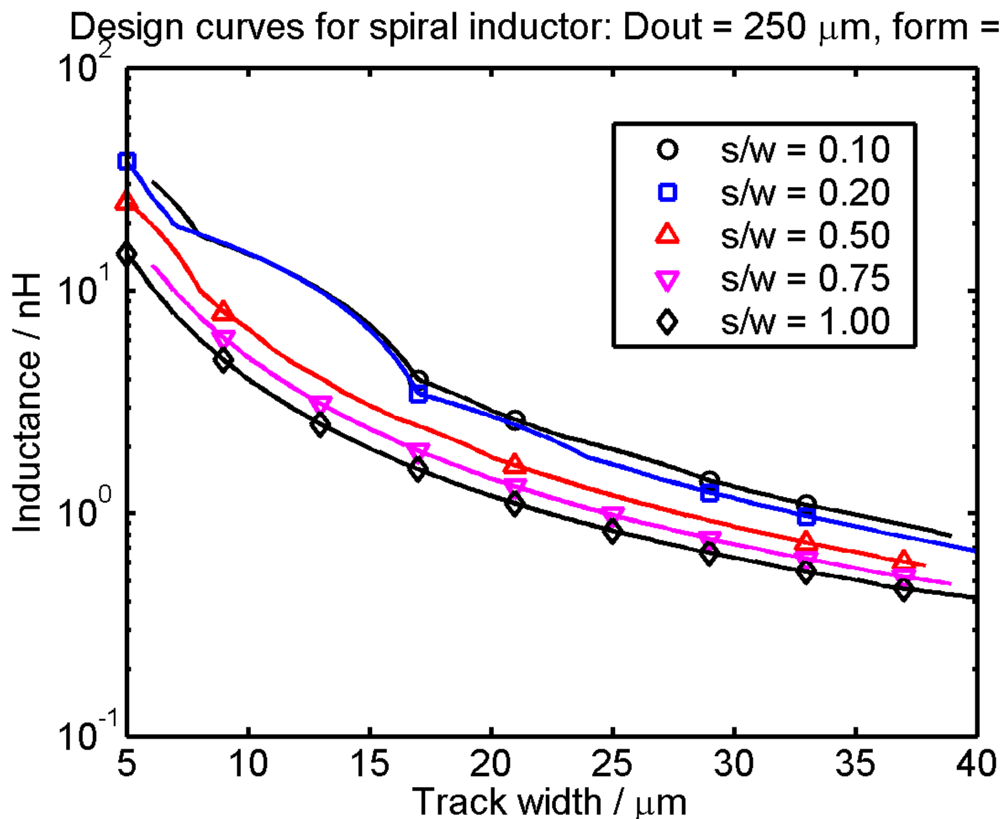


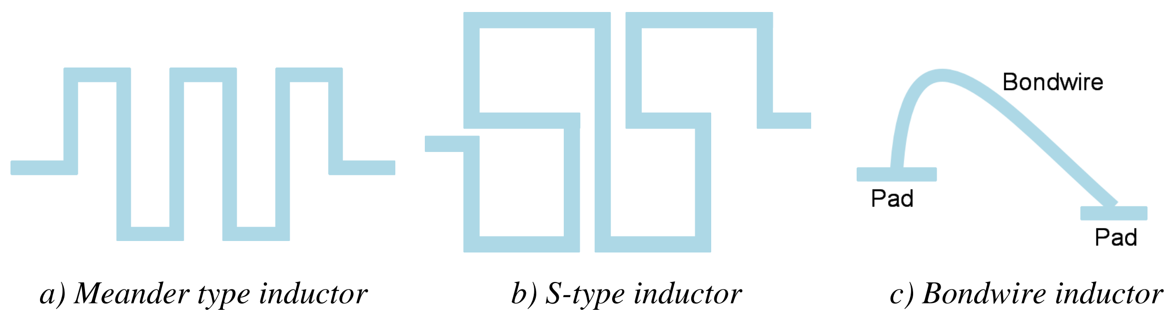
Fig. 2.5: Design curves for the maximum inductance of octagonal spiral inductors having external diameter D_{OUT} = 250 μm, track width w between 5 and 40 μm and track spacing s defined by the s / w ratios between 0.1 and 1.0.

2.5. Other types of integrated inductors

Spiral inductors are the most common used design for fabricating on-chip inductive devices due to the fact of being compact and presenting the better quality factor for a planar figure. The main drawback associated to this kind of structure is the need of 2 metal layers or one air bridge or wire bonding step to connect the innermost segment to an RF port. Single loop spiral [Bahl 2003], meander type [Wadell 1991] (fig. 2.6a) and S-type inductors (fig. 2.6b) are

devices that can be fabricated using a single layer of metal, simplifying the technological requirements to fabricate integrated inductors. The drawback associated to these structures is the absence of positive mutual inductance contribution in the single loop geometry, and the negative mutual inductance presented by currents flowing in opposite directions along parallel segments. In spite of having a good length to area ratio, the meander inductors present less inductance than a linear section of conductor with the same length due to the negative mutual inductance contribution term, and tend to exhibit low quality factors [Stojanovic 2006]. S-type inductors also suffer from this same problem, but the negative inductance term is reduced by minimizing the number of segments with negative mutual inductance terms.

When the on-chip space is limited and the designer needs inductive elements near the input and output ports of the RF circuit, inductors can be fabricated by exploiting the inductive behavior of the bondwires [Steyaert 1994] (fig. 2.6c). These devices can be modeled to the first approximation as straight circular cross section conductors having the same nominal length of the bondwire connection [Bahl 2003]. Additional modeling effort is needed in order to take into account the irregular and curved form of the bondwires as well as to take into account mutual inductance terms presented by wires in close proximity [Mouthaan 1997, Harm 1998].



a) Meander type inductor *b) S-type inductor* *c) Bondwire inductor*

Fig. 2.6: Examples of alternative geometries for the fabrication of on-chip inductors.

The availability of new MEMS fabrication techniques using thick sacrificial layers enables the fabrication of solenoid and toroidal inductors [Park 2003, Nieminem 2004], expected to have good RF performances due to less parasitic coupling to the substrate and good inductance per wire length ratio presented by these geometries.

2.6. Simplified physical model of integrated spiral inductors

Figure 2.7 shows an equivalent circuit model proposed for spiral inductors built on top of low to moderate resistivity silicon wafers [Yue 2000]. The network formed by C_{INS1}, C_{INS2}, R_{SUB1}, R_{SUB2}, C_{SUB1} and C_{SUB2} represents the parasitic effects of the substrate in this first order basic model.

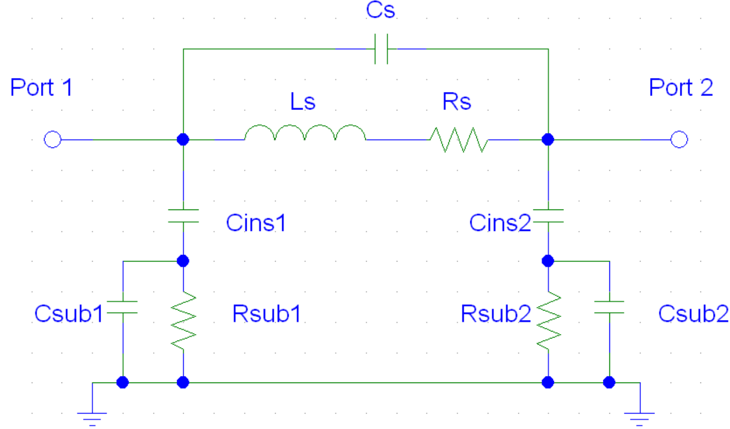


Fig. 2.7: Equivalent circuit model of a spiral inductor built on top of low to moderate resistivity substrate.

The 1-port quality factor for this equivalent circuit model is given by [Yue 2000]:

$$Q = \underbrace{\frac{\omega L_S}{R_S}}_{spiral\ only} \underbrace{\frac{R_P}{R_P + [(\omega L_S / R_S)^2] R_S}}_{self-resonance\ factor} \underbrace{\left(1 - \frac{R_S^2 C_0}{L_S} - \omega^2 L_S C_0\right)}_{substrate\ loss\ factor} \quad \text{(eq.2.32)},$$

with

$$R_P = \frac{1}{\omega^2 C_{INS}{}^2 R_{SUB}} + \frac{R_{SUB}(C_{INS} + C_{SUB})^2}{C_{INS}{}^2} \quad \text{(eq.2.33)},$$

and

$$C_P = C_{INS} \frac{1 + \omega^2 (C_{INS} + C_{SUB}) C_{SUB} R_{SUB}{}^2}{1 + \omega^2 (C_{INS} + C_{SUB})^2 R_{SUB}{}^2} \quad \text{(eq.2.34)}.$$

The first term in eq. 2.32 represents the intrinsic spiral quality factor (due only to spiral metal series resistance), the second term represents the self resonance factor and third term is defined as the substrate loss factor.

The main inductance L_S is calculated by different methods and formulae. Methods presented in [Greenhouse 1974] and [Mohan 1999] are the most frequently used ones.

First order approximations have been proposed to calculate the parasitic terms of this model as function of the inductor geometry and the physical properties of the used metal and substrate [Yue 2000].

The series resistance can be estimated as [Eo 1993]:

$$R_S = R_{DC} \frac{t}{\delta(1-e^{-t/\delta})} = \frac{l}{\sigma\delta\, t(1-e^{-t/\delta})} \qquad \text{(eq.2.35)},$$

where t is the conductor thickness,

$$\delta = \sqrt{\frac{2}{\sigma\omega\mu}} \qquad \text{(eq.2.36)}$$

is the skin depth and

$$R_{DC} = \frac{l}{\sigma w t} \qquad \text{(eq.2.37)}$$

is the DC resistance of the spiral, σ the conductivity of the metal, w the spiral track width, l is the total length of the spiral and ω is the angular frequency.

The insulator and substrate capacitance can be estimated using these relations:

$$C_{INS} = \frac{1}{2} lwC_{INS}'' ,\ C_{INS}'' \approx \frac{\varepsilon_{INS}}{t_{INS}} \qquad \text{(eq.2.38)},$$

$$C_{SUB} = \frac{1}{2} lwC_{SUB}'', \; C_{SUB}'' \approx \frac{\varepsilon_{SUB}}{t_{SUB}} \quad \text{(eq.2.39)},$$

where C_{INS}'' and C_{SUB}'' are the capacitance per unit area of the spiral / substrate insulation layer and the substrate respectively, calculated approximately as function of their dielectric constants ε_{INS} and ε_{SUB} and their thicknesses t_{INS} and t_{SUB}.

The substrate resistance can be estimated as:

$$R_{SUB} = \frac{2}{lwG_{SUB}''}, \; G_{SUB}'' \approx \frac{\sigma_{SUB}}{t_{SUB}} \quad \text{(eq.2.40)},$$

where G_{SUB}'' is the substrate conductance per unit area, calculated approximately from its conductivity σ_{SUB} and thickness t_{SUB}.

The parallel spiral capacitance C_S is usually considered as due mainly to the underpass segment, and is calculated as:

$$C_S = \varepsilon_{INS} \frac{nw^2}{t_{INS,M1}} \quad \text{(eq.2.41)},$$

where w is the underpass track width (supposed to be the same of the spiral inductor) and $t_{INS,M1}$ is the thickness of the insulator between the underpass and the first level of metal. This equation explicitly ignores the capacitive coupling between adjacent inductor tracks, which is in fact the main contribution to the parallel parasitic capacitance. Chapter 5 addresses more accurate methods to calculate the capacitance C_S.

Many other models have been proposed in the literature [Crols 1996, Bahl 1998]. They are in general obtained by fitting physics-based equations to large sets of measured or electromagnetic simulated data. The accuracy and limits of applicability of this simple first order model as well as other models available in the literature should be toughly analyzed before drawing conclusions outside the design space and technology profile where the considered models were validated.

Although not very accurate, this first order model gives the first insight one should have in order to improve the performance of these devices. Fig. 2.8 shows the contribution of each quality factor term of eq. 2.32 for a typical spiral inductor fabricated on top of low resistivity 10 Ω cm standard CMOS substrate. One can notice that at lower frequencies (below 1 – 2 GHz), the most important performance limitation comes from the finite conductivity of the metal. The peak value and position of the quality factor is affected by the overall parasitics associated to the device, and the resonant frequency (where Q goes to zero), is mainly defined by the parasitics coming from the substrate and by the parallel stray capacitance (interspiral / underpass) capacitance.

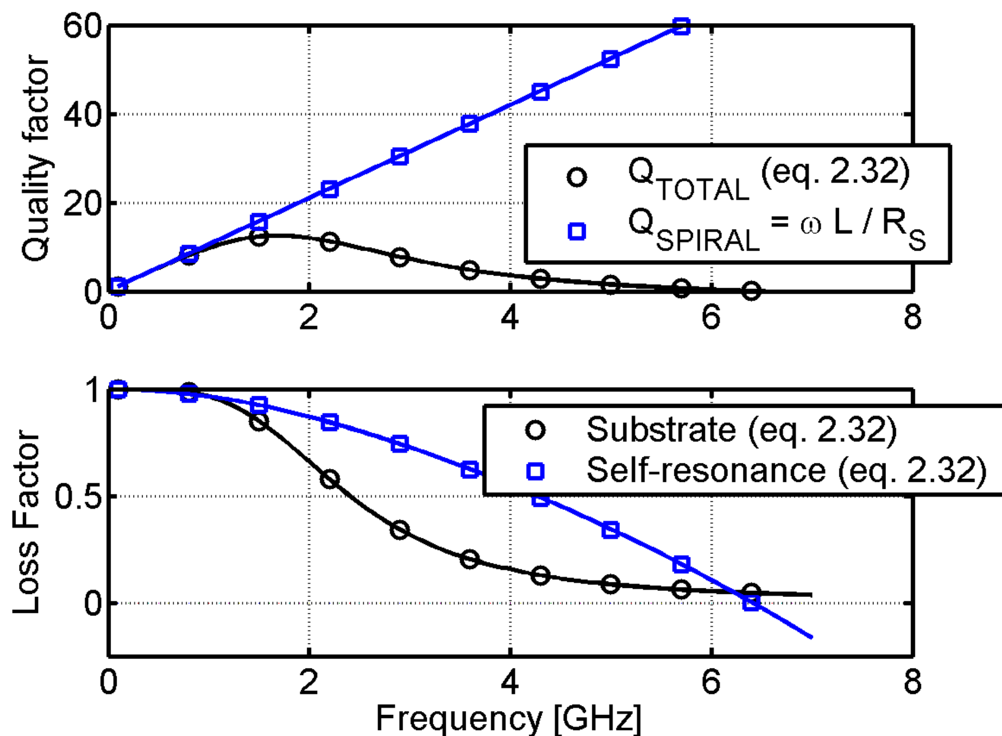


Fig. 2.8: Quality factor limitations for inductors built on top of high to moderate conductivity substrates. In this simulation, typical values are used: L_S = 1.2 nH, R_S = 1.2 Ω, C_S = 200 fF, C_{INS} = 250 fF, R_{SUB} = 120 Ω and C_{SUB} = 50 fF.

For inductors built on top of low resistivity silicon wafers and using thin aluminum metallization layers, typical peak quality factors that can be obtained are in the range of 5 – 10, with self-resonances below 3 GHz. These poor RF performances motivates the use of new technologies having thick highly conductive layers associated to low κ polymers as well as

the use of micromachining techniques or high resistivity substrates in order to reduce the impact of the substrate-related losses.

This first order model was used as a guide for optimization of spiral inductor designs initially fabricated in this thesis. This model points the need of reducing the associated parasitics, especially the ones originated from the substrate, in order to have higher quality and higher self-resonant frequencies. Further observations and improvements based on measurements and electromagnetic simulations will be discussed in detail in the chapter 5.

Summary

This chapter presented the basic definitions and technological limitations associated to the fabrication of integrated inductors on top of silicon substrates. The inductance calculation problem involves calculations as function of conductor geometries that were discussed in detail. From the technological point of view, the major drawback of integrate spiral inductors are associated to their poor RF performances originated from the thin layer metallization losses and substrate-induced losses. A first-order model initially used in this thesis for the estimation of the performance of spiral inductors was also presented.

Chapter 3

Copper / polyimide fabrication process

One of the main objectives of this research is the development of a process flow for the fabrication of copper / low κ high quality factor devices having a low thermal budget and being compatible with other CMOS back-end techniques. A process flow using the equipments and procedures available in the clean rooms of the EPFL Center of Micro and Nanofabrication (CMI) was developed and validated in the frame of this research.

3.1. Proposed process flow

Preliminary experiments were conducted with the available processing equipment in order to establish a process flow to fabricate thick high-conductivity copper lines embedded in low κ polymer.

For the metal deposition, copper electroplating was chosen for a variety of reasons, amongst them:

- Copper is a high-conductivity metal, which is a key factor for the fabrication of high quality factor passives. Typical thin-film resistivity of electroplated copper films is about 2.0 μΩ cm, considerably less than the traditional aluminum used in standard IC interconnects (between 3.3 and 5.0 μΩ cm depending on the deposition process and conditions).
- It is possible to deposit considerably high thicknesses using the electroplating process. The high deposition rate, about 0.5 μm/min, allows obtaining thickness in the range of 10 μm in a time frame of a few minutes.

- The electroplating of copper with organic addictives is used in advanced interconnects and is reported for its excellent step coverage, allowing the fabrication of thick metal structures with relatively large aspect ratios. This choice was also related to the availability of advanced CMP steps, good step coverage, low resistivity of the films, and much higher resistance of copper against electromigration with respect to aluminum.

The main drawbacks and issues associated to the copper electroplating based processes are:

- Organic contamination of the films, which can result in opaque color aspect with a resistivity higher than the expected one. Careful set of the additives and on the used current density values is necessary to control the electrical quality of the obtained films.
- Non-uniformity of deposition due to local current density thickness dependency. For thin seed layers the thickness tends to be higher in the border of the wafer than in the center.
- Copper films tends to oxidize promptly just after deposition, and special care concerning the time between different process steps and previous cleaning of the layers is needed in order to avoid excess contact resistance and adhesion problems between oxidized layers.
- Adhesion between copper and polymers is known to be poor, and the use of additional adhesion promoter layers is needed to avoid early delamination problems.
- Copper is well known as a microelectronics contaminant and a fast diffuser in polymers, requiring the use of special anti-diffusion barriers between copper and used polymers or semiconductor materials and special care and limitations with respect to the availability of process steps in a clean room that is also used for microelectronic-compatible processing.
- There is no well established solutions for the dry etching of thick copper films available to date, where a high etch rate with selectivity to standard masking materials would be desirable [Steinbrüchel 1995, Markert 1997, Lee 2004]. The definition of copper films in modern interconnects is mainly performed by means of a chemical-mechanical polishing (CMP) step using a dual damascene approach [Kaanta 1991].

3.2. Development of the process flow

Figure 3.1 shows the developed process flow for the fabrication of 2-metal level structures embedded in polyimide built on top of silicon wafers.

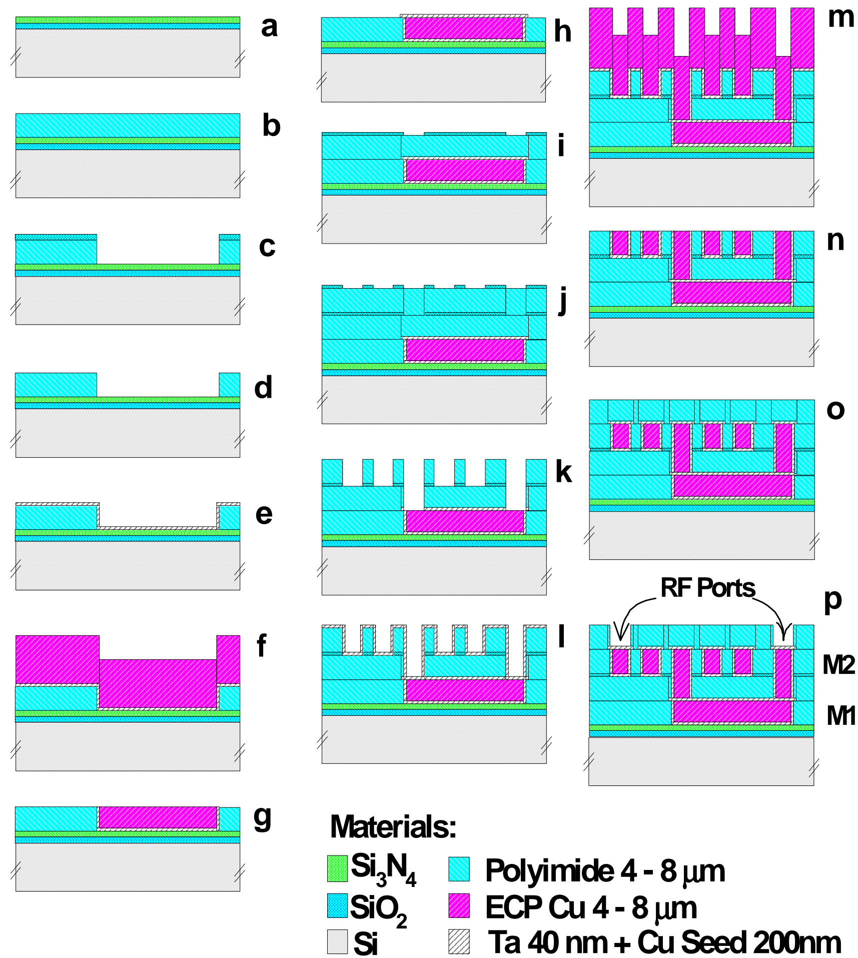


Fig. 3.1: Established process flow for the fabrication of thick-Cu / polyimide embedded passive devices on top of silicon wafers.

First, a thin thermally grown silicon oxide layer is used to insulate the first level of metal of the silicon wafer surface. A Si_3N_4 buffer layer is deposited on top of the SiO_2 in order to reduce the induced stress on the silicon wafer.

Polyimide is then spin on (PI 2610 or PI 2611 from Dupont, ε_R = 2.9) at typical thicknesses between 1.5 µm and 4 µm, defining the thickness of the first metal layer. Polyimide film is then cured at 250 or 300 ^oC for 1 h.

A 0.3-μm thick sputtered SiO_2 layer is used as hard-mask to pattern the polyimide mold using O_2-based plasma etch recipe (*c, d*). This process enables the fabrication of vertical walls with up to 5 μm resolution for 10 μm-thick lines. A 40 nm-thin tantalum layer and a 0.2 μm-thick copper layer are deposited by sputtering (*e*), working as diffusion barrier between copper and polyimide and as seed layer for the electroplating of a thick copper layer (*f*). The copper lines are then defined by a fast removal rate chemical-mechanical polishing step (CMP, *g*) capable of polishing films much thicker than the ones traditionally used in thin-metal layer interconnects. This step was developed specifically in the framework of this thesis project in order to provide a high-speed process capable to define thickness between 1 and 8 μm needed for the fabrication of high Q passives [Pisani 2003b, Pisani 2004].

The successive repetition of these process steps (*h-p*) provide a second level of metal with a via in between.

The steps *i-n* are performed to define both the second level of metal and via using a single CMP step. This process is known as the buried via method [Steinbrüchel 2001], and has some inherent advantages and issues associated to it. In the step (*i*) the hard mask is etched without etching the underneath polyimide. The second level of polyimide is deposited and the second hard mask is then defined (*j*). A single etch step is then used to define both metal 2 and via level moulds. This approach presents as the major advantage the use of lithography steps on top of planar surfaces, which enables to change the thickness of each layer independently and without the need of critical lithographic steps or redoing the optimization of the lithographic conditions for different via layer thickness. An issue that can arise from this is the increased probability of contamination due to redeposition on the bottom line of the channels. The plasma etching of the polyimide is very vertical, and high aspect ratios vertical structures can be obtained by this double layer etch technique. This approach also permits to have a single CMP step to define 2 levels of metal at the same time, simplifying the process flow and reducing the number of CMP steps needed, which is one of the most critical fabrication steps. Furthermore, after the second electroplating step (*m*), the topography of the patterns to step is more irregular, having two different levels where there is a via. Although the CMP step tends to planarize the surface, the more irregular it is in the beginning of the process, the more non-uniformity will be observed in the final result (*n*).

3.3. Copper CMP process

The dual damascene approach adopted in this work [Patrick 1991], requires CMP of copper in order to define the lines embedded into the polymer (steps *e* to *f* and *m* to *n* of fig 3.1). The CMP process is based on the use of an abrasive material plate that interacts with the surface of the wafer through a solution having a mixture of chemical reactants that oxidize the copper and contain also silica abrasive nanoparticles that participate in the mechanical removing part of the process.

Fig. 3.2: Photo of the main CMP setup used in this work (polishing head on the left, conditioning head on the right, polishing pad at the bottom).

The main process parameters (schematically shown in fig. 3.3) are the working pressure (*WP*), defined as the pressure between the polishing head and the underling rotating plate, the rotation speed of both polishing head (*HS* – head speed) and plate (*PS* – plate speed) and the nature and flow of the polishing solution used (slurry). There is an additional pressure parameter applied to the center of the wafer defined as back pressure (*BP*). This parameter permits to compensate for slight differences in the pressure and chemical species distribution along the wafer surface, and is set as a fraction of the main working pressure. The polishing cycles are alternated by conditioning steps using a diamond-covered abrasive head that recondition and clean the polishing plate surface after some minutes of processing. The polishing materials are consumables that degenerate relatively quickly with time and usage, and constant monitoring and conditioning of the tool is needed in order to have reproducible results.

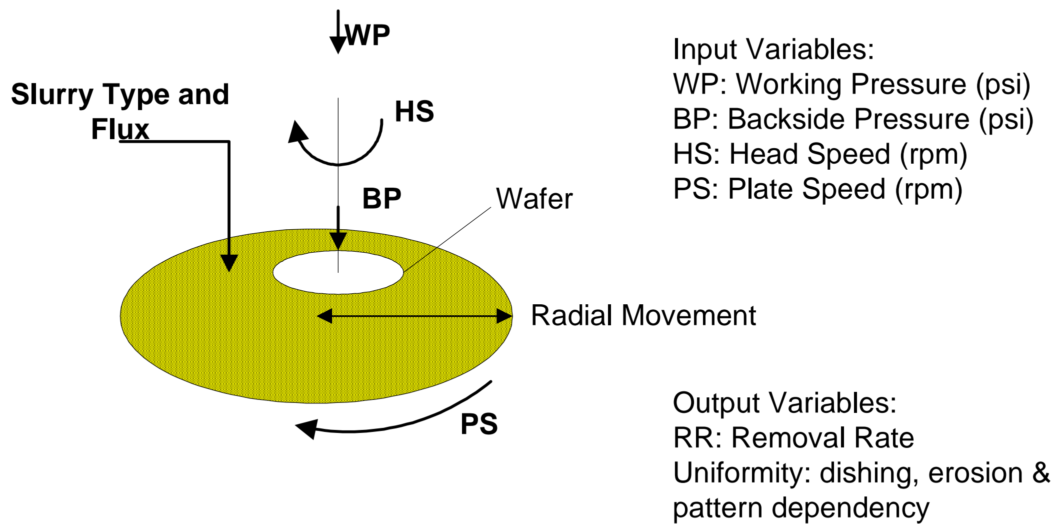


Fig. 3.3: Schematic view of a CMP tool showing the basic input and output process parameters.

As main output parameters, the film mean removal rate (*RR* in nm/min or μm/min) and the uniformity of the removal rate all along the wafer are usually measured.

CMP is a pattern dependent process, which means that the removal rate depends on the size and density of the topographical parameters presented along the wafer surface. The main defects that this dependency generates are known as dishing and erosion. Dishing makes that large structures are polished faster on their central area, making in general negative bowled surfaces for large structures like RF Pads or massive RF ground planes. Erosion occurs due to a faster polishing on denser structures, making them to have less thickness than the overall mean level of polishing of the surface. Both defects are schematically illustrated in the fig. 3.4.

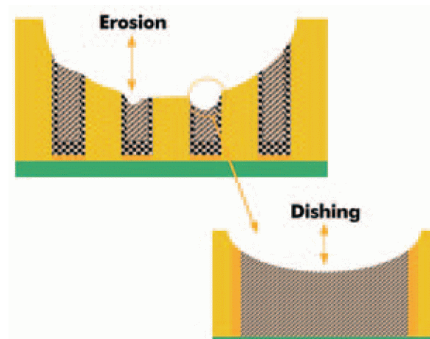


Fig. 3.4: Schematic representation of common CMP imperfections: erosion and dishing.

Copper CMP tends to be very sensitive to a number of factors. First, the chemicals used etch copper with selectivity with respect to copper oxide, and the first seconds of polishing present lower mean removal rates up to the time where this oxide is removed and the reactants are well adsorbed by the surface. In order to keep good uniformity of the processes, lower working pressures should be used, which is a factor that tends to reduce the removal rate, what lead some negative impact in the performance requirements for the polishing of thick copper films.

Self-annealing of copper is another phenomenon that can cause instability on CMP results and due to self-recrystallization of copper during the first hours after electroplating the film [Ritzdorf 1998, Ritzdorf 1999, Lagrange 2000]. Based on that, it is advisable to wait at least 48 h before proceed to the CMP of electroplated films, or to do a thermal treatment to accelerate the self-annealing process of the films.

Typical thickness used in traditional microelectronics interconnects are in the order of 0.5 to 1 μm. Slurries traditionally used for this type of polishing are a solution based on a mixture of abrasive particles having typical sizes from 25 to 50 nm, an acid that attacks the copper and other chemicals to block excessive copper corrosion and stabilize the pH of the solution. Typical removal rates are around 0.2 μm/min for working pressures around 27.6 kPa (4 psi).

In this work, CMP process was used to define much thicker structures, with typical thicknesses in the order of 4 to 8 μm. For this propose, special formulations were studied in order to have high removal rates, in the order of 1 to 3 μm/min. These solutions are much more aggressive and the final result presented more pronounced dishing and erosion effects. Nevertheless, these effects can be kept at acceptable levels by a careful selection of the polishing conditions and by the fact that they are less important on thick films than on thin ones.

A series of experiments using different slurries formulation and polishing conditions was conducted. The best results were obtained using a solution having 30% of a base 25-nm-sized alumina abrasive particles solution, peracetic acid as oxidant agent, and BTA (benzotriazole) as surfactant and corrosion inhibitor. Relatively low working pressures (in the 13.8 – 27.6 kPa

or 2 – 4 psi range) and low speeds (30 – 35 rpm) gave the best results in terms of uniformity, with a mean removal rate between 1 and 3 μm/min.

3.4. Adhesion and diffusion issues

The adhesion between copper and polymers is reported to be weak [Steinbrüchel 2001]. It is especially problematic when one uses CMP as definition step, since the pressures on the surface during the processing are very high and the adhesion of the polymer / metal stacks can be solicited to its extremes. Simple adhesive tape tests can help to identify early adhesion problems and help to diagnose major problems in the process.

Moreover, copper is known to be a fast diffuser into both polymers and semiconductor materials, and anti-diffusive layers must be employed in order to avoid this problem.

Sputtered tantalum was chosen to fulfill both requirements. Tantalum has been studied in advanced interconnects as an efficient diffusion barrier between copper and polymers [Steinbrüchel 2001]. It presents also the desirable good adhesion properties with both polyimide and copper, serving as a good adhesion layer promoter for the fabricated stack. Studies shown that the minimum recommended thickness for these proposes are around 10 – 20 nm. 40-nm nominal thickness was chosen for the sputtering deposition in order to have some safety margin, especially in the vertical walls, where the effective thickness could be the half of the nominal one. This deposition was performed in a Balzers BAS 450 sputtering tool, with a final vacuum in the order of $3 \cdot 10^{-6}$ mbar.

Some simple tests showed that the adhesion is highly sensitive to a number of factors, nominally the degree of cleanliness of the surfaces and the formation of thin tantalum oxide layers when these layers are exposed to ambient pressure. The solution to these issues suggests the following surface treatments before and during tantalum deposition:

- If the underlying surface that will receive the thin tantalum film is polyimide, it should be cleaned from any previous polymeric residues originated from the plasma etching process. An optical or electronic microscopy inspection should be need at this step in order to ensure that the surfaces are smooth and clean after the O_2 plasma etching step.

- Just before loading the wafers into the sputtering tool, a slight O_2 plasma treatment of the surface is recommended in order to remove residual polymeric films and humidity adsorbed on the surface. A quick 30-s plasma treatment at 5 mbar and 300 sccm O_2 flow showed to be effective. The lithographic residues should be carefully removed before this step, since it is too aggressive to the polyimide and the time and temperature of the step should be reduced in order to avoid loss of polyimide thickness.
- Before the tantalum sputtering, an argon plasma cleaning step of the surface is needed. The power level should be relatively low in order to do not damage the polyimide surface, what can also result in severe adhesion problems. The recommended conditions in a BAS 450 sputtering tool are: 33 sccm of Ar, $5.3 \cdot 10^{-3}$ mbar of pressure, a power level that does not produce more than -200 V of DC polarization to voltage in the plasma, during 3 to 5 min.
- One should ensure the best final pressure of the sputtering tool in order to minimize the residual oxygen present in the chamber. This residual gas can be consumed by the tantalum during the deposition resulting in adhesion problems.
- Tantalum oxide can pose problems in both adhesion and contact resistance between different metal layers, since it is an insulator and has not the same good adhesion properties of the tantalum film. The 0.2 µm copper electroplating seed layer should be deposited in the same process step (just switching the sputtering target after Ta deposition, without breaking the setup vacuum in between), in order to completely avoid exposition of the tantalum layers to the ambient atmosphere.

3.5. Fabrication results

The complete process flow was broken down into 2 parts in order to validate the basic process steps that were used more than one time for the definition of 2 metal level structures. A 1 mask basic process covering the steps *a-g* was designed and studied in details before running all the steps listed in figure 3.1.

3.5.1. Substrates used

The devices were built on top of <100> silicon wafers, having 100 mm of diameter (4 inches). As the resistivity of the substrate plays an important role in the RF performance of the

devices, high resistivity silicon wafers having a minimum resistivity of 8 kΩ cm were used. Since devices for CMOS-compatible applications were aimed, the influence of the substrate resistivity on the RF performance was also studied. Different silicon resistivities between 0.1 and 100 Ω cm were used during the fabrication.

For most process development and tests where the RF performance were not taken into account, test-grade wafers having uncontrolled resistivity values between 0.1 and 100 Ω cm were used. Some subsequent development and study using quartz substrates will also be presented in chapter 4. This type of substrate is used due to its insulating properties and relatively low dielectric constant, delivering excellent RF performances.

3.5.2. Wafer insulation

The devices are insulated from the silicon wafer by a 1 μm thermally grown silicon dioxide layer. Part of the experiments was conducted with wafers having a stress-compensated double layer of 0.6 μm of thermally grown SiO_2 covered by a stress compensating buffer layer of 0.4 μm of LPCVD deposited Si_3N_4 layer.

3.5.3. Polyimide deposition

PI 2610 and PI 2611 polyimides from Dupont were chosen as low κ dielectric (ε_R = 2.9) [Dupont]. This choice is related to its low dielectric constant, previous experience with this material in other microfabrication projects and good material properties like hardness and thermal stability. Polyimide has good mechanical and chemical resistance, can be anisotropically etched by plasma and has a certain degree of freedom in the cure temperatures. Different types of polyimide can cover different thickness needs, in photosensitive and non-photosensitive configurations. PI 2610 and 2611 are part of a non-photosensitive family. The option for non-photosensitive type of polyimides adds some process steps related to the hard mask and lithographic definition, but gives more freedom in the choice of final thickness of the metal layers without having to change the lithographic conditions. The SiO_2 hard mask plasma etching process presents more scalability in this aspect and can provide very vertical and deep walls, more adequate for the fabrication of thick rectangular section conductors used in inductors and transmission lines. PI 2610 is less viscous and adapted for thickness between

1.2 and 4 μm. PI 2611 has the same polymeric base but is more viscous, enabling the deposition of thickness between 4 and 10 μm. The spin curve (final thickness after thermal curing as function of spin-on rpm at a given time) is shown in fig. 3.5 [Dupont 1997].

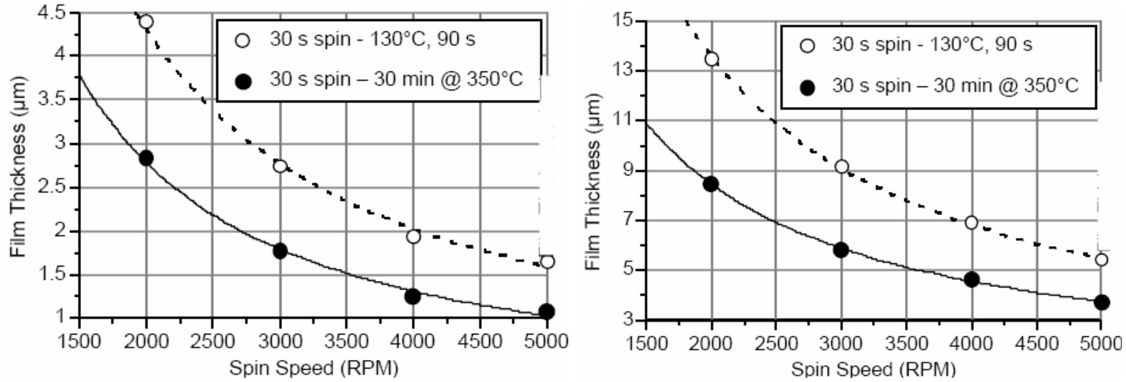


Fig. 3.5: Spin-on curves for soft baked and hard baked PI2610 and PI2611 Dupont polyimides (for 30 s of spinning).

The basic steps followed in the deposition of PI 26xx polyimides are the following:

- Pre-cleaning of the surface using isopropanol alcohol (IPA),
- Thermal treatment at 130 ^{o}C / 5 min in order to eliminate any trace of humidity that is not favorable to the adhesion promoter application and deposition steps,
- Application solution of α-amino propyltriethoxysilane (VM-651) diluted at 0.05% on IPA. This is an adhesion promoter based on oxysilanes diluted in an organic solvent. It improves the adhesion of polyimide films when applied on top of SiO_2 and Si_3N_4 surfaces. This adhesion promoter is effective only on top of substrates that form a native oxide. Deposition of polyimide on top of cured polyimide layers or layers that do not form native oxide is better followed by a plasma descum step instead (recipe previously presented).
- Deposition of the polyimide at the desired spin-on conditions (typically 3000 rpm / 30 s for a 4 μm-thick PI 2611 layer),
- Soft bake at 130 ^{o}C / 5min in order to solidify the deposited film and promote initial evaporation of part of the solvent content,
- Hard bake in N_2 environment at 250 ^{o}C / 1h + 300 ^{o}C / 1h in order to provide the complete elimination of the solvent agent and hardening of the film. Polyimide cannot be exposed to temperatures exceeding 150 / 200 ^{o}C in oxygen-containing environment without an important risk of burning the films.

- Thickness and uniformity inspection using reflectometry technique.

Figure 3.6 shows a thickness mapping measured on a 100 mm wafer just after the long hard bake, measured using a Nanospec 6100 Fourier transform reflectometer. Optical parameters of the polyimide are known to be not constant and films with a few µm cannot be considered as transparent anymore, conditions that make the measurement less precise. The presented result should be considered as qualitative only and confirmation by other techniques like mechanical profilometry can show deviations around 10-25% for the real thickness values.

Final non-uniformity is around 10% of the mean thickness, which is due mainly to the high viscosity of the polyimide and to the fact that manual deposition equipment is used. A reduction in the range of 30% to 40% on the thickness after the hard bake is observed, indicating that a large amount of solvent is evaporated in this step. This diminution in the bulk volume of the film should be carefully monitored and can be a source of problems of adhesion and residual stresses when polyimide is used as a sacrificial layer.

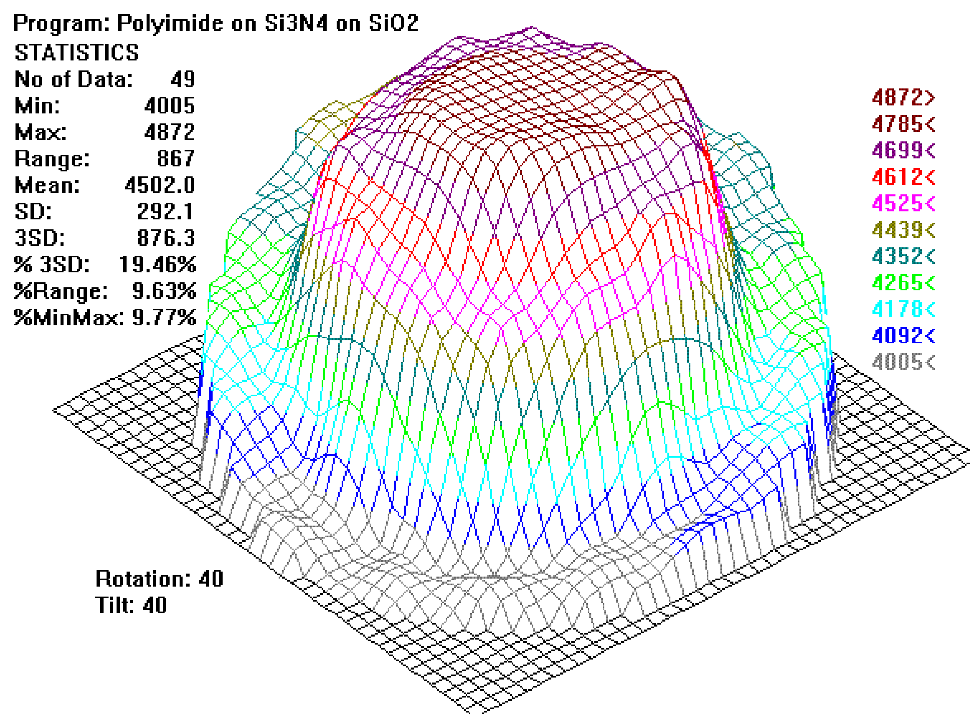


Fig. 3.6: Thickness distribution map after soft bake and hard bake for a typical PI 2611 deposited polyimide layer (measured by reflectometry).

3.5.4. Polyimide hard mask deposition

The O_2 plasma etching of polyimide is not selective with respect to photoresist, both being etched at rates around 1 µm/min in typical conditions. SiO_2 was used as a hard mask polyimide etching, presenting a selectivity between 20:1 and 50:1 at typical etching conditions. At a maximum thickness of 10 µm, a film between 0.3 and 0.5 µm showed to be enough to permit the etching of the whole polyimide thickness without mask damage. The SiO_2 film was deposited in a multi-chamber Pfeifer Spider 600 sputtering system, with a typical deposition rate of 30 nm/min (ambient temperature, 1000 W of plasma power, $5.0 \cdot 10^{-3}$ mbar of pressure, and 33 sccm of argon flow). The thickness of this film was confirmed by using the same recipes on top of test bare silicon wafers having the thickness measured using by a Nanospec 6100 reflectometry measurement tool.

3.5.5. Lithography

Exposition to hexamethyldisilazane (HMDS) at low pressure (1 Torr) and high temperature (150 ^{0}C) was applied to the wafers before the resist deposition. This step ensures good adhesion between the photoresist and the SiO_2 layer.

A positive, high resolution Shipley S1805 resist at 1 µm nominal thickness was used. The reduced thickness permits to obtain a good resolution (between 1.5 and 2 µm) and define fine structures on top of the SiO_2 hard mask.

The resist exposition dose was about 40 mJ/cm^2 (about 4 s with a 10 mW/cm^2 g-line UV-lamp in a MA 150 alignment / exposition tool). The designs were aligned to the preceding levels by using alignment markers located on 2 places in the border of the wafers.

After development the wafers were inspected by optical microscopy and profilometry for correct development, resolution, alignment and resist thickness.

3.5.6. Hard mask definition

The lithographic patters are then transferred to the SiO_2 hard mask by CF_4 plasma etching, performed in a STS inductively coupled plasma etching tool (ICP), at etch rates around 0.25 µm/min (typically 1 – 2 min to etch down a 0.3 – 0.5 µm SiO_2 film). This step is very critical because a visual control of the SiO_2 etching end-point is not possible since it is much thinner than the polyimide film underneath and masked by the resist present on most of the surface. The best way to ensure a complete etch of this film is to adopt enough overetching time (a factor 1.5 to 2) or by using a test wafer with the same base SiO_2 film and lithography to control precisely the etch rate. The second method is preferred since a long overetch can attack the polyimide film with CF_4 species forming polymeric compounds that can be hard to remove and produce side products that can change the polyimide etch step and eventually contaminate the bottom line of the trenches with hard to clean polymeric films. An excessive overetch time can also damage the hard mask since the etch rate of the resist is close to the one of the SiO_2 (about 4-5 minutes of CF_4 plasma can almost strip the resist used as mask for the SiO_2 etch).

3.5.7. Polyimide etch

An O_2 plasma etching of the polyimide in the same ICP tool was performed, just pumping out the chamber and changing the gas and etching conditions. This procedure showed to be more effective in terms of reducing the possibility to adsorb humidity and forming side products by exposing the CF_4 / polyimide products to the ambient atmosphere. A process at 1000 W of plasma power (ICP), 100 W at the substrate RF polarization and 20 sccm of pure O_2 at 5 mbar etches the polyimide anisotropically with rates between 0.75 and 1.0 µm/min. The rates are sensitive to the loading of the process, the lower rate presented when a 100% unprotected polyimide film is etched. For a typical 5% – 10% polyimide surface exposure, typical etch rate values are around 1.0 µm/min.

A typical result of the polyimide etched cavity can be seen in fig. 3.7. The process offers very vertical walls and relatively clean profiles. Sometimes a thin polymeric film can be observed along the walls, which is attributed to undesirable polyimide or CF_4 polymeric etch byproducts. This can be avoided by ensuring a good cleaning of the plasma reactor. It is

recommended to run a SF_6 / O_2 clean step before the first etching process and to check the good cleaning state of the reactor walls periodically.

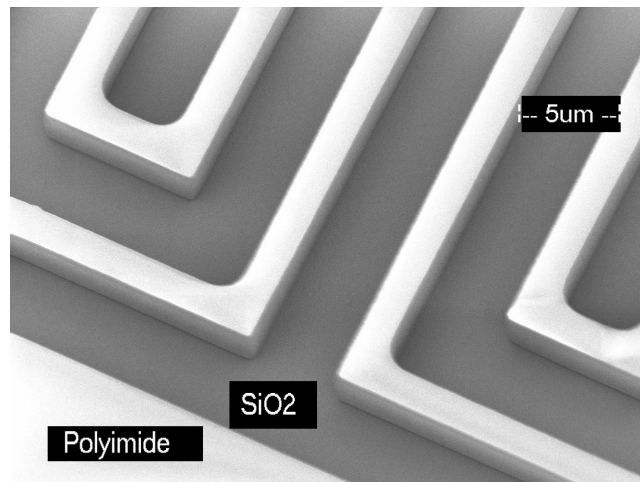


Fig. 3.7: SEM picture of a polyimide plasma-etched mould.

3.5.8. Hard mask removal

Different tests were performed keeping the remaining SiO_2 hard mask after the polyimide etch. The low temperature sputtered oxide can be heavily bombarded by the O_2 plasma etching of the polyimide film, especially during the etching the buried via layer (what practically doubles the etching time). Tests keeping this oxide presented in general adhesion problems, suggesting that the best technique is to etch this film away after its usage as a hard mask. This will ensure a cleaner surface for the tantalum deposition and make the 2 metal layers free of a low quality and higher dielectric constant dielectric.

This film is removed using the same CF_4 plasma etching used to define the hard mask for the polyimide, with the necessary care to do not perform too long overetching in order to not produce CF_4 / polyimide side-products that can also pose problems with respect to the adhesion to the metal.

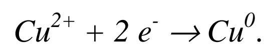
3.5.9. Seed layer deposition

The polyimide mould is treated by an O_2 plasma descum just before loading the wafers into the sputtering tool in order to slightly etch the surface and improve its adhesion with the tantalum layer. 40 nm-tantalum barrier / adhesion layer is deposited, followed by a deposition

of 0.2 μm of copper that will protect the tantalum layer to subsequent oxidation and serve as electroplating seed layer. Independent of the problem related to tantalum oxidation and adhesion, preliminary tests showed that a very thin tantalum layer is not conductive enough to ensure good electroplating conditions (the better the surface conductance is, the better are the electroplating starting conditions).

3.5.10. Copper electroplating

The process is based on the electrochemical reduction of Cu^{2+} ions presented in a $CuSO_4$ + H_2SO_4 + NaCl solution containing organic compounds addictives that improve the step coverage and conductivity of the final film obtained. The main deposition reaction can be described as:



$$Cu^{2+} + 2\,e^{-} \rightarrow Cu^{0}.$$

The electrons for the reaction are provided by the application of an external constant electrical current through a current source, the wafer being at the negative electrode. The reaction is reversible and copper ions are introduced into the solution at the positive-polarized copper electrode side. This kind of deposition is possible only on top of conductive substrates.

The deposition rate is approximately proportional to the current density, being at a nominal value of 1.0 μm/min for a current density of 50 mA/cm^2. Lower current densities provide higher quality films and proved to be less sensitive to the quality and age of the bath additives. The bath presents degeneration in the quality of the result as function of the age and usage of the solution, which can be observed by measuring the resistivity of the obtained films and visually checking the bright and clear aspect of the films after deposition (which becomes opaque when the concentration of addictives and pH needs correction). The measured resistivity was 2.4 μΩ cm using the higher current densities with aged baths. Correct addicted baths working at 25 mA/cm^2 (1.385 A of current for an 84 mm circular diameter deposition surface) give the best resistivity result at 2.0 μΩ cm. The resistivity measurement was made by measuring the sheet resistance by four-point method using a Tencor Omnimap RS-75 prober. The thickness of deposited films by wafer mass variation and by profilometry using a Tencor Alphastep 500 tool. The wafer mass increase was measured in

an analytical balance at a rate of about 49.45 mg/µm for a 84 mm-circular substrate (considering the copper density d_{CU} = 8.920 g/cm^3).

The trench filling capability and the topography of the electroplating process step was monitored by profilometry measurements and SEM observations. Profilometer measurements confirmed a step difference on the electroplated films equal to the thickness of the polyimide trenches. A typical profile is shown in fig. 3.8. The results were obtained by cleaving the wafer along a group of copper lines, what damaged the structures in some degree and made the observation of the details of the cross section more difficult. Further measurements using focused ion beam technique were performed for the final 2 metal-level structures. The electroplating process proved to fill-in trenches as small as 2 µm in width, with a 2:1 aspect ratio, making it suitable to fill-in vias in a dual damascene definition approach. For wide structures having $w > h$, the copper filling is not perfect and a residual step with a high slightly lower than the polyimide thickness is observed. This height difference is attenuated in the CMP step (although not completely removed).

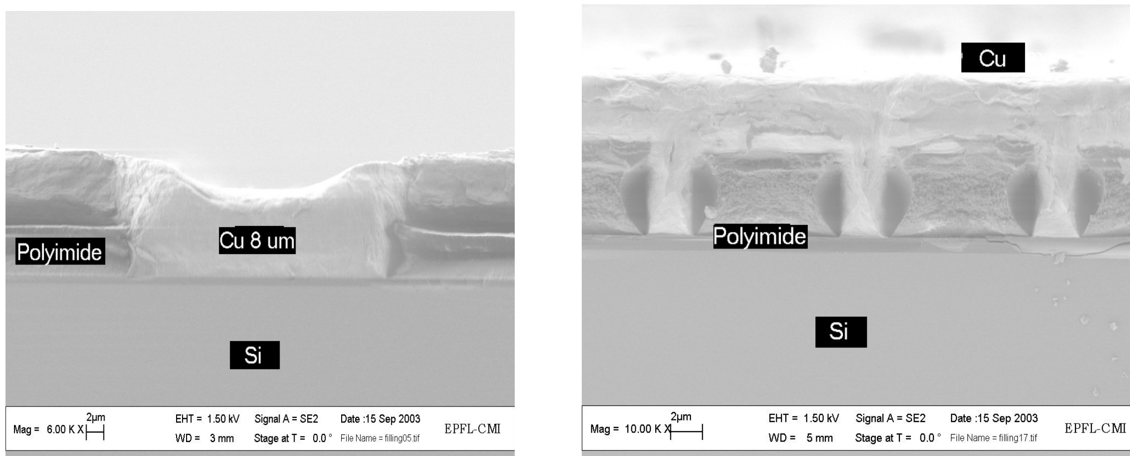


Fig. 3.8: SEM cross section view of a polymer mould filled after the electroplating step. (a) 8 µm-wide 2µm thick structure and (b) 2 µm wide and 4 µm thick structure.

3.5.11. Electroplating uniformity optimization

The current-driven electroplating process is highly sensitive to the uniformity of the current density on the electroplated surface, and the process tends to be inherently non-uniform. An optimization study for the setup used in this thesis is presented in fig. 3.9. In this experiment, different surface coverage fixtures surrounding the border of the wafer were installed in order to reduce the local current density and compensate for the initial +30% in the thickness

observed when no fixture was used. The repetitions having he same colors / symbols were performed at different times and using different wafers in order to check the reproducibility of the results (in the order of ±2.5 % in most of the cases). The depositions were made at 25 mA/cm^2 (deposition rate about 0.5 µm/min giving 8 µm after 16 min of deposition).

The uniformity improvement fixture is a disk made of 1.5 mm thick PVC, placed at a distance of about 1 cm of the wafer surface in order to reduce the current density in the wafer border area. The external diameter of the disk is fixed at 102 mm. Experiments with different values of the internal diameter (30, 52 and 58 mm) and different number of small 1.8 mm diameter holes (72, 60 and no holes at all) were performed. Table 3.1 shows a summary of the 3 studied fixtures.

Fixture	D_{OUT} **(mm)**	D_{IN} **(mm)**	**# of holes / diameter**
#1	102	30	72 / ϕ1,8 mm
#2	102	52	60 / ϕ1,8 mm
#3	102	58	no holes

Table 3.1: Geometrical parameters of the uniformity improvement fixtures studied. D_{OUT} *is the outer disk diameter,* D_{IN} *is the internal disk diameter. Fixture #1 and #2 have small 1.8 mm-diameter small circular holes uniformity distributed over the disc area.*

The best result obtained had a difference between -5 and -10 % in the copper thickness measured at the border of the 100 mm diameter wafer, obtained using a disk of 58 mm of internal diameter and with no holes on its surface (configuration #3 in table 3.1). The maximum deposition diameter is 84 mm and the maximum radii of measurement were limited to 40 mm due to the 5 mm diameter 4-point probing sampling size.

The best results in terms of resistivity were obtained using the recommended organic addictives (which should be corrected periodically due to aging and usage of the bath) and using reduced current densities (25 mA/cm^2 instead of the usual recommended 50 mA/cm^2 setting). 4-point sheet resistance measurement and profilometer thickness measurement established a thin film resistivity of (2.0 ± 0.1) µΩ cm, which is about 16% more than the bulk reference value (1.72 µm cm). This difference is attributed to organic contamination in the films and probably cannot be further improved using electrochemical baths.

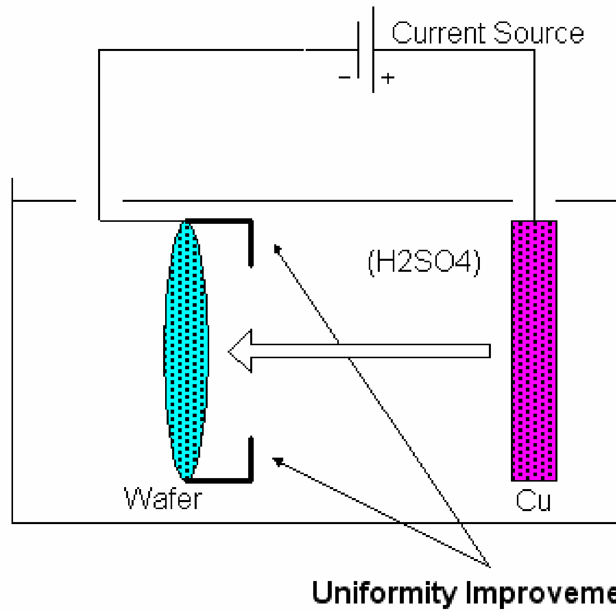


Fig. 3.9: Schematic view of a copper electroplating bath. The wafer border is protected by the uniformity improvement fixture in order to reduce the current density in the wafer border region and increase the overall uniformity across the wafer diameter.

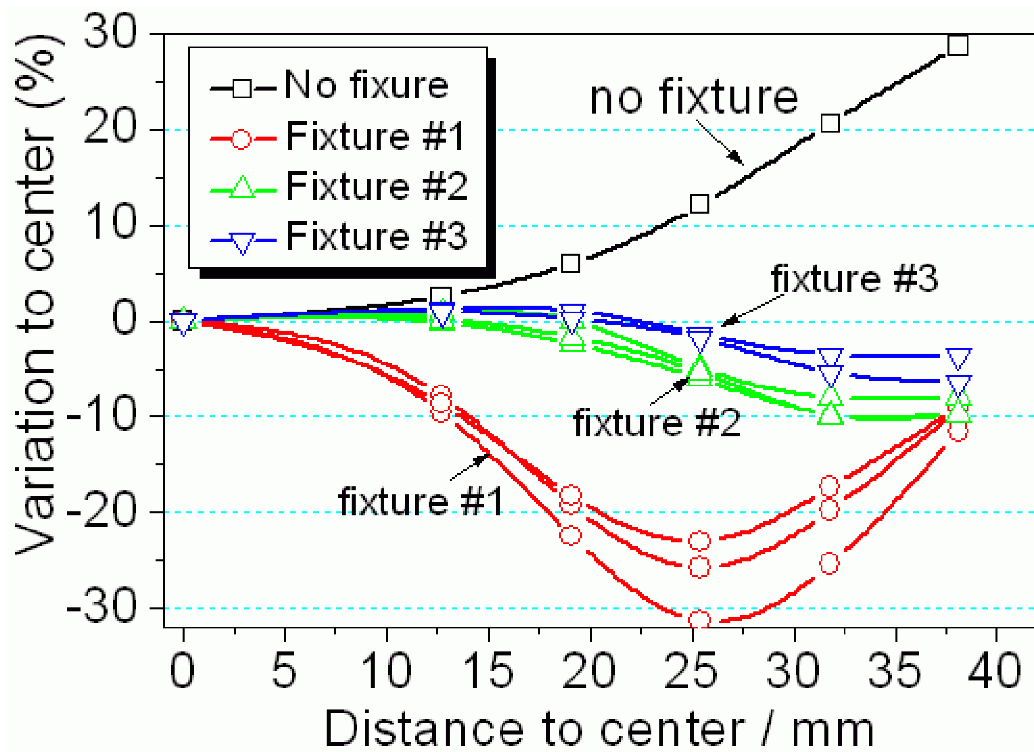


Fig. 3.10: Border to center thickness variation using different current uniformity improvement fixtures of table 3.1.

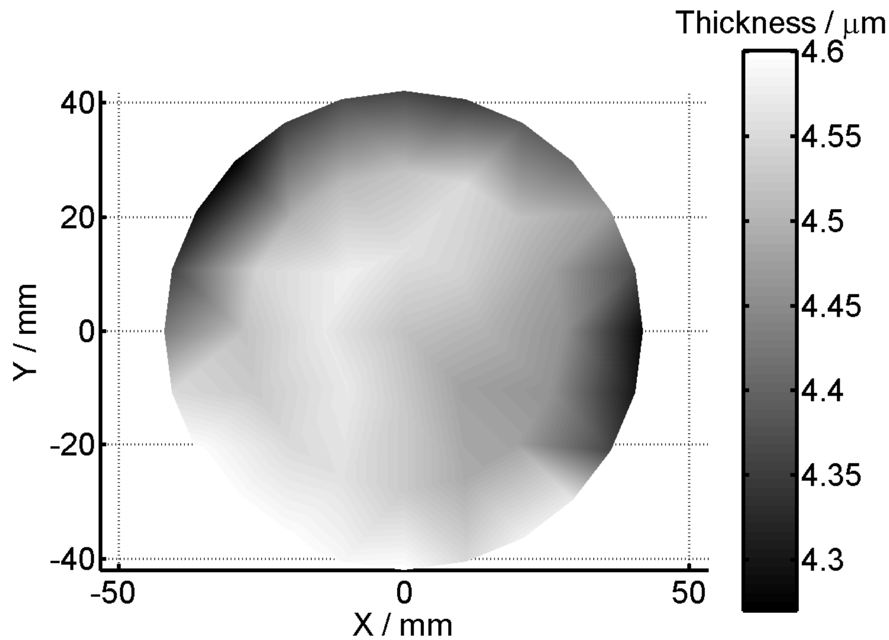


Fig. 3.11: Thickness distribution along the wafer after electroplating of 4.5 μm nominal thickness copper layer (thickness measured by 4-point method resistance measurement using a KLA Tencor Omnimap RS75 setup).

3.5.12. Copper CMP

Fig. 3.12 shows the cross section of copper lines embedded in polyimide after the CMP step. Some dishing in the copper film can be observed, which is at a level of about 0.15 – 0.30 μm below the polyimide one (value measured by profilometry for a group of parallel lines having track width w = 50 μm and track spacing s = 20 μm). Although this value can be considered high for most thin-film CMP process, it is in the range of 10% of the nominal thickness of the copper film, and can be considered acceptable for a high-speed CMP process step operating on thick copper films.

Figure 3.13 shows a picture of a comb-like long perimeter capacitor with 20 x 300 μm-long structures with track width w = 5 μm, track spacing s = 5 μm and thickness t = 5 μm. DC electrical measurements showed a very low leakage current of less than 1 nA for applied voltages up to 5 V, showing that there is no metal residue between the lines after the CMP process, although the copper lines integrity is ensured by the electrical continuity of the central serpentine part (left-up and right-down electrodes).

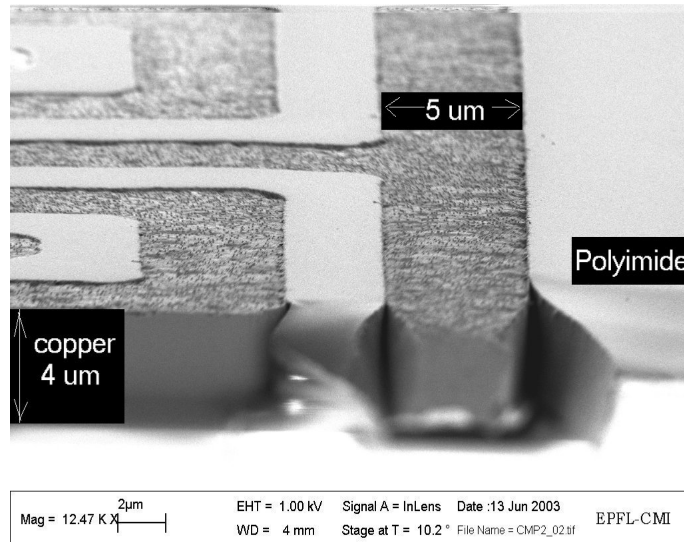


Fig. 3.12: Copper lines embedded in polyimide after CMP process.

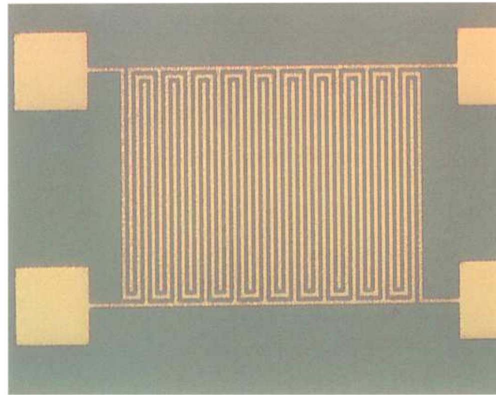


Fig. 3.13: Comb-like serpentine for metal integrity and intermetal leakage current test. The square pads have 100 µm x 100 µm size.

3.5.13. Two metal level process

After validating the fabrication steps needed to produce copper lines embedded into low κ polymer, the process flow was extended to accommodate 2 levels of metal needed to fabricate spiral inductors with an underpass connection. A process with 2 metal levels can also enable the fabrication of shielded RF structures as well as metal-insulator-metal (MIM) capacitors, allowing the fabrication of relatively complex interconnect networks without the need of auxiliary techniques like wire-bonding that can add unpredictable parasitics to the devices. A two metal level process can also provide the necessary interconnection between different components of a passive network, enabling the fabrication of circuits like filters, LC tanks and transmission lines.

Figure 3.14 shows the via etching result in O_2 plasma. Both polyimide layers are covered with a thin oxide layer used as hard mask.

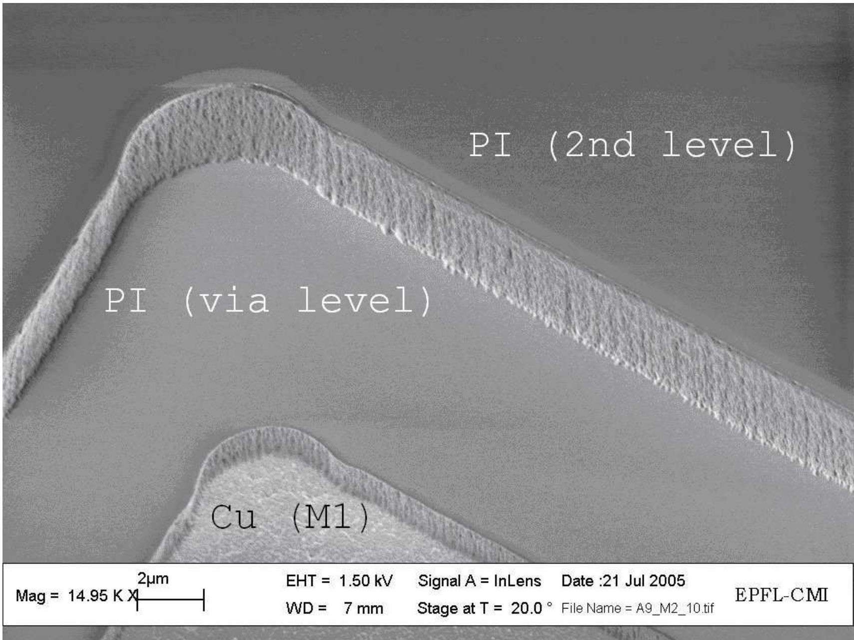


Figure 3.14: SEM picture showing the via and second polyimide level definition openings on top of the firs- level copper layer.

Figure 3.15 shows schematically a passive network that can be fabricated using a 2 metal level structure with a interconnecting via in between.

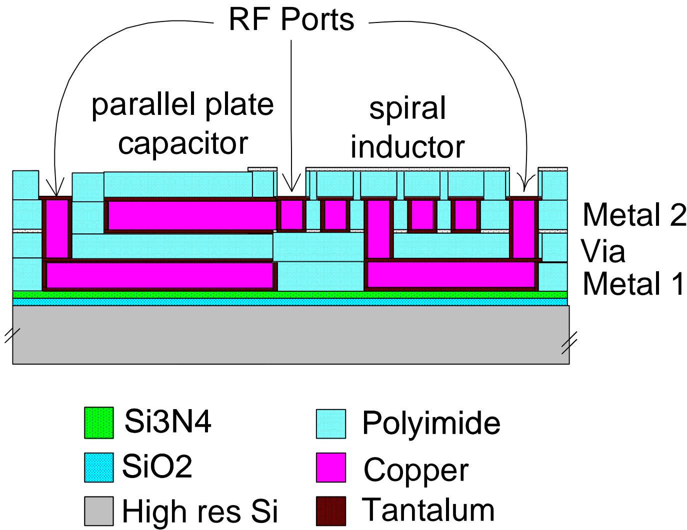


Fig. 3.15: Cross section view of a spiral inductor / MIM capacitor passive network that can be fabricated using a 2 metal level process.

3.6. Process characterization test structures

The next paragraphs present test structures especially designed to characterize the performance of the developed process steps in terms of metal resistivity and contact resistance.

3.6.1. Copper resistivity

To characterize the resistivity of the metal, long serpentine-like 4-point probing resistors with different track width and access to 4, 8, 16 and 20 fingers were designed [Pisani 2005b]. These tests structures have a total resistance given by

$$R_{4P} = \frac{N\rho_{CU} lw}{t} \qquad \text{(eq.3.1)}$$

where N is the number of fingers, l the length of a single finger, w the width of the finger, t the thickness of the metal and ρ_{CU} the resistivity of the copper. The use of 4 points makes the result independent of the contact resistance between the probes and the test structure, which can be bigger than the resistance of the device itself, especially for thick copper films. The resistivity of the copper films produced in this work was always in the range of 2.0 ± 0.2 μΩ cm. This value were confirmed by 4-point measurement over large surface patterns surrounded by thick resist lines fabricated in order to permit direct thickness evaluation by profilometry.

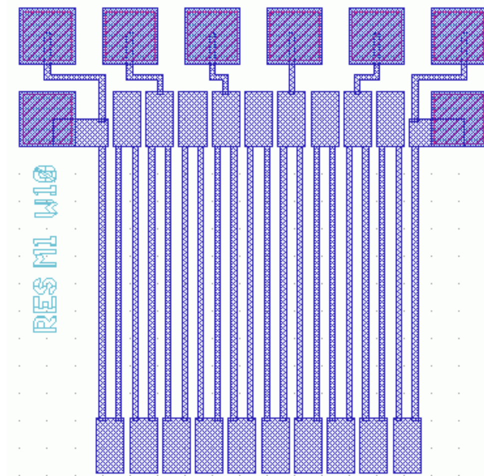


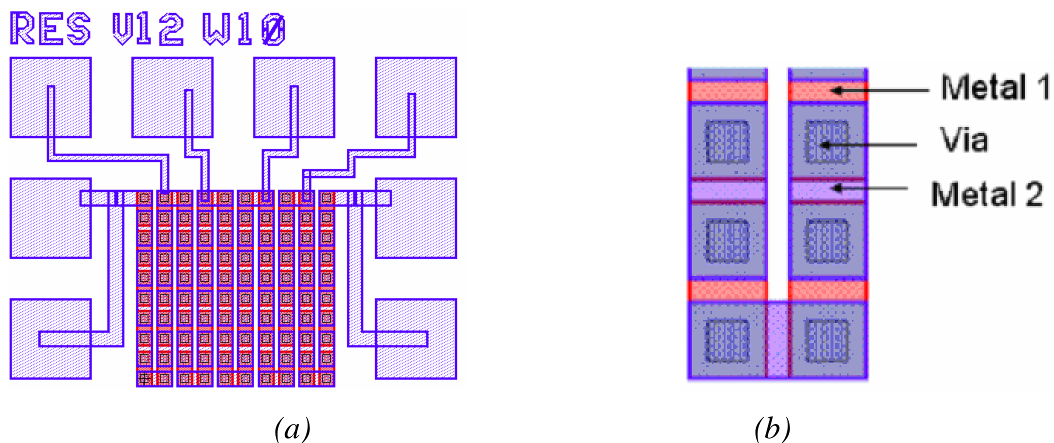
Fig. 3.16: Test structure designed for sheet resistance / metal resistivity characterization by the 4 point method.

3.6.2. Via contact resistance

The major issues in extending the basic process flow to 2 metal levels were the contact resistance at the via level and the additional non-uniformity at the CMP level since the 2nd level of metal is thicker and has extra topography to accommodate the via.

The contact resistance is a very important aspect to be taken into account with integrated spiral inductors. High quality factor devices have less than 1 Ω of series resistance. The contact resistance of a via in between can thus decrease dramatically the performance of this type of device. Typical via resistances in the order of a few mΩ for big vias and no more than 1 Ω for very small ones should be obtained (in the last case a large number of small vias should be put in parallel in order to ensure the lower possible series resistance).

In order to characterize the contact resistance between the 2 metal levels, via-chain structures containing a matrix of 100 vias designed in groups of 20 and having different contact sizes were designed and fabricated [Pisani 2004c, Pisani 2005b, Pisani 2005c]. The basic structure for these matrices of contacts can be seen in fig. 3.18.



(a) *(b)*

Fig. 3.18: (a) Via-chain structure with 100 vias to test the contact resistance between the metal 1 and metal 2 layers (pad size is 100 x 100 μm^2, via size is 10 x 10 μm^2). (b) detail showing the design of the metal 1 / via / metal 2 alternating structure.

Four-point measurements were performed in order to deembed the contact resistance between the DC probes and the structure on the measurement data (2 points are used for current

injection and 2 for voltage sensing, similarly to the technique used to extract the DC conductivity of the metal).

Fig. 3.19 shows the results obtained for a 10 x 10 μm^2 in the first 2 metal-level structure fabricated. A mean resistance per via of more than 2 Ω/via was initially measured, an excessive value that represents more than the typical value of the series resistance of a spiral inductor (in the range of 0.5 to 1 Ω).

Further investigations were conducted by focused ion beam imaging (FIB). Figure 3.20 shows the cross section view of a 10 µm via, with a zoomed view in the interface between the metal 1 and the via structure. The roughness of the interface suggests the presence of a contaminant film between the 2 levels. The probable cause should be the oxidation of the underlying copper layer induced by the plasma etching of the polyimide (fig. 3.1 j-k) or an undesired CF_4 etching side product deposited on this surface. Etching away the underling tantalum protection of metal 1 is done by the same CF_4 plasma step used to remove the remaining SiO_2 hard mask existing on top of metal 2 and via polyimide mould (fig. 3.1 k). The main hypothesis is that it is originated from a polymeric side product issued from the polyimide / O_2 / CF_4 treatment that cannot be completely removed in the O_2 descum step performed before the 2nd tantalum liner deposition (l). In fact, this step should not be extended for too long time in order to avoid excessive loss of the polyimide and the oxidation of the underlining copper, which will also end up resulting in a bad contact resistance.

The best results were obtained by a 30 s immersion of the copper exposed structures into a 5% H_2SO_4 solution diluted in water that softly etches the surface of the copper. This step is followed by the O_2 plasma surface activation of the polyimide and by immediately loading the wafers into the tantalum sputtering tool in order to avoid subsequent oxidation of the underlying copper film.

Figure 3.21 shows the final metal 1 / via / metal 2 stack image obtained by FIB analysis. Metal 1 is 1.5 µm, via is 3 µm and metal 2 is 5 µm-thick. The interface between the 2 metal layers is clear, which is confirmed by the contact resistance measurement showed in table 3.2. The maximum resistance per via is in the order of a few mΩ / via, which should not affect the

RF performance of high Q inductors (having a minimum series resistance in the 300 – 500 mΩ range).

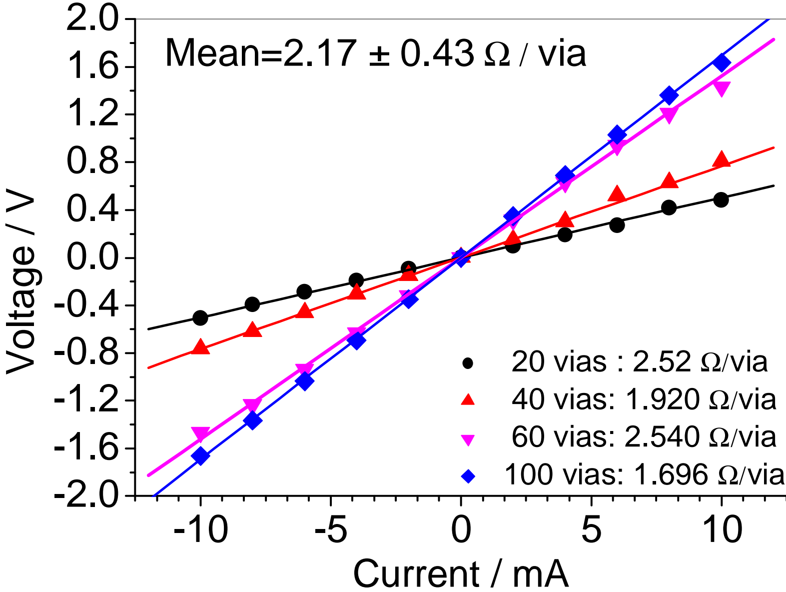


Fig. 3.19: Initial via resistance measurement for the 10 x 10 μm² via chain structure.

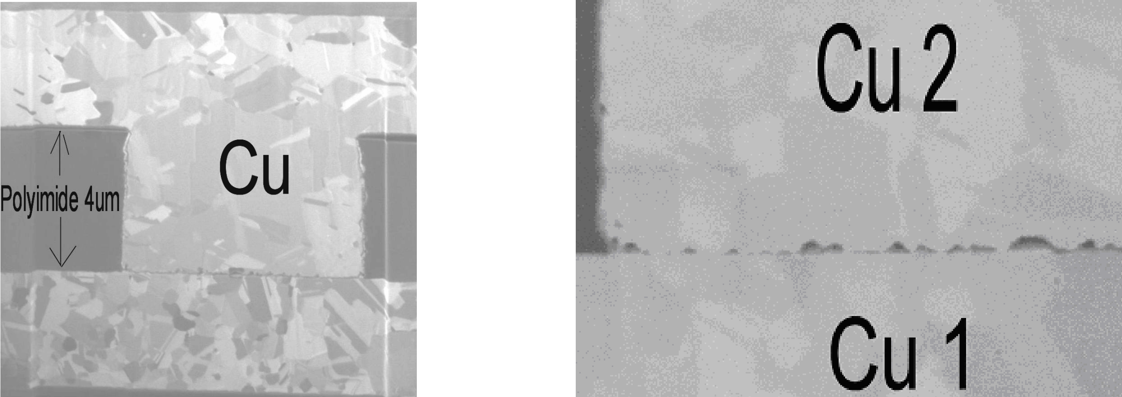


Fig. 3.20: FIB cross section view of the metal 1 / via / metal 2 structure, with a detailed view on the roughness of the metal 1 / via interface.

Via size (μm)	Number of vias	Resistance (mΩ)	Uncertainty (mΩ)	Resistance/Via (mΩ/via)	Mean ± dev (mΩ / via)
10	20	764	14	38.2	25 ± 11
10	40	860	17	21.5	
10	60	1014	15	16.9	
10	80	1145	14	14.21	
10	100	3496	16	34.96	
40	20	84	22	4.2	3.66 ± 0.31
40	40	141	26	3.52	
40	60	210	21	3.5	
40	80	274.5	28	3.43	
40	100	364.1	55	3.64	

Table 3.2: Via contact resistance for 10 x 10 μm^2 and 40 x 40 μm^2 structures.

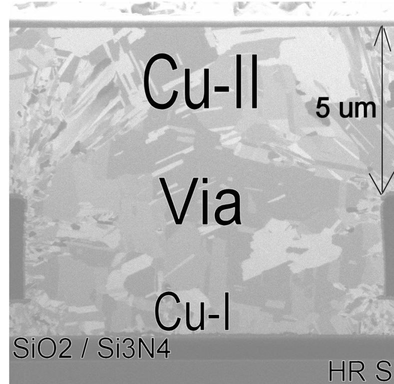


Fig. 3.21: FIB cross sectional view of the metal 1 / via / metal 2 stacked structure after bottom line cleaning optimization.

FIB analysis showed also that the interface copper / tantalum / polyimide is clean and smooth, suggesting that no major problems with this stack of materials are presented.

3.7. Fabricated devices and RF performances

Figure 3.22 shows some spiral inductor designs fabricated using the developed process steps. These devices have surrounding RF pads for the electrical characterization. Fixed capacitors and various test structures were also designed and fabricated.

RF electrical characterization of the fabricated inductors was performed using full 2-port S-parameter measurements in a microprober equipped with an HP 8719D vector network analyzer (VNA) and Cascade Microtech RF ground-signal-ground probes (GSG). The RF setup is calibrated in the range of frequencies from 0.05 to 13.51 GHz using an *Impedance*

Standard Substrate (ISS) with SOLT references (short-circuit, open-circuit, load and thru). The maximum power level used to test the devices was limited to 0 dBm. The data is saved by a computer program written in Matlab that takes the data through the GPIB interface bus of the VNA.

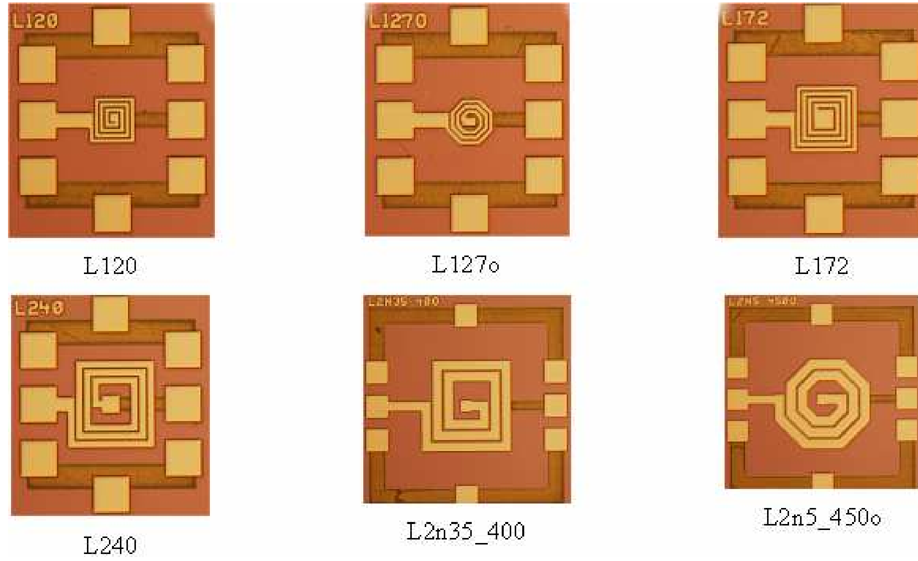


Fig. 3.22: Examples of spiral inductors fabricated using the developed process steps.

Measured S-parameter data are then transformed into Y-parameters and inductance and quality factor of the devices are calculated from the equivalent 1-port impedance of the device as [Yue 2000]:

$$L = \frac{imag\left(\frac{1}{y_{11}}\right)}{2\pi f} \quad \text{(eq.3.2)},$$

and

$$Q = \frac{imag\left(\frac{1}{y_{11}}\right)}{real\left(\frac{1}{y_{11}}\right)} \quad \text{(eq.3.3)},$$

where L is the inductance, Q is the quality factor, f is the measurement frequency and $1 / y_{11}$ is the equivalent complex impedance of port 1 when port 2 is connected to the ground.

These formulae are commonly used for isolated inductors (not connected to other resonating components), working below the self-resonant frequency. The resonant frequency is defined when the expression for Q (eq. 3.3) goes to 0.

It should be noted that, even if one port parameters are more frequently used to characterize the device, the 2-port measurement gives more accurate results in order to extract the inductor parameters [Aguilera 2002b]. Non-linear least squares fitting routines were used to fit the equivalent circuit model of the device to the measured S-parameter data [Pisani 2004b, Pisani 2005].

Fig. 3.23 shows the measured and equivalent fitted RLC model S-parameter data for a 2.5 nH inductor optimized to work in a 2.45 GHz VCO (octagonal spiral inductor with D_{OUT} = 450 μm, n = 2.5 turns, w = 45 μm and s = 10 μm). The thick noisy line represents the measured S-parameter data. Guess and fitted lines are thinner and superimposed in these graphs. The guessed lines results are obtained by direct calculation of the component values from Y parameters and the equivalent π circuit model of fig. 2.7. The equivalent circuit model fits well both the moduli and phase of the measured data up to the resonant frequency. This device has a peak quality factor of 38 at a frequency of 2.6 GHz and a self-resonant frequency of 10.2 GHz. The quality factor exceeds 20 over a wide frequency range spawning from 1 to 6 GHz, making a single device usable in different frequency standards (GSM, IMS, UMTS, Bluetooth and WLAN) without the need of having multiple components to fit into different applications.

Table 3.3 shows the extracted equivalent circuit parameters for this device. A calculation using eq. 2.40, although very approximate, suggests that the substrate resistance should be in the order of several kΩ (σ_{SUB} = 0.0125 S/m, t_{SUB} = 525 μm, $G_{SUB}'' = \sigma_{SUB} / t_{SUB}$ = 23.81 S/m^2, l = 2500 μm, w = 45 μm, R_{SUB} ~ 700 kΩ), although the extracted value is in the order of hundreds of Ω. A conductive layer resulted from charge accumulation during the thermal oxidation process of the high resistivity silicon wafer can be the cause of this discrepancy [Wu 1999]. This layer can greatly reduce the resistivity of the silicon on the interface between

the oxide and the high resistivity silicon. The presence of this higher conductivity thin layer near the surface can be highly detrimental for the quality factor of RF passive devices built on top of silicon substrates. Solutions to this issue based on a deposition of relatively low quality amorphous silicon can alleviate this issue by providing recombination centers that can help to keep the local resistivity of the silicon high [Gamble 1999, Jansman 2003, Rong 2004].

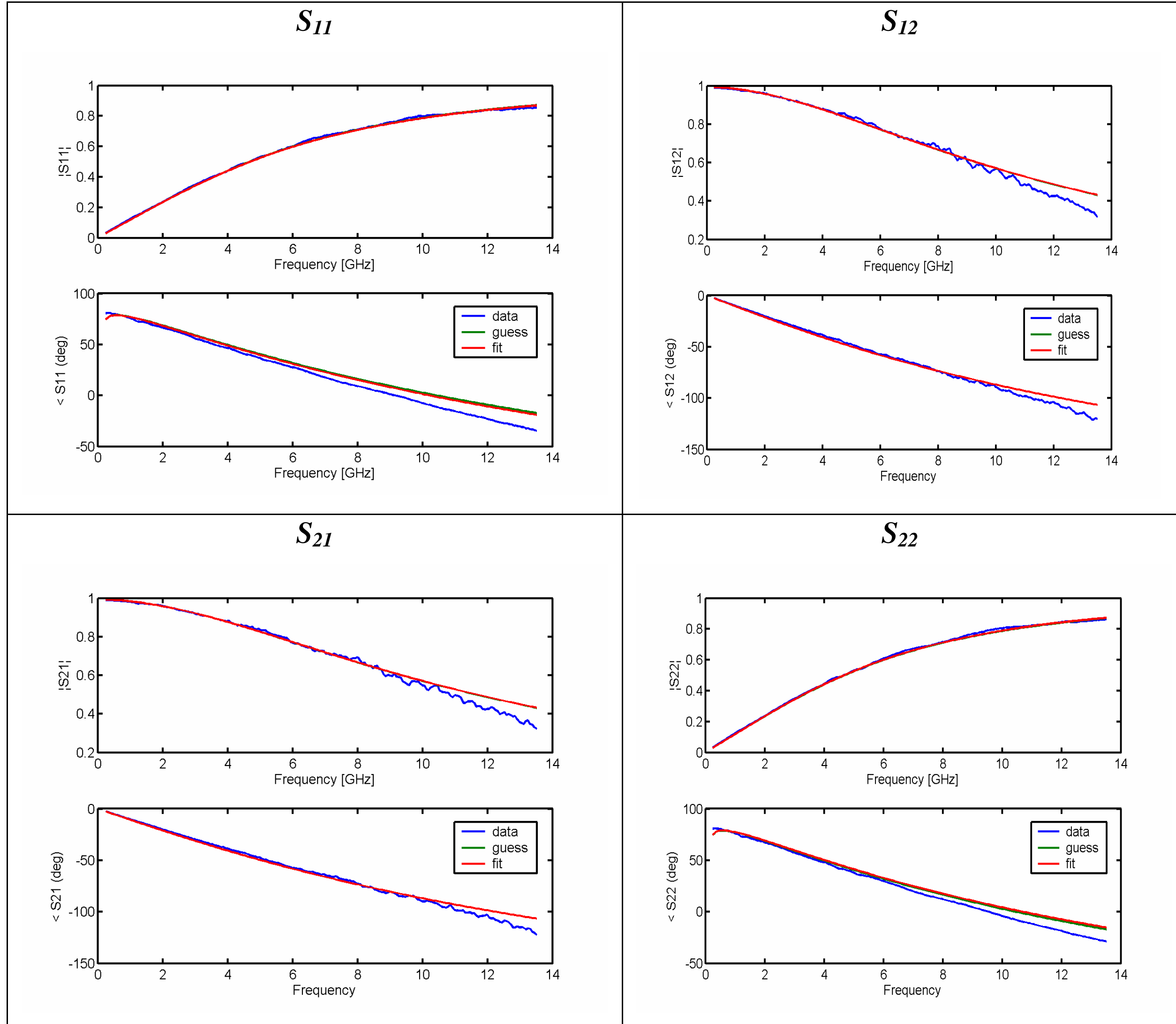


Fig. 3.23: Four complex S parameter inductor measured data (in blue, thick, noisy line)) and S-parameter data for the equivalent circuit fit (red, smooth). Fit was performed between 0.05 and 10 GHz and is representative for the device only below its self-resonant frequency.

Table 3.4 shows the extracted electrical performance of different prototype inductors fabricated using the thick Cu / polyimide technology module. The self-resonant frequency SRF is defined as the frequency where the eq. 3.2 goes to zero. Beyond this frequency, the device will behave as a capacitor. Different frequency bandwidths are defined as function of a minimum desired quality factor. For optimized devices, self-resonance frequencies above 8 –

10 GHz were demonstrated. Quality factors in excess of 20 over a wide frequency range were also demonstrated (typically from 2 to 6 GHz), enabling the operation of a single device covering different frequency standards (for example in a GSM or WLAN module). These performances are in the current state-of-the-art for inductors built on top of silicon wafers [Carchon 2004].

$L_S = 2.45$ nH $R_S = 0.67\ \Omega$ $C_P = 0$ fF $C_{INS1} = C_{INS2} = 110$ fF $R_{SUB1} = R_{SUB2} = 115\ \Omega$ $C_{SUB1} = C_{SUB2} = 500$ fF Peak quality factor: $Q_{MAX} = 38$ @ 2.60 GHz Self-resonant frequency: $f_{RES} = 10.2$ GHz

Table 3.3: Fitted equivalent circuit model and extrapolated performance for the 2.5 nH / 2.45 GHz inductor.

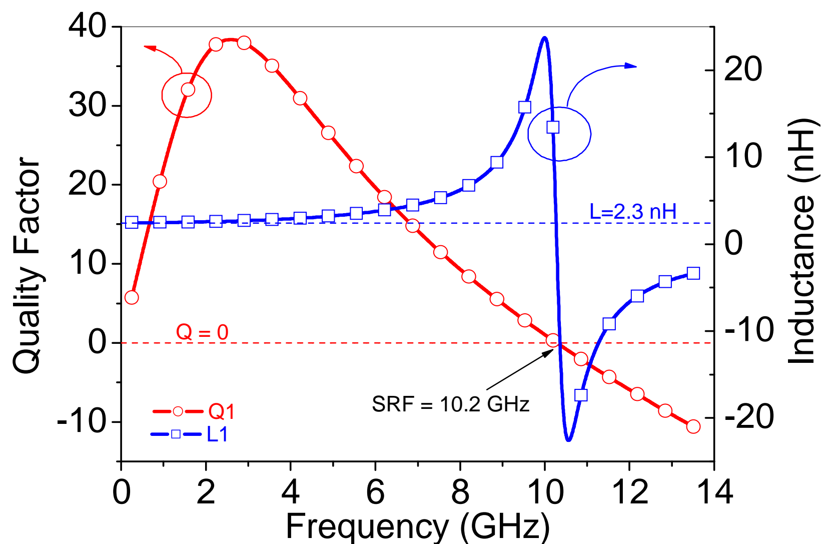


Fig. 3.24: Equivalent RLC model inductance (eq. 3.1) and quality factor (eq. 3.2).

Fixed capacitors like the one showed in fig. 3.25 were also fabricated measured.

Geometry	Device	L (nH) @ 1 GHz	Qmax *	f(Qmax) GHz	SRF GHz	BW (Q>5) f1 (GHz)	f2 (GHz)	BW (Q>10) f1 (GHz)	f2 (GHz)	BW (Q>20) f1 (GHz)	f2 (GHz)
Optimized	**L1n4_400**	1.66	25	4.0	13.0	-	-	0.5	10.0	2.0	6.0
	L1n4_400o	1.65	25	4.0	13.5	-	-	0.5	11.0	2.0	6.0
	L23n1_450	2.45	25	4.0	9.5	-	-	0.5	8.0	1.8	6.0
	L2n1_450	2.23	25	4.0	10.0	-	-	0.5	8.5	1.8	6.0
	L2n1_500o	2.34	25	4.0	10.0	-	-	0.5	8.5	1.8	6.0
	L2n5_450o	2.50	25	4.0	9.5	-	-	0.5	8.5	1.8	6.0
	L2n35_400	9.83	20	1.5	4.0	-	-	0.5	3.0	-	-
	L460_fin	2.52	25	4.0	9.0	-	-	0.5	7.5	1.8	6.0
	L460_fout	2.82	25	2.5	8.5	-	-	0.5	7.0	1.8	6.0
Non-optimized	**L120**	0.90	10	6.0	-	1.0	12.0	-	-	-	-
	L127o**	0.80	10	6.0	-	1.0	-	-	-	-	-
	L172	1.93	12	6.0	13.5	0.5	11.0	4.0	8.0	-	-
	L240	1.98	20	6.0	12.0	-	-	1.0	9.5	-	-
	L400	5.22	15	3.0	7.0	-	-	1.0	5.0	-	-
	L450	4.26	13	2.5	6.5	0.3	5.7	1.0	4.5	-	-
	L450o	5.09	18	3.0	7.0	0.5	6.0	1.0	5.5	-	-
	L488o	4.19	20	2.5	7.0	-	-	0.5	5.5	-	-
	Lc10n	6.31	15	3.0	6.5	-	-	0.8	5.5	-	-
	Lc30n	16.60	18	1.5	3.5	-	-	0.5	2.5	-	-
	Lc50n	29.80	13	1.0	3.0	-	-	0.5	2.0	-	-
	Lf_0n6_200o**	0.49	20	6.0	-	-	-	1.8	7.5	-	-
	Lf_0n6_22o**	0.55	20	6.0	-	-	-	0.5	7.5	-	-

Table 3.4: Extracted electrical performance of various prototype inductors fabricated with the thick Cu / polyimide module.

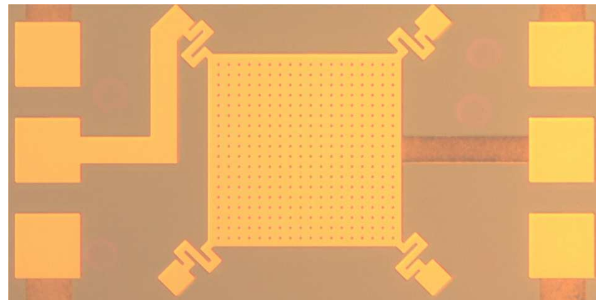


Fig. 3.25: 0.77 pF, 300 x 300 μm^2 squared fixed capacitor with RF pads for full 2-port RF measurement.

In direct analogy with the definitions used for inductors, effective capacitance *C* and quality factor *Q* below the self resonant frequency are defined as function of the equivalent 1-port impedance $1/y_{11}$ as:

$$C_1 = \frac{-1}{2\pi f . imag(1/y_{11})} \qquad \text{(eq.3.4),}$$

$$Q_1 = \frac{-imag(1/y_{11})}{real(1/y_{11})} \qquad \text{(eq.3.5).}$$

A peak quality factor of 40 with a resonant frequency of 6.5 GHz were demonstrated with a design that has not been fully optimized using electromagnetic simulations (fig. 3.26 and 3.27), suggesting that the developed fabrication technology can also be used to fabricated other types of high Q devices.

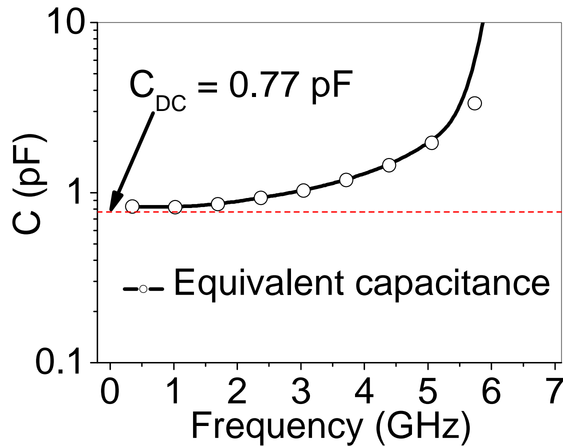


Fig. 3.26: Equivalent capacitance of the 0.77-pF squared MIM capacitor (eq. 3.4).

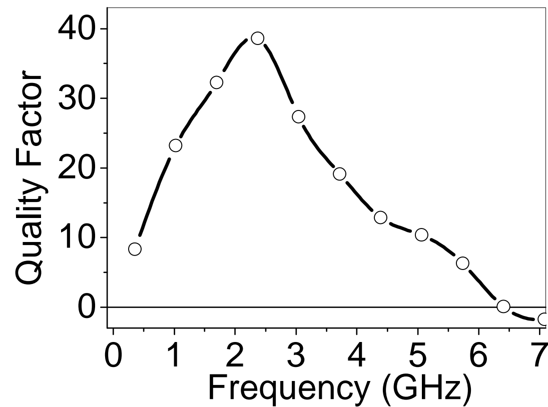


Figure 3.27: Quality factor of the 0.77-pF squared MIM capacitor (eq. 3.5).

3.8. Other process development based on this process module

The developed process steps were used as base technological platform for the development of other RF MEMS fabrication processes.

Fig. 3.28 shows the concept adopted to fabricate high Q thick copper inductors and out-of-plane actuators on top of aluminum membrane RF MEMS platform [Fritschi 2004, Fritschi 2005]. The use of thick copper layers enables multiple advantages for building high electrostatic force laterally actuated variable MEMS capacitors co-integrated with high Q inductors [Mehdaoui 2005, Mehdaoui 2007].

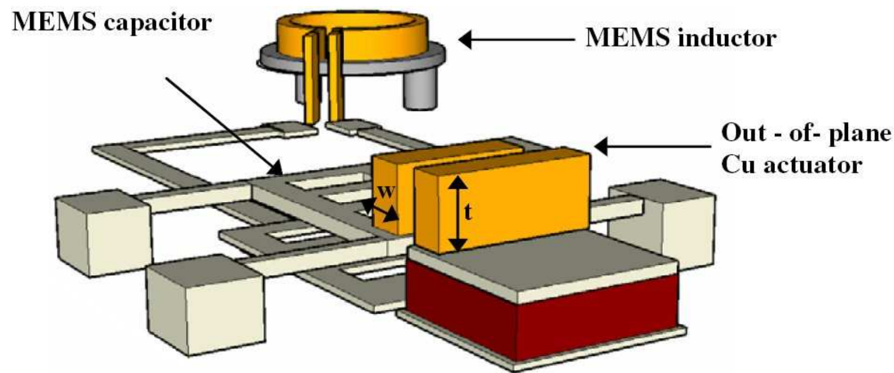


Fig. 3.28: Concept adopted for a mixed aluminum / thick copper MEMS platform with high Q inductors co-integrated with variable capacitors [Mehdaoui 2005, Mehdaoui 2007].

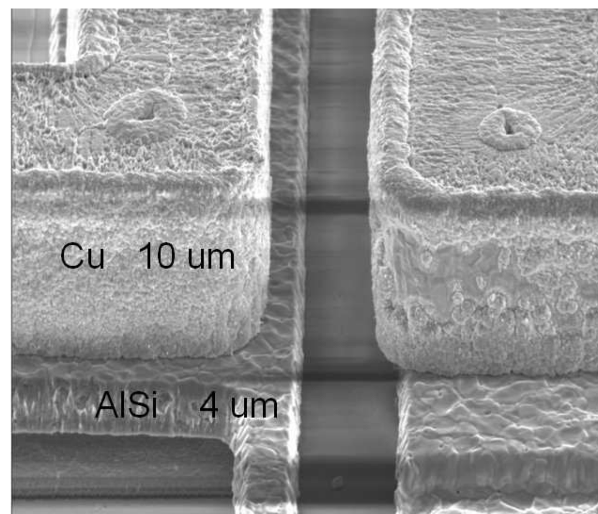


Fig. 3.29: SEM picture showing the thick copper layer on the out-of-plane actuator built on top of a 4 μm-thick released aluminum membrane variable capacitor [Mehdaoui 2007].

3.9. Filter applications using high Q passive devices

The availability of high Q passive devices make possible to associate a number of them to fabricate filters and tuning matching network circuits. A complete analysis on the filter synthesis using discrete components with finite quality factor is beyond the scope of this thesis and is well explained in the literature [Zverev 1967, Helszajn 1994].

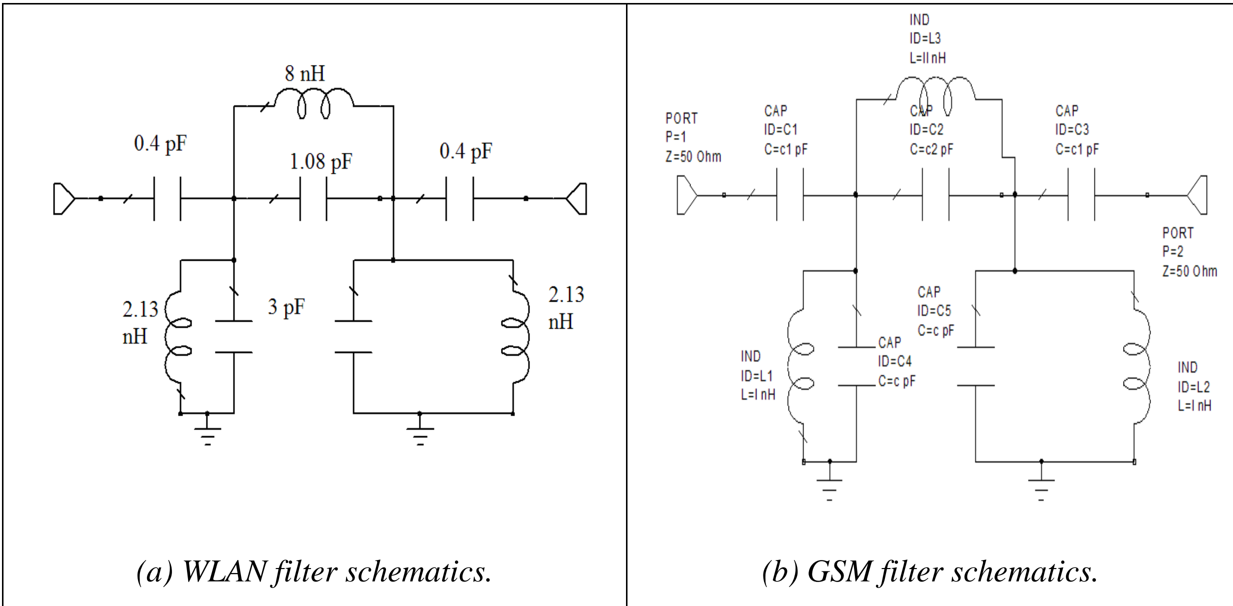
Two LC bandpass filters were designed to initially operate in the GSM (1.8 MHz) and WLAN (5.2 GHz) standards.

These solutions can be designed using LC passive components with moderate levels of losses, solutions which were not possible to date due to the limited performance of these passives due to losses (low quality factors) and low self-resonant frequencies (high parasitic capacitances).

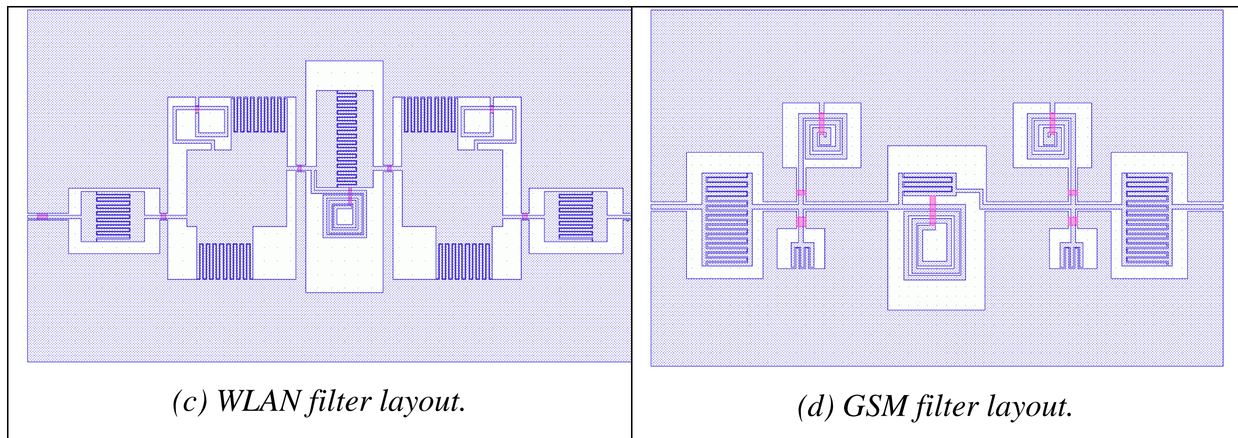
The classical Butterworth and Chebyshev filter synthesis presented in the literature [Chen 1995] usually do not take into account the finite quality factor of the devices. The limited quality factor strongly degenerate the responses introducing both insertion losses (the level of the signal that passes in the pass band) and reduction in the selectivity (the distance between the gain in the pass band and outside it).

One way of including these effects in the response calculation is by replacing pure inductance and capacitance by complex counterparts defined as $L^* = L\cdot(1-j/Q_S)$ and $C^* = C\cdot(1-j/Q_P)$, where $Q_S = \omega L/R_S$ is the series quality factor of the inductors and $Q_P = \omega R_P C$ is the parallel quality factor of the capacitors. These substitutions are valuable when using synthesis tools with natural extensions to complex arithmetic, e.g. like Matlab.

Figure 3.30 shows the schematics and layout of 2 planar LC band pass filters designed for the GHz range (designs kindly provided by IMT Bucharest in the frame of the European Research project Amicom).



(a) WLAN filter schematics. *(b) GSM filter schematics.*



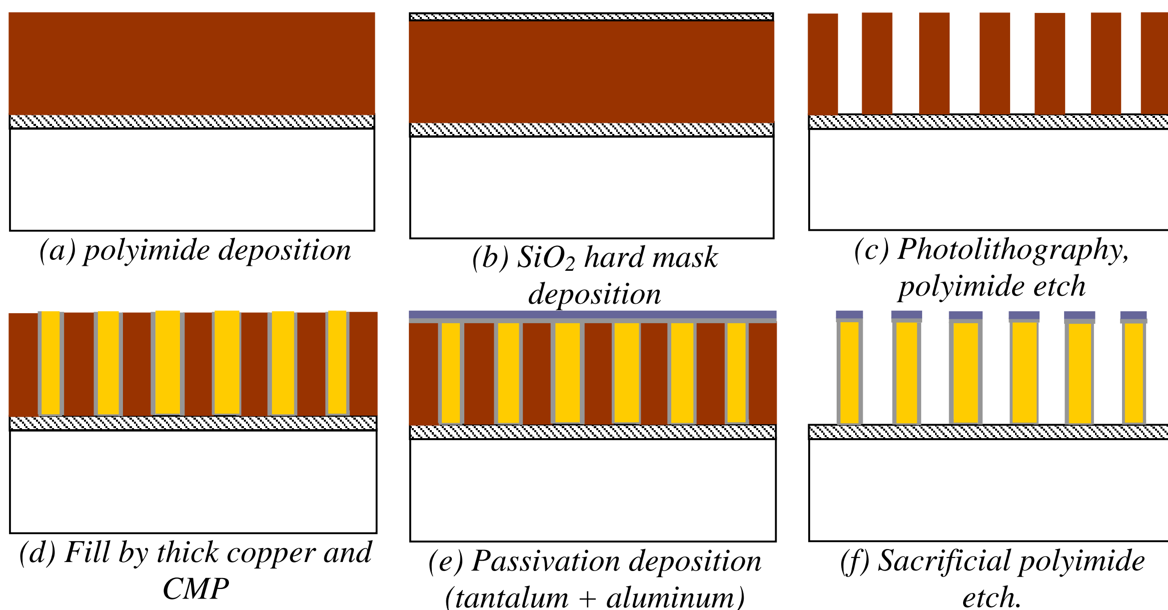
(c) WLAN filter layout.

(d) GSM filter layout.

Fig. 3.30: Schematics and layout for the designed filter circuits: WLAN (a and c) and GSM (b and d).

These designs were fabricated using a simple process flow using 1 level of thick high conductive metal (10 µm electroplated and CMP-polished copper covered by tantalum) on top of high resistivity silicon (ρ = 8 kΩ cm, 525 ± 25 µm thick, ε_R = 11.9), show in fig. 3.31.

Polyimide is spin on and dry etched by O_2 plasma using SiO_2 hard mask to serve as mould for a CMP process, like in the process flow described in chapters 4 and 5. The devices are covered by a layer of 100 nm of tantalum (diffusion barrier and adhesion promotion) and 200 nm of aluminum (adhesion layer for the subsequent bonding). The air bridges are formed by gold write bonding (70 µm diameter wire soldered in a ball bonder tool).



(a) polyimide deposition

(b) SiO_2 hard mask deposition

(c) Photolithography, polyimide etch

(d) Fill by thick copper and CMP

(e) Passivation deposition (tantalum + aluminum)

(f) Sacrificial polyimide etch.

Fig. 3.31: Process flow used to fabricate the filter demonstrator.

Figure 3.32 shows SEM pictures of the fabricated devices, with a closed view near the air bridges of one of the spiral inductors.

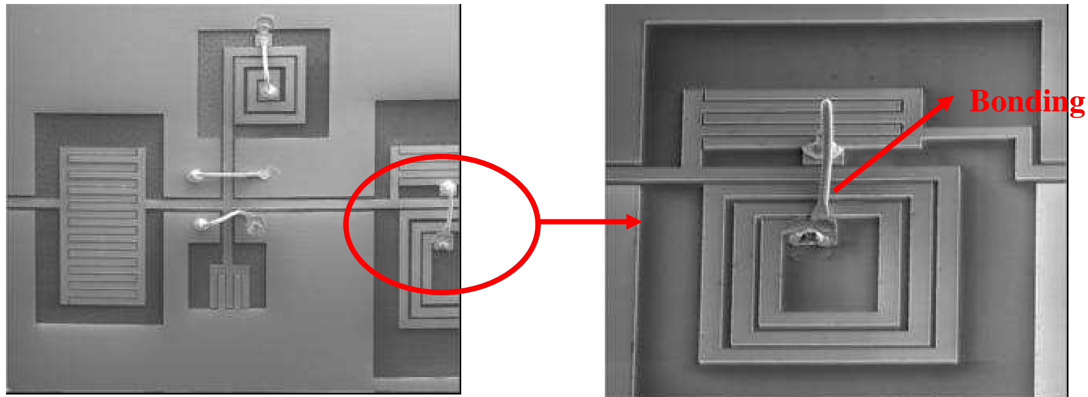


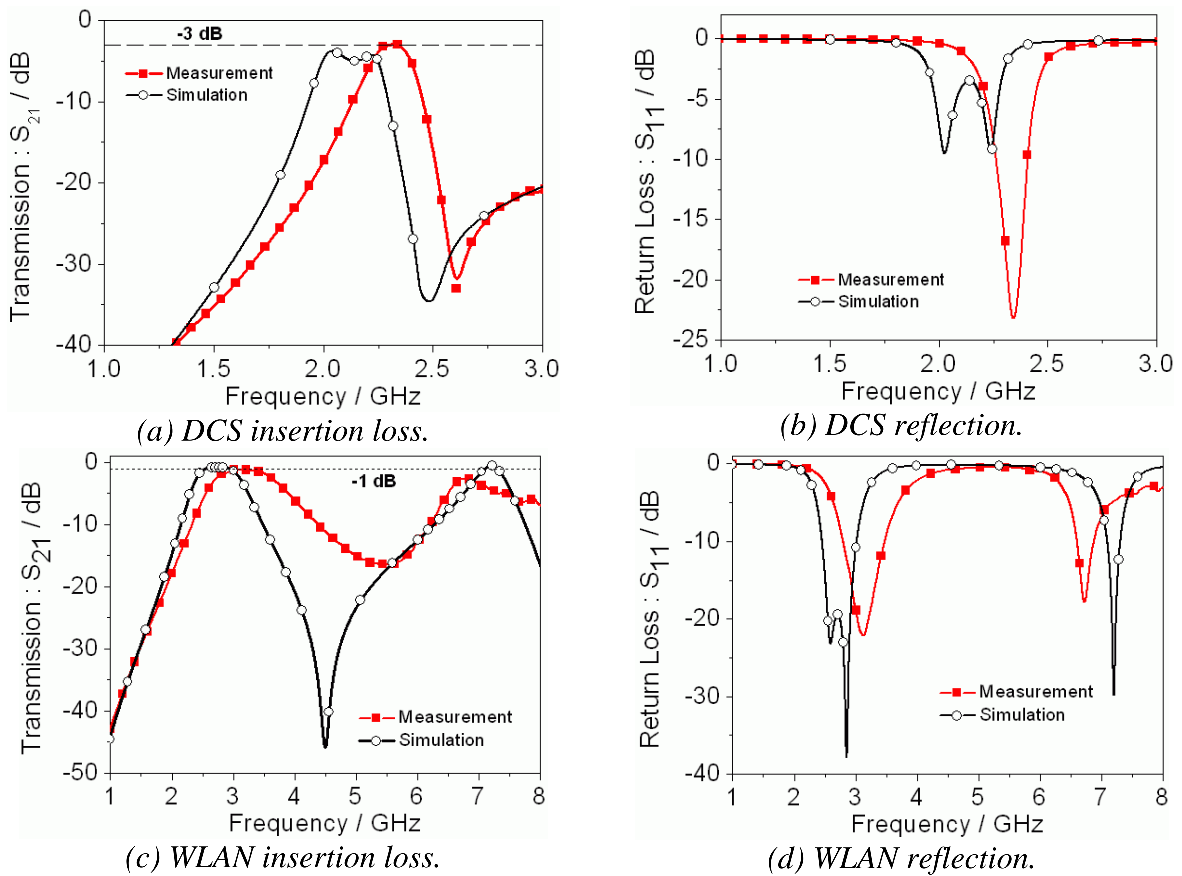
Fig. 3.32: SEM pictures of the fabricated filters, showing in detail the air bridge connection of one of the spiral inductors.

The 2-port S-parameter response of these filters was measured using an HP 8719D vector network analyzer calibrated by the SOLT method to make measurements in the range of 0.05 to 6 GHz. There results are shown in figure 3.33.

The response of these filters did not match the prediction using the lumped-element component values of fig. 3.30a and 3.30b (1.8 GHz for the central frequency of the GSM filter and 5.2 GHz for the central frequency of the for the WLAN one). The response of these filters was predicted using simple analytical formulae for each lumped component and by combining the impedances and admittances of these components in the ABCD matrix response, without considering any mutual coupling and transmission line effects between the elements. The expected responses were also confirmed by SPICE circuit simulations.

In order to correctly predict the performance of these devices, full wave electromagnetic simulations using ADS momentum were performed [Agilent 2005]. As the circuits are relatively large in size and number of components, the simulation options had to be set for very coarse meshing in order to be capable of simulating the design on a 2 GB-RAM PC computer. For these designs in particular, one cannot have a fine mesh around the edges of the conductors, which affect considerably the accuracy of the simulations. This shows one of the main drawbacks of full wave simulations when the size of the circuit and number of

components become relatively large. Although further development using electromagnetic simulations and more accurate prediction of the capacitances (especially the ones of the interdigital capacitor, which are strongly affected by the fabrication tolerances) need to be carried out, the fabricated circuits demonstrate very promising performances in terms of insertion losses (1.2 dB) and by exhibiting rejection superior to 20 dB out of the pass band, being capable to fulfill the filtering specifications of the GSM, UMTS and WLAN standards. The measured performance is similar to the one reported using high Q inductor fabricated by thick metal modules based on the low temperature co-fired ceramic (LTCC) [Choi 2007].



(a) DCS insertion loss. *(b) DCS reflection.*

(c) WLAN insertion loss. *(d) WLAN reflection.*

Fig. 3.33: RF measurements of performances of the fabricated filters.

	WLAN (5.2 GHz)	GSM (1.8 GHz)
Center frequency	3.2 GHz	2.2 GHz
Bandwidth	1.0 GHz	0.3 GHz
Insertion loss	-1.2 dB	-5.6 dB
Return loss	-21 dB	-11.5 dB

Table 3.5: Measured performance of the fabricated filters.

In the chapter 4, further fabrication developments to build high Q inductors and RF MEMS packaging based on thick-copper metallization and CMP will be also presented.

Summary

This chapter discussed the experimental approach developed and used to fabricate the devices presented in this thesis. The process is inspired by the dual damascene process used to fabricate modern IC interconnects, and was especially adapted to produce thick metal layers, with thickness between 1 to 10 μm. Basic aspects like adhesion improvement, the use of tantalum as anti-diffusion barrier, the optimization of the electroplating bath and the dry plasma etching of the polyimide mould were addressed. The best electroplating results were obtained using a standard organic added bath working at 25 mA/cm^2 and protecting the wafer border with a ring, that reduced the non-uniformity from 30% to 10%. The measured resistivity of the copper films was 2.0 ± 0.1 μm cm, about 15% more than the bulk reference value (1.72 μΩ cm). The best CMP results were obtained using both low working pressures (WP about 4 psi) and speeds (about 30 / 35 rpm for the plate and head speeds). The thickness of the copper layer was monitored by mass measurements (49 mg of copper per μm removed on 4 inches wafers) and by 4-point measurements. Test structures were developed to qualify the 2 metal level process, which exhibited good contact resistance after cleaning optimization and low leakage current for comb-like capacitor leakage measurements.

This chapter presented one application of high Q passive devices built on top of high resistivity substrates and using thick metal definition steps developed in this thesis. Although the response of the filters did not fully matched the EM simulations, insertion losses as low as 1.2 dB were demonstrated, suggesting that this technology can provide devices for multi-gigahertz operation circuits, although further development is still needed in order to better synthesize and predict the response of these devices.

The original contributions of this thesis for the advancement of the state-of-the art in the fabrication techniques are related to the establishment of a new CMP process capable to tackle with films much thicker than the ones traditionally used in microelectronic interconnects and by the introduction of a low thermal budget thick metal MEMS fabrication process compatible of the current trends in high-speed interconnects fabrication (use of copper and low κ dielectrics). This process flow closes a gap of compatibility between CMOS and MEMS processing, enabling the fabrication of thick-metal MEMS using the same

technology framework available for the fabrication of high-speed interconnects. This technology platform permitted to fabricate devices with RF performances in the current state-of-the art in terms of both peak quality factor and frequency of operation, exhibiting broadband behavior (Q > 10 in the 1 to 6 GHz range), which enables the use of a single device in different operating frequencies without the inconvenient of having low Q devices usually reported in large bandwidth applications [Yeo 2000]. Low-loss bandpass LC filters were also demonstrated, showing new possibilities of use of this topology that usually cannot be fabricated on chip due to prohibitive level of losses when built using on-chip passives.

Chapter 4

High Q inductors and RF packaging using quartz substrates

This chapter presents an alternative process flow developed for the fabrication of high quality factor passive devices directly embedded in insulating substrates, namely floating glass and quartz wafers [Leroy 2006, Leroy 2007]. This technique showed to be promising in terms of offering excellent RF performances due to the complete suppression of the underneath lossy silicon substrate. Further development also demonstrated that the quartz substrate can be used as a functionalized RF MEMS packaging cover [Leroy 2006b].

With the availability of new state-of-the art ICP plasma etching equipments capable of performing deep reactive ion etching of quartz substrates, the possibility to produce thick copper lines embedded directly on an insulator substrate was investigated. The deep trenches are filled by copper electroplating and the lines are defined by copper CMP in a damascene like approach, using the same approach developed for copper inductors embedded in polyimide. The main advantage of this technique is the high resistivity of the quartz ($2 \cdot 10^{14}$ Ω cm @ 20 °C), which reduces dramatically the substrate-related RF losses.

Many previous works revealed that RF performances are strongly dependent on the limited metallization thickness and on the conductivity of the substrate [Burghartz 1998, Yue 2000]. Some solutions have been investigated to increase these performances. For reducing substrate-related losses, high resistivity silicon or SOI substrates have been used [Reyes 1996], insulating the inductor from the silicon substrate. Etching a cavity underneath the inductor has also been investigated [Lakdawala 2002].

Even if inductors with high Q factors and resonant frequencies can be manufactured on top of low resistivity silicon wafers [Carchon 2004], covering most of the telecommunication applications, the nature of the substrate remains a recurrent limitation [Pisani 2003, Pisani 2004b]. Yoon et al. investigated the RF performances of the same solenoid inductor design fabricated on both silicon and glass substrates [Yoon 1999]. On-glass inductors provided a significant increase in both quality factor (45%) and self resonant frequency (2.5 times higher). The increase in the performance is related to a considerable reduction in the parasitic capacitance and resistance associated to the substrate.

4.1. Fabrication Process

Fig. 4.1 shows a schematic cross section view of the technology steps developed to fabricate thick copper spiral inductors embedded in a quartz substrate. A 2 μm sputtered amorphous silicon film is used as hard mask for the etching of the quartz cavities (fig. 4.1a). This a-Si hard mask is patterned by thin-resist photolithography followed by a SF_6 / C_4F_8 dry plasma etching step (fig. 4.1b). The quartz substrate is then patterned by C_4F_8 / CH_4 / Ar plasma etching step performed in a state-of-the-art Alcatel AMS 200 DSE ICP dry etcher (fig. 4.1c). After stripping off the amorphous silicon mask (fig. 4.1d), the quartz mould is cleaned in a piranha bath (H_2SO_4 / H_2O_2) and receives 0.1 μm sputtered chromium as adhesion layer and a 0.2 μm sputtered copper as seed layer (fig. 4.1e). The mould is filled out with 4.8 μm of high conductive electroplated copper (resistivity ρ = 2.0 μΩ cm, fig. 4.1f). Copper lines are then defined by a damascene approach using a high removal rate chemical-mechanical polishing receipt (CMP, fig 4.1g) [Pisani 2004]. The CMP stops at the top chromium layer which is removed in a very selective chromium to copper wet etch bath (fig. 4.1h).

A protection layer is then defined in order to avoid copper oxidation and to have good electrical contacts to the devices. The protection is made of 0.2 μm titanium and 0.6 μm of aluminum layers deposited successively in the same multi-target evaporator system, which prevents exposition of the first film to air (fig. 4.1i). The protection layer is patterned by lift-off process, using reversal thin-resist (fig. 4.1j). Finally, connections are established by bonding a 25 μm diameter gold wire between the inductor central pad and the lateral RF port (fig. 4.1k).

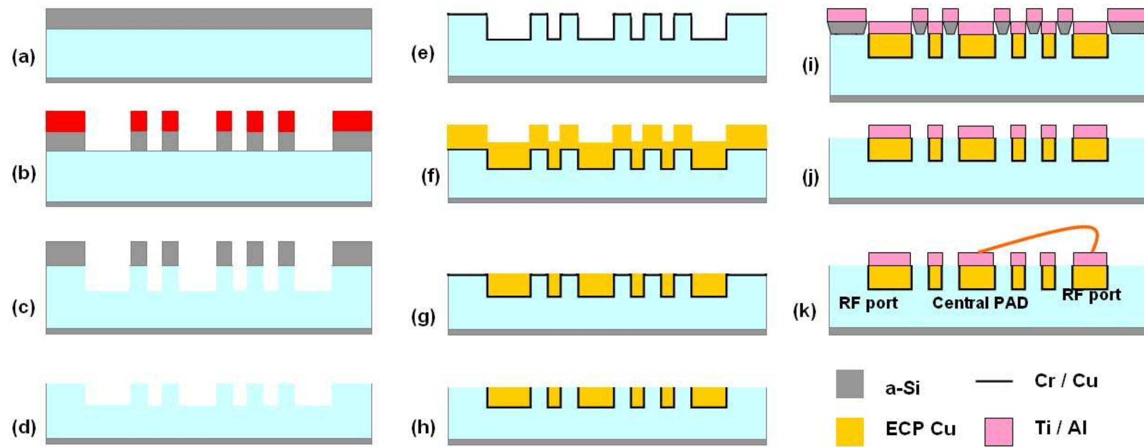


Fig. 4.1: Schematic cross section view of the coil fabrication process flow: (a) a-Si deposition (PVD), (b) a-Si dry etching, (c) Quartz dry etching, (d) a-Si mask strip, (e) Adhesion and seed layers deposition (Cr / Cu, PVD), (f) Cu electroplating, (g) Chemical mechanical polishing, (h) Top Cr wet etching, (i) Lithography and protection layer deposition (Ti / Al), (j) Lift-off, (k) Gold wire bonding.

4.2. Fabrication Results

Fig. 4.2 shows scanning electron microscopy (SEM) pictures of quartz etched mould. C_4F_8 / CH_4 / Ar plasma etching is a very selective process (> 20:1 to amorphous silicon) that provides very vertical walls [Pavius 2004].

A SEM picture of a final fabricated device can be seen in fig. 4.3.

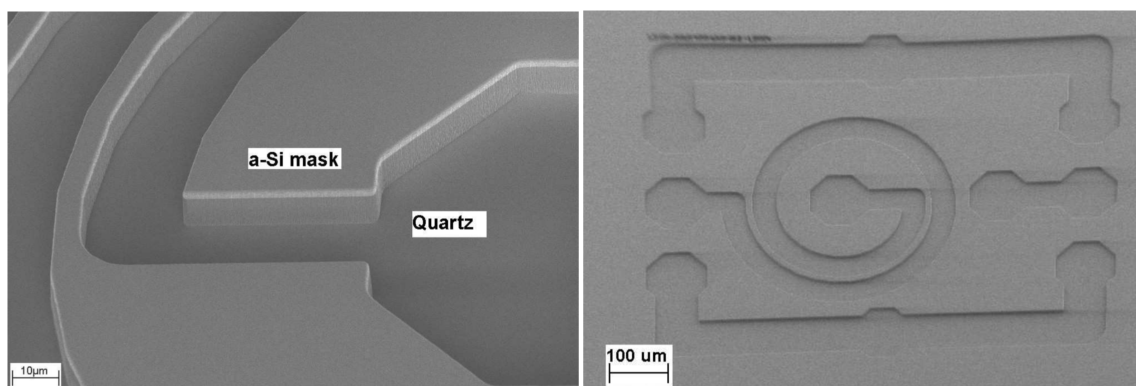


Fig. 4.2: SEM closed view of a 4 μm deep dry etched quartz inductor mould (40 μm track width and 8 μm track spacing).

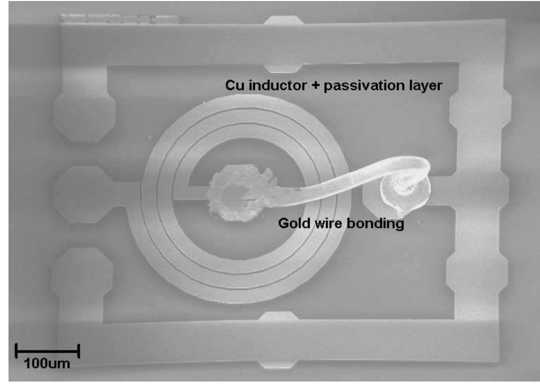


Fig. 4.3: View of a fabricated 3-turn circular spiral inductor (400 μm outer diameter, 40 μm track width, 8 μm track spacing).

4.3. RF Performance results

Two devices of 3.8 and 9.0 nH nominal inductances fabricated using this process were characterized and analyzed in detail in the 0.05 – 13.5 GHz frequency range, using the same methods presented in the previous chapter.

Dimensions and calculated inductance of each device are summarized in table 4.1. Expected inductance values are calculated following the current sheet method presented in chapter 2 (eq. 2.29, [Mohan 1999]). The thicker layer used in this work with respect to [Mohan 1999] explains a reduction of a few percent in the inductance values with respect to the predicted ones (inductance decreases with both increasing track width and thickness, but must of practical formulae neglect the thickness dependency).

	L_1	L_2
D_{OUT} (μm)	800	800
w (μm)	20	40
s (μm)	12	12
form	octagonal	circular
# of turns	1.5	3
$L_{(PREDICTED)}$	4.3 nH	9.3 nH
$L_{(MEASURED)}$	3.8 nH	9.0 nH

Table 4.1: Dimensions and inductances of two analyzed inductors.

Figs. 4.4 and 4.5 show respectively the extracted inductance values L (eq. 3.2) and Q-factors (eq. 3.3) of these 2 inductors.

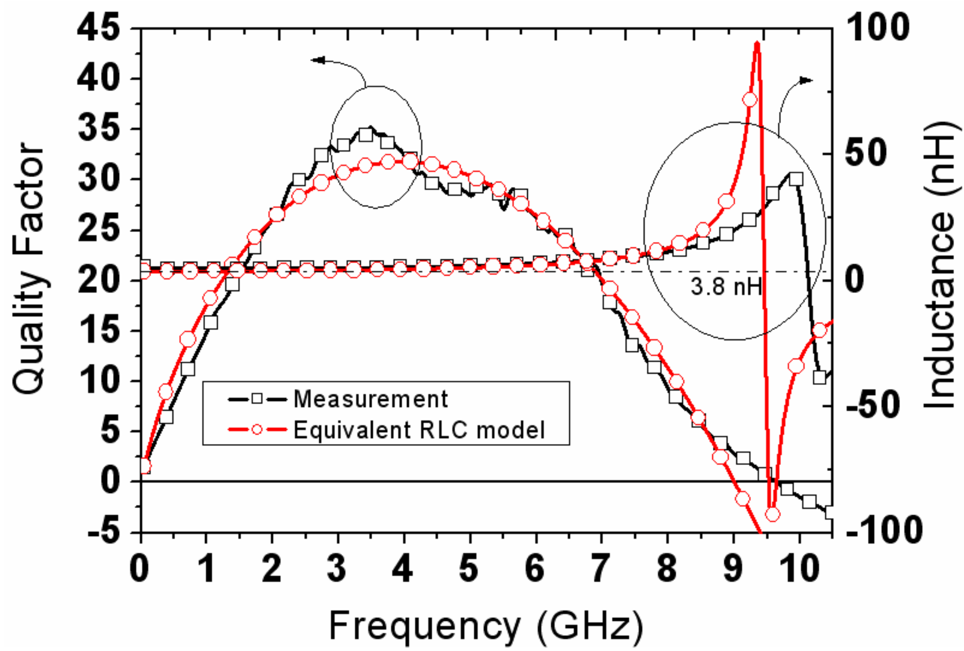


Fig. 4.4: Extracted inductance (eq. 3.2) and Q-factor (eq. 3.3) vs. frequency for the 3.8-nH device.

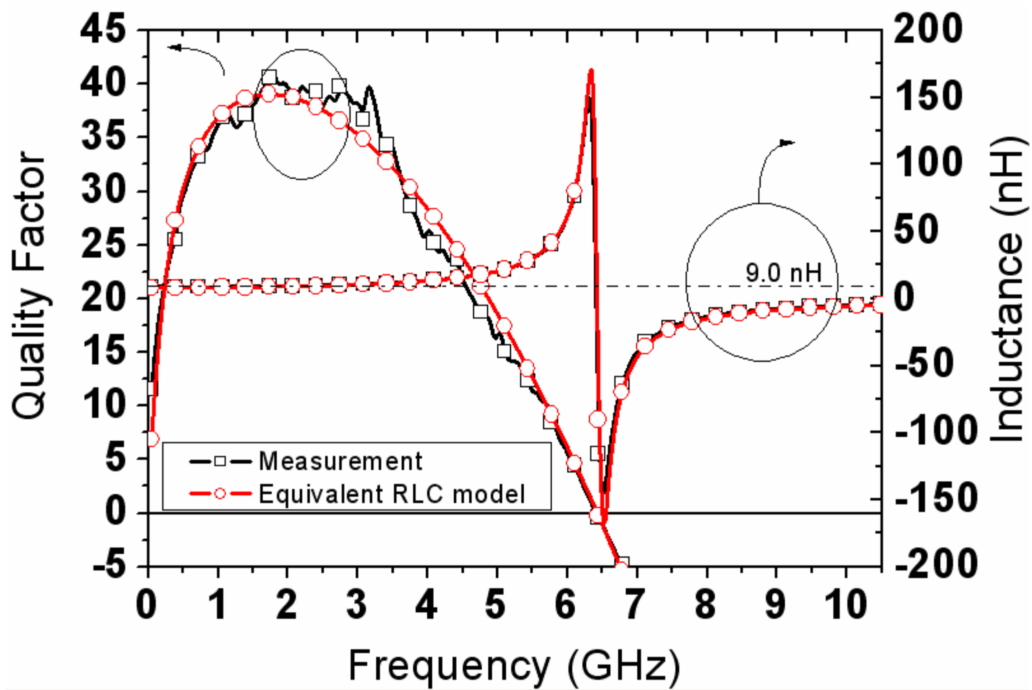
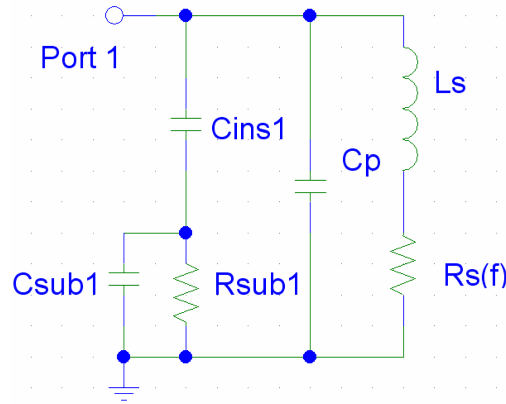


Fig. 4.5: Extracted inductance (eq. 3.21) and Q- factor (eq. 3.3) vs. frequency for the 9.0 nH circular inductor.

A broadband RLC equivalent circuit of a spiral inductor was used in order to model the measured parameters. Fig. 4.6 shows the equivalent 1-port circuit [Yue 2000] and the values of the parameters extracted from the measurements using a dedicated procedure (non-linear least squares fit on the S-parameter and on impedance data).



Device	L_S	$R_{S(DC)}$	C_P
L_1	3.8 nH	0.62 Ω	83 fF
L_2	9.0 nH	0.48 Ω	67 fF

Fig. 4.6: Equivalent broadband RLC model of a spiral inductor [1] and extracted values for L_1 and L_2 devices (C_{INS1}, R_{SUB1} and C_{SUB1} substrate parameters are negligible).

In the model of fig. 4.6, R_S accounts for the series resistance of the metal tracks and is dependent of the frequency in the form $R_S(f) = R_{DC} + a\sqrt{f} + bf$ where R_{DC} is the low frequency resistance and ***a*** and ***b*** are constants depending on the device geometry that accounts for the skin and proximity effects. These effects increase the resistance as function of the frequency. C_P is the parasitic parallel capacitance that comes mainly from the capacitive coupling between adjacent inductor tracks. C_{INS1} and C_{SUB1} accounts for the parasitic capacitances between the measurement ports and between the spiral tracks and the backside ground of the wafers. R_{SUB1} accounts for the resistive losses in the substrate, due to the substrate conductivity as well as to eddy currents induced by the magnetic field of the inductor. This value ranges from typically some ohms to hundreds of ohms when the spiral is designed on top of low resistivity substrates. This resistance decreases the peak quality factor as well as the self resonant frequency. For the devices built on top of quartz substrates, the contribution of the substrate is reduced to its minimum by the use of an insulating substrate, and only the C_P value needs to be considered to produce an accurate equivalent circuit model.

For the 3.8-nH inductor (fig. 4.4). A peak quality factor of 35 at 3.5 GHz and a self-resonant frequency of 9 GHz were measured. For the 9.3-nH inductor (fig. 4.5), measured peak quality factor is 40 at 2.1 GHz and resonant frequency is 6.5 GHz.

It should be pointed that the fabricated devices exhibit a broadband Q-behavior, with Q exceeding 20 in the range of 1 to 5 GHz, enabling the use of such devices in multiband circuits. The achieved performances in terms of Q_{MAX} and *SRF* are in the current state-of-the-art for integrated inductors [Carchon 2004].

4.4. Functionalized quartz packaging

The packaging is one of the most important parts of the MEMS devices being considered today, together with the MEMS reliability, a critical issue for the success of future RF MEMS device technologies [Jourdain 2001]. An adapted packaging ensures correct working conditions of the component by protecting it from the outside environment (particles and moisture being usual failure causes) and in some cases it provides the operating environment (vacuum, gas) compatible with the expected performances.

Moreover, for RF MEMS operating at GHz frequency, the packaging parasitics should be controlled to not jeopardize the device figures of merit. High-resistivity packaging and very short interconnects are then needed. On the other hand, for any functionally successful packaging the associated cost should stay very low compared to the device itself, which motivates increased interest in wafer-level packaging solutions. Despite the relatively large number of packaging solutions and studies [Butler 1998, Jourdain 2005, Pisani 2004b], the functionality of the cap itself is an aspect that was not studied and very rarely exploited.

In this part of the work a wafer-level packaging solution for RF MEMS is addressed, the packaging being functionalized by fabricating high Q inductors on top of it. This solution could be an interesting candidate for LC tanks or integrated ladder filter solutions that need high Q inductors and tunable MEMS capacitor components using a hybrid technology fabrication. Moreover, such a solution can offer an increased functionality per volume, being one of the most compact possible ones.

4.5. Wafer-level packaging process

Performances of the packaged RF MEMS significantly depend on the height between the device and the bottom of the sealing cavity. A new process allowing the fabrication of thick layers (thicker than 40 µm) and with low thermal budget was chosen apart from other existing wafer-packaging bonding solutions using BCB [Jourdain 2005] or other soft photoresists [Gallant 2005].

Fig. 4.7 shows an example of a measured performance of a CPW line covered by various packing wafer resistivity and distance from the line [Jourdain 2003]. In order to avoid changes in the naked line response, high resistivity packaging at a distance higher than 25 µm should be used.

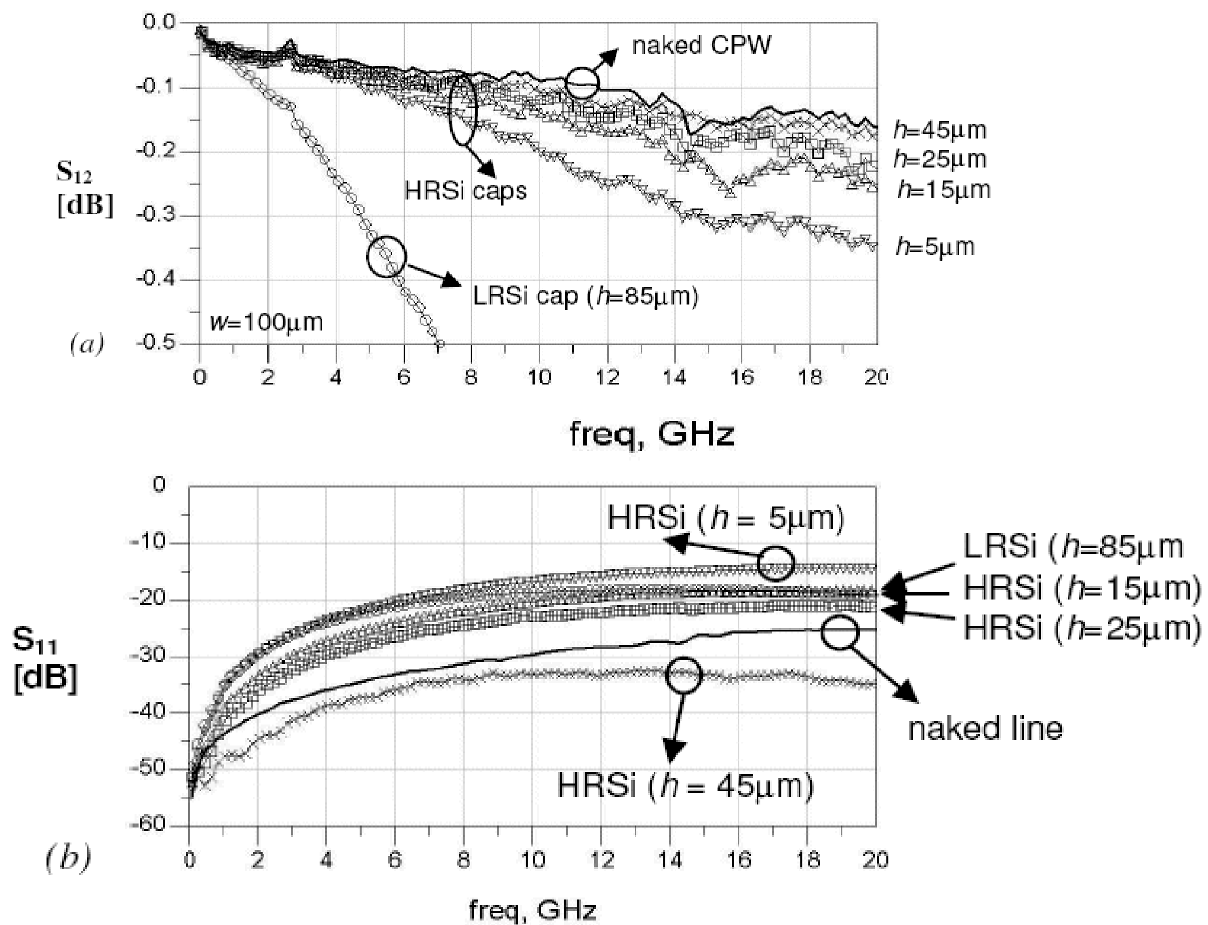


Fig.4. 7: Study showing the impact of the resistivity and cap-distance of the RF performance of a packed CPW line [Jourdain 2003].

Furthermore, a low thermal budget process can prevent RF MEMS with membranes from being warped during the packaging process. The technological process chosen is based on adhesive bonding of two SU-8 layers on two separated wafers: a partially soft baked layer at the bottom of the cap wafer and a photolithography patterned layer on the device wafer. The wafers are brought into contact, pressed together and heated until the glass transition temperature of the SU-8, resulting in the polymerization of the two layers together and the wafers to become bonded. Fig. 4.8 shows a schematic cross section view of the technology steps used for the bonding process (B steps refer to the bonding wafer ones and C steps refers to the cap wafer ones).

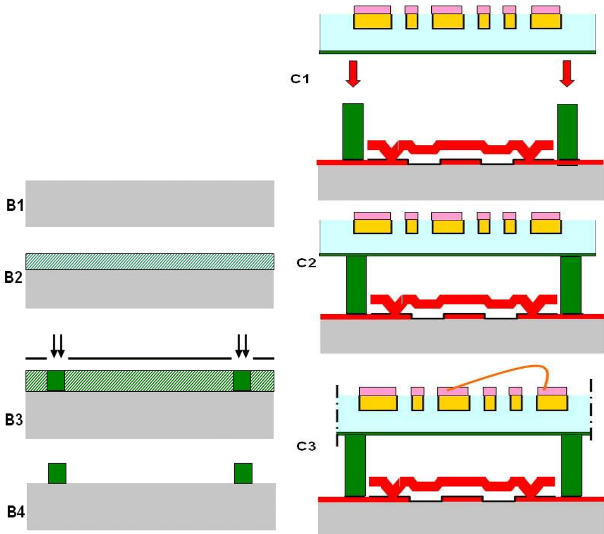


Figure 4.8: Schematic cross section view of the technological steps used for defining the quartz substrate as packaging and the bonding process. The high gap (50 µm) between the MEMS and the packaging (C3) allowing parasitics reduction motivated the choice of SU-8 as bonding solution.

4.6. SU-8 photolithography

SU-8 patterning is a well-established multi-step process with associated parameters dependent on the thickness of the layers. First, the wafers receive a dehydration and cleaning treatment for 7 minutes in O_2 plasma to improve the adhesion of the SU-8 film (fig. 4.8 B1). The wafers are then spin-coated. Two commercially available SU-8 negative photoepoxies from Gersteltec SA were used (GM1040 and GM1070) [Gersteltec]. GM 1040 is suitable to obtain thin layers (0.8 to 10 µm) and GM 1070 to obtain thick layers between 50 and 500 µm. A 50 µm-thick layer was spin-coated on the device wafer (fig. 4.8 B2), while a very thin layer

(about 1 µm) was spin-coated as a bonding layer on the backside of the cap wafer (fig. 4.8 C1). The parameters of the spin coating process are listed in table 4.2.

Parameters	Device wafer	Package wafer
Speed	2400 rpm	4000 rpm
Acceleration	100 rpm/s	100 rpm/s
Time	40 s	40 s
Thickness	50 µm	1 µm

Table 4.2: Spin coating parameters for the packaging and device wafer.

After the spinning, a relaxation step is needed in order to improve the uniformity of the SU-8 film. Relaxation time is determined by the thickness of the photoresist. It ranges from 5 minutes for 1 µm-thick layers to 2 hours for 50-µm thick layers. The wafers are then dried on a hotplate during a soft bake step. The soft bake is done at 2 temperatures: first bake is performed at 65°C resulting in the evaporation of the solvent from the SU-8 film and second at 95°C. The duration for each bake is fixed by the thickness of the film. The wafers are then cooled down to room temperature. The photolithography process stopped after the soft bake for the 1 µm-thick bonding layer. No patterning of the SU-8 is necessary. A full layer coverage ensures increase in the bonding surface without the need of precise wafer alignment.

Cross-linking process is initiated by exposing the SU-8 film to UV. This step is conducted on a Süss Microtech MA6 mask aligner, with hard contact used to improve exposure homogeneity (Fig. 4.8 B3). The required exposure dose depends on the thickness of the SU-8 and on the intensity of the i-line UV light (365 nm). For 50 µm-thick SU-8 film, 650 mJ/cm^2 UV exposure dose was used. Exposure only initiates chemical amplification in the SU-8 and the cross-linking process is really slow at room temperature. It is enhanced by a thermal treatment called post-exposure bake, making the exposure areas insoluble in the developer. This step is the most critical one and is performed in a progressive ramp to avoid cracking on the resist. The wafers were ramped linearly from room temperature to 65 °C and from 65 °C to 90 °C at a 2 °C/min rate, baked for a time period fixed by the thickness of the SU-8 film and then cooled down to room temperature. Finally the wafers were developed by immersion and slight agitation in a propylene glycol monomethyl ether acetate solution (PGMEA) for 3 minutes and rinsed with isopropanol (Fig. 4.8 B4). Fig. 4.9 shows a picture of one developed

SU-8 seal bond. The holes designed permit a better reflow of the resist along the channel during the bonding step.

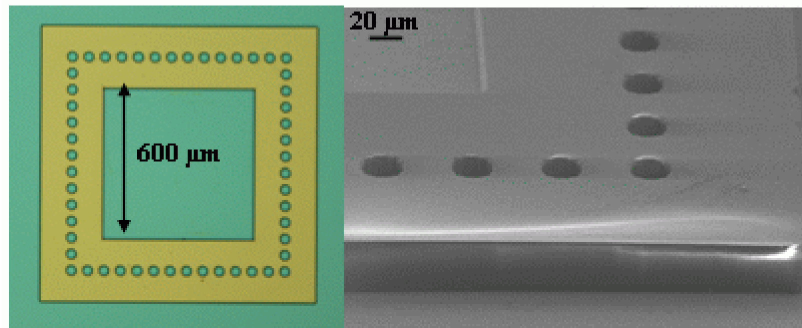
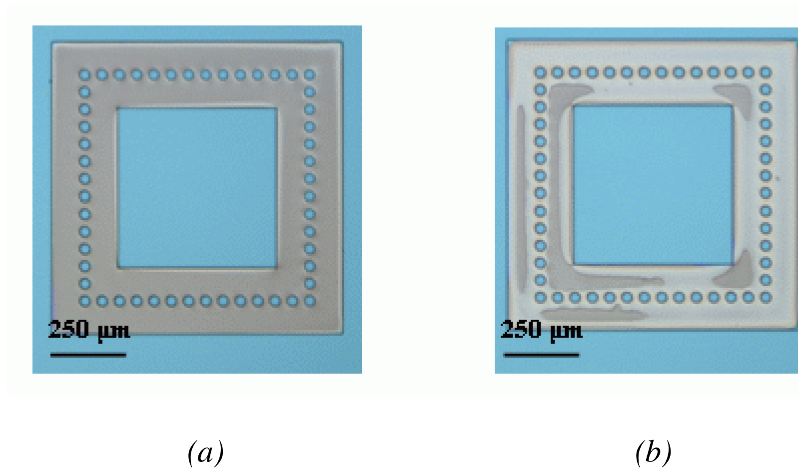


Fig. 4.9: Optical microscope and SEM pictures of a developed SU-8 cavity.

4.7. Bonding Process

The last step of the process is the bonding of the device and cap wafers together. Bonding is based on the polymerization of both SU-8 layers while kept together under pressure. At this step at least one of the two films should not be totally cross-linked before the bonding process. The cross-linking should be done during this step. That is the reason why the cap wafer was not exposed to UV light.

The bonding process was performed in a Süss Microtech SB6 bonder. An O_2 plasma pre-bonding treatment was done for 30 s on the device wafer. Meanwhile the cap wafer was UV exposed through a glass plate with hard contact. Subsequently the two wafers were aligned in a Süss Microtech BA6 mask aligner and transferred into the bond chamber. The two wafers were brought into contact and heated at 65 °C for 5 minutes, then heated at 95 °C for 15 minutes, applying a force of 615 N on the stack (Fig. 4.8 C1, Fig. 4.8 C2). The bonding process was performed at atmospheric pressure under nitrogen atmosphere. Fig. 4.10 shows optical microscope pictures of fully-bonded and partially bonded cavities. At the end of the bonding, a detailed optical inspection enabled the estimation of the bonding yield, which is about 80% (of fully bonded SU-8 cavities). This yield can be further increased by optimizing the size of the bonding ring as well as the size and number of holes for resist reflowing along it.



(a) *(b)*

Figure 4.10: SU-8 structures after bonding process: (a) a bonded structure, (b) a partially bonded structure.

4.8. Package characterization

Once the wafers are bonded, the upper wafer, i.e. the quartz wafer, was diced in order to singularize the caps (Fig. 4.11). This step allowed a qualitative evaluation of the bonds strength and adhesion of the SU-8 films on each wafer.

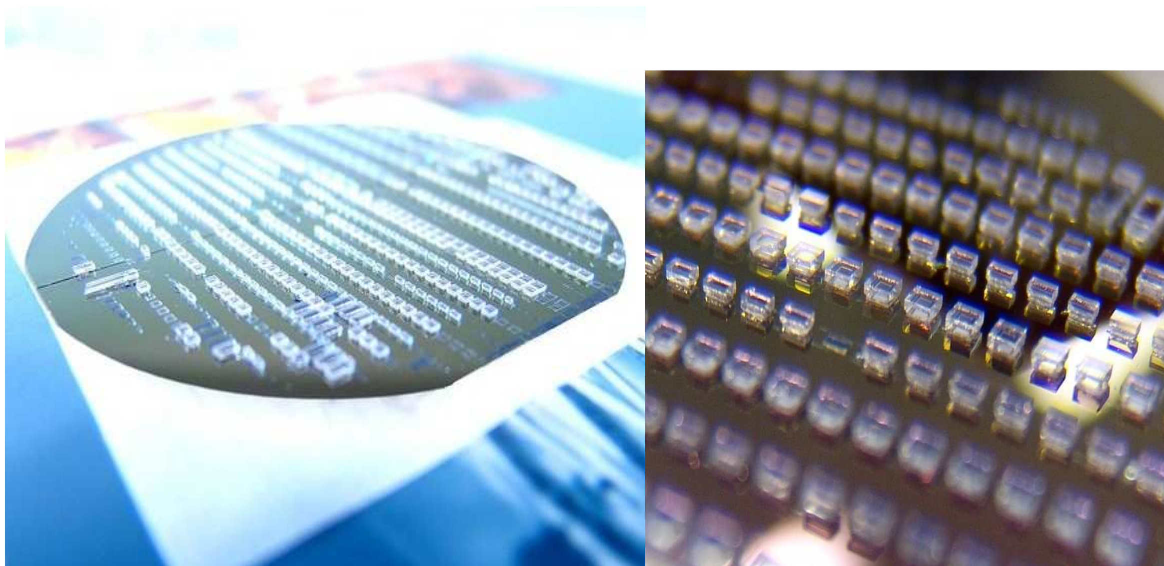


Figure 4.11: Wafer level packaging pictures after dicing the quartz caps.

4.9. Bond strength and adhesion

Quartz wafer was diced in order to remove all unusable quartz and keep just bonded quartz caps at the top of SU-8 cavities. In spite of the very low bonding surface (only 12% of the wafer surface), adhesion and bonds strength were strong enough to allow the dicing without de-bonding. Pictures of bonded and diced quartz caps are presented in Fig. 4.11.

4.10. Wettability

Even if all the tests of this study were performed with a dummy silicon wafer covered by 0.5 µm of wet silicon dioxide working as a device wafer, the compatibility of this packaging process with SF_6 released MEMS, e.g. tunable capacitors fabricated in [Fritschi 2004], was fully tested. A first bonding test was performed with a dummy wafer covered with 0.5 µm wet oxide and exposed one minute to SF_6 gas. The bonding did not withstand after dicing and wafers de-bonding occurred at the SU-8 / SU-8 interface during the dicing process. Drop wettability tests were performed to investigate the impact of SF_6 gas on the wetting tendency of SU-8 films. The shape of the drop is directly linked to the wettability of the material: round drop is characteristic of a hydrophobic surface when a battered one shows a hydrophilic surface. Micro drops with the same volume were deposited on the SU-8 surface at different steps of the process and their shapes were observed under the optical microscope.

First test showed that SU-8 was hydrophilic after development (Fig. 4.12a). This test suggests that a hydrophilic nature provides a successful bonding. Second test revealed that fluorine chemistry had an impact on the wetting tendency of the SU-8. Indeed one minute exposure to SF_6 gas resulted in the SU-8 becoming hydrophobic (Fig. 4.12b). Among the solutions investigated to reverse the wetting tendency of the SU-8 film, the O_2 plasma treatments showed to be efficient (Fig. 4.12c), and provides a solution to solve the packaging compatibility with SF_6 release of MEMS.

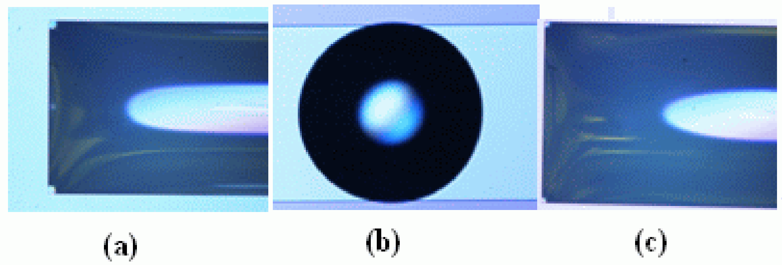


Figure 4.12: Drop tests at different steps of the process: (a) just after development, (b) after 1 minute SF_6 plasma, (c) after 1 minute SF_6 plasma and 30 seconds O_2 plasma treatment.

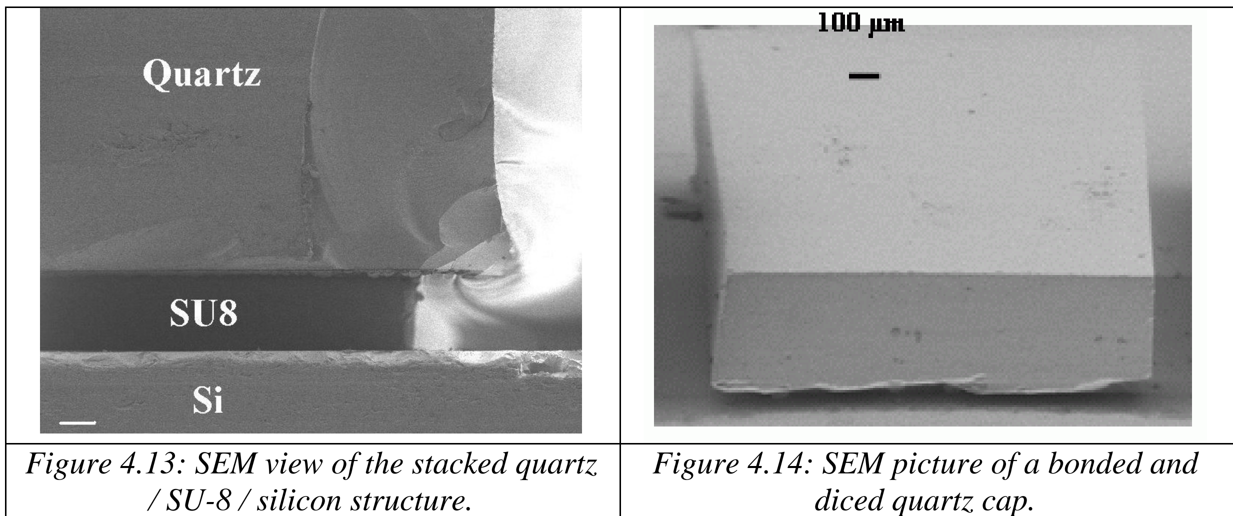


Figure 4.13: SEM view of the stacked quartz / SU-8 / silicon structure.	*Figure 4.14: SEM picture of a bonded and diced quartz cap.*

Summary

This chapter studied an alternative process flow developed to fabricate passive passives, suitable to fabricate both high Q inductors and transmission lines. This process is based on the deep reactive ion etching of quartz substrate and direct patterning of copper lines using the basic steps developed for the copper / polyimide process module. A functionalized wafer level packaging solution (WLP) is also presented. Both sides of the quartz wafer are used: the top to fabricate high Q inductors and the bottom to provide semi-hermitic high RF performance RF MEMS seal. The process uses thick SU-8 resist processed at relatively low thermal budget, making it suitable to package movable membrane RF MEMS devices and offering a new and original development of a hybrid high-performance functionalized RF packaging. The packaging process was particularly optimized to be compatible with SF_6 released membrane RF MEMS switches and tunable capacitors [Fritschi 2004].

The original contribution of this study resides in the use for the first time of deep anisotropic dielectric etching associated to thick metal CMP to fabricate high-performance passives and by the realization of an original doubly-functional packaging solution by using 2 sides of the wafer, one to fabricate high Q passives and another to protect the encapsulated wafer. Innovation is also introduced by the use of SU-8 for RF applications were traditionally BCB is used. The use of a thick resist gives more freedom in terms of choice of the cap height to do not degenerate the RF performances (> 40 μm), without the need of deep reactive ion etching of the capping wafer.

Chapter 5

Simulation, characterization and modeling of spiral inductors

5.1. RF passive simulation tools

Predictive modeling is an essential step in the design of any electronic device. The capability to model the behavior and performance of the device as function of the technology profile, geometry and frequency is needed in order to provide optimal designs within the desired specifications before effectively fabricating the components. Inspire of its relatively simple geometry, the design and optimization of spiral inductors is constrained by complex, frequency-dependent phenomena that affect both inductance calculation and losses estimation. Accurate frequency-dependent loss calculation is needed in order to correctly predict the quality factor, which is one of the major limitations imposed in the design of on-chip small footprint passive devices. Some simple equations suitable for 1st order hand calculations are available in the literature, but these approximations show to be too rough in order to accurately predict the equivalent circuit model of passive devices.

The approach to tackle with this modeling task involves in general the calculation of equivalent circuit parameters from the solutions of Maxwell equations by the use of specialized numeric solvers. Several RF passive and spiral inductor computer simulation tools are available in commercial or free versions. They can be divided in 2 main categories depending on how they model the devices. Electromagnetic (EM) simulation tools solve Maxwell equations numerically in the time or frequency domain and give as result S-parameter data or RLCK (resistance, inductance, capacitance and mutual inductance) parameters of the of the device. Simulation tools that fall in this category are, amongst many

other: Fasthenry [Kamon 1994, Guan], ADS-Momentum [Agilent 2005], Sonnet [Sonnet], Zeland IE3D [Zeland], Ansoft HFSS [Ansoft 2006] and CST Microwave studio [CST]. These tools have different degrees of accuracy related to the way used to discretize the Maxwell equations and the fact that some approximations are used or not: use or assumption of special types of symmetries, 2 or 3-D approximations, boundary value conditions assumed, number and type of cells used to discretize the problem (meshing), use of quasi-static approximations, and if radiation effects are taken into account or not [Hanington 1968]. These tools are computationally intensive and take typically hours to days of computing time to accurately simulate a single device. They are essentially used for validation of measurement-based models or for calibration of other faster methods. The second class of simulation tools are based on equivalent RLCK semi-analytical solutions and produce as output a SPICE circuit netllist or the S-parameter data as function of the frequency for the proposed equivalent network. KSU Spiral [KSU], VeloceRF [Helic, Koutsoyannopoulos 1997], OEA Spiral [OEA] simulators, amongst others, fall in this category. These tools are much less computationally intensive than direct EM solving and can produce results for a device in a few seconds or minutes. They are suitable for optimizations (were comparing many devices spawning a large device space and picking up the best performer is needed), but can be very inaccurate if the models are not well calibrated against measurements and full wave simulation tools. Some tools like ASITIC [Niknejad 1998, Niknejad 2000] falls between these two categories, and can be used to solve numerically for S-parameter data as well as for fast equivalent circuit extraction.

In this work, ADS-Momentum and Matlab were used as main simulation tools. Part of the designs and simulations were also conducted using ASITIC, VeloceRF (simulations performed by Helic SA – Athens – Greece) and HFSS (simulations performed by EPFL-LEMA) as alternative tools. The major drawback faced when using ASITIC to model the devices used in this thesis were related to lack of calibration and convergence when using frequencies above 5 GHz and due to bad estimation of losses for devices built on top of high resistivity substrates. The numeric stability is compromised when the resistivity of the substrate is higher than 1 kΩ cm and the uniformly distributed meshing grid becomes too demanding in terms of memory when a fine mesh is requested, what is needed for correct loss estimation especially at frequencies above 3 GHz. In fact, this tool is calibrated and validated for frequencies below 3 GHz and using devices built on top of low resistivity substrates [Niknejad 2000]. VeloceRF simulations present as advantage a seamless integration with

other Cadence design tools [Cadence], but needs a number of semi-empirical parameters as input and lack some functionality in order to predict frequency-dependent losses of the substrate. Although these tools can be effectively considered and used to design and model spiral inductors, care must be taken to interpret the results and some calibration against measured devices is needed in order to provide accurate results, especially in very high frequencies above 3 – 5 GHz range.

From the analytical point of view, the design and optimization of spiral inductors involve tedious and error prone calculations. There are many parasitic calculation models available in the literature that will be analyzed in detail in the next paragraphs. All the equations and models used in this thesis were coded using Matlab [Mathworks] and grouped in a specialized toolbox entitled *"RF Analysis and Passive Design Toolbox"* [Pisani 2004d]. This toolbox is one of the outcomes of this thesis project and is available for free on the Internet. This tool was also successfully used to perform RF parameter extraction and analysis in other RF passive fabrication and analysis projects [Fritschi 2007, Mehdaoui 2006, Mehdaoui 2007b, Mehdaoui 2007c].

5.2. Measurement-based models

Measurement-based models are probably the most used ones. For a given technology, a large number of devices is designed, fabricated and measured. The characteristics and performances of the fabricated devices are correlated with the geometrical and technological parameters and give the circuit designer the choice for different device sizes, inductance densities, inductance values, peak quality factor or the quality factor at a given operating frequency. The major inconvenient of this approach is a certain lack of physical insight of the parameters that affect the performance of the device, the need to fabricate and measure accurately a large number of devices to gather the needed information and difficulties to apply the obtained results for technological profiles different of the one used in the reference device library.

Equivalent circuit parameters are extracted from S-parameter measured data, usually by non-linear least squares fitting of the equivalent circuit parameters using impedances or admittances. One should be careful when running this process since sometimes the extracted parameters can produce good fit but can lack of physical significance and scalability on real physical parameters of the devices. The equivalent RLCK circuits are suitable for doing

SPICE-like simulations of the devices, but are usually valid over a narrow range of frequency values since most of physical phenomena in spiral inductors are strongly dependent on the frequency of operation. Some complex circuit models have been proposed in order to take into account frequency-dependent behavior like skin and proximity effects without having frequency-dependent components in the equivalent circuit network [Kim 1996, Sen 1998, Mei 2003].

Measurement-based models are also highly affected by additional parasitics added by the RF routing and padding used to connect the device to the RF setup and by the inherent limitations of the S-parameter measurement setup. Pad parasitics effects can be usually subtracted from the measurements by a careful measurement of dummy structures especially designed to compensate for the extra parasitics introduced by the pads needed for the probing of the devices [Cho 1991, Vandamme 2001, Watenberg 2002]. This process, known as deembedding, is generally done in 2 steps, one for compensating for the series impedance of the RF probes and other for compensating for the parasitics of the pads, especially parallel capacitance that can be introduced by large RF pads.

5.3. Simulation-based models

This approach is somewhat similar to the measurement-based one, but in this case a large number of electromagnetic simulations is used to explore the design space and draw up conclusions about the performance trends in the results. Usually this approach needs to be calibrated against measurements in order to make sure the simulation models and options are accurate and the correct physical parameters are defined for the simulation. This approach is more adequate when used in addition to measurement and analytical modeling as a validation step based on the numeric solution of the Maxwell equations.

5.4. Analytical models

Analytical models are highly desirable to model any kind of device, and in particular integrated inductors. They can provide all the necessary physical insight for the devices and permit to synthesize and optimize them in a fast, accurate and effective manner. They are not easy to produce for spiral inductors, since an elevated number of physical phenomena play an

important role in these devices, defining how the parasitic resistances and capacitances should be evaluated.

The resistance of the spiral is a function of the frequency. It is affected by both skin and proximity effects. Skin effect pushes the current toward the metal surfaces at high frequency regime, making the resistance increase roughly with the square root of the frequency. Proximity effect is due to the coupling between adjacent spiral tracks. The magnetic field of the external tracks couples into the innermost ones, pushing the current lines toward the external diameter of the spiral. This phenomenon is very difficult to model analytically since it depends on all geometrical parameters of the spiral. A number of empirical studies have been done about this topic [Kuhn 2001, Tuncer 1993] and practical equations involving the frequency and the geometrical parameters of the devices have been proposed, but none of them can model this phenomenon accurately. Roughly, the proximity effect makes the resistance of the spiral increase with the frequency in the form f^{α} with the exponent α being between 1 and 2.

The parasitic capacitances that set the resonant frequency of the device are distributed and come from many different contributions: track to track capacitance, coupling to the surrounding ground lines and to the substrate.

The RF modeling of the substrate is also essential, since an important part of the losses on spiral inductors come from it. Accurate modeling of the substrate losses involves knowing how much energy is injected in and absorbed by the low conductive substrate through the electromagnetic field produced by the spiral. One of these mechanisms are eddy currents produced by the circulating magnetic field of the spiral that induces currents in the body of the substrate by inductive coupling. Bulk eddy currents are negligible when $\rho_{SUB} > 1\ \Omega$ cm (quasi-TEM mode), and dominant when $\rho_{SUB} < 0.01\ \Omega$ cm (skin effect mode) [Niknejad 1998, Niknejad 2001].

In very high frequencies, the properties of the dielectrics can be affected by dispersion [Gupta 1981], and in general the physical properties like the dielectric constant, assumed to be constant, should be modeled as functions of the frequency.

A complete modeling approach should also take into account thermal effects, specially in power devices that are subject to operate in temperatures higher the ambient one were the devices usually have the RF parameters measured [Shi 2004, Grovers 1997, Bhattacharya 2004]. By the same way, the substrate parasitic resistance and capacitance are affected by the temperature what also impact the performance of the device. [Shi 2004] suggests that differences of between 8 and 20% less in the quality factor and up to 20% less in the self-resonant frequency can occur when the temperature of operation of aluminum inductors changes in the range of 25 ^{o}C to 85 ^{o}C (*TCR* of $3.7 \cdot 10^{-3}$ / ^{o}C @ 25 ^{o}C was measured for the metal traces). The resistance temperature coefficient or resistance (*TCR*) of copper is estimated to be about $4.3 \cdot 10^{-3}$ @ 25 ^{o}C [Cech 1993, Brandes 1983]. The *TCR* for doped silicon is estimated to be between $8 \cdot 10^{-3}$ and $9 \cdot 10^{-3}$ / ^{o}C @ 25 ^{o}C [Shi 2004, Arora 1993]. [Shi 2004] also reports the temperature coefficient of capacitance (*TCC*) for the silicon substrate to be in the order of $-8.7 \cdot 10^{-3}$ / ^{0}C @ 25 ^{o}C.

5.5. ADS Momentum simulations

Advanced Design System from Agilent has an EM simulation module based on the method of moments [Hanington 1968], called Momentum. All the simulations done with Momentum in this work neglected radiation losses (using RF mode). Neglecting radiation produces results much faster and does not affect the accuracy of the results for spiral inductor designs, since all devices are very small with respect to the wavelength and radiation losses do not play primary role. Preliminarily simulations enabling and disabling this mode were done to numerically verify this hypothesis. ADS documentation gives these empirical equations to help deciding if radiation losses are important considering a typical device size *D* in mm and a simulation frequency *f* in GHz [Agilent 2005]:

$$D(mm) < \frac{150}{f(GHz)} \qquad \text{(eq.5.1).}$$

Spiral inductors studied in this thesis have always less than 1 mm in size and less than 20 GHz for the operating frequency, largely satisfying this equation.

For circuits made on top of finite thickness substrates, these empirical relations for the simulation frequency f in GHz considering the dielectric constant of the substrate $\varepsilon_{R,sub}$ and its thickness t_{SUB} are also suggested [Agilent 2005]:

$$f(GHz) < \frac{300}{t_{SUB}(mm)\sqrt[\alpha]{\varepsilon_{R,SUB} - 1}} \quad \text{(eq.5.2)},$$

for the frequency of operation f, or

$$t_{SUB} < \frac{\lambda_0}{\sqrt[\alpha]{\varepsilon_{R,SUB} - 1}} \quad \text{(eq.5.3)},$$

for the substrate thickness t_{SUB}, where λ_0 is the free-space wavelength given by $\lambda_0 = c / f$, and α a constant ranging from $\alpha = 20$ if a ground plane is placed in the backside of the substrate and $\alpha = 10$ if the backside of the substrate is at an open bound domain with air. For the simulations done in this thesis, the substrate thickness is 525 ± 25 µm for both silicon and quartz wafers, with $\varepsilon_{R,SUB}$ ranging from 3.8 (quartz) to 11.9 (silicon). In the frequency range of interest for this work (0.05 to 20 GHz), the free space wavelength varies from 6 m to 15 mm and eqs. 5.1 and 5.2 are also largely satisfied.

The meshing options revealed to be important in the simulation of spiral inductors. Coarse meshing options usually tend to underestimate losses and give quality factors overestimated in respect to the reality. Bad meshing is usually one of the most frequent source of inaccuracies and overestimation of performances when doing EM simulations. For the simulations presented in the next paragraphs, the finest possible meshing options were used to run the simulations on a PC with 1 or 2 GB or RAM memory. All the available modeling effects like thick metallization (3-D approximations), special meshing options to tackle with the skin depth effect and the substrate RF properties were used in order to give the maximum possible accuracy in the results. Typical simulation times were in the range of 3 to 30 hours per device depending on the configuration of the computer, the geometry of the device, the complexity of the selected meshing and the number of frequency points. Usually 10 to 15 points in the frequency range of 0.05 to 15 GHz where simulated, and expanded into a larger number of points using adaptative frequency sampling and rational expansion interpolations on the S-

parameter data. This approach proved to be more effective than simulating a large number of frequency points with less accurate meshing options, since the interpolation ensures the correct values in the fixed points used to calculate the interpolated solution and showed to be capable to predict correctly the frequency values for the main inductor parameters (notably the peak quality factor f_{QMAX} and the self resonant frequency *SRF*).

5.6. HFSS simulation for a 2.5 nH inductor

In order to validate the accuracy of EM simulations done by Momentum, a reference simulation of a 2.5 nH device was performed using HFSS. The meshing used is shown if fig 5.1. Fig. 5.2 shows the current density at 2.4 GHz.

One can notice that the current distribution is not uniform along the width, suggesting that proximity effect is important for this device.

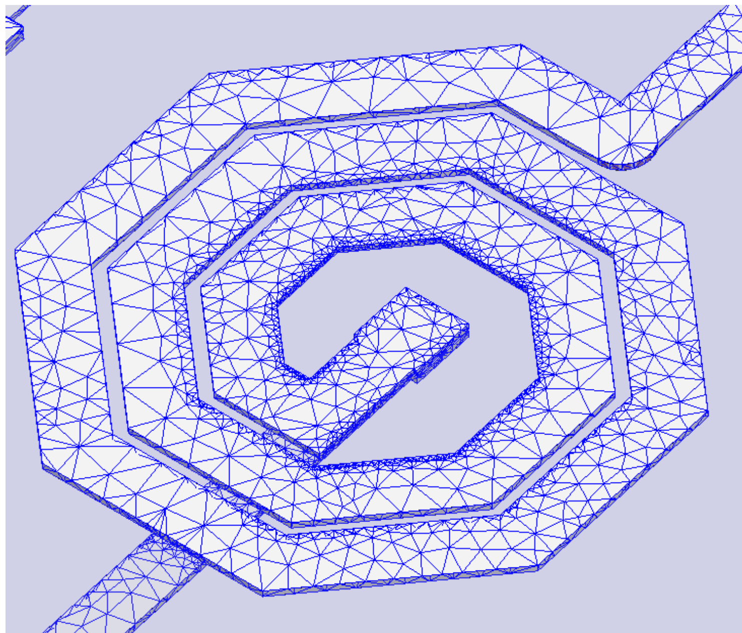


Fig. 5.1: Meshing used in the HFSS simulation of the L2n5 device. Adaptative triangular meshing generates more cells where the current density changes are more important.

The same device simulated by ADS presented similar results, with maximum 10% of differences in the main device parameters (table 5.1), confirming a consistent behavior between the 2 tools, even if ADS is frequently reported as being a limited 2-D simulation tool with limited accuracy. In fact, the version 2005 offers some 3-D functionality useful to

simulate thick-metal inductor designs that were used in the simulated designs presented in this thesis.

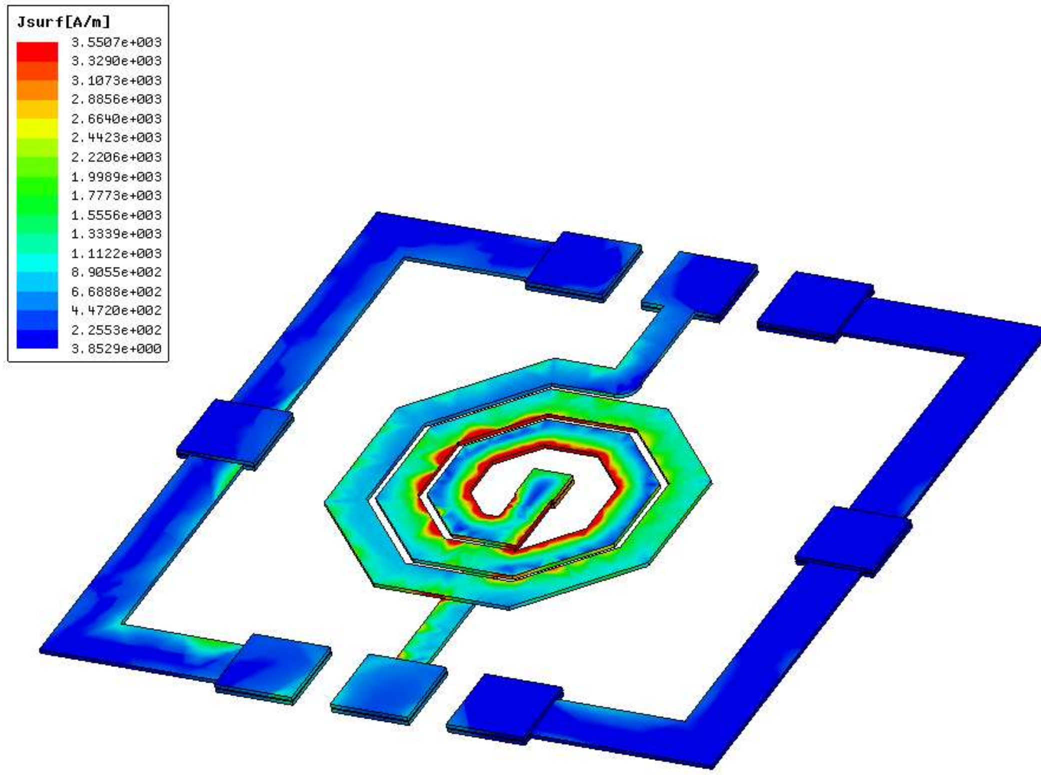


Fig.5.2: HFSS current density simulation for the L2n5 copper inductor device. The simulation is done at 2.45 GHz and shows that the current density can vary by a factor of 3 along inner track due to proximity effect (port P1 is on the top right central pad and port P2 is on the bottom left central pad).

Simulator	fQmax	Qmax	L @ Qmax	SRF	L @ 2.40 GHz	Q @ 2.40 GHz	Port
	GHz		nH	GHz	nH		
ADS version 2005a	4.38	38.4	2.55	12.14	2.33	34.2	P1
	4.56	38.7	2.56	12.56	2.33	34.2	P2
HFSS version 9.2	4.19	35.7	2.76	10.56	2.48	32.6	P1
	4.31	36.0	2.76	10.88	2.48	32.7	P2

Table 5.1: Simulation results for the L2n5 device using different tools (Agilent ADS Momentum version 2005a and Ansoft HFSS version 9.2).

The simulation options used to produce the results of table 5.1 are listed here for clarity:

- For ADS Momentum 2005a: mesh frequency = 5 GHz, mesh density = 20 cells/wavelength, edge meshing = on, transmission line mesh = on (using 5 divisions), thin overlay extraction = on, mesh reduction = off, horizontal currents = on, simulation mode = RF, thick metal expansion = yes, *MOM3D_USE_THICKLOSSMODEL = 2* (set in the *momentum.cfg* configuration file)

- For HFSS 9.2: mesh frequency = 2.5 GHz, mesh refinement passes = 12, solving inside the metal = off (using this feature would require more than 2 GB of RAM memory available to perform this simulation).

For more details about the meaning of each option, the reader should refer to the documentation of each software [Agilent 2005, Ansoft 2006].

5.7. Geometric parameter definitions

Figure 5.3 shows the cross section view along the thickness of a typical spiral inductor device. The outer diameter D_{OUT} is defined as the outmost distance between two parallel segments. The inner diameter D_{IN} is defined as the innermost distance between 2 parallel segments. The track width is w, and the track spacing is s. The example device in fig. 5.3 has $n = 2$ turns.

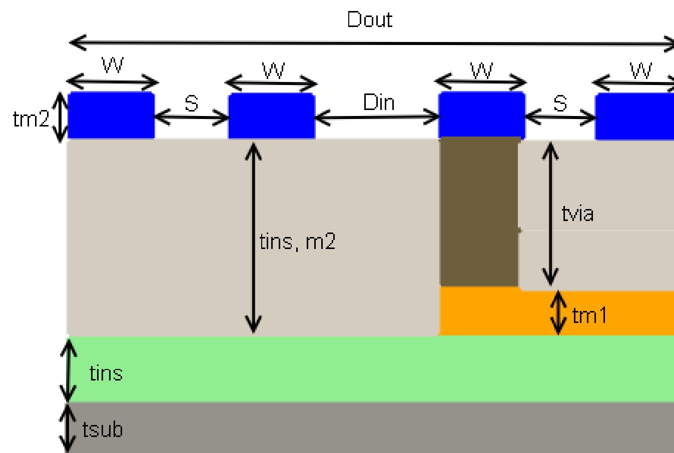


Fig. 5.3: Cross section view of a spiral inductor with the definition of the main geometrical parameters.

The total length l_{SQ} of a square spiral is given exactly by:

$$l_{SQ} = 4n(D_{OUT} - w) - (2n-1)^2(w+s) \quad \text{(eq.5.4).}$$

For a N_S-sided polygonal spiral, the total spiral length l_{POLY} can be calculated exactly from its geometrical parameters as:

$$l_{POLY} = n\,N_S \tan\frac{\pi}{N_S}\left[D_{OUT} - w + 0.5(w+s) - \frac{(n\,N_S - 1)(w+s)}{N_S}\right] \quad \text{(eq.5.5).}$$

Exact circular spiral length l_{CIRC} can be found by taking $N_S \rightarrow \infty$ in eq. 5.5:

$$l_{CIRC} = \pi\, n \left[D_{OUT} - w - (n - 0.5)(w + s) \right] \qquad \text{(eq.5.6).}$$

Ignoring the polygonal line length variation between consecutive segments, one can find an approximation considering the spiral as made of polygons circumscribed in concentric circles as:

$$l_{POLY} \cong n\, N_{SIDES}\, D_{AVG} \tan \frac{\pi}{N_{SIDES}} \qquad \text{(eq.5.7).}$$

For a circular spiral, this approximation gives:

$$l_{CIRC} \cong \pi\, n\;\; D_{AVG} \qquad \text{(eq.5.8).}$$

Eqs. 5.7 and 5.8 give an overestimation between 2 and 5% on the real value of the length, depending on the form and on the $(w+s)/D_{OUT}$ ratio of a given spiral.

The lateral perimeter of a spiral is important when parasitic fringing capacitances are specified, and can be defined as being simply 2 times the length. For short spirals or rectangular segments, a term $2w$ should be added giving in general: $P = 2l + 2w$.

The interspiral length (the length of the middle line between two adjacent segments) can be calculated replacing D_{OUT} by $D_{OUT}' = D_{OUT} - w - s$, and the number of turns n by $n' = n-1$ in eq. 5.4 to 5.7.

Some spiral software or formulae use the internal diameter instead of the external one. This parameter can be easily obtained from the others as:

$$D_{IN} = D_{OUT} - 2\left[n(w+s) - s \right] \qquad \text{(eq.5.9).}$$

Other spiral software use the center to center track distance diameter, that can be simply calculated as $D_{CENTER} = D_{OUT} - w$. ASITIC uses a very particular definition for polygonal

spirals, which is the radius R of the circle containing the spiral. The outer diameter can be obtained from this one as:

$$D_{OUT} = 2R\cos(\pi / N_S) - (1/2 - 1/N_S)(w + s) + w \qquad \text{(eq.5.10).}$$

In other contexts, like for deducing inductance calculation formulae, the average diameter is more meaningful, and can be calculated as the average between the external and internal ones:

$$D_{AVG} = \frac{D_{OUT} + D_{IN}}{2} = D_{OUT} - n(w + s) + s \qquad \text{(eq.5.11).}$$

The metal area used by the spiral is useful when calculating parallel plate equivalent capacitance, and is given simply by the width and the length of the spiral:

$$A_{METAL} = l \cdot w \qquad \text{(eq.5.12).}$$

5.8. Inductor design space

For copper / polyimide inductors fabricated on top of silicon substrates, a number of devices were designed to attain fixed values of inductance (mainly 2, 5 and 10 nH) at different optimal frequencies (2.45, 1.0 and 0.8 GHz). The device geometries studied are shown in table 3.4 (chapter 3). These same devices were fabricated on top of low resistivity (0.3 to 20 Ω cm) and high resistivity (> 8 kΩ cm) substrates in order to evaluate the influence of this parameter in the performance of the devices.

For glass inductors, a different approach was used. In order to validate the modeling methodology and generate useful device information covering the largest possible area in the given design space without increasing too much the number of devices to fabricate and measure. A design-of-experiments (DOE) approach were used to produce a set of 21 devices covering nominal initial inductance values of 2, 5 and 10 nH approximately. The outer diameter values were fixed to be 220 μm, 400 μm and 800 μm, the track width to be 10 μm, 20 μm or 40 μm, the track spacing to be 8 μm or 12 μm the for number of sides to be 4 (square), 8 (octagon) or 32-sided polygons (almost circular). The number of turns was

adjusted to give the desired inductance when all the other parameters are fixed by solving the eq. 2.30 for the nearest half number of turns. The studied devices are summarized in the table 5.2. A schematic view of the geometry of devices is shown in fig. 5.4.

	L (nH)	Dout (µm)	w (µm)	s (µm)	Ns	n
Ldoe 1	1.3	220	10	12	32	2
Ldoe 2	1.3	220	10	8	32	2
Ldoe 3	1.3	220	10	8	8	2
Ldoe 4	1.3	400	40	12	32	1.5
Ldoe 5	1.3	400	40	8	32	1.5
Ldoe 6	4.3	400	20	12	32	3
Ldoe 7	4.3	400	20	8	4	2.5
Ldoe 8	4.3	400	20	8	32	3
Ldoe 9	4.3	400	10	12	8	2.5
Ldoe 10	4.3	800	40	8	4	1.5
Ldoe 11	4.3	800	20	12	32	1.5
Ldoe 12	4.3	800	20	8	32	1.5
Ldoe 13	4.3	800	20	12	8	1.5
Ldoe 14	9.3	400	10	8	32	4
Ldoe 15	9.3	400	10	8	8	4
Ldoe 16	9.3	800	40	12	4	2.5
Ldoe 17	9.3	800	40	8	4	2.5
Ldoe 18	9.3	800	40	12	32	3
Ldoe 19	9.3	800	40	8	32	3
Ldoe 20	9.3	800	10	12	4	2
Ldoe 21	9.3	800	20	12	8	2.5

Table 5.2: Geometrical description of the 21 inductors fabricated in this study.

5.9. Influence of the RF pads and ground rings on the RF performance of spiral inductors

In this paragraph the influence of the RF pads and ground rings on the performance of spiral inductors is studied. These pads are necessary to have RF probing and external circuit contact access to the device, and should be designed in such a manner to do not impact too much the performance of the device.

The major effects are image currents introduced by having the routing around the device (what decreases the total inductance value) and some additional parasitic coupling between the device and the ground lines. RF pads add substrate coupling which can be translated into additional capacitance in general additional substrate losses when the pads are large and the resistivity of the substrate is low.

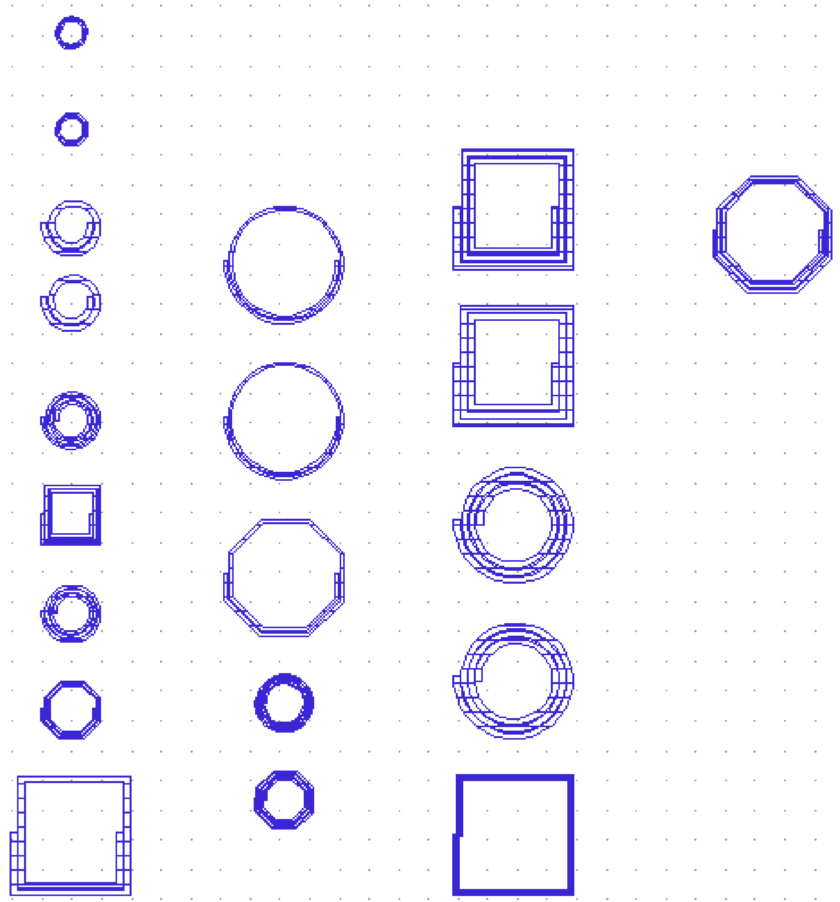


Fig. 5.4: Comparative view of the 21 inductors fabricated in this study (see table 5.2 for geometrical parameter details).

Figure 5.5 shows the top view of different devices simulated in order to verify the impact of the RF pads on the performance of a 2.5 nH octagonal inductor. This octagonal device has n = 2.5 turns, D_{OUT} = 450 µm, w = 45 µm and s = 10 µm. Simulations of the same device were performed on top of high resistivity (8 kΩ cm) and low resistivity (0.3 Ω cm) substrates, for different routing schemes showed in fig. 5.5.

Fig. 5.6 shows the simulated quality factor the each one of these configurations (on top of a high resistivity 8 kΩ cm substrate).

The same simulations were performed for the same device geometry, but using a 0.3 Ω.cm low resistivity substrate in order to verify if this tendency have a dependency on the type of substrate used. The results are shown in the table 5.3.

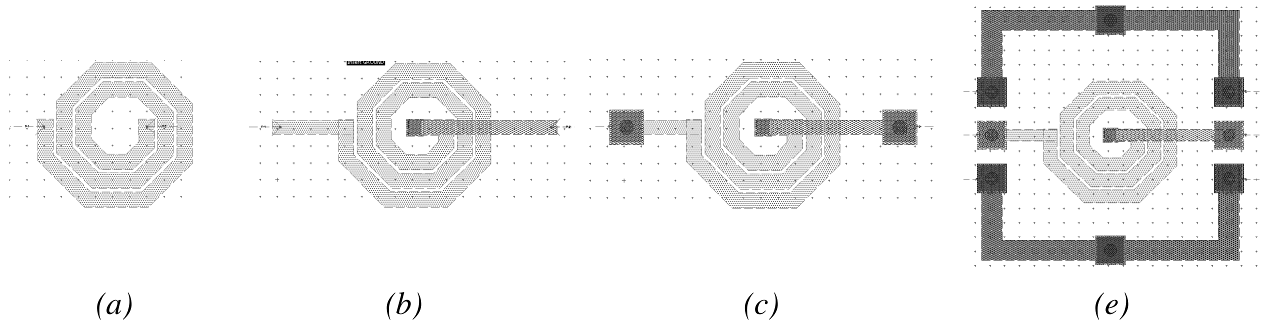


Fig. 5.5: Break down of a spiral inductor design in (a) naked spiral, (b) spiral + access lines, (c) spiral + access lines + contact pads, (d) spiral + access lines + contact pads + ground ring (complete device used in fabrication and measurements).

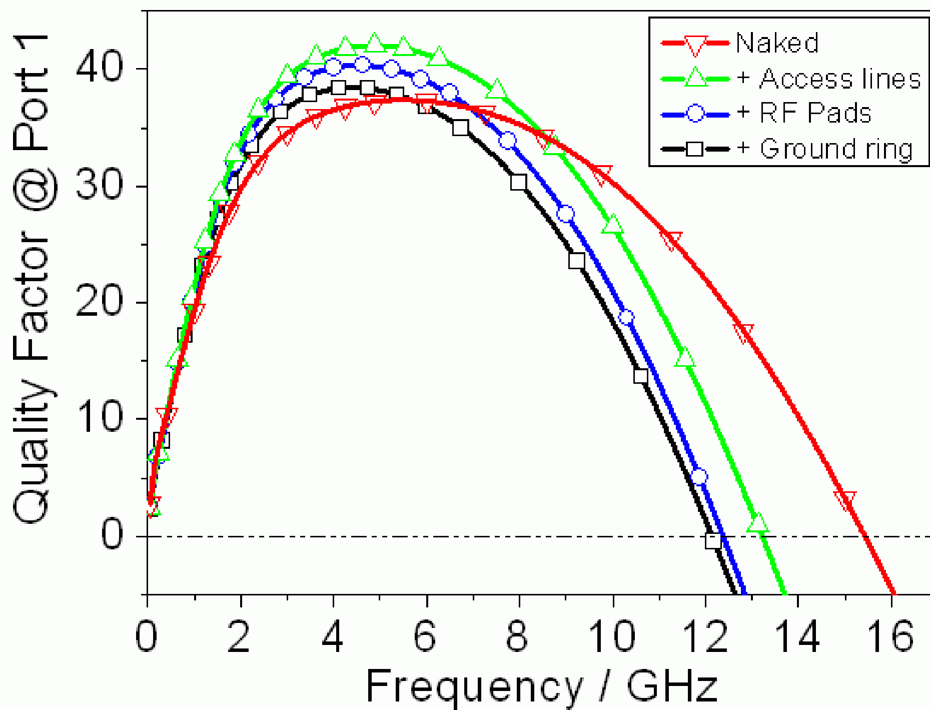


Fig. 5.6: Quality factor of the different spiral inductor designs of fig. 5.5 built on top of an 8 kΩ cm silicon substrate.

Device	fQmax (GHz)	Qmax	Lqmax (nH)	SRF (GHz)	L (1 GHz)	Q (1 GHz)	R (1 GHz)	Port
Naked spiral	5.50	37.37	2.08	15.44	1.87	19.37	0.61	**P1**
	6.13	38.27	2.07	17.48	1.87	19.38	0.61	**P2**
Added access lines	4.94	42.04	2.45	13.22	2.17	21.47	0.63	**P1**
	4.75	41.88	2.42	13.36	2.17	21.45	0.63	**P2**
Added pads	4.50	40.37	2.39	12.38	2.13	21.07	0.64	**P1**
	4.50	40.51	2.38	12.70	2.13	21.07	0.63	**P2**
Added ground ring	4.38	38.45	2.55	12.14	2.28	20.36	0.70	**P1**
	4.56	38.68	2.56	12.56	2.28	20.37	0.70	**P2**

Table 5.3: Extracted parameters for the devices of fig. 5.5 built on top of a high resistivity silicon wafer (8 kΩ cm): peak quality factor parameters, self resonant frequency and parameters at 1 GHz for both port 1 (left side) and port 2 (right side).

Device	fQmax (GHz)	Qmax	Lqmax (nH)	SRF (GHz)	L (1 GHz)	Q (1 GHz)	R (1 GHz)	Port
Naked	2.63	29.72	2.02	8.47	1.89	19.19	0.62	P1
	2.63	29.27	2.02	8.70	1.88	19.16	0.62	P2
Added access lines	2.38	31.56	2.38	7.17	2.19	21.15	0.65	P1
	1.38	21.18	2.44	3.92	2.30	19.42	0.74	P2
Added pads	1.56	22.98	2.38	4.60	2.22	19.74	0.71	P1
	1.22	19.03	2.42	3.42	2.31	18.28	0.79	P2
Added ground ring	1.63	23.25	2.54	4.80	2.37	19.42	0.77	P1
	1.31	19.70	2.58	3.67	2.44	18.35	0.84	P2

Table 5.4: Extracted parameters for the devices of fig. 5.5 on top of a low resistivity silicon wafer (0.3 Ω cm): peak quality factor parameters, self resonant frequency and parameters at 1 GHz for both port 1 (left side) and port 2 (right side).

As conclusion from this study, it is clear that that both ground rings and RF pads have an important influence on the performance of the spiral inductor and should be taken into account when modeling the device. All the important parameters are affected by the access lines parasitics and surrounding RF connections.

5.10. Effect of metallization thickness and substrate resistivity

In this paragraph, the influence of the substrate resistivity and the top metal thickness on the performance of a 2.1-nH nominal spiral inductor is analyzed. This device is a square spiral having D_{OUT} = 450 μm, w = 40 μm and s = 10 μm. Two different substrate resistivities were simulated: low resistivity silicon (LR-Si) at 0.3 Ω cm and high resistivity silicon (HR-Si) at 8 kΩ cm. Two different top metal thicknesses were also simulated, t_{M2} = 5 μm and t_{M2} = 8 μm. The results are shown in table 5.5 and fig. 5.7 respectively.

Thickness / Substrate	fQmax (GHz)	Qmax	Lqmax (nH)	SRF (GHz)	L (1 GHz)	Q(1 GHz)	R (1 GHz)	Port
t(M2) = 5um, LR-Si	1.56	27.21	2.63	4.70	2.46	23.05	0.67	**P1**
	1.28	23.01	2.67	3.61	2.54	21.68	0.74	**P2**
t(M2) = 8 um, LR-Si	1.41	29.67	2.50	4.90	2.40	27.62	0.55	**P1**
	1.16	26.23	2.54	3.69	2.48	25.89	0.60	**P2**
t(M2) = 5 um, HR-Si	4.31	45.76	2.67	11.75	2.37	24.09	0.62	**P1**
	4.50	46.05	2.69	12.04	2.37	24.09	0.62	**P2**
t(M2) = 8 um, HR-Si	4.25	45.77	2.66	11.75	2.37	24.09	0.62	**P1**
	4.44	46.04	2.67	12.04	2.37	24.09	0.62	**P2**

Table 5.5: EM simulated performance of a 2.1 nH nominal inductor (L2n1_450) as function of the top metal thickness t(M2) and the resistivity of the substrate.

Increasing the thicknesses from 5 to 8 μm does not increase significantly the quality factor, mainly because the resistance of the metal tracks is limited by the skin effect. At 2 GHz and 5 GHz (peak of the quality factors) the skin depth on copper (eq. 2.36) is equal to about 1.5 μm

and 1.0 µm respectively. On the other hand, increasing the resistivity of the substrate can increase the quality factor by about 50%, suggesting that at very high frequency the substrate related losses are the dominating ones when using thick metal layers ($t > 4$ µm).

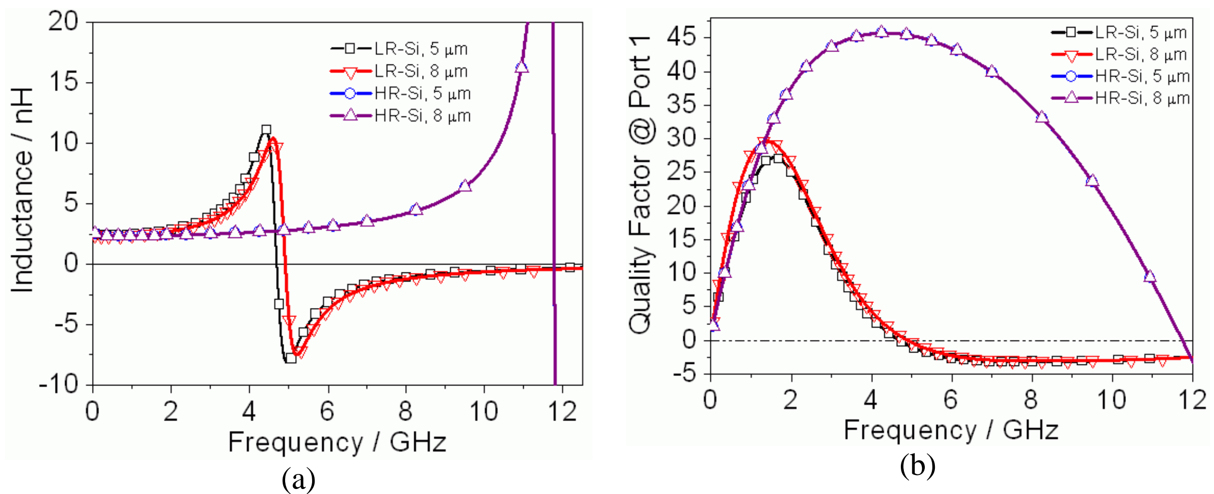


Fig. 5.7: Inductance (a) and quality factor (b) plots for the L2n1_450 device as function of the frequency for different substrate resistivity (LR – low resistivity and HR – high resistivity) and different top metal thicknesses (5 µm and 8 µm). For the high resistivity substrate, 5 and 8µm curves cannot be clearly distinguished.

5.11. Physics based model for spiral inductors

As discussed before, physics-based model for spiral inductors are difficult to set since there are many important physical phenomena occurring in parallel that affects the performance of the device. On the other hand, a physics, scalable based model is highly desirable in order to perform fast simulations, generate equivalent circuit models and give insight about the design trade-offs and possible optimizations. An accurate physics-based model for spiral inductors based on transmission line equations is proposed in the following paragraphs.

5.11.1. Spiral losses

The series resistance R_S is responsible for most of the losses in the device. Chapter 2 presented a model proposed by Yue in 2000, which is probably the most referenced one [Yue 2000]. Many other models are presented in the literature. Some of them seem to be more adequate for spiral inductors made of rectangular cross section striplines [Massin 2002, Neagu 1997, Lotfi 1995, Pettenpaul 1988]. An overview of the results given by these various models as function of the frequency for a typical microstrip rectangular line having $w = 20$ µm and $t =$

5 µm is shown in fig. 5.8. This figure shows the ratio $K_R(f) = R(f) / R_{DC}$ defining the resistance increase factor as function of the frequency. w_N and t_N are defined as the normalized width and thickness as function of the skin depth: $w_N = w/\delta$ and $t_N = t/\delta$ respectively. In the frequency range of interest for this work, the skin effect will limit a lot the current, giving a factor K_R than can represent many times the DC resistance. Although all these models scale well $\sqrt{f}$, suggesting that they do take skin effect limited current flow into account. The large differences between them come from the assumptions done in the approximations of each model or device studied in the specific papers can result in large differences between the estimation of the resistance using these models.

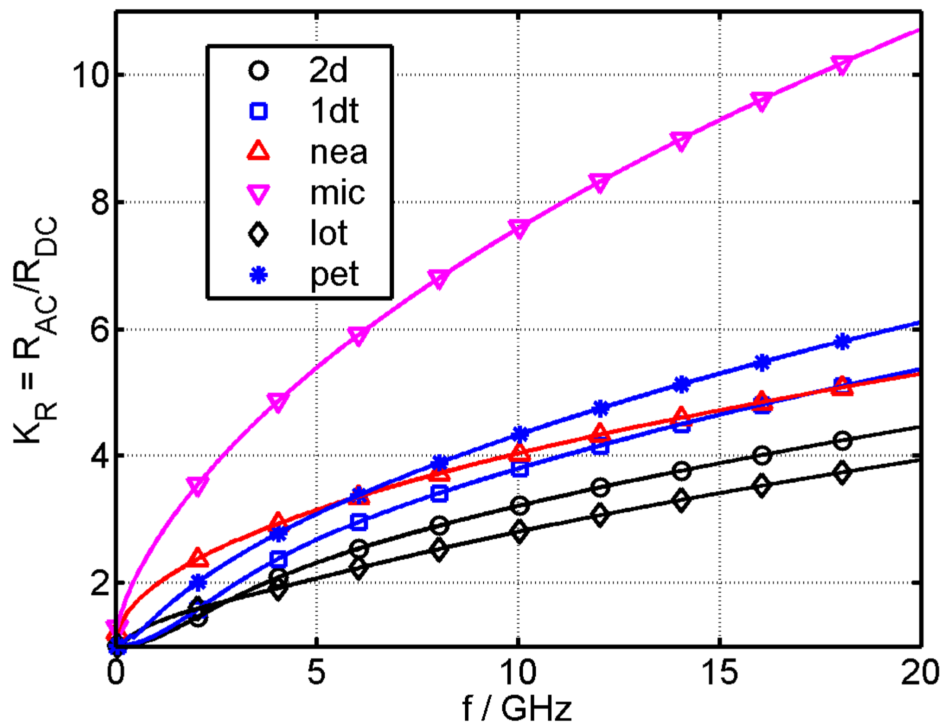


Fig. 5.8: AC resistance increase factor for a microstrip line having w = 20 µm and t = 5 µm as function of the frequency for different models proposed in the literature: 1-D [Jackson 1975], 2-D approximations [Massin 2002], [Neagu 1997], microstrip approximation [Yue 2000], [Lotfi 1995] and [Pettenpaul 1988].

ADS momentum and ADS Libra (using MLIN component – microstrip line [Hammerstad 1980]) simulations were conducted in order to evaluate the best model for a stripline with typical dimensions used in spiral inductors studied in this work. The results are shown in fig. 5.9. ADS and Libra give similar results for higher resistivity substrates, and Libra plots were

omitted for clarity. The influence of the type and resistivity of the substrate is also shown comparatively to the resistance of a microstrip having only air as surrounding dielectric.

Appendix A presents a detailed discussion on the approximations used in each model and make comparisons between them and results obtained by 3D EM simulations performed using Fasthenry.

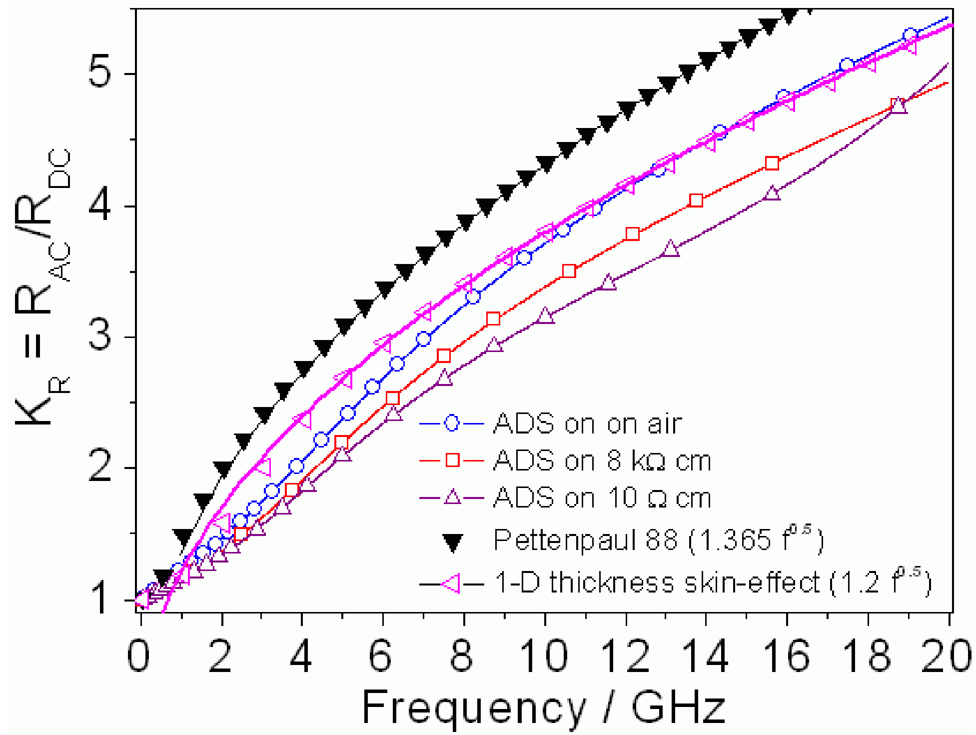


Fig. 5.9: Comparison between various resistance calculation models and ADS Momentum and Libra simulations performed on top of different substrates.

Direct comparison with full-wave simulations suggests that the model presented in [Pettenpaul 1988] is the most accurate one over a large sampling of device geometries and working frequencies. This model calculates the AC resistance as:

$$R_{AC}(w,t,f)=\begin{cases}\dfrac{l}{\sigma wt}\left[\dfrac{0.43093p}{1+0.041(t/w)^{1.19}}+\dfrac{1.1147+1.2868p}{1.2296+1.287p^{3}}+0.0035(t/w-1)^{1.8}\right] & if\ \ p\geq 2.5\\ \dfrac{l}{\sigma wt}\left[1+0.0122p^{(3+0.01p^{2})}\right] & if\ \ p<2.5\end{cases} \quad \text{(eq.5.13)},$$

where

$$p = \sqrt{2 f \sigma \mu w t} = \frac{1}{\delta}\sqrt{\frac{2wt}{\pi}} \quad \text{(eq.5.14),}$$

is a non dimensional parameter defined as the "normalized frequency".

This model also gives similar results of ones obtained by rigorous partial element equivalent circuit (PEEC) analysis [Antonini 1999, Weeks 1979] and by the approximated 1-D skin depth effect taken only along the thickness [Jackson 1975].

For copper conductors, the following empiric relation was observed to represent well the resistance as function of the frequency above 1 GHz (compatible with the one presented in [Abdo-Tuko 1993]):

$$R_{AC} = 1.3\sqrt{\frac{f}{1\,GHz}} R_{DC} \quad \text{(eq.5.15).}$$

The dependency of the losses with the substrate properties will be addressed in the next paragraphs.

The thin microstrip line model [Yue 2000], is valid only at low frequencies (below 2 GHz) and for thin strips ($t < 2\delta$), and cannot be used for thick metal spirals working at high GHz range.

For spiral inductors, it is also important to consider the properties of the substrate as well as the coupling between neighbor tracks. Fig. 5.9 suggests that the properties of the substrate affects the overall propagation properties of any transmission line and should be taken into account even for non-coupled single microstrip lines built on top of silicon.

5.11.2. Current crowding effect

Current crowding is the effect of having an increase in the AC resistance on the inner tracks of a spiral inductor due the concentration of the current caused by the magnetic field produced

by the external turns. The most referenced empirical model proposed in the literature for this phenomenon is proposed by [Kuhn 2001], by defining a critical frequency f_{CRIT} where the current crowding effect becomes important. This frequency is given by:

$$f_{CRIT} = \frac{3.1(w+s)}{2\pi\mu w^2} R_{SH} \qquad \text{(eq.5.16)},$$

where w and s are the width and spacing of the spiral inductor and R_{SH} is the sheet resistance of the spiral metal. Above this frequency, the resistance increase due to the current crowding effect is supposed to vary quadratically with the frequency as:

$$R_{CROWD} = R_{DC}\left[1 + 0.1\left(\frac{f}{f_{CRIT}}\right)^2\right] \qquad \text{(eq.5.17)}.$$

This equation is only a rough approximation valid only for the devices studied in the reference article. It does not take into account the number of turns, the form or the diameter of the spiral inductor, and in general can highly overestimate the AC resistance of a spiral. Figure 5.10 shows a plot of this equation for a spiral inductor having w = 20 µm, s = 5 µm and R_{SH} = 2.0 µΩ cm / 5 µm = 4 mΩ / sq.

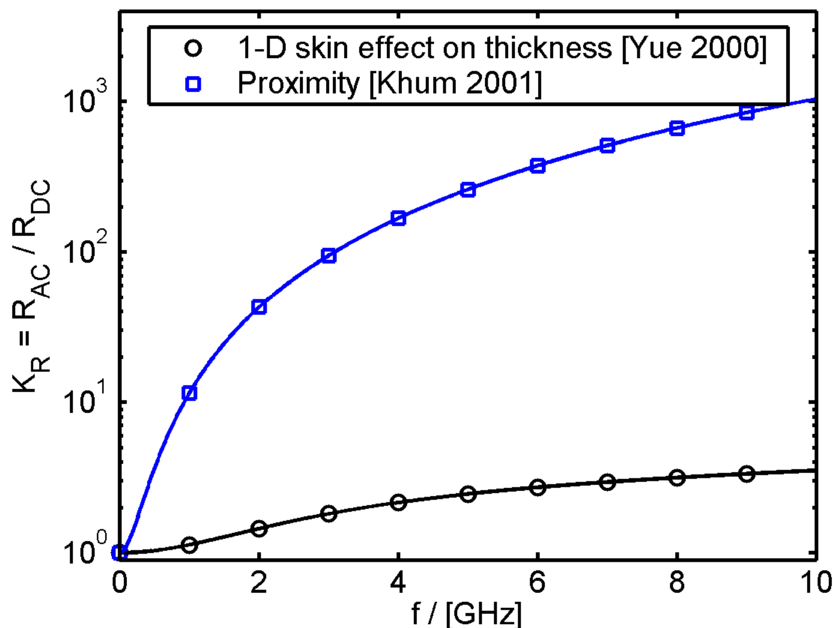


Fig. 5.10: Plot of current crowding increase resistance factor $K_R(f) = R_{CROWD}(f) / R_{DC}$ (eq. 5.17) as function of the frequency (w = 20µm, s=5µm, t = 5µm). The thin microstrip approximation (eq. 2.35, [Yue 2000]) is also shown for comparison.

This model clearly overestimates the importance of the current crowding effect, which contributes only with a fraction of the increase resistance with respect to the skin effect contribution. More accurate models for this phenomenon needs long simulation and measurement-based effort that is beyond the scope of this thesis. Such modeling effort should be capable to predict the increase in the resistance as function of the geometrical parameters of the spiral inductor and the frequency, without overlapping with other frequency-dependent phenomena, namely the skin effect.

5.11.3. Coupled strip line model for spiral inductors

In the following paragraphs, a transmission line-based model for spiral inductors will be proposed, based on coupled strips (CPS) equations. This model will suppose that adjacent tracks can be treated as parallel striplines, which is a reasonable approximation for large polygonal inductors or inductors having low number of sides per turn (namely squares and octagons). On the other hand, this model will take into account only the coupling between adjacent inductor segments, neglecting the interaction between a given segment and other ones farther away than the closest neighbor.

This model involves the evaluation of the characteristic impedance Z_0 of the transmission line and its capacitance per unit length C'. For the quasi-static approximation and at moderate losses in a non magnetic medium ($\mu_R = 1$), these parameters are related as:

$$Z_0 \cong \frac{1}{\sqrt{L'C'}} = \frac{1}{\sqrt{L'\varepsilon_{R,EFF} C_0^{'}}} = \frac{1}{\sqrt{\varepsilon_{R,EFF}}} Z_0^{AIR} \qquad \text{(eq.5.18)},$$

where L' is the inductance per unit length, $\varepsilon_{R,EFF}$ is the effective relative dielectric constant, C_0' is the capacitance per unit length in the absence of any dielectric (when the CPS line is surrounded only by air) and Z_0^{AIR} is the characteristic impedance of the CPS line calculated in the absence of any other dielectric than air.

An analytical solution for the quasi-static TEM case is possible by using Schwarz-Christoffel transformation and conformal mapping [Kirschning 1984, Gupta 1996, Churchill 1996, Simons 2001]. For the CPS on air, the capacitance per unit length is given by:

$$C'_{CPS,0} = \varepsilon_0 \frac{K(k)}{K(k')} \quad \text{(eq.5.19)},$$

with

$$k' = \sqrt{1-k^2} = \frac{s}{s+2w} \quad \text{(eq.5.20)},$$

where *K(k)* is the complete elliptic integral of the first kind [Spiegel 1968], *k* and *k'* are the arguments for the elliptic integral defined as function of the strip width *w* and spacing *s*.

The following approximations are useful to numerically evaluate the ratio *K(k) / K(k')*, which frequently appears in coupled strips transmission line problem formulations [Hilberg 1969]:

$$\frac{K(k)}{K(k')} = \begin{cases} \dfrac{\pi}{\ln\left[\dfrac{2(1+\sqrt{k'})}{(1-\sqrt{k'})}\right]}, & 0 \le k \le \dfrac{1}{\sqrt{2}} \\ \dfrac{1}{\pi}\ln\left[\dfrac{2(1+\sqrt{k})}{(1-\sqrt{k})}\right], & \dfrac{1}{\sqrt{2}} \le k \le 1 \end{cases} \quad \text{(eq.5.21)}.$$

These approximations give a maximum relative error of $3 \cdot 10^{-6}$ at $k = 1 / \sqrt{2}$.

A complete solution for multi layer dielectrics is possible by calculating partial capacitances due to each individual dielectric layer. A detailed treatment for this problem is given in the literature [Gupta 1996, Chen 1997, Simons 2001]. The effective relative dielectric constant is given by the ratio of the actual capacitance C_{CPS} by the one $C_{CPS,0}$ having no other dielectric medium than air.

$$\varepsilon_{R,EFF}^{CPS} = \frac{C'_{CPS}}{C'_{CPS,0}} = 1 + \frac{1}{2}\frac{K(k)}{K(k')}\left[(\varepsilon_R^{A1} - 1)\frac{K(k_{A1})}{K(k'_{A1})} + (\varepsilon_R^{A2} - \varepsilon_R^{A1})\frac{K(k_{A2})}{K(k'_{A2})} + (\varepsilon_R^{A3} - \varepsilon_R^{A2})\frac{K(k_{A3})}{K(k'_{A3})} + \ldots\right.$$
$$\left.(\varepsilon_R^{B1} - 1)\frac{K(k_{B1})}{K(k'_{B1})} + (\varepsilon_R^{B2} - \varepsilon_R^{B1})\frac{K(k_{B2})}{K(k'_{B2})} + (\varepsilon_R^{B3} - \varepsilon_R^{B2})\frac{K(k_{B3})}{K(k'_{B3})} + \ldots\right]$$

(eq.5.22),

where ε_R^{Ai} is the relative dielectric constant of the i-th layer above the CPS (summed from the top to the bottom), ε_R^{Bi} is the relative dielectric constant of the i-th layer below the CPS (summed from the bottom to the top) and k is the argument of the elliptic integral calculated as:

$$k_{Xi} = \sqrt{1 - \frac{\sinh^2(\pi a / 2h_{Xi})}{\sinh^2(\pi b / 2h_{Xi})}} \qquad \text{(eq.5.23)},$$

when the i-th layer does not have a top or bottom ground metal cover and

$$k_{Xi} = \sqrt{1 - \frac{\tanh^2(\pi a / 2h_{Xi})}{\tanh^2(\pi b / 2h_{Xi})}} \qquad \text{(eq.5.24)},$$

when the i-th layer has a top or bottom ground metal cover. The geometrical parameters a, b and h_i are defined as (fig. 5.11):

$$2a = s \qquad \text{(eq.5.25)},$$

$$2b = s + 2w \qquad \text{(eq.5.26)},$$

$$h_{Xi} = \sum_{j<i} t_{Xj} \qquad \text{(eq.5.27)}.$$

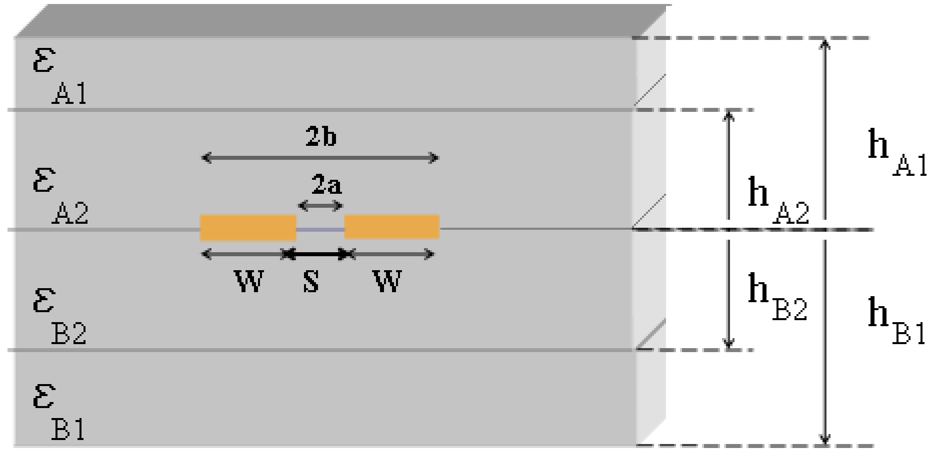


Fig. 5.11: Schematic view of a multi-dielectric sandwiched thin coupled strip lines (CPS) circuit.

Where *s* is the CPS spacing, *w* is the CPS track width, *t* is the thickness of the film above or below the line and h_{oi} is the height of the *i*-th film end above or below the line, admitted to be very thin in this first approximation. One can note that, for a stripline on air sitting on top of a substrate of a dielectric constant ε_R, the effective dielectric constant $\varepsilon_{R,EFF}$ calculated by eq. 5.22 simply give the well known $(\varepsilon_R + 1)/2$ result that appear in most of practical formulae for CPS and CPW lines built on top of a single dielectric layer.

These equations consider the thickness of the CPS line negligible. An additional term due to the parallel plate capacitance contribution due the thickness *t* of the metal line can be added:

$$C'_{TCPS} = C'_{CPS} + \varepsilon_R \varepsilon_0 \frac{t}{s} \quad \text{(eq.5.28)},$$

where the term $\varepsilon_R \varepsilon_0 t / s$ is the parallel plate capacitance per unit length contribution originated from the thickness *t* and distance *s* of the CPS line.

The characteristic impedance of the CPS line is given by [Simons 2001]:

$$Z_0^{CPS} = \frac{Z_0^{AIR}}{\sqrt{\varepsilon_{R,EFF}}} = \frac{\eta_0}{\sqrt{\varepsilon_{R,EFF}}} \frac{K(k')}{K(k)} \quad \text{(eq.5.29)}.$$

The resistance per unit length R_C' of the conductor can be calculated accurately using the current density distribution derived from the conformal imaging method [Owywang 1958, Hoffmann 1987, Royal 1989, Ghione 1993] as:

$$R_C' = \frac{Z_0 R_F \sqrt{\varepsilon_{R,EFF}}}{4\eta_0 d \cdot K(k) \cdot K(k')[1-(w/d)^2]} \times \left\{ \frac{2d}{w}\left[\pi + \ln\left(\frac{4\pi\, w(1-w/d)}{t(1+w/d)}\right)\right] + 2\left[\pi + \ln\left(\frac{4\pi\, d(1-w/d)}{t(1+w/d)}\right)\right]\right\} \quad \text{(eq. 5.30).}$$

The reader should note the correct factor in the denominator of eq. 5.30 is 4 η_0, and not 0.4 η_0 as presented in [Hoffmann 1987]. R_F is the AC surface resistance given by:

$$R_F = \sqrt{\pi f \rho \mu} = \delta / \rho \quad \text{(eq.5.31),}$$

where $d = w+2s$, $k = w/d$, $k' = \sqrt{1-k^2}$, $K(k)$ is the complete elliptic integral of the first kind, $\varepsilon_{R,EFF}$ is the effective dielectric constant and $\eta_0 \cong 120\ \pi\ \Omega \cong 377\ \Omega$ is the vacuum characteristic impedance.

The equation 5.30 is valid when $t > 3\ \delta$ and $t << w,s$. This equation gives acceptable results when $t > 2\ \delta$ and $t < (w,s)$, which is not always true for thin film inductors, but holds well for the devices studied in this thesis (having the metal thickness between 5 and 8 μm). Plots of the skin depth δ as function of the frequency for different metals (silver, copper, gold and aluminum) are shown in fig.5.12.

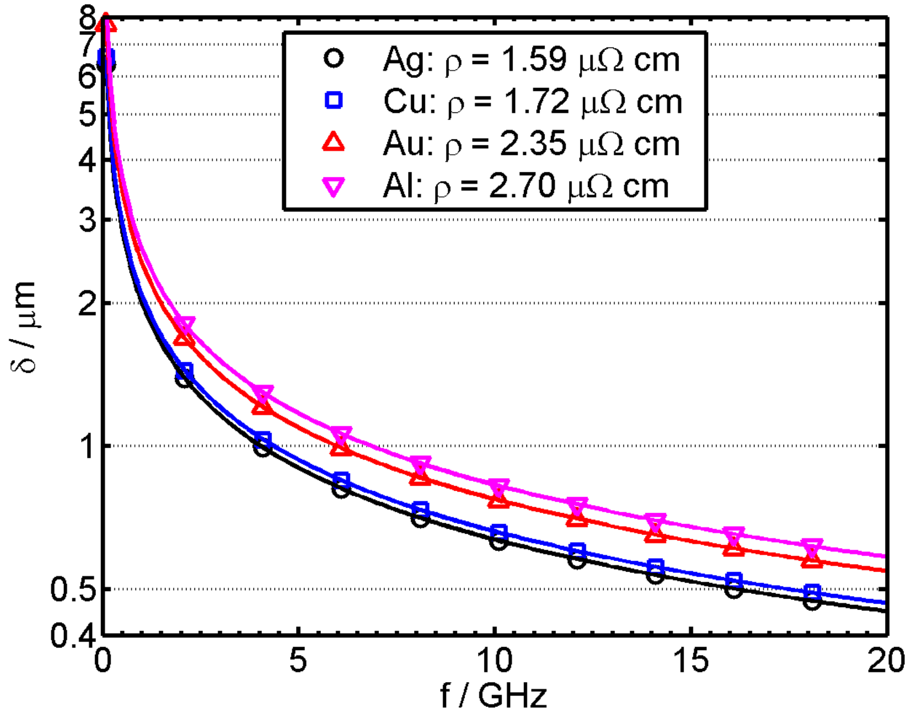


Fig. 5.12: Skin depth (eq. 2.37) for different metals as function of the frequency.

The substrate losses are taken unto account by using the complex dielectric constant of the substrate, considered as being a semi-insulating medium having a real dielectric constant ε_{SUB} and a resistivity ρ_{SUB}. The complex dielectric constant ε_{SUB}^{*} can be written as [Hoffmann 1987]:

$$\varepsilon_{SUB}^{*} = \varepsilon_{SUB} - j\frac{1}{\rho_{SUB}\omega} = \varepsilon_{SUB}(1 - j\tan\delta_{SUB}) \qquad \text{(eq.5.32)},$$

where $tan\ \delta_{SUB}$ is the loss tangent factor and ω is the angular frequency. The parallel conductance per unit length G_{SUB}'' is calculated as a function of the capacitance per unit length C' and the loss tangent factor as:

$$G_{SUB}' = \omega C' \tan\delta_{SUB} = \frac{C'}{\rho_{SUB}\varepsilon_{SUB}} \qquad \text{(eq.5.33)}.$$

The final model for the spiral inductor is represented by a transmission line with distributed parameters per unit length R_C' (eq. 5.30), $L' = L / l_{SPI}$ (eqs. 2.30 and 5.4 to 5.6), C' (eq. 5.28) and G_{SUB}' (eq. 5.33), shown schematically in fig. 5.13.

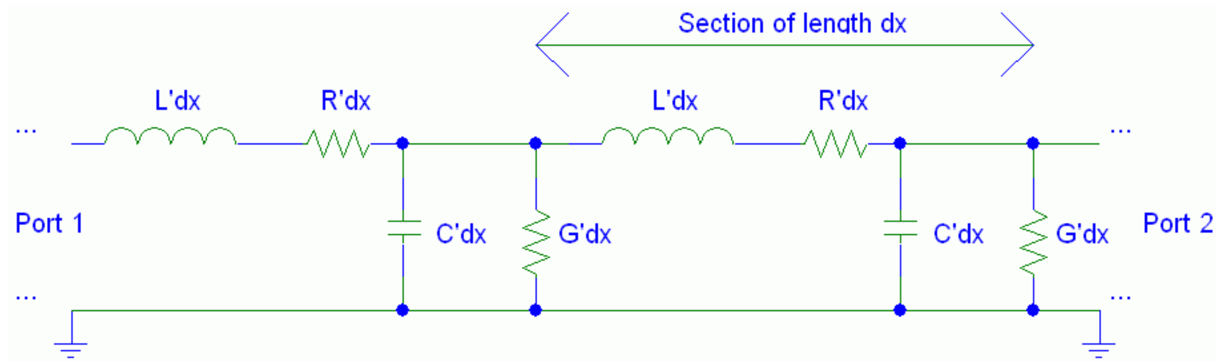


Fig. 5.13: Transmission line equivalent circuit model for a microstripe spiral inductor.

The transmission line can be discretized by choosing a number of sections large enough in order to make the model broadband as function of the frequency. The *ABCD* matrix is the preferred form to represent the line, permitting to easily associate it with another circuit blocks by simple matrix multiplication operations. The *ABCD* matrix of a lossy transmission line is given by:

$$M = \begin{pmatrix} \cosh(\gamma l) & Z_0^* \sinh(\gamma l) \\ Y_0^* \sinh(\gamma l) & \cosh(\gamma l) \end{pmatrix} \quad \text{(eq.5.34)},$$

where

$$\gamma = \sqrt{(R' + j\omega L')(G' + j\omega C')} = \alpha + j\beta \quad \text{(eq.5.35)}$$

is the propagation constant and

$$Z_0^* = \sqrt{\frac{j\omega L' + R'}{j\omega C' + G'}} \quad \text{(eq.5.36)}$$

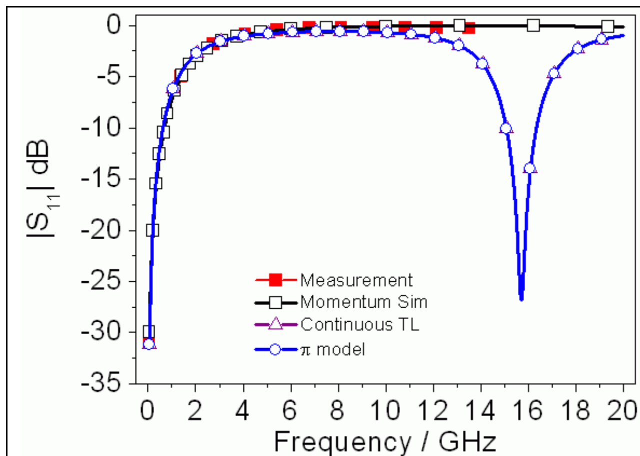
is the complex characteristic impedance and Y_0^* is simple defined as $1 / Z_0^*$.

The *ABCD* matrix can be easily converted into *S* or *Y* parameters [Pozar 1998], and the equivalent inductance and quality factor of the inductor can be determined using eq. 3.2 and eq. 3.3.

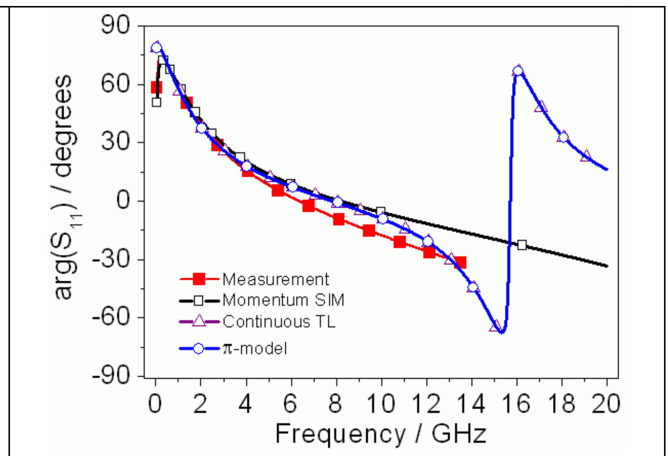
An example of the results produced by the proposed model and compared to EM simulations and measurements is shown in the next following paragraphs.

The device L_{DOE15} is analyzed in detail (table 5.2). This device is an octagonal inductor with D_{OUT} = 400, n = 4 turns, w = 10 μm, s = 8 μm, made on top of quartz substrate, for which the fabrication process was presented in chapter 4. The low frequency inductance is 8.3 nH. The other parameters of the model are $\rho = 2.0 \cdot 10^{-8}$ Ω m for the metal conductivity (copper), t = 5 μm for the metal thickness, ε_R = 3.8 for the substrate relative dielectric constant, $\rho_{SUB} = 1.0 \cdot 10^6$ Ω m for the substrate. The effective dielectric constant seen by the spiral is $\varepsilon_{R,EFF}$ = 2.4 (eq. 5.22). The gap length (eq. 5.4 to 5.6 evaluated in the mid-point between the spiral segments) is l_G = 3173 μm, and the low frequency resistance R_{DC} (eq. 2.37) is 1.75 Ω, corresponding to a spiral length of l_{SPI} = 4364 μm (eq. 5.4 to 5.6). At frequencies above 1 GHz, the resistance is well approximated by $R_{AC}(f) = 1.17\, R_{DC} \sqrt{f / 1\,GHz}$.

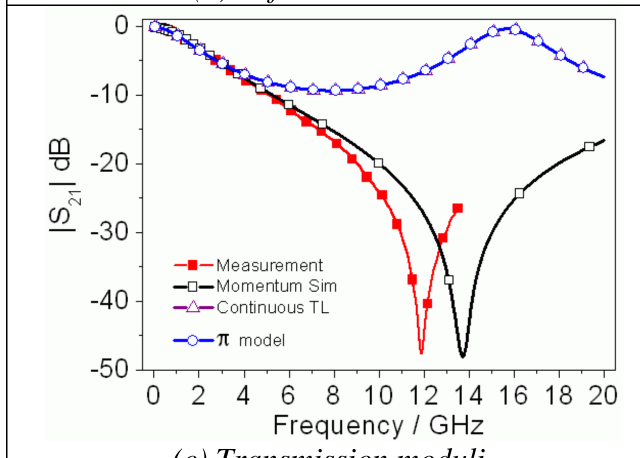
Figures 5.14a to 5.14h show the results for the extracted inductance and quality factor as function of the frequency for this device. Results obtained using ADS Momentum EM simulator are also shown. The quality of the model is confirmed by the good agreement between different parameters of the inductors, namely the low frequency inductance, the peak quality factor value and frequency position, and the value of the self-resonant frequency. The computation of the results was performed using the developed specialized Matlab toolbox [Pisani 2004d].



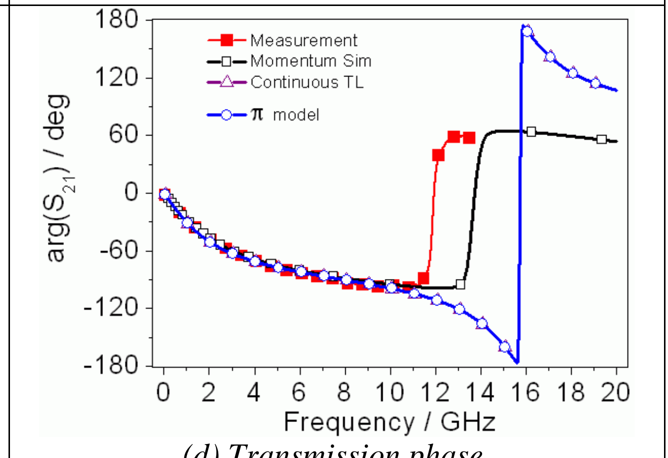
(a) Reflection moduli.



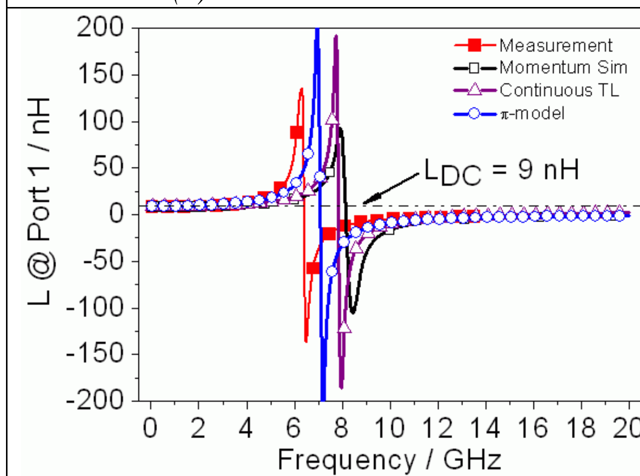
(b) Reflection phase.



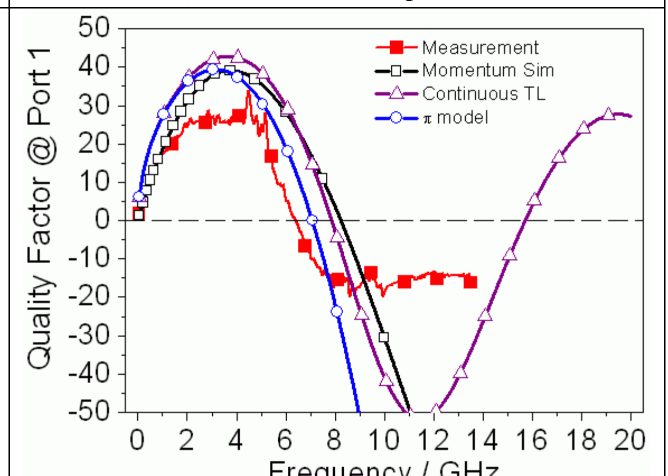
(c) Transmission moduli.



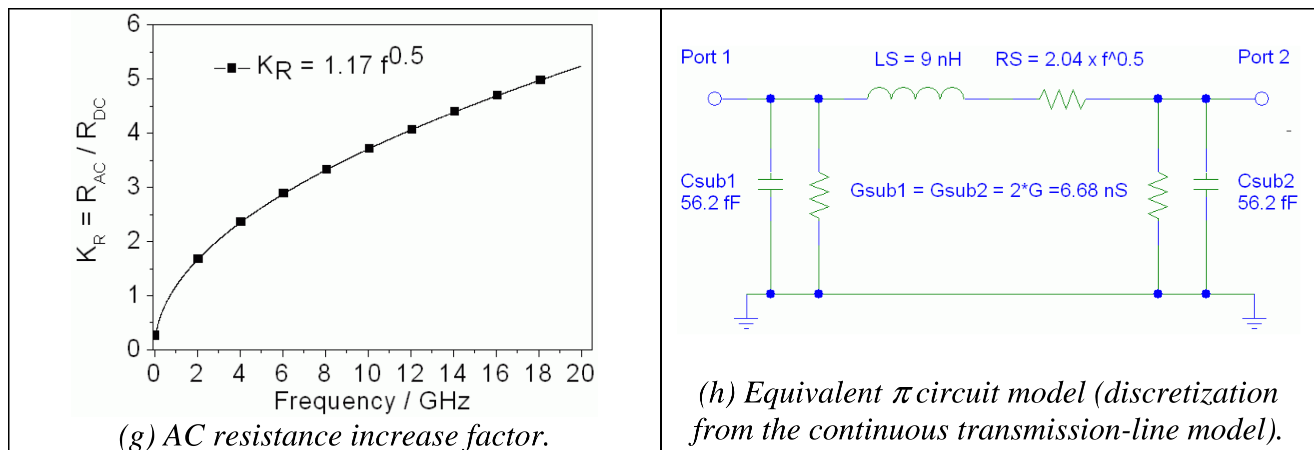
(d) Transmission phase.



(e) Effective inductance.



(f) Quality factor.



(g) AC resistance increase factor.

(h) Equivalent π circuit model (discretization from the continuous transmission-line model).

Fig. 5.14: Measured, EM simulated and proposed model results for the S-parameter data (a-d), inductance (e), quality factor (f) and equivalent π circuit model (g,h) for the L_{DOE15} 9-nH nominal inductance device.

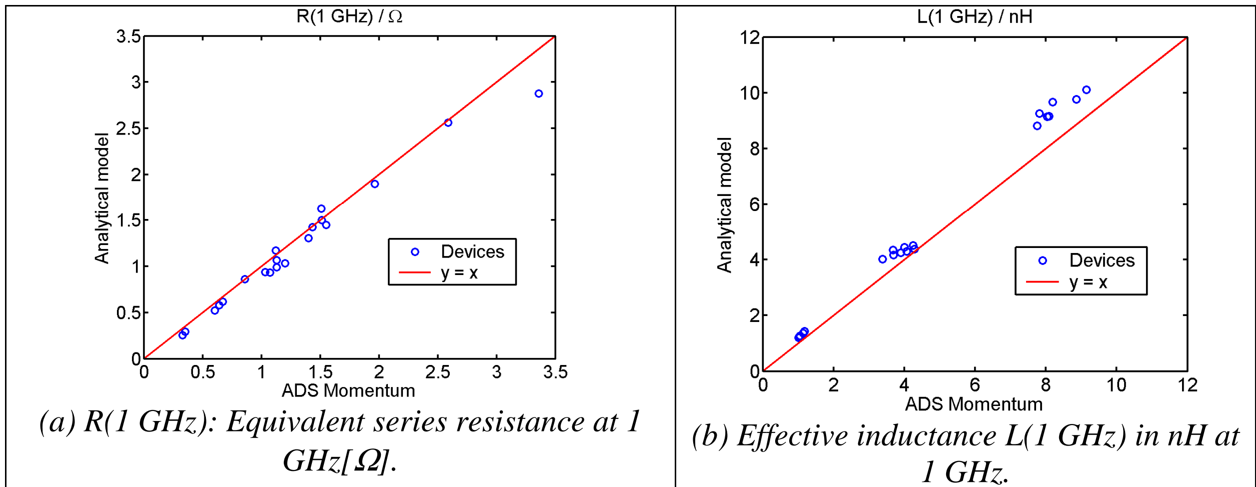
The noise observed in the quality factor extracted directly from S-parameter measurements (fig. 5.14f) comes from the instability of this method of extraction when measuring high quality factor devices. The uncertainty in the measurements is proportional to the quality factor itself, making the experimental result having more noise and uncertainty near the peak quality factor [Rebeiz 2003]. The proposed model cannot produce accurate results above the resonant frequency, mainly because the transverse electromagnetic mode of propagation (TEM) will not be valid anymore and other approximations should be used to calculate the transmission line parameters. This does not affect overall quality of the proposed model since for all practical uses inductors are considered to work below the self-resonant frequency (between 6 and 8 GHz for this device). The continuous transmission line model is the one using eq. 5.34 for the transfer matrix of the device (fig. 5.13). The π-model is a 3 section simplification of this model shown in fig. 5.14h. This model can provide good accuracy in the results by using a low order lumped RLC model when the device size is small compared to the wavelength.

5.11.4. Comparison between the analytical model and EM simulations

In this paragraph, the overall accuracy of the proposed analytical model is analyzed in comparison to full wave electromagnetic simulation results. The 21 devices described in table 5.2 were simulated using the proposed analytical model presented in the previous paragraphs as well as using ADS Momentum 2005a EM simulation tool. Various electrical parameters of the inductors were extracted from the S-parameter data (see paragraph 3.7) and from the

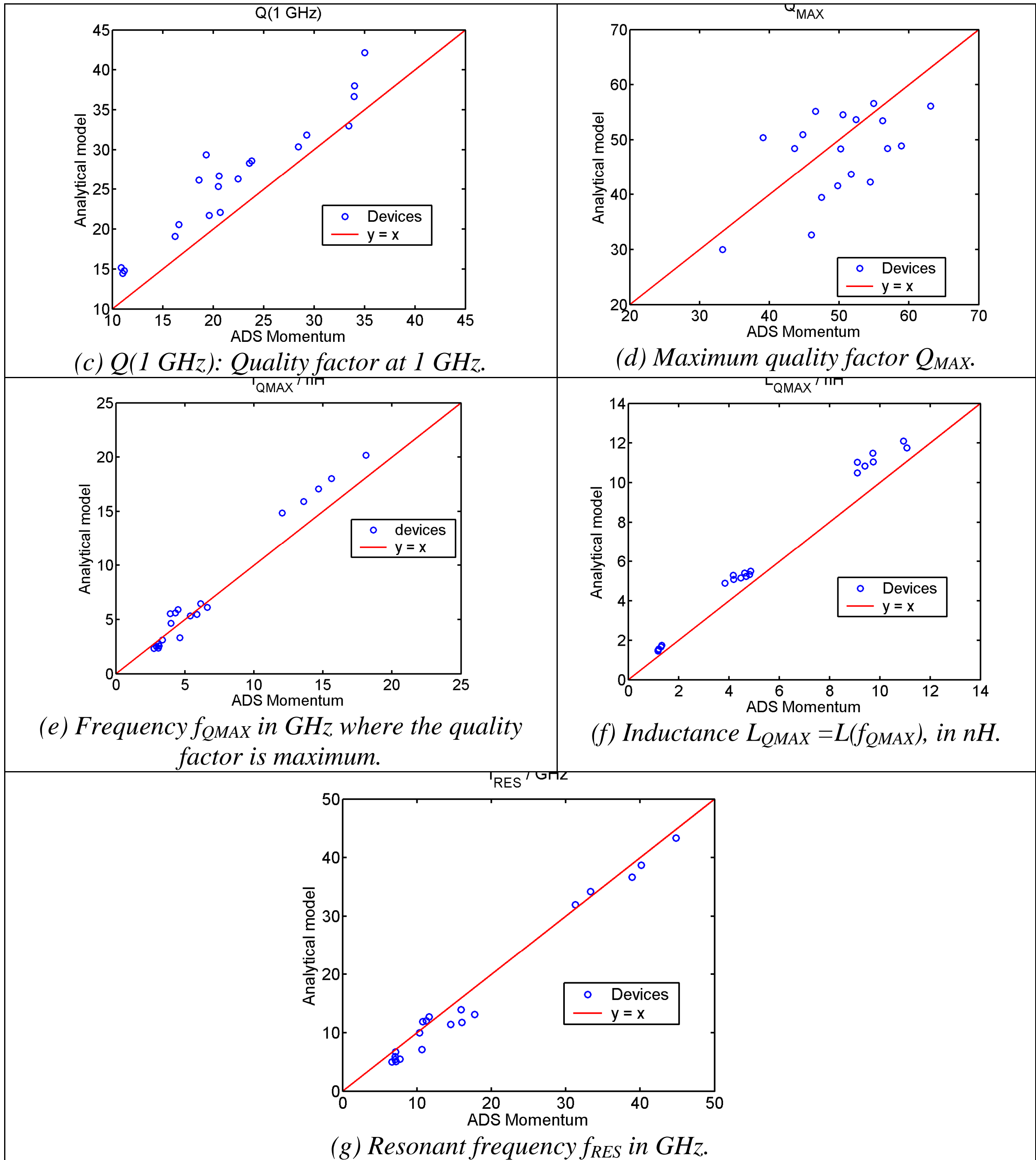
equivalent circuit parameters obtained from the analytical model (previous paragraph). Fig. 5.15 shows comparative plots between results obtained by ADS Momentum simulations (plotted in the X-axis, used as reference) and the proposed analytical model (plotted in the Y-axis). The line $Y = X$ corresponding to a hypothetical case where both results would be identical is also shown. The following representative parameters were plotted:

- *R(1 GHz)*: the equivalent series resistance evaluated at $f = 1$ GHz (frequency where the skin effect starts to become important, shown in fig. 5.15a),
- *L(1 GHz)*: the effective inductance (eq. 3.2) evaluated at $f = 1$ GHz (fig. 5.15b),
- *Q(1 GHz)*: the quality factor (eq. 3.3) evaluated at $f = 1$ GHz (fig. 5.15c),
- Q_{MAX}: the maximum value of the quality factor (fig. 5.15d),
- f_{QMAX}: the frequency for what the quality factor is maximum (fig. 5.15e),
- L_{QMAX}: the effective inductance (eq. 3.2) at the frequency where the quality factor is maximum (Q_{MAX}), shown in fig. 5.15f,
- f_{RES}: the resonant frequency where the quality factor (eq. 3.3) equals to zero (fig. 5.15g).



(a) R(1 GHz): Equivalent series resistance at 1 GHz[Ω].

(b) Effective inductance L(1 GHz) in nH at 1 GHz.



(c) Q(1 GHz): Quality factor at 1 GHz.

(d) Maximum quality factor Q_{MAX}.

(e) Frequency f_{QMAX} in GHz where the quality factor is maximum.

(f) Inductance $L_{QMAX} = L(f_{QMAX})$, in nH.

(g) Resonant frequency f_{RES} in GHz.

Fig. 5.15: Comparison between EM-simulated and analytical model results for the devices presented in table 5.1.

The better overall correlation between EM-simulated and calculated results was obtained when using an effective length slightly larger than the one calculated by replacing D_{OUT} by D_{OUT}-w-s and n by n-1 in eqs. 5.5 to 5.7 used to evaluate the effective CPS line length used in eq. 5.28, 5.30 and 5.33 to calculate the total spiral parasitics from the CPS line parameters evaluated per unit length. The best correlation between data were obtained by using an effective diameter $D_{OUT}' = D_{OUT} - 0.5(w+s)$ and an effective number of turns $n' = n - 0.5$ for

the equivalent CPS line. The effective length higher than the expected one for the inter-metal gap of the spiral is attributed to corner effects in the inductor turns, what effectively add parasitics to the device due to the discontinuities in the CPS transmission line model assumed to have constant characteristic impedance in the preceding paragraphs.

The overall accuracy of the analytical model can be considered good taking into account the wide design space covered by the 21 devices of the table 5.2. In fact, these devices were statistically designed to produce the maximum possible geometrical parameter variations for devices with inductor values of 2, 5 and 10 nH. These inductance values are also in the range of values required for the most practical applications of spiral inductors operating in the GHz frequency applications.

The predictions for the inductance values in figs 5.15b and 5.15f suggest that the analytical model gives some overestimation in the values of the inductance calculated by the current sheet model (eq. 2.29 – 2.31 and table 2.1). This is physically reasonable since this model does not take into account the dependency of the inductance with the thickness (thick metal layers being less inductive than thin ones). This is one of the reasons that make the analytical model probably overestimate the quality factors (fig. 5.15c and 5.15d). The quality factor is directly proportional to the inductance for a given fixed frequency. The quality factor is certainly the most difficult parameter to be accurately modeled since it depends on a complex combination of all the parasitic parameters of the device (eq. 2.32 – 2.34 shows how it depends on these parameters for a simple π network). A complete analysis should also consider the accuracy of the simulation tool, since it was used as reference to present the dispersion in the results, the plotted curves represents a combined dispersion coming from both simulated and modeled values around the real physical values. Even if the maximum quality factor cannot be always accurately modeled, the frequency where it occurs (fig. 5.15e) and the usable frequency range of the device (fig. 5.15g) can be estimated with a relatively good accuracy, making this modeling strategy suitable for optimization proposes when searching for designs having a maximum quality factor at a given operating frequency is needed.

5.11.5. Numeric optimization of inductor devices

The proposed model enables the calculation of the main electrical parameters of a spiral inductor design from its geometrical and fabrication technology parameters. The model is valid for frequencies below the first self-resonance of the device, a frequency range where these devices are effectively used in practical applications.

Furthermore, the availability of these equations in a form of a Matlab toolbox enables to write simple computer scripts to explore large design spaces of devices, allowing the designer to produce optimal designs within a few seconds or minutes of computation, a task that takes many hours of computation using EM-based simulation tools or pure measurement-based modeling approach. This approach is similar to the one proposed in [Post 2000], but using a more accurate model and having more freedom in the choice of the optimization parameters.

With an accurate physics-based model available, the circuit designer can quickly and easily analyze trade-offs on parameters in order to have the desired performance (namely a given value of inductance, device area, quality factor and self-resonant frequency).

As an example, the optimization of a 9 nH device taking the L_{DOE15} design presented in the previous paragraph as starting point is presented. Let us suppose the problem of finding a similar device to work in a WLAN front end. A maximum quality factor at 5.2 GHz is desired in that case one can start by limiting the maximum diameter of the inductor to be 400 µm, fixing its form as octagonal (having a quality factor better than squares). In order to explore a discrete domain of parameters, one can specify a tolerance for the inductance value, in this example 9 nH $\pm$ 5%.

Based on this fast numerical model, one can easily optimize for different spiral inductor parameters by direct search for the design parameter of interest in a given inductor design space (set of allowed geometric parameters).

The applied constrains to the numeric simulations are shown in table 5.6.

Parameter	Symbol	Constrains
External diameter	D_{OUT}	between 100 and 400 µm, with steps of 25 µm
Number of turns	N	between 1 and 10, with steps of 0.25, adjusted to give the requested inductance
Track width	w	between 10 and 50 µm with steps of 5 µm
Track spacing	s	between 3 and 10 µm, with steps of 1 µm
Inductance range	L_S	between 8.55 and 9.45 nH (9.0 ± 5% nH)
Spiral Form (sides / turn)	N_S	octagonal (fixed at 8)

Table 5.6 : Simulation constrains applied to the optimization a 9-nH nominal inductor.

The simulation of the whole design space takes a few minutes on a PC running Matlab 6.5 at 1.2 GHz. The initial design space contained about 10,500 devices from what 189 fall within the desired inductance range.

Simulated results for the optimum designs are shown in table 5.6.

Design	D_{OUT} µm	N turns	w µm	s µm	L_S [(a)] nH	Q_{MAX}	f_{QMAX} GHz	f_{RES} GHz	A_{SPI} x 10^5 µm^2	FMI x 10^{-3} GHz/µm^2
Q_{MAX} @ any f	400	4	10	8	11.1	49.9	3.7	7.9 [(b)]	1.60	2.10
Q_{MAX} @ 5.2 GHz	375	4.5	10	10	10.7	29.7 23.6 [(c)]	3.3 5.2 [(c)]	7.4	1.41	1.56
FMI_{MAX}	275	7.5	10	5	10.5	28.4	3.5	7.4	0.76	2.31

(a) Effective inductance at f_{QMAX}.
(b) This design has also the highest resonant frequency f_{RES}.
(c) The maximum Q at f = 5.2 GHz does not mean the maximum along all the frequencies.

Table 5.6: Results for a numeric optimization modeling of a 9 nH inductor built using the quartz / copper technology module.

The figure of merit for an inductor FMI was calculated by eq. 2.13. This model suggests that the maximum possible quality factor for a 9-nH inductor should be around 50 and the maximum resonant frequency around 8 GHz. These values are dependent on the inductance value, since it basically sets the size of the device and by consequence the amount of parasitics associated to it.

Summary

This chapter presented the tools and models used for electromagnetic simulation of passive devices. A simple yet accurate physics-based model for spiral inductors on top of low-conductive substrates was developed and validated by experimental measurements and ADS Momentum electromagnetic simulations. This model uses important approximations and simplifications for the modeling of the spiral inductor, namely the thickness must be larger than the skin depth (so the minimum frequency of validity is about 1 GHz), and the coupling between non-adjacent segments and the proximity effect is neglected (current crowding effect). Although simple this model gives better estimation of losses than the thin microstrip one traditionally cited in the literature, and is capable to model the device using a simple π model that is accurate at least to the first resonance frequency. The accuracy of the model was demonstrated by direct comparison with S-parameter data (both reflection and transmission), as well as with effective inductance and quality factor data.

This simple numerical model was used to demonstrate the possibility to optimize spiral inductor designs by directing searching a large number of designs in a given design space, a procedure that is unpractical using computationally intensive EM simulations or by fabricating large number of devices to explore the design space.

The original contribution of this thesis for the analytical modeling of spiral inductors is related to a better understating and estimation of the 2-D skin effect losses in rectangular conductors (given resistance results much less than the traditional models used in the literature), to a more rigorous calculation of the parasitic capacitances in the spiral (giving results of an order of magnitude higher than the ones obtained by the model most cited in the literature), to the introduction of a broadband transmission-line equivalent circuit capable to model the device up to its first self-resonance and for an optimization numeric approach that is centered on circuit device parameters (namely inductance and quality factor at a given frequency), instead of using purely empirical observations of the dependency of these parameters on the geometry of the device (external diameter, track width, track spacing and spiral form). The AC resistance calculation was empirically validated by 3-D EM simulations performed over a large design space (track width between 1 and 100 μm, aspect ratio between 1 and 100% and frequencies between 0.01 and 20 GHz, studied in more detail in appendix A).

Chapter 6

Conclusions and perspectives

6.1. General conclusions

This thesis presented the development of a technology alternative for the fabrication of high quality factor and high self-resonant frequency thick metal RF MEMS passive devices compatible with CMOS back-end processing, having low thermal budget (< 300 ^{o}C) and aligned to the current trends in modern high speed interconnects (use of copper / low κ damascene approach). This technology module offers 2 metal levels and a via in between, with typical thickness in the range of 1.5 to 10 μm. The use of planar lithography steps and hard masks (buried via method), associated to the planarization offered by the CMP make the process highly scalable, allowing to obtain different thicknesses of metal with minimal changes in the processes parameters.

Spiral inductors were fabricated and studied as demonstration vehicles for this technology. High quality factors in the range of 30 to 50 and high self-resonant frequency in the range of 6 to 15 GHz were demonstrated, values that are in the current state-of-the-art for CMOS-compatible processes. These devices exhibit high bandwidth (Q > 20) over a wide frequency range, enabling their use in different telecommunication standards / frequencies, like GSM, ISM (Bluetooth), WLAN and in ultra-wideband (UWB) applications.

High performance filters with insertion loss as low as 1.2 dB were demonstrated, performances that cannot be usually obtained using small footprint on chip passive components.

Furthermore, the developed technology module showed to be capable to fabricate also high Q fixed and variable capacitors, proving to be a viable platform for high Q RF MEMS devices fabrication.

The use of CMP with the buried via approach and SiO_2 hard mask and anisotropic dry etch of deep trenches in polyimide makes the process lithography planar and scalable to obtain different thickness without complicated changes and tuning of process parameters. The CMP time were reduced by the use of high-speed CMP slurry suitable for the fabrication of thick metal MEMS (removal rates in the range of 1 to 3 μm/min). This CMP step presents levels of dishing and erosion much higher than the ones traditionally used in thin film interconnects, what does not imply in a major issue since in terms of relative values the thickness variation due to these effects are under a controllable range of values (2 to 5 % of the nominal thickness of the layer).

A careful control in the addictives and the use of uniformity thickness improvement fixtures in the electroplating bath provide good levels of uniformity (around 10%) and resistivity for the copper films (2.0 μΩ cm), which is only 15% above the minimum value that can be obtained using thick bulk copper as material.

High-quality factor inductors were studied on top of insulating substrates (namely quartz). State-of-the-art deep reactive ion etching was used to produce deep cavities in the quartz wafer and pattern thick copper lines directly embedded in an insulator substrate. For the first time, a functional packaging concept were presented and developed. Both sides of the packaging quartz wafer were used to fabricate high Q inductors and encapsulate silicon wafers that can contain other RF MEMS devices. This functional packaging presents high RF performance potential (high Q inductors and low-loss and high-gap RF device protection of 40 μm), offers a good degree of scalability with less wafer surface consumption per function

and less parasitics due to a significant reduction in the interconnection lengths between discrete components that can be fabricated using heterogeneous technological platforms. Particularly, the packaging bonding process was optimized to work with RF MEMS processes using fluorine-based release steps, and exhibited high yield after optimization of the adhesion between the different SU-8 resist layers.

This research presented also a contribution to the RF modeling, simulation and optimization of RF MEMS devices, in particular spiral inductors, by careful measurement-based and EM-simulation based models associated to statistical design techniques (design of experiments) in order to efficiently cover the desired design space with a reduced number of devices and having the maximum information available for the studied set.

Although measurement and simulation based models and equivalent circuit modeling were successfully used to model the devices, a physics-based scalable model was developed in order to accurately synthesize and predict the performance of the devices for a given number of expected parameters, namely the inductance, maximum device size, maximum quality factor at a given operating frequency or frequency range and self-resonant frequency. These models can also provide SPICE-equivalent circuit models suitable for fast analog circuit simulation and easy of use block-connecting of devices in order to build more complex functions like filters and tuning matching networks. The major advantage of the proposed methodology, centered in the inductance value instead of the geometrical parameters of the device, is the opportunity to give the designer the best possible solution for a given technology profile and for the desired inductor specifications (inductance, frequency and available area).

6.2. Perspectives for future research

Although the use of polyimide as sacrificial layer and the successful fabrication of free standing copper membranes were demonstrated, the stress of the electroplated copper should be studied and optimized to produce flatter membranes needed for switches and tunable capacitors. Another point to be optimized is the contact resistance between the copper layers

and between the copper and other metal layers, since the polyimide release etch can oxidize copper, which needs a protection layer (tantalum in the framework of this research). Although tantalum is an excellent choice as adhesion layer and anti-diffusion barrier, it does not behave very well for standard processes like wire bonding and flip-chipping, and additional interfacing materials like Ni-Cr or Al (successfully used for the copper / quartz inductors) should be adopted to successfully interface the fabricated devices with other technology modules and circuits.

More progress is also needed in the direction of building out-of-plane and variable devices. Out-off-plane inductors are less prone to substrate related losses and can help to attain the desired RF performances on top of low resistivity substrates by means of a reduced magnetic coupling with the substrate. Although solenoid and toroidal devices present good inductance per wire perimeter and surface ratio, they can suffer from low quality factors due to the increased number of alternating contacts between different metal layers (increasing the series resistance due to the contact resistance between 2 layers), and need thickness in the range of 40 μm to 80 μm to produce loops large enough in order to provide compact structures, especially when the inductance values exceeds 10 nH.

Another alternative to be explored is the use of very thick dielectrics in order to minimize the magnetic coupling between the spiral and the substrate. This technique is viable when using polyimide or BCB layers than can provide up to 20 μm of thickness in a single or 2-step deposition with minimal delaminating problems [Metz 2004]. The same technology can be used to fabricate on-chip transformers with the same benefits of loss reduction and increase in the resonance frequency observed for spiral inductors.

Furthermore, the use of the processes developed along this thesis to make LC circuits like LC tanks, filters, switch banks, and transmissions lines can make possible the development of a complete RF MEMS solution using a low-cost, low-loss, low-thermal budget CMOS compatible technology platform that contributes to insert RF MEMS into current RF-IC interconnects fabrication framework with reduced process overhead and development effort.

Appendix A: Skin effect in conductors

This appendix shows more details about the AC resistance models presented in chapter 5. The exact solutions for an infinitely long cylindrical wire and an infinite planar conductor with finite thickness are presented. Approximations and accuracy for rectangular strip conductors by using approximations based on the exact solutions for cylindrical and infinite plane conductors are discussed using numeric 3-D simulation results obtained using Fasthenry simulation tool as reference.

A.1. Cylindrical wire

The AC current distribution inside an infinitely long cylindrical wire can be analytically calculated [Ramo 1984]. In this case, by the symmetry of the problem, the current density is function only of the distance r to the wire center and points always to the direction $\hat{z}$ perpendicular to the cross section of the conductor:

$$\vec{J} = J_Z(r)\hat{z} \qquad \text{(eq. A1).}$$

The Maxwell equations for a good conductor (neglecting the displacement current term) under time harmonic AC current regime ($j\omega$ referring to the $\partial / \partial t$ operator) can be written as:

$$\vec{\nabla} \times \vec{H} = \vec{J} = \sigma\vec{E} \qquad \text{(eq. A2),}$$

$$\vec{\nabla} \times \vec{E} = -j\omega\mu\vec{H} \qquad \text{(eq. A3).}$$

From these 2 equations, one can derive the differential equation for the current density J:

$$\nabla^2\vec{J} = j\omega\mu\sigma\vec{J} \qquad \text{(eq. A4).}$$

For the infinitely long cylindrical wire, eq. A4 reduces to:

$$\frac{d^2J_Z}{dr^2} + \frac{1}{r}\frac{dJ_Z}{dr} + T^2 J_Z = 0 \qquad \text{(eq. A5),}$$

where J_Z is an exclusive function of the radial distance r. The general solution of this differential equation is in the form:

$$J_Z = AJ_0(Tr) + BH_0^{(1)}(Tr) \quad \text{(eq. A6)},$$

with A and B constants, J_0 the 0-th order Bessel function, $H_0^{(1)}$ the 0-th order of the 1st kind Henkel function and T a constant calculated as function of the skin depth δ (eq. 2.36):

$$T = \sqrt{-j\omega\mu\sigma} = \frac{1-j}{\delta} \quad \text{(eq. A7)}.$$

$H_0^{(1)}$ is divergent at $r = 0$, setting the constant $B = 0$. From the current density $J_Z(r_0) = \sigma E_0$ at the conductor surface, one can obtain A as function of the electric field E_0 at the surface of the conductor:

$$J_Z = \frac{\sigma E_0}{J_0(Tr_0)} J_0(Tr) \quad \text{(eq. A8)}.$$

The magnetic field can be obtained from the total current using the Ampère's law as:

$$\oint \vec{H} \cdot d\vec{l} = I \quad \text{(eq. A9)}.$$

The magnetic field has always the direction of Φ and a dependency only in r, so:

$$2\pi r_0 H_\Phi(r_0) = I \quad \text{(eq. A10)}.$$

From eq. A2, A3 and A10, the following relations can be written:

$$H_\Phi = \frac{1}{j\omega\mu}\frac{dE_Z}{dr} = \frac{1}{j\omega\mu\sigma}\frac{dJ_Z}{dr} = \frac{1}{j\omega\mu\sigma}\frac{d}{dr}\left[\frac{\sigma E_0}{J_0(Tr_0)} J_0(Tr)\right] = -\frac{\sigma E_0}{T}\frac{J_0'(Tr)}{J_0(Tr_0)} \quad \text{(eq. A11)}.$$

From the right side of eq. A11 and eq. A10, the total current becomes:

$$I = -\frac{2\pi r_0 \sigma E_0}{T} \frac{J_0^{'}(Tr)}{J_0(Tr_0)} \quad \text{(eq. A12).}$$

The internal impedance per unit length is defined as:

$$Z_i^{'} \equiv \frac{E_Z(r_0)}{I} = -\frac{T}{2\pi r_0 \sigma} \frac{J_0(Tr_0)}{J_0^{'}(Tr_0)} \quad \text{(eq. A13).}$$

The following expansion for eq. A13 is useful in low-frequency regime ($r_0 << \delta$):

$$Z_{i,LF}^{'} \approx \frac{1}{\pi r_0^2 \sigma}\left[1 + \frac{1}{48}\left(\frac{r_0}{\delta}\right)^2\right] + j\omega \frac{\mu}{8\pi} \quad \text{(eq. A14).}$$

Eq. A14 gives approximately the DC resistance per unit length $1 / \pi r_0^2 \sigma$ in the case $r_0 << \delta$ and shows that the low-frequency internal inductance per unit length is a constant independent of the wire diameter and equal to $\mu / 8\pi = 0.5$ nH/m for non-magnetic metallic wires.

At high frequencies when $r_0 >> \delta$, the following expansion for eq. A13 is useful:

$$Z_{i,HF}^{'} \approx \frac{1+j}{2\pi r_0 \sigma \delta} = \frac{1+j}{2\pi r_0} R_F \quad \text{(eq. A15).}$$

Eq. A15 illustrates the Wheeler rule that states at very high frequency regime the internal reactive inductance is equal to the internal resistance. The decrease in the internal inductance due to skin effect current constriction is the reason for the reduction of the total inductance of a conductor when the frequency increases. One can note this for example the frequency-dependent factor T presented in eq. 1 of [Greenhouse 1974] inductance calculation formula.

Figure A1 shows a plot of relative values derived from eq. A13. One can notice that when the radius exceeds the skin depth value the AC resistance and internal inductance starts to vary rapidly with the frequency. The linear dependency with δ means a dependency with $\sqrt{f}$ for

the AC resistance, defining the skin effect regime. This is explicitly shown in the variation rates plot as function of frequency shown in fig. A2.

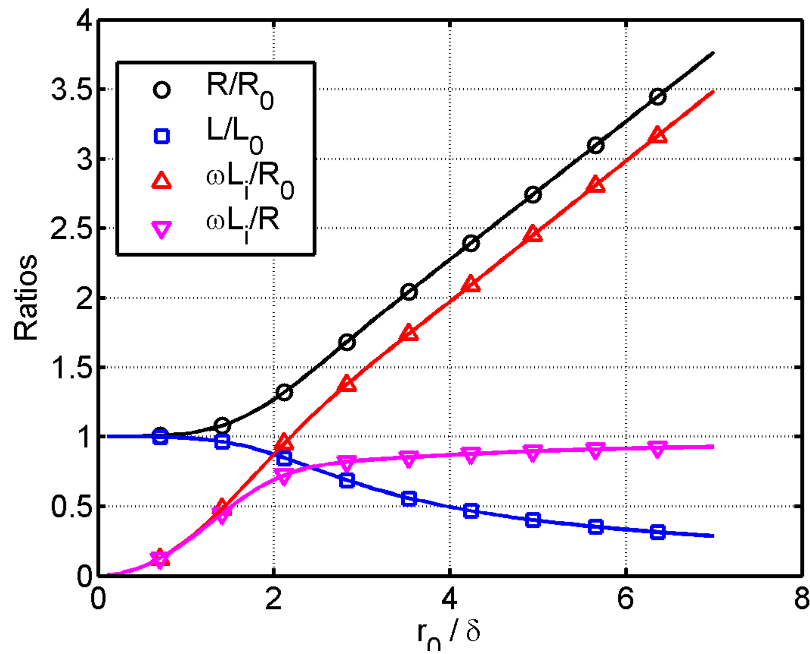


Fig. A1: AC resistance, inductance and impedance relative ratios for a cylindrical wire as function of the radius r_0 normalized by the skin depth δ.

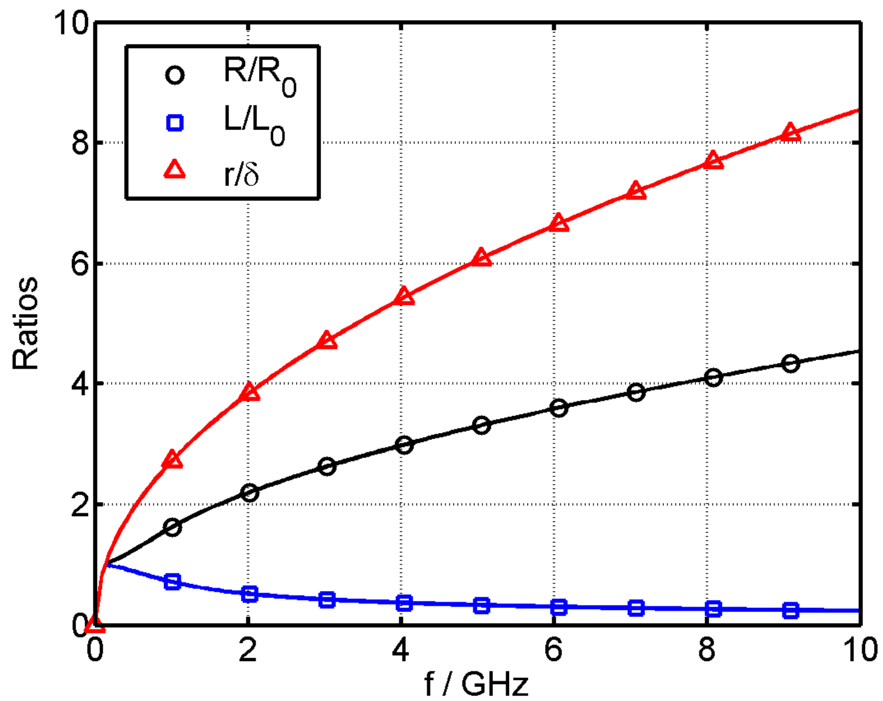


Fig. A2: Relative resistance, inductance and radius to skin depth ratios as function of the frequency for a circular wire with $r = 5.64\ \mu m$ ($100\ \mu m^2$ of area).

A.2. Infinitely long and wide rectangular stripline with finite thickness

Let us consider the rectangular conductor of fig. A3. When $w / t >> 1$ or when $w \rightarrow \infty$ most of the current is distributed along the thickness of the conductor and an analytic solution depending only on the vertical position z is possible. In this case, a solution $J = J_Z(z)$ is admitted. Although not physically reasonable for all values of w, t and skin depths δ, a simple analytical solution is possible for this case and it provides some insight about the AC resistance behavior of thin rectangular striplines [Jackson 1975].

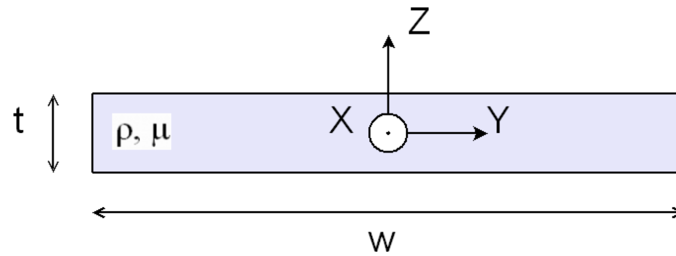


Fig. A3: Rectangular conductor of width w, thickness t and choice of the coordinate system.

In this case, a solution of eq. A4 can be written in the form

$$J(z) = Ae^{\gamma z} + Be^{-\gamma z} \qquad \text{(eq. A16).}$$

Choosing the z origin in the center of the conductor, by symmetry $J(z) = J(-z)$ and $A = B$. Directly from eq. A4:

$$\gamma = \sqrt{j\omega\mu\sigma} = \frac{1+j}{2\delta} \qquad \text{(eq. A17).}$$

The constant A can be obtained as function of the total current density per unit length $J_S = I / w$ along w: $\int_{-t/2}^{t/2} A(e^{\gamma z} + e^{-\gamma z})dz = J_S$, giving:

$$A = \frac{\gamma \, J_S}{2\sinh\frac{\gamma \, t}{2}} \qquad \text{(eq. A18).}$$

The expression for the current density is then:

$$Jz(z) = \frac{\gamma J_S}{2\sinh\frac{\gamma t}{2}}\cosh\gamma z \qquad \text{(eq. A19).}$$

.

Figure A4 shows plots of $/ J_Z / J_S /$ for $t = 5$ µm and for different frequencies between 1 and 10 GHz (t / δ between 2.4 and 7.6). One can note that when $t > 4\ \delta$ the current non-uniformity starts to be more pronounced. The ratio $x / \delta > 4$, where x is a characteristic dimension of the conductor, is sometimes used as a practical rule to know if skin effect should be taken into account in the electrical modeling of a conductor for the given operating frequency.

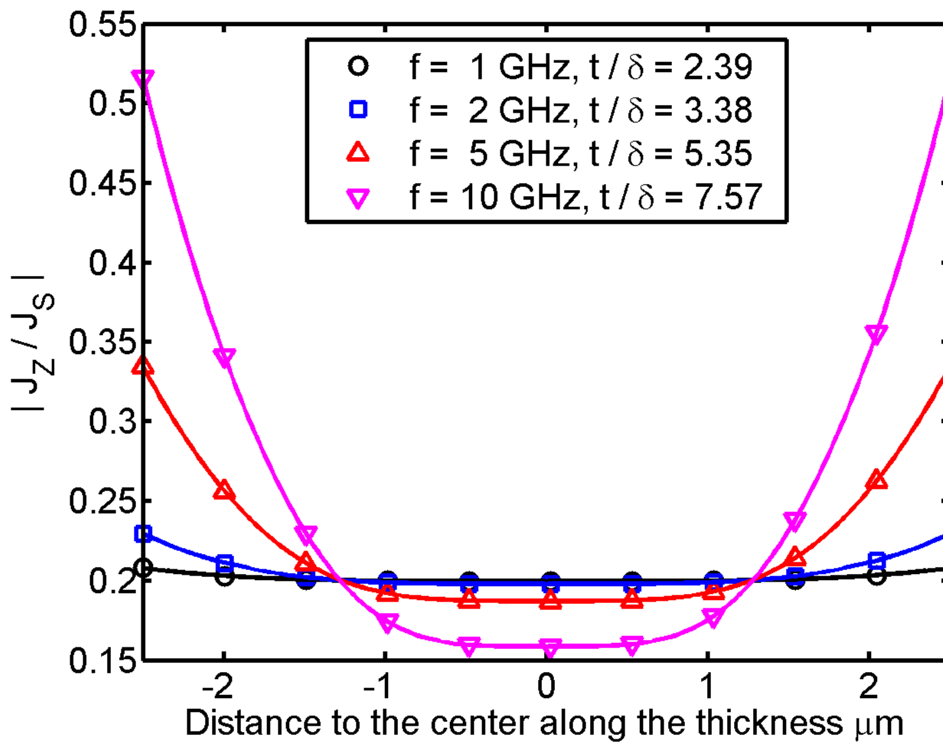


Fig. A4: Normalized current distribution $|J_Z/J_S|$ along a 5 µm-thick, infinitely wide rectangular conductor at different frequencies.

The resistance per unit length can be obtained from the total current and from the current density by summing the power dissipated on all surface elements dS_m of the surface S of the conductor:

$$R'_{AC}\,|\,I\,|^2=\sum_S \frac{1}{\sigma\, dS_m}\,|\,I_m\,|^2=\sum_S \frac{1}{\sigma\, dS_m}\,|\,J_m\,|^2\, dS_m^2=\frac{1}{\sigma}\int_S |\,J_m\,|^2 dS \qquad \text{(eq. A20)}.$$

Applying this equation to the current distribution given by eq. A19, one can obtain:

$$R_{AC}(f)=\frac{\rho l}{w t_{EFF}}=\frac{\rho l}{w}\frac{1}{2\delta\left[\dfrac{\cosh(t/\delta)-\cos(t/\delta)}{\sinh(t/\delta)+\sin(t/\delta)}\right]} \qquad \text{(eq. A21)},$$

with t_{EFF} an effective AC thickness given by:

$$t_{EFF}=2\delta\left[\frac{\cosh(t/\delta)-\cos(t/\delta)}{\sinh(t/\delta)+\sin(t/\delta)}\right] \qquad \text{(eq. A22)}.$$

A.3. Rectangular stripline

Eq. A4 does not have an exact analytical solution in the case of a rectangular cross-section conductor of width w and thickness t. Several approximations strategies are proposed in the literature, amongst them:

- Making assumptions about the current density behavior and solving eq. A4 approximately [Eo 1993, Neagu 1997, Yue 2000, Du 2006],
- Solve eq. A4 numerically [Chari 1977, Weeks 1979, Waldow 1987, Antonini 1999],
- Make some assumptions to simplify the problem, like approximating the cross section of the rectangular conductor by an ellipse [Lotfi 1995], considering the conductor is infinitely wide when $w >> t$ [Perruisseau-Carrier 2006] or find approximate formulae to extend the validity of the infinite wide conductor solutions for finite ones [Massin 2002],
- Propose equations obtained by fitting over a large design space of devices and frequencies [Pettenpaul 1988, Nieuwoudt 2007].

A brief presentation of some models available in the literature will follow.

Eo and Eisenstadt [Eo 1993] proposed an approximate model for rectangular section conductors made by simple assumptions about the behavior of the 2-D skin effect in rectangular conductors. The AC resistance is calculated as:

$$R_{AC}(f) = \frac{\rho l}{w t_{EFF}} \qquad \text{(eq. A23).}$$

Where the effective thickness t_{EFF} is given by:

$$t_{EFF} = \delta\left[1 - \exp\left(\frac{-t}{\delta}\right)\right]\left(1 + \frac{t}{w}\right) \qquad \text{(eq. A24).}$$

Neagu et al. [Neagu 1997] proposed a simple model to calculate the AC resistance based on simplified analysis of skin depth effect combined with the strip line geometric parameters w and t:

$$R_{AC} = \frac{\rho l}{wt}\left[1 + \frac{wt}{2\delta(w+t)}\right] \qquad \text{(eq. A25).}$$

[Yue et al. 2000] proposed a simple model considering a purely exponential behavior of the current density along the thickness. This approximation is valid only if there is a ground plane near the strip line, what is not true for lines built on top of thick insulating substrates like quartz or high resistivity silicon. The current density is assumed to have a maximum in the bottom line of the conductor and vary exponentially following the skin depth rule along the conductor thickness:

$$J(z) = J_0 e^{-z/\delta} \qquad \text{(eq. A26).}$$

The total current is obtained by integrating J along the conductor thickness:

$$I = w\int_0^t J_0 e^{-z/\delta} dz = J_0 w\delta(1 - e^{-t/\delta}) \qquad \text{(eq. A27).}$$

From this expression, one can identify the effective thickness t_{EFF} and the AC resistance as:

$$t_{EFF} = \delta(1 - e^{-t/\delta}) \quad \text{(eq. A28)},$$

$$R_{AC}(f) = \frac{\rho l}{w\delta(1 - e^{-t/\delta})} \quad \text{(eq. A29)}.$$

Lotfi et al. proposed a model for rectangular conductors by approximating their section by ellipses and by semi-empirical fitting of asymptotic behavior at low and high frequency regimes, giving [Lotfi 1995]:

$$R_{AC} = \frac{\rho l}{wt}\left[1 + \left(\frac{f}{f_1}\right)^2 + \left(\frac{f}{f_2}\right)^{0.5}\right]^{0.10} \quad \text{(eq. A30)},$$

with frequencies f_1 and f_2 are obtained to match the behavior at low and high frequency regimes. These frequencies are calculated as:

$$f_1 = \frac{\pi^2 \rho}{2\mu\, wt} \quad \text{(eq. A31)},$$

and

$$f_2 = \frac{\pi^2 \rho}{\mu t^2 K((t/w)^2)} \quad \text{(eq. A32)}.$$

This model is validated for low-frequency regime between 10 kHz and 100 MHz and for millimeter-size rectangular power foils and care should be taken to apply it for µm-size structures operating at GHz.

[Nieuwoudt 2007] proposed a model for the 2-D skin effect based on fitted data obtained from Fasthenry simulations performed over a large design space of rectangular stripline designs. This model proposes to use corrections to the 1-D skin effect based on the geometric parameters w and t of the rectangular strip:

$$R_{AC}(f) = \rho \frac{l}{wt_{EFF}(f)} \qquad \text{(eq. A33)},$$

where R_{AC} is the AC resistance, ρ the metal resistivity, l the track length, w the track width and t_{EFF} the effective AC thickness given by:

$$t_{EFF} = \delta_{EFF}(1 - e^{-t/\delta_{EFF}})(1.087 + 2.74r - 1.203r^2) \qquad \text{(eq. A34)}.$$

The parameter $r < 1$ defines the aspect ratio t / w of the stripline (simply calculated as w / t if $t > w$):

$$r = \begin{cases} w/t & if\ w < t \\ t/w & if\ t > w \end{cases} \qquad \text{(eq. A35)}.$$

The effective skin depth δ_{EFF} is calculated using a corrected expression defining an effective frequency f_{EFF}:

$$\delta_{EFF} = \sqrt{\frac{\rho}{\pi \mu f_{EFF}}} \qquad \text{(eq. A36)}.$$

$$f_{EFF} = f(0.971 + 0.096r - 0.0281r^2) \qquad \text{(eq. A37)}.$$

Pettenpaul et al. [Pettenpaul 1988] proposed a model based on numeric fitting of results obtained by [Hafner 1937]:

$$R_{AC}(w,t,f) = \begin{cases} \frac{l}{\sigma wt}\left[\frac{0.43093p}{1+0.041(t/w)^{1.19}} + \frac{1.1147+1.2868p}{1.2296+1.287p^3} + 0.0035(t/w-1)^{1.8}\right] & if\ p \geq 2.5 \\ \frac{l}{\sigma wt}\left[1+0.0122p^{(3+0.01p^2)}\right] & if\ p < 2.5 \end{cases} \qquad \text{(eq. A38)},$$

where

$$p = \sqrt{2 f \sigma \mu w t} = \frac{1}{\delta}\sqrt{\frac{2wt}{\pi}} \quad \text{(eq. A39)}$$

is a non dimensional parameter usually named as "normalized frequency". These expressions are reported to be 3 to 5% accurate when $t / w < 12$ and $2 <= p <= 3$.

Massin et al. proposed in 2002 [Massin 2002] the following model considering that the infinite plane solution can be applied simultaneously along both the width and thickness (fig. A5):

$$R_{AC}(f) = \frac{\rho l}{wt - (w - w_{EFF})(t - t_{EFF})} \quad \text{(eq. A40)},$$

where the effective width and thickness are obtained using eq. A21 for both w and t directions:

$$w_{EFF} = 2\delta\left[\frac{\cosh(w/\delta) - \cos(w/\delta)}{\sinh(w/\delta) + \sin(w/\delta)}\right] \quad \text{(eq. A41)},$$

$$t_{EFF} = 2\delta\left[\frac{\cosh(t/\delta) - \cos(t/\delta)}{\sinh(t/\delta) + \sin(t/\delta)}\right] \quad \text{(eq. A42)}.$$

Fig. A5: Effective conduction area calculated from the 2D model of [Massin 2002].

In order to take into account proximity effect in spiral inductors, this paper proposed to replace the skin depth δ by an effective skin depth δ_{EFF} given by:

$$\delta_{EFF} = \frac{\delta}{\xi} \quad \text{(eq. A43)},$$

where ξ is an empirical factor between 1 and 3 used to increment the resistance calculation due to the proximity effect. It is suggested that typical values for spiral inductors studied in the reference article have typical values $\xi = 1.7$ [Peck 1995, Massin 2003].

A.4. Fasthenry simulations and comparison between AC resistance calculation models

Due to the complexity of the problem, the best approach is to model a rectangular wire numerically by EM simulation. In order to draw clear conclusions about the validity of these models for the structures studied in this thesis, a set of simulations performed in Fasthenry, a 3-D EM simulation tool, were performed [Kamon 1994]. Fig. A6 shows a sample Fasthenry simulation script used to simulate a rectangular stripline with $w = 20$ µm, $t = 5$ µm operating in the frequency range of 0.01 to 20 GHz.

```
* stripe_w20_t5.inp: Fasthenry simulation script for a rectangular stripe
* w = 2e-005 m, t = 5e-006 m, t/w = 0.25, len = 0.001 m
* rho = 1.72414e-008 Ohm m, mur = 1, fmin = 1e+007, fmax = 2e+010
* fmesh = 20 GHz, delta = 0.467295 um,
* kdelta = 0.1,                         dx = 0.0467295 um (max)
* kw0 = 0.00233648, kw = 0.00196078,    dw = 0.0392157 um
* kt0 = 0.0093459,  kt = 0.00793651,    dt = 0.0396825 um
* nwinc = 16, nhinc = 12, 192 segments

.Units m
.Default x=0.0 y=0.0 z=0.0
.Default w=2.0e-005 h=5.0e-006
.Default rho=1.72414e-008
.Default nwinc=16 nhinc=12 rw=2 rh=2

N1 x=0.0 y=0.0 z=0.0
N2 x=0.001 y=0.0 z=0.0
E1 N1 N2 w=2.0e-005 h=5.0e-006 rho=1.72414e-008 nwinc=16 nhinc=12 rw=2 rh=2

.external N1 N2 cond1
.freq fmin=1.0e+007 fmax=2.0e+010 ndec=4

.end
```

Fig. A6: Example showing a Fasthenry simulation script and parameters. Dimensions are $w = 20$ µm, $t = 5$ µm, length = 1 mm, $\rho = 1.72 \cdot 10^{-8}$ Ω m (bulk copper), mesh of 192 segments with a minimum discretization of 0.04 µm (about 10% of the skin depth at 20 GHz - the highest operating frequency).

In order to correctly predict losses using EM simulation, fine meshes are needed, especially near the conductor surface where the current density varies very rapidly as function of the position. A discretization step of 10% of the skin depth at the highest simulation frequency was chosen in order to avoid mesh induced artifacts in the results. The meshing used for the

20 μm x 5 μm track can be seen in fig. A7. The solid lines delimitates the rectangular meshing domains, and the dotted lines show the approximate position of the skin depth at different frequencies (1, 2, 5, 10 and 20 GHz).

The smallest features near the conductor surface have 0.4 μm, about 10% of the skin depth at 20 GHz for copper bulk conductivity ($\sigma = 5.8 \cdot 10^7$ S/m, $\delta = 0.05$ μm @ 20 GHz).

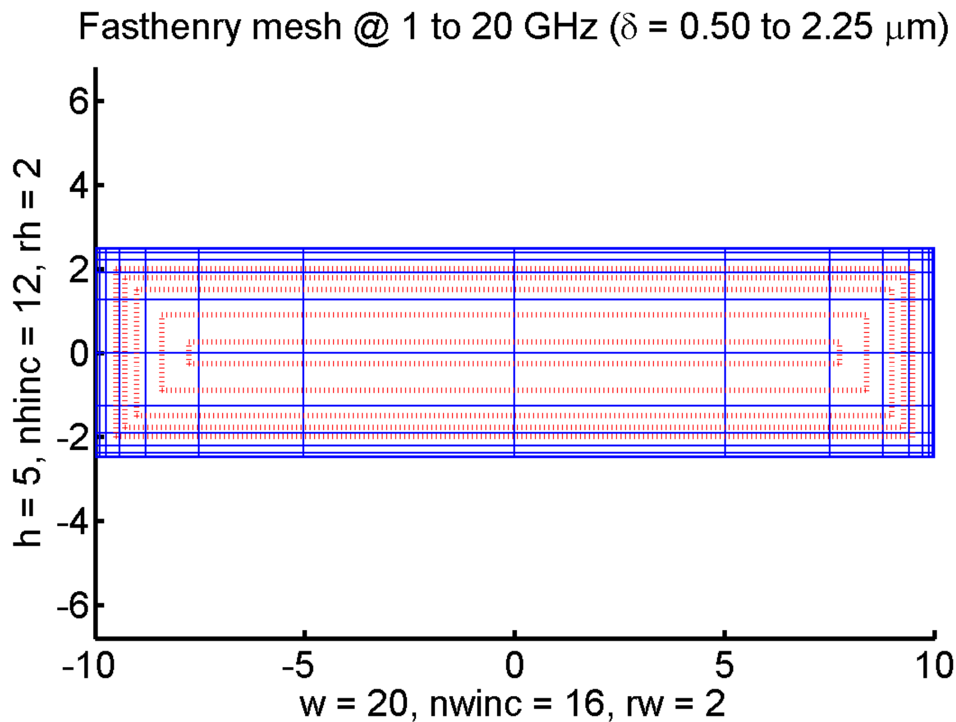


Fig. A7: Skin depth position (dotted lines) at different frequencies for a 20 μm-wide and 5 μm-thick wire. From the inner to the outer part: at 1, 2, 5, 10 and 20 GHz. Solid lines represent Fasthenry adopted meshing (16 divisions along the width and 12 divisions along the thickness with a minimum rectangle size of 0.04 μm x 0.04 μm near the corners).

Fig. A8 shows the simulated values for the frequency-dependent resistance increase factor $K_R = R_{AC}(f) / R_{DC}$ for the rectangular conductor of fig. A7 as function of the frequency compared with all the models presented in the previous paragraphs. Taking 3-D EM simulations as reference, it seems that the Pettenpaul model has the best overall accuracy in the results. The 1-D thickness effect taken along the thickness tend to underestimate the losses in the whole frequency range

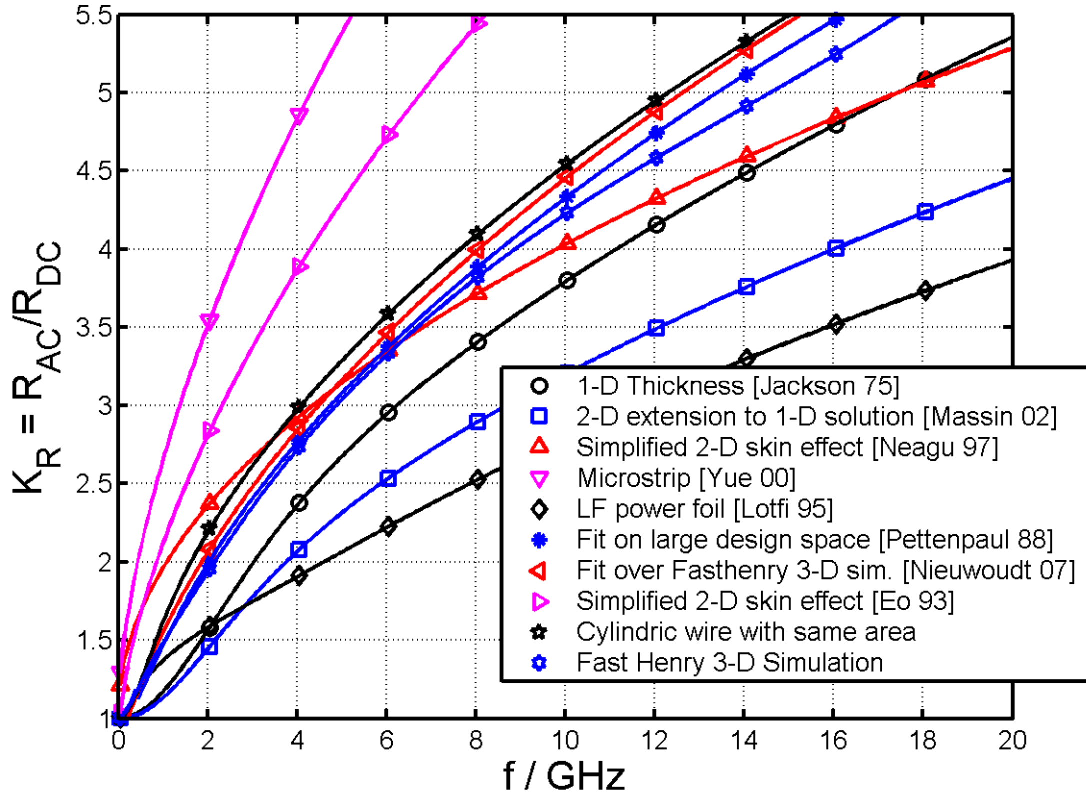


Fig. A8: Comparison between different models for AC resistance calculation presented in the literature and Fasthenry 3-D simulation.

In order to cover a design space representative of the typical dimensions used to fabricate spiral inductors, a set of 49 additional simulations were performed covering 7 fixed widths between 1 and 100 µm (w = 1, 2, 5, 10, 20, 50 and 100 µm) and 7 different aspect ratios t / w between 1 and 100% (t / w = 1%, 2%, 5%, 10%, 20%, 50% and 100%). The values of the simulated thicknesses are summarized in table A1 for the different values of w and t / w, covering a large thickness design space between 0.01 µm and 100 µm. The conductivity of the metal was fixed at $\sigma = 5.8 \cdot 10^7$ S/m, corresponding to the one of the bulk copper.

Fasthenry simulates only log-spaced frequency ranges. Frequencies were chosen to cover the range from 0.01 to 20 GHz with 4 frequency points per decade (giving 14 distinct simulation frequencies approximately equal to 0.01, 0.0178, 0.0316, 0.0562, 0.1, 0.178, 0.316, 0.562, 1, 1.78, 3.16, 5.62, 10 and 17.8 GHz respectively). The skin depth for these frequencies varies from 20.1 µm at 0.01 GHz to 0.50 µm at 17.8 GHz. In terms of dimensions compared to the skin depth, the design space for w values is between 2 δ and 200 δ and the values of t cover the region from 0.02 to 200 δ.

w (um)	t / w = 0.01	0.02	0.05	0.10	0.20	0.50	1.00
1	0.01	0.02	0.05	0.10	0.20	0.50	1.00
2	0.02	0.04	0.10	0.20	0.40	1.00	2.00
5	0.05	0.10	0.25	0.50	1.00	2.50	5.00
10	0.10	0.20	0.50	1.00	2.00	5.00	10.00
20	0.20	0.40	1.00	2.00	4.00	10.00	20.00
50	0.50	1.00	2.50	5.00	10.00	25.00	50.00
100	1.00	2.00	5.00	10.00	20.00	50.00	100.00

Table A1: Thicknesses for the additional 49-device Fasthenry design space covering widths between 1 and 100 μm and aspect ratios t / w between 1 and 100%.

For comparison proposes, each geometry and each simulated frequency is considered as a single analysis case, giving a total population of 50 x 14 = 700 simulations used to compare the relative accuracy of all the available AC resistance calculation models. Fig. A9 shows a plot of the percentage of devices exceeding a given level of error. The error is taken as the percentage difference between the value produced by the model concerned and the respective Fasthenry simulation result for the same parameters (width, thickness and frequency).

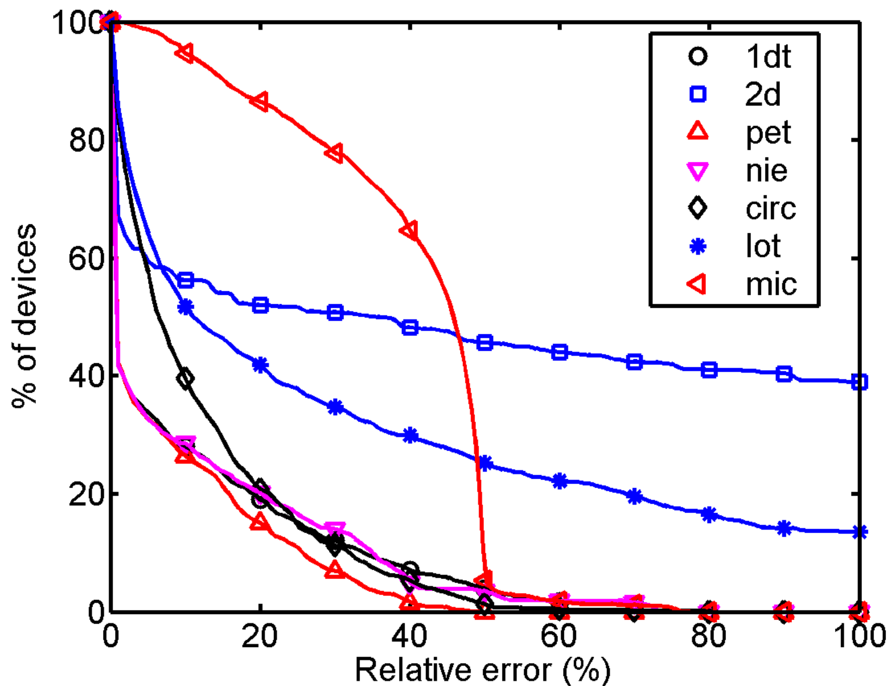


Fig. A9: Error distribution for selected AC resistance models. Labels refers from the top to the bottom respectively to: 1-D skin effect along the thickness ("1dt"), 2-D approximation model using 1-D solution in both directions("2d", [Massin 2002]), [Pettenpaul 1988] model ("pet"), [Nieuwoudt 2007] model ("nie"), a cylindrical wire with a total area equal to w.t ("cyl"), [Lotfi 1995] model ("lot") and the thin microstrip model [Yue 2000] ("mic").

The better overall error distribution is observed for the model presented in [Pettenpaul 1988]. For this model, about 10% of the devices present errors larger than 25%, what exceeds the 3 to 5% accuracy stated in the article because the simulated design space is larger than the one used in the referred paper for fitting the proposed model. Some other models can present more than 50% error in 20% of the devices, and should be used with care and considering the dimensions and frequency range for what they are effectively validated. Taking the rectangular wire as being a cylindrical wire with the same area (effective radius $r_0 = \sqrt{wt/\pi}$ used in eq. A12) gives less than 10% of error for more than 40% of devices. As a general conclusion, no model available to date is capable to give good results over a large design space, but considering the possibility of using the overall best quality match, [Pettenpaul 1988] is the best model, nearly followed by the 1-D skin effect taken along the thickness and by the fitting-based model proposed by [Nieuwoudt 2007]. These models are a good choice for qualitative modeling of a large-design space and large-bandwidth devices aimed to be analyzed in this thesis. Since an optimal solution is found for a design, different models can be used to evaluate the accuracy of the loss estimation considering the device width, thickness and main operating frequency. For real inductor devices, any analytical solution proposed will be still qualitative because a complete solution should take into account proximity effects, the presence of ground planes near the inductor and the dielectric constant of the surrounding media (transmission line propagation constant loss dependency).

CPS-like analysis used in chapter 5 to compute the losses in the inductor model are based on similar assumptions of the ones used by the 1-D skin depth calculation along the thickness and care should be taken with the generalization of the results obtained using this approach.

Worst case designs are probably squared wires, designs for which the t / w aspect ratio is maximum and the assumption $w >> t$ is not valid at all. A plot for the relative error distribution for the devices having $w = t$ is shown if fig. A10. The statistic is made using only 7 wires at 14 frequency points (population of 98 samples) and probably more simulations are needed to make more precise conclusions. The covered design space between 1 and 100 µm is large to suggest that Pettenpaul and 1-D skin effect along the thickness are still good qualitative models. As a general conclusion, in spite of using assumptions that are not physically reasonable, some models can still have some useful numeric qualitative behavior to

be used. Further work is necessary by using other simulation tools and accurately measured experimental data to better understand the accuracy of each approximation.

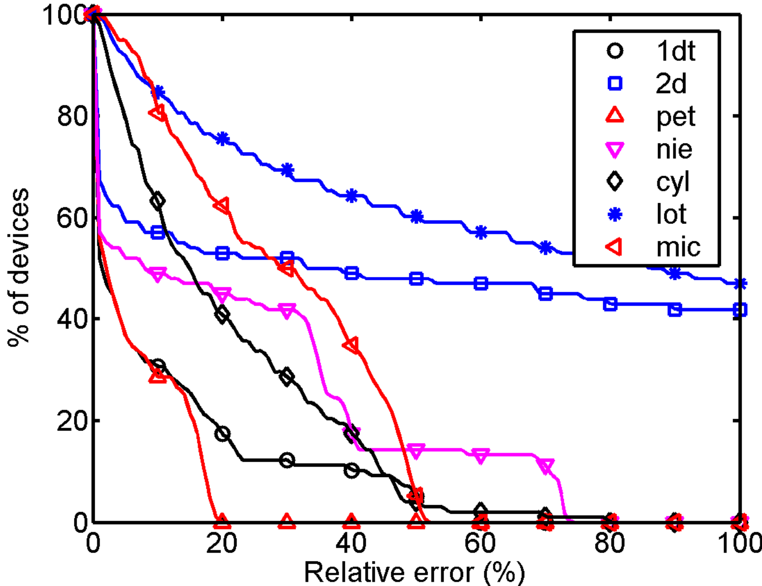


Fig. A10: Relative error distribution for different AC resistance calculation models for squared wires with widths between 1 and 100 μm considering Fasthenry simulations as reference.

Bibliography

[Abdo-Tuko 1993] M. Abdo-Tuko, M. Naghed, and I. Wolff, "Novel 18/36 GHz (M)MIC GaAs FET frequency doublers in CPW-Techniques under the consideration of the effects of coplanar discontinuities", IEEE Transactions on Microwave Theory and Techniques, vol. 41, no. 8, pp. 1307 – 1315, Aug. 1993.

[Agilent 2005] Agilent ADS Momentum manual, Aug. 2005 (file "mom.pdf" in the ADS 2005a documentation). See also http://eesof.tm.agilent.com/products/momentum_main.html. (available in Feb. 2007).

[Aguilera 2001] J. Aguilera, J. de Nó, A. García-Alonso, F. Oehler, H. Hein, and J. Asuerer, "A guide for on-chip inductor design in a conventional CMOS process for RF applications", Applied Microwave & Wireless, pp. 56 – 65, Oct. 2001.

[Aguilera 2002] J. Aguilera and R. Berenguer, "Design and test of integrated inductors for RF applications", Kluwer Academic Publishers, 2002.

[Aguilera 2002b] J. Aguilera, G. Matías, J. de Nó, A. García-Alonso, and R. Berenguer, "A comparison among different setups for measuring on-wafer integrated inductors in RF applications", IEEE Transactions on Instrumentation and Measurement, vol. 51, no. 3, June 2002, pp. 487 – 491.

[Ansoft 2006] Ansoft HFSS simulator manual (file "hfss_onlinehelp.pdf" in the HFSS 9.2 documentation). See also: http://www.ansoft.com. (available in Feb. 2007).

[Antonini 1999] G. Antonini, A. Orlandi, and C.R. Paul, "Internal impedance of conductors of rectangular cross section", IEEE Transactions on Microwave Theory and Techniques, vol. 47, no. 7, pp. 979 – 985, 1999.

[Arnold 1992] R. G. Arnold and D. J. Pedder, "Microwave characterization of microstrip lines and spiral inductors in MCM-D technology", IEEE Transactions on Components, Hybrids, and Manufacturing Technology, vol. 15, pp. 1038 – 1045, Dec. 1992.

[Arora 1993] N. Arora, "MOSFET models for VLSI circuit simulation theory and practice", Springer-Verlag, New York, 1993, pp. 17 – 33.

[Bacher 1995] W. Bacher, W. Menz, and J. Mohr, "The LIGA technique and its potential for microsystems-a survey", IEEE Transactions. Industrial Electronics, vol. 42, no. 5, pp. 431 – 441, 1995.

[Bahl 1998] I.J. Bahl and P. Bhartia, "Microwave solid state circuit design", John Willey, New York, 1998.

[Bahl 2001] I. J. Bahl, "High-performance inductors", IEEE Transactions on Microwave Theory and Techniques, vol. 49, pp. 654 – 664, 2001.

[Bahl 2003] I. Bahl, "Lumped elements for RF and microwave circuits", Artech House, Boston, 2003.

[Baringer 1993] W. B. Baringer and R. W. Brodersen, "MCM's for portable applications", in Proceedings of IEEE Multichip Module Conference, Santa Cruz, CA, 1993, pp. 1 – 5.

[Benaissa 2003] K. Benaissa, J.-Y. Yang, D. Crenshaw, B. Williams, S. Sridhar, J. Ai, G. Boselli, S. Zhao, S. Tang, S. Ashburn, P. Madhani, T. Blythe, N. Mahalingam, and H. Shichijo, "RF CMOS on high-resistivity substrates for system-on-chip applications", IEEE Transactions on Electron Devices, vol.50, pp. 567 – 576, 2003.

[Beyne 1995] E. Beyne, R. Van Hoof, and A. C. Aachen, “The use of BCB and photo-BCB dielectrics in MCM-D for high-speed digital and microwave applications”, in Proceedings of the International Multichip Modules Conference, Denver, CO, 1995, pp. 513 – 518.

[Bhattacharya 2004] K. Bhattacharya and M.J. Deen, “Microwave CMOS traveling wave amplifiers: performance and temperature effects”, IEEE Microwave and Wireless Components Letters, vol. 14, pp. 16 – 18, 2004.

[Biondi 2005] T. Biondi, A. Scuderi, E. Ragonese and G. Palmisano, “Sub-nH inductor modeling for RF IC design”, IEEE Microwave and Wireless Component Letters, vol. 15, no. 12, pp. 992 – 924, Dec. 2005.

[Brandes 1983] E. Brandes, “Smithells metal handbook”, 6th ed., Butterworth, 1983, chapter 18.

[Brank 2001] J. Brank, J. Yao, M. Eberly, A. Malczewski, K. Varian, and C. Goldsmith, “RF MEMS-based tunable filters”, International Journal of RF and Microwave Computer-Aided Engineering, vol. 11, no. 5, pp. 276 – 284, Sept. 2001.

[Bryan 1995]] H.E. Bryan, “Printed inductors and capacitor”, Tele-tech and electronic Industries, Dec. 1995.

[Burghartz 1996] J. N. Burghartz, D. C. Edelstein, K. A. Jenkins, C. Jahnes, C. Uzoh, E. J. O’Sullivan, K. K. Chan, M. Soyuer, P. Roper, and S. Cordes, “Monolithic spiral inductors fabricated using a VLSI Cu-damascene interconnect technology and low-loss substrates”, IEEE IEDM Technical digest, pp. 451 – 454, 1996.

[Burghartz 1996b] J. N. Burghartz, M. Soyuer, and K. A. Jenkins, “Integrated RF and microwave components in BiCMOS technology”, IEEE Transaction on Electron Devices, vol. 43, no. 9, pp. 1559-70, 1996.

[Burghartz 1997] J. N. Burghartz, D. C. Edelstein, K. A. Jenkins, and Y. H. Kwark, “Spiral inductors and transmission lines in silicon technology using copper-damascene interconnects and low-loss substrates”, IEEE Transaction on Microwave Theory and Techniques, vol. 45, pp. 1961 – 1968, Oct. 1997.

[Burghartz 1997b] J.N. Burghartz, A. E. Ruehli, K. A. Jenkins, M. Soyuer, and D. Nguyen-Ngoc, “Novel substrate contact structure for high Q silicon-integrated spiral inductors”, in IEEE IEDM Technical Digest, Washington, D.C., Dec. 1997, pp. 55 – 58.

[Burghartz 1998] J.N. Burghartz, “Progress in RF inductors on silicon - understanding substrate losses”, in Proceeding of the IEEE International Electron Devices Meeting (IEDM), 1998, pp. 523 – 526.

[Butler 1998] J.T. Butler, V.M. Bright, J.H. Comtois, “Multichip module packaging of microelectromechanical systems”, Sensors and Actuators A, vol. 70, 1998, pp. 15 – 22.

[Cadence] http://www.cadence.com (available in Feb. 2007).

[Carazzetti 2005] P. Carazzetti, M.-A. Dubois, and N.-F. de Rooij, “High-performance micromachined RF planar inductors”, in Proceedings of the 13th Conference on Solid-State Sensors, Actuators and Microsystems, 2005 (Transducers'05), vol. 1, June 2005, pp. 1084 – 1087.

[Carchon 2004] G.J. Carchon, W. de Raedt and E. Beyne, “Wafer-level packaging technology for high Q on-chip inductors and transmission lines”, IEEE Transactions on Microwave Theory and Techniques, vol. 52, pp. 1244 – 1251, 2004.

[Cauton 1968] M. Caulton, S. P. Knight, and D. A. Daly, “Hybrid integrated lumped-element microwave amplifiers”, IEEE Transaction on Electron Devices, vol. ED-15, pp. 459 – 466, 1968.

[Cech 1993] J.M. Cech, A.F. Burnett and C.-P. Chien, “Reliability of passivated copper multichip module structures embedded in polyimide”, IEEE Transactions on Components, Hybrids and Manufacturing Technology, vol. 16, no. 7, Nov. 1993, pp. 752 – 758.

[Chaki 1995] S. Chaki, S. Aono, N. Andoh, Y. Sasaki, N. Tanino, and O. Ishihara, “Experimental study on spiral inductors”, in Proceedings of the IEEE Microwave Symposium Digest, Apr. 1995, pp. 753 – 756.

[Chan 2003] K.T. Chan, C.H. Huang, A. Chin, M.F. Li, D.-L. Kwong, S.P. McAlister, D.S. Duh, and W.J. Lin, “Large Q-factor improvement for spiral inductors on silicon using proton implantation”, IEEE Microwave and Wireless Components Letters, vol. 13, no. 11, Nov. 2003, pp. 460 – 462.

[Chang 1993] J. Y.-C. Chang, A. A. Abidi, and M. Gaitan, “Large suspended inductors and their use in a 2 μm CMOS RF amplifier”, IEEE Electron Device Letters, vol. 14, pp. 246 – 248, May 1993.

[Chari 1977] M. Chari, and Z. Csendes, “Finite element analysis of the skin effect in current carrying conductors”, IEEE Transactions on Magnetics, vol. 13, no. 5, Sep. 1977, pp. 1125 – 1127.

[Chen 1995] W.-K Chen (ed.), “The circuits and filters handbook”, CRC & IEEE Press, Boca Raton, 1995.

[Chen 1997] E. Chen and S. Y. Chou, “Characteristics of coplanar transmission lines on multilayer substrates: Modeling and experiments”, IEEE Transactions on Microwave Theory and Techniques, vol. 45, pp. 939 – 945, June 1997.

[Chen 2001] Y. E. Chen, Y. K. Yoon, J. Laskar, and M. Allen, “A 2.4 GHz integrated CMOS power amplifier with micromachined inductors”, IEEE Microwave Theory and Techniques Society Symposium Digest, June 2001, pp. 67 – 70.

[Chen 2006] J. Chen and J.J. Liou, “Improved and physics-based model for symmetrical spiral inductors”, IEEE Transactions on Electron Devices, vol. 53, no. 6, June 2006, pp. 1300 – 1309.

[Cho 1991] H. Cho and D. E. Burk, “A tree-sped method for de-embedding of high-frequency S-parameter measurements”, IEEE Transactions on Electron Devices, vol.38, no. 6, pp. 1371 – 1375, June 1991.

[Chomnawang 2002] N. Chomnawang, J.B. Lee, and W.A. Davis, “Micromachined on-chip 3D inductors”, in Proceedings of the IEEE Emerging Telecommunication Technologies Conference, Richardson, Texas, USA, Sep. 2002.

[Choi 2007] S.-C. Choi, J.-E Youm, K. Heo, J.-H. Lim, C.-H Park, and S.-W. Hwang, “LTCC bandpass filter using 3D coupled helical inductors”, Microwave and Optical Technology Letters, vol. 49, no. 5, May 2007, pp. 1146 – 1147.

[Churchill 1996] R. V. Churchill and J. W. Ward, “Complex variables and applications”, 6th ed., New York, McGraw-Hill, 1996.

[Contopanagos 2007] H. Contopanagos and A. G. Nassiopoulou, “Integrated inductors on porous silicon”, Physica Status Solidi (a), vol. 204, no. 5, May 2007, pp. 1454 – 1458.

[Craninckx 1995] J. Craninckx and M. S. J. Steyaert, “Low-noise voltage controlled oscillators using enhanced LC-tanks”, IEEE Journal of Solid State Circuits, pp. 794 – 802, Sept. 1995.

[Craninckx 1997] J. Craninckx and M. S. J. Steyaert, “A 1.8-GHz CMOS low phase noise voltage controlled oscillator with prescaler”, IEEE Journal of Solid State Circuits, pp. 1474 – 1482, Dec. 1995.

[Crols 1996] J. Crols P. Kinget, J. Craninckx, and M. Steyaert, "An analytical model of planar inductors on lowly doped silicon substrates for analog design up to 3 GHz", in Proceedings of the Symposium on VLSI Circuits, 1996 pp. 28 – 29.

[CST] CST Microwave studio, see http://www.cst.com (available in Feb. 2007).

[Dahlmann 2001] G. W. Dahlmann, E. M. Yeatman, P. R. Young, I. D. Robertson, and S. Lucyszyn, "MEMS high-Q microwave inductors using solder surface tension self-assembly", IEEE Microwave Theory and Techniques Society Digest, pp. 329 – 332, 2001.

[Dahlmann 2002] G. W. Dahlmann, E.M. Yetman, P. Young, I.D. Robertson, and S. Lucyszyn, "Fabrication, RF characteristics and mechanical stability of self-assembled 3D microwave inductors", Sensor and Actuators A, vol. 97 – 98, pp. 215 – 220, 2002.

[Danesh 2002] M. Danesh and J.R. Long, "Differentially driven symmetric microstrip inductors", IEEE Transactions on Microwave Theory and Techniques, vol. 50, no. 1 , Jan. 2002, pp. 332 – 341.

[de los Santos 1999] H.J. de los Santos, "Introduction to microelectromechanical (MEM) microwave systems", Artech House, 1999.

[de los Santos 2002] H.J. de los Santos, "RF MEMS circuit design for wireless communications", Artech House, 2002.

[Dill 1964] H.G. Dill, "Designing inductors for thin-film applications", Electronic Design, vol. 12, pp. 52 – 59, 1964.

[Djordjevic 1994] A.R. Djordjevic and T.K. Sarkar, "Closed formulas for frequency-dependent resistance and inductance per unit length of microstrip and strip transmission lines", IEEE Transactions on Microwave Theory and Techniques, vol. 42, no. 2, pp. 241 – 248, Feb. 1994.

[Du 2006] Y. Du and W. Dai, "Capture high-frequency partial inductance more accurately by gauss quadrature integration with skin-effect model", IEEE Transactions on Microwave Theory and Techniques, vol. 54, no. 3, Mar. 2006, pp. 1287 – 1294.

[Dubois 2005] M. Dubois, C. Billard, J. Carpentier, P. Vincent, G. Parat, C. Muller, "Above-IC FBAR technology for WCDMA and WLAN applications", Proc. of the 2005 IEEE Ultrasonics Symposium, vol. 1, Sept. 2005, pp. 85 – 88.

[Dupont 1997] Dupont and HD Microsystems, "Pyralin polyimide coatings for electronics, VM-651 and VM-652 Adhesion Promoters, 1997 (http://www.hdmicrosystems.com).

[Dupont] Dupont and HD Microsystems, "Pyralin polyimide coatings for electronics", PI 2610 Series – Product Information and Process Guidelines (http://www.hdmicrosystems.com).

[Edelstein 1998] D. C. Edelstein and J. N. Burghartz, "Spiral and solenoidal inductor structures on silicon using Cu – damascene interconnects", in Proceedings of the International Interconnect Technology Conference, San Francisco, CA, 1998, pp. 18 – 20.

[Eo 1993] Y. Eo and W.R. Eisenstadt, "High speed VLSI interconnect modeling based on S-parameter measurements", IEEE Transactions on Components, Hybrids and Manufacturing Technology, vol. 16, no. 5, Aug. 1993, pp. 555 – 562.

[Erdil 2007] E. Erdil, K. Topalli, M. Unlu, O.A. Civi, and T. Akin, "Frequency tunable microstrip patch antenna using RF MEMS technology", IEEE Trans. on Antennas and Propagation, vol. 55, no. 4, Apr. 2007, pp. 1193 – 1196.

[Frédérico 2003] S. Frédérico, C. Hibert, R. Fritschi, Ph. Flückiger, Ph. Renaud, and A.M. Ionescu, "Silicon sacrificial layer dry etching (SSLDE) for free standing RF MEMS architectures", in Proceedings of the 16th IEEE International Conference on Micro Electro Mechanical Systems (MEMS'03), Kyoto, Japan, Jan. 2003, pp. 570 – 573.

[Fritschi 2004] R. Fritschi, S. Frédérico, C. Hibert, P. Flückiger, P. Renaud, D. Tsamados, J. Boussey, A. Chovet, R.K.M. Ng, F. Udread, J.-P. Curty, C. Dehollain, M. Declercq, and A.M. Ionescu, "High tuning range AlSi RF MEMS capacitors fabricated with sacrificial amorphous silicon surface micromachining", Microelectronic Engineering, vol. 73 – 74, pp. 447 – 451, June 2004.

[Fritschi 2005] R. Fritschi, M.B. Pisani, C. Hibert, Ph. Flückiger, A.M. Ionescu, "Technology module for above-IC co-integration of RF MEMS capacitors and inductors". Proc. of the 6th Workshop on MEMS for Millimeter-Wave Communications (MEMSWAVE'05), Lausanne, Switzerland, June 2005, pp. 107.

[Fritschi 2007] R. Fritschi, "Above-IC RF MEMS devices for communication applications", PhD Thesis, Ecole Polytechnique Federale de Lausanne (EPFL), no. 3778 (2007). (http://library.epfl.ch/theses/?nr=3778)

[Fukushige 2003] T. Fukushige, Y. Yokoyama, S. Hata, K. Masu, and A. Shimokohbe, "Fabrication and evaluation of an on-chip micro-variable inductor", Microelectronic Engineering, vol. 67 – 68, 2003, pp. 582 – 587.

[Gallant 2005] A. J. Gallant and D. Wood, "Surface micromachined membranes for wafer level packaging", Journal of Micromechanics and Microengineering. vol. 15, no. 7, pp. S47 – S52. July 2005.

[Gamble 1999] H.S. Gamble, B.M. Armstrong, S.J.N. Mitchell, Y. Wu, V.F. Fusco, and J.A.C. Stewart, "Low-loss CPW lines on surface stabilized high-resistivity silicon", IEEE Microwave and Guided Wave Letters, vol. 9, no. 10, pp. 395 – 397, Oct. 1999.

[Gersteltec] http://www.gersteltec.ch.

[Ghione 1993] G. Ghione, "A CAD-oriented analytical model for the losses of general asymmetric coplanar lines in hybrid and monolithic MICs", IEEE Transactions on Microwave and Techniques, vol. 41, no. 9, pp. 1499 – 1510, Sept. 1993.

[Greenhouse 1974] H. M. Greenhouse, "Design of planar rectangular microelectronic inductors", IEEE Transactions on Parts, Hybrids, and Packaging, vol. PHP-10, pp. 101 – 109, June 1974.

[Grover 1962] F.W. Grover, "Inductance calculations: Working formulas and tables", Dover Publications, 1962 (reediction of the original 1946 book).

[Grovers 1997] R. Grovers, D.L. Harame, and D. Jadus, "Temperature dependence of Q and inductance in spiral inductors fabricated in a silicon-germanium / BiCMOS technology", IEEE Journal of Solid-State Circuits, vol. 32, pp. 1455 – 1459, 1997.

[Guan] B. Guan, P. Rott, and M. J. Feldman, "Fasthenry 2.0R", University of Rochester.

[Gupta 1981] K. C. Gupta, R. Garg and R. Chadha, "Computer-aided design of microwave circuits". Norwood (MA), Artech House, 1981.

[Gupta 1996] K.C. Gupta, R. Garg, I.J. Bahl and P. Bhartia, "Microstrip lines and slotlines", 2nd ed., Artech House, 1996.

[Hafner 1937] S.J. Hafner, "Alternating current of rectangular conductors", Proceedings of the Institute of Radio Engineers, vol. 25, pp. 434 – 447, 1937. (see also [Pettenpaul 1988])

[Hammerstad 1980] E. Hammerstad and O. Jensen, "Accurate models for microstrip computer-aided design", in IEEE Microwave Theory and Techniques Symposium Digest, 1980, pp. 407 – 409.

[Hanington 1968] R.F. Hanington, "Field computation by moment methods", Maxillan, New York, 1968.

[Hara 1988] S. Hara, T. Tokumitsu, T. Tanaka, and M. Aikawa, “Broad-band monolithic microwave active inductor and its application to miniaturized wide-band amplifiers”, IEEE Transactions on Microwave Theory and Techniques, vol. 36, no. 12, pp. 1920 – 1924, 1988.

[Harm 1998] A.O. Harm and K. Mouthaan and E. Aziz and M. Versleijen, “Modelling and simulation of hybrid RF circuits using a versatile compact bondwire model”, in Proceedings of the European Microwave Conference, Amsterdam, pp. 529-534, Oct. 1998.

[Haslett 2001] J.W. Haslett C. Leifso and J. G. McRory, “Monolithic tunable active inductor with independent Q control”, IEEE Transactions on Microwave Theory and Techniques, vol. 49, no. 4, pp. 671 – 676, Apr. 2001.

[Hayashi 1996] H. Hayashi, M. Muraguchi, Y. Umeda, and T. Enoki, “A high-Q broad-band active inductor and its application to a low-loss analog phase shifter”, IEEE Transactions on Microwave Theory and Techniques, vol. 44, no. 12, pp. 2369 – 2374, 1996.

[Helic] Helic SA, VeloceRF inductance modeling tool, http://www.helic.com. (available in Jan. 2007).

[Helszajn 1994] J. Helszajn, “Microwave planar passive circuits and filters”, John Wiley & Sons, Chichester, 1994.

[Hilberg 1969] W. Hilberg, “From approximations to exact relations for characteristic impedances”, IEEE Transactions on Microwave Theory and Techniques, vol. MTT-17, no. 5, pp. 259 – 265, 1969.

[Hoer 1965] C. Hoer and C. Love, “Exact inductance equations for rectangular conductors with applications to more complicated geometries”, Journal of Research of the National Bureau of Standards, vol. 69C, no. 2, pp. 127 – 137, Apr. – June 1965.

[Hoffmann 1987] R.K. Hoffmann, “Handbook of microwave integrated circuits”, Norwood, MA. Artech House, 1987.

[Hsu 2002] H.-M. Hsu, J.-G. Su, Y.-S. Lin, M.-H. Tseng, J. C.-H. Lin, J. Y.-C. Sun, D. Tang, T.-T. Yang, T.-S. Tu, and L.-F. Lin, “High-Q broadband copper spiral inductors with Q = 45 on proton-bombarded semi-insulating silicon substrate”, in Proceedings of the 2002 IEEE Asia-Pacific Conference on ASIC, Aug. 2002, pp. 113 – 116. (http://www.ap-asic.org/2002/2C-4.pdf).

[Hung 2004] J.-J. Hung, L. Dussopt, and G.M. Rebeiz, “Distributed 2- and 3-bit W-band MEMS phase shifters on glass substrates”, IEEE Transactions on Microwave Theory and Techniques, vol. 52, no. 2, pp. 600 – 606, Feb. 2004.

[Jackson 1975] J.D. Jackson, “Classical Electrodynamics”, Wiley, New York, 1975.

[Jansman 2003] A.B.M. Jansman, J.T.M. van Beek, M.H.W.M. van Delden, A.L.A.M. Kemmeren, A. den Dekker, and F.P. Widdershoven, “Elimination of accumulation charge effects for high-resistive silicon substrates”, in Proceedings of the 33rd European Solid-State Device Research Conference (ESSDERC '03), Estoril, Portugal, Sept. 16 – 18, 2003, pp. 3 – 6.

[Jeong 2003] I. Jeong, K.-J. Kim, T.-O. Kong, J.-S. Kim, H.-K. Choi, C.-M. Nam, D.-W. Kim, and Y.-S. Kwon, “High performance RF integrated passive devices on thick oxide substrate using Cu-BCB process”, Microwave and Optical Technology Letters, vol. 37, no. 1, Apr. 2003, pp. 49 – 52, Apr. 2003.

[Jiang 2000] H. Jiang, Y. Wang, J.-L. A. Yeh, and N. C. Tien, “On-chip spiral inductors suspended over deep copper-lined cavities”, IEEE Transactions on Microwave Theory and Techniques, vol. 48, no. 12, pp. 2415 – 2423, Dec. 2000.

[Jourdain 2001] A. Jourdain, S. Brebels, W. De Raedth, and H.A.C. Tilmans, "Influence of 0-level packaging on the microwave performance of RF-MEMS devices", in Proceedings of the 31st European Microwave Conference, Oct. 2001, pp. 1 – 5.

[Jourdain 2003] A. Jourdain, X. Rottenberg, G. Carchon and H.A.C. Tilmans, "Optimization of 0-level packaging for RF-MEMS devices", in Proceedings of the 12th International Conference on Solid-State Sensors, Actuators and Microsystems (Transducers'03), vol. 2, pp. 1915 – 1918, June 2003.

[Jourdain 2005] A. Jourdain, P. De Moor, K. Baert, I. De Wolf and H. A. C. Tilmans, "Mechanical and electrical characterization of BCB as a bond and seal material for cavities housing (RF-) MEMS devices", Journal of Micromechanics and Microengineering, vol. 15, pp. S89 – S96, July 2005.

[Kaanta 1991] C.W. Kaanta, SG. Bombardier, W.J. Cote, W.R. Hill, G. Kerszykowski, H.S. Landis, D.J. Poindexter, C.W. Pollard, G.H. Ross, J.G. Ryan, S. Wolff, and J.E. Cronin, "Dual damascene: a ULSI wiring technology", in Proceedings of the 8th International IEEE VLSI Multilevel Interconnection Conference, 1991, pp. 144 – 152.

[Kamon 1994] M. Kamon, M.J. Tsuk and J. White, "Fasthenry: A multipole accelerated 3-D inductance extraction program", IEEE Transactions on Microwave Theory and Techniques, vol. 42, no. 9, pp. 1750 – 1758, Sept. 1994 (See also http://www.rle.mit.edu/cpg/research_codes.htm and http://www.fastfieldsolvers.com, available in Jan-2007).

[Kaunisto 1995] R. Kaunisto, P. Alinikula, and K. Stadius, "Active inductors for GaAs and bipolar technologies", Analog Integrated Circuits and Signal Processing, vol. 7, pp. 35 – 48, 1995.

[Kim 1996] S. Kim and D. P. Neikirk, "Compact equivalent circuit model for the skin effect", in Proceedings of IEEE Microwave Theory and Techniques Society International Microwave Symposium Digest, June 1996, vol. 3, pp. 1815 – 1818.

[Kim 1998] Y.-J. Kim and M. G. Allen, "Surface micromachined solenoid inductors for high frequency applications", IEEE Trans. Components, Packaging, and Manufacturing Technology, Part C, vol. 21, no. 1, pp. 26 – 33, 1998.

[Kim 1999] S.-J. Kim, Y.-G. Lee, S.-K. Yun, H.-Y. Lee, "Realization of high-Q inductors using wirebond technology", Proc. of the 1999 IEEE Asia-Pacific Conference on ASIC, 1999, pp. 13 – 16 (http://www.ap-asic.org/1999/proceedings/1-4.pdf)

[Kirschning 1984] M. Kirschning and R.H. Jansen, "Accurate wide-range design equations for the frequency-dependent characteristic of parallel coupled microstrip lines", IEEE Transactions on Microwave Theory and Techniques, vol. 32, pp. 83 – 90, Jan. 1984 (this reference has some mistakes corrected in the Agilent ADS manuals).

[Koutsoyannopoulos 1997] Y. Koutsoyannopoulos, Y. Papanos, C. Alemanni and S. Bantas, "A generic CAD model for arbitrarily shaped and multi-layer integrated inductors on silicon substrates", in Proceedings of the 1997 European Solid-State Circuits Conference (ESSCIRC'97), pp. 320 – 323, Sep. 1997.

[Koutsoyannopoulos 2000] Y. Koutsoyannopoulos, Y. Papananos, S. Bantas, and C. Alemanni, "Performance limits of planar and multi-layer integrated inductors", IEEE International Symposium on Circuits and Systems (ISCS 2000), May 2000, Geneva, Switzerland, pp. II-160 – 163.

[KSU] Kansas State University, Spiral Modeling Program (http://www.eece.ksu.edu/vlsi/spiralmod/, in Feb-2007).

[Kuhn 2001] W. B. Kuhn and N. M. Ibrahim, "Analysis of current crowding effects in multiturn spiral inductors", IEEE Transactions on Microwave Theory and Techniques, vol. 49, no. 1, pp. 31 – 38, 2001.

[Lagrange 2000] S. Lagrange, S.H. Brongersma, M. Judelewicz, A. Saerens, I. Vervoort, E. Richard, R. Palmans, and K. Maex, "Self-annealing characterization of electroplated copper films", Microelectronic Engineering, vol. 50, pp. 449 – 457, 2000.

[Lakdawala 2002] H. Lakdawala, X. Zhu, H. Luo, S. Santahannan, L.R. Carley and G.K. Fedder, "Micromachined high Q inductors in a 0.18-μm copper interconnect low-k dielectric CMOS process", IEEE Journal of Solid State Circuits, vol. 37, pp. 394 – 403, 2002.

[Lee 1999] H.-Y. Lee, Y.-G. Lee, S.-J. Kim, and S.-K. Yun, "Novel high Q solenoid inductor using bondwires for GaAs monolithic microwave integrated circuits (MMICs)", Japanese Journal of Applied Physics, vol. 38, pp. L1523 – L1524, 1999.

[Lee 2001] J.-M. Lee, T.-W. Lee, S.Ho. Park, B.-G. Min, M.P. Park, K.-H. Lee, and I.-H. Choi, "Comparison of frequency response of spiral inductors with different figures", Semiconductor Science Technology, vol. 16, pp. 66 – 71, 2001.

[Lee 2004] S. Lee and Y. Kuo, "Hydrogen bromide plasma-copper reaction in a new copper etching process", Thin Solid Films, vol. 457, no. 2, June 2004, pp. 326 – 332.

[Lee 2007] H.H. Lee and J.Y. Park, "Fully embedded high Q circular stacked spiral inductors into organic substrate", Microwave and Optical Technology Letters, vol. 49, no. 5, May 2007, pp. 1074 – 1077.

[Leroy 2006] C. Leroy, M. B. Pisani, C. Hibert, D. Bouvet, M. Puech and A.M. Ionescu, "High quality factor copper inductors integrated in deep dry etched quartz substrates", in Proceedings of the 2006 Symposium on Design, Test, Integration and Packaging of MEMS / MOEMS (DTIP 2006), Stresa, Italy, Apr. 2006.

[Leroy 2006b] C. Leroy, M.B. Pisani, R. Fritschi, C. Hibert and A.M. Ionescu, "High quality factor copper inductors on wafer level quartz package for RF MEMS applications", in Proceedings of the 2006 European Solid-State Device Research Conference (ESSDERC'06), Montreux, Switzerland, Sept. 2006.

[Leroy 2007] C. Leroy, M. B. Pisani, C. Hibert, D. Bouvet, M. Puech and A.M. Ionescu, "High quality factor copper inductors integrated in deep dry etched quartz substrates", Microsystems Technologies, vol. 13, pp. 1483 – 1487, July 2007.

[Liao 2003] C. Liao, C.-W. Liu, and Y.-M. Hsu, "Observation of explosive spectral behaviors in proton-enhanced high Q inductors and their explanations", IEEE Transactions on Electron Devices, vol. 50, pp. 758 – 763, 2003.

[Lin 2002] Y.-S. Lin and H.-M. Hsu, "High-performance micromachined tapered spiral inductors with resonant frequency of 17 GHz", Microwave and Optical Technology Letters, vol. 35, no. 1, Oct. 2002, pp. 56 – 60.

[López-Villegas 2000] J. M. López-Villegas, J. Samitier, C. Cané, P. Losantos, and J. Bausells, "Improvement of the quality factor of RF integrated inductors by layout optimization", IEEE Transactions on Microwave Theory and Techniques, vol. 48, no. 1, pp. 76 – 83, Jan. 2000.

[Lotfi 1995] A.W. Lotfi and F.C. Lee, "Two-dimensional skin effect in power foils for high frequency applications", IEEE Transactions on Magnetics, vol. 31, no. 2, pp. 1003 – 1006, 1995.

[Lu 2007] H. Lu, B. Pillans, J.-C. Lee and J.-B. Lee, "High aspect ratio air core solenoid inductors using an improved UV-LIGA process with contrast enhancement material", Microsystems Technologies, vol. 13, no. 3 – 4, pp. 237 – 243, Feb. 2007.

[Madou 1997] M. Madou, “Fundamentals of microfabrication”. Boca Raton (FL, USA), CRC Press, 1997.

[Malba 1998] D. J. Malba, V. Malba, J. J. Ou, A.-F. Bernhardt, and B.E. Boser, “A low noise RF voltage-controlled oscillator using on-chip high Q three dimensional coil inductor and micromachined variable capacitor”, in Proceedings of the International Electron Devices Meeting (IEDM'98), 1998, pp. 128 – 131.

[Malba 1998b] V. Malba, D. Young, J. J. Ou, A. F. Bernhardt, and B. E. Boser, “High performance RF coil inductors on silicon”, in Proceedings of the Electronic Components and Technology Conference, Seattle, WA, 1998, pp. 252 – 255.

[Markert 1997] M. Markert, A. Bertz and T. Gessner, “Mechanism studies of Cu RIE for VLSI interconnections”, Microelectronic Engineering, vol. 37 – 38, Nov. 1997, pp. 127 – 133.

[Massin 2002] C. Massin, G. Boero, F. Vincent, J. Abenhaim, P.-A. Besse, and R.S. Popovic, “High-Q factor RF planar microcoils for micro-scale NMR spectroscopy”, Sensors and Actuators A, vol. 97 – 98, pp. 280 – 288, 2002.

[Massin 2003] C. Massin, “Microfabricated planar coils in nuclear magnetic resonance”. PhD Thesis, Ecole Polytechnique Federale de Lausanne (EPFL), no. 2913 (2003). (http://library.epfl.ch/theses/?nr=2913)

[Mathworks] Mathworks Inc., Matlab® (Matrix Laboratory), http://www.mathworks.com.

[Mei 2003] S. Mei and Y. I. Ismail, “Modeling skin effect with reduced decoupled R-L circuits”, in Proceedings of the International Symposium on Circuits and Systems (ISCAS'03), May 2003, vol. 4, pp. 588–591.

[Mehdaoui 2005] A. Mehdaoui, R. Fritschi, M. Pisani, F. Casset, A. Ionescu and P. Ancey, “Mixed AlSi-copper technological process for quasi-vertical integration of RF MEMS passive devices”, in Proceedings of the Conference on MEMS for Millimeter-Wave Communications (MEMSWAVE’05), Lausanne, Switzerland, June 2005, pp. 105.

[Mehdaoui 2006] A. Mehdaoui, M.B. Pisani, R. Fritschi, P. Ancey and A.M. Ionescu, “Vertical co-integration of AlSi MEMS tunable capacitors and Cu inductors for tunable LC blocks”, in Proceedings of the Micro and Nanoengineering Conference (MNE'06), pp. 17 – 20, Sep. 2006, Barcelona, Spain.

[Mehdaoui 2007] A. Mehdaoui, C. Fillit, D. Tsamados, R.Y. Fillit, C. Billard, P. Ancey, and A.M. Ionescu, “Co-integration of highly tunable MEMS capacitor and high quality factor AlSi inductors”, in Proceedings of the 8th International Symposium on RF MEMS and RF Microsystems (MEMSWAVE'07), Barcelona, June 2007.

[Mehdaoui 2007b] A. Mehdaoui, M.B. Pisani, R. Fritschi, P. Ancey and A.M. Ionescu, “Vertical co-integration of AlSi MEMS tunable capacitors and Cu inductors for tunable LC blocks”, Microelectronic Engineering, vol. 84, no. 5 – 8, May – Aug. 2007, pp. 1369 – 1373.

[Mehdaoui 2007c] A. Mehdaoui, “Capacités variables et inductances MEMS RF pour une intégration Above IC”. PhD Thesis, Ecole Polytechnique Federale de Lausanne (EPFL), Electronics Laboratory (LEG), no. 3790, 2007. (http://library.epfl.ch/theses/?nr=3790)

[Metz 2004] S. Metz, “Polyimide-based microfabrication technologies for microelectrodes and microfluidic devices in biomedical engineering”. PhD Thesis, Ecole Polytechnique Federale de Lausanne (EPFL), no. 2807, 2003. (http://library.epfl.ch/theses/?nr=2807)

[Mohan 1999] S. S. Mohan, M. Hershenson, S. P. Boyd, and T. H. Lee, “Simple accurate expressions for planar spiral inductances”, IEEE Journal of Solid State Circuits, pp. 1419 – 1424, Oct. 1999.

[Mohan 1999b] S.S. Mohan, The design, modeling and optimization of on-chip inductor and transformer circuits, PhD thesis, Stanford University, Dec. 1999. (available on line at http://www-smirc.stanford.edu/papers/Thesis-mohan.pdf by Dec. 2006).

[Mohan 1998] S. S. Mohan, M. Hershenson, S. P. Boyd, and T. H. Lee, "On-chip spiral inductors with patterned ground shields for Si-based RF IC's", IEEE Journal of Solid State Circuits, pp. 743 – 752, May 1998.

[Mohan 1999] S. S. Mohan, M.M. Hershenson, S.P. Boyd and T.H. Lee, "Simple accurate expression for planar spiral inductances", IEEE Journal of Solid State Circuits, vol. 34, pp. 1419 – 1424, 1999.

[Moore 1965] G.E. Moore, "Cramming more components onto integrated circuits", Electronics, vol. 38, no. 8, Apr. 1965. (ftp://download.intel.com/museum/Moores_Law/Articles-Press_Releases/Gordon_Moore_1965_Article.pdf, on line in Apr-2007).

[Moore 1995] G.E. Moore, "Lithography and the future of Moore's law", in Proceedings of SPIE, vol. 2432, May 1995. (ftp://download.intel.com/museum/Moores_Law/Articles-Press_Releases/1995_SPIE_Speech.pdf in Apr-2007).

[Mouthaan 1997] K. Mouthaan, R. Tinti, M. de Kok, H.C. de Graaff , J.L. Tauritz and J. Slotboom, "Microwave modelling and measurement of the self- and mutual inductance of coupled bondwires", in Proceedings of the 1997 Bipolar / BiCMOS Circuits and Technology Meeting, pp. 166-169, Sept. 1997.

[Nam 1997] C. M. Nam and Y. S. Kwon, "High-performance planar inductor on thick oxidized porous silicon (OPS) substrate," IEEE Microwave and Guided Wave Letters, vol. 7, no. 8, pp. 236 – 238, 1997.

[Neagu 1997] C.R. Neagu and H.V. Jansen, "Characterization of a planar microcoil for implantable microsystems", Sensors and Actuators A, 62 (1997) 599 – 611.

[Nexus] http://www.nexus.com.

[Ng 2001] K.T. Ng, B. Rejaei, and J.N. Burghartz, "Ground pattern for improved characteristics of spiral RF transformers on silicon", Digest of Papers of Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems, 2001, pp. 75 – 78.

[Nguyen 1990] N. M. Nguyen and R. G. Meyer, "Si IC-compatible inductors and LC passive filters", IEEE Journal of Solid-State Circuits, vol. 25, pp. 1028 – 1031, 1990.

[Nguyen 1998] C.T.-C. Nguyen, L.P.B. Katerhi, and G.M. Rebeiz, "Micromachined devices for wireless communications", in Proceedings of the IEEE, vol. 86, no. 8, pp. 1856 – 1758, Aug. 1998.

[Nguyen 2002] C.T.-C Nguyen, "RF MEMS for wireless applications", in 60th Device Research Conference Digest (DRC'02), June 2002, pp. 9 – 12.

[Nieminem 2004] H. Nieminem, J. Kankaanpää, V. Ermolov, S. Silanto and T. Ryhänen, "RF MEMS for 0.8 – 2.5 GHz applications in mobile terminals", in Proceedings of the 4th Workshop on MEMS for Millimeter-Wave Communications (MEMSWAVE'04), 2004, pp. A42 – A48.

[Nieuwoudt 2007] A. Nieuwoudt and Y. Massoud, "Analytical wide-band modeling of high frequency resistance in integrated spiral inductors", Analog Integrated Circuits and Signal Processing, vol. 50, no. 2, Feb. 2007, pp. 133 – 136.

[Niknejad 1998] A.M. Niknejad and R.G. Meyer, "Analysis, design, and optimization of spiral inductors and transformers for Si RF IC's", IEEE Journal of Solid-State Circuits, vol. 33, no. 10, pp. 1470 – 1481, Oct. 1998.

[Niknejad 2000] A.M. Niknejad and R.G. Meyer, "Design, simulation and applications of inductors and transformers for Si RF ICs", Kluwer Academic Publishers, 2000. See also http://rfic.eecs.berkeley.edu/~niknejad/asitic.html (2007).

[Niknejad 2001] A. M. Niknejad and R. G. Meyer, “Analysis of eddy-current losses over conductive substrates with applications to monolithic inductors and transformers”, IEEE Transactions on Microwave Theory and Techniques, vol. 49, pp. 166 – 176, 2001.

[O98] K. O, “Estimation methods for quality factors of inductors fabricated in silicon integrated circuit process technologies”, IEEE Journal of Solid-State Circuits, vol. 33, no. 8, Aug. 1998, pp. 1249 – 1252.

[OEA] OEA International Spiral (http://www.oea.com in 2007).

[Owywang 1958] G.H. Owyang and T.T. Wu, “The approximate parameters for slots lines and their complement”. International Radio Engineers Transactions On Antennas and Propagation, vol. AP-6, no. 1, 1958, pp. 49 – 55.

[Ozgur 1999] M. Ozgur, M. Zaghloul and M. Gaitan, “High Q backside micromachined CMOS inductors”, in Proc. of the IEEE International Symposium on Circuits and Systems, vol.2, pp. 577 – 580, 1999.

[Park 1997] M. Park, S. Lee, H.K. Yu, J.G. Koo, and K.S. Nam, “High Q CMOS-compatible microwave inductors using double-metal interconnection silicon technology”, IEEE Microwave and Guided Wave Letters (see also IEEE Microwave and Wireless Components Letters), vol. 7, no. 2 , Feb. 1997, pp. 45 – 47.

[Park 2003] J.-W. Park, J. Y. Park, Y.-H. Joung, and M.G. Allen, “Tunable RF MEMS microinductors for future communication systems”, in Proceedings of the IEEE International Microwave and Optoelectronics Conference (IMOC'03), vol. 1, Sept. 2003, pp. 541 – 545.

[Patrick 1991] W.L. Patrick, W.L.O. Guthrie, C.L. Standley and P.M. Schiable, “Application of chemical-mechanical polishing to the fabrication of VLSI circuit Interconnections”, Journal of the Electrochemical Society, vol. 138, no. 6, pp. 1978 – 1784, June 1991.

[Pavius 2004] M. Pavius, C. Hibert, P. Flückiger and P. Renaud, “Profile angle control in SiO2 deep anisotropic dry etching for MEMS fabrication”, in Proceedings of the IEEE International Conference on Microelectromechanical Systems (MEMS'04), pp. 669 – 672, 2004.

[Peck 1995] T.L. Peck, R.L. Magin, and P.C. Lauterbur, “Design and analysis of microcoils for MNR microscopy”, Journal of Magnetic Resonance B, vol. 108, no. 2, 1995, pp. 114 – 124.

[Perruisseau-Carrier 2006] J. Perruisseau-Carrier, R. Fritschi, P. Crespo-Valero, and A.K. Skrivervik, “Modeling of periodic distributed MEMS - Application to the design of variable true-time delay lines”, IEEE Transactions on Microwave Theory and Techniques, vol. 54, no. 1, pp. 383 – 392, Jan. 2006.

[Pettenpaul 1988] E. Pettenpaul, H. Kapusta, A. Weisgerber, H. Mampe, J. Luginsland, and I. Wolff, “CAD models of lumped elements on GaAs up to 18 GHz”, IEEE Transactions on Microwave Theory and Techniques, vol. 36, no. 2, 1988, pp. 294 – 304. (see also [Hafner 1937] and [Waldow 1987])

[Pham 2001] N.P. Pham, P.M. Sarro, K.T. Ng, J.N. Burghartz, “A micromachining post-process module with pattern transfer in deep cavities for RF silicon technology”, in Proceedings of the 14th IEEE International Conference on Micro Electro Mechanical Systems (MEMS'01), pp. 345 – 348.

[Piazza 2006] G. Piazza, P.J. Stephanou, A.P. Pisano, “Piezoelectric aluminum nitride vibrating contour-mode MEMS resonators”, Journal of Microelectromechanical Systems, vol. 15, no. 6, Dec. 2006, pp. 1406 – 1418.

[Pieters 1998] P. Pieters and E. Beyne, "Spiral inductors integrated in MCM-D using the design space concept", in Proceedings of the 7th IEEE Multichip Modules and High Density Packaging, 1998. Apr. 1998, pp. 478 – 483.

[Pieters 2001] P. Pieters, K. Vaesen, S. Brebels, S.F. Mahmoud, W. de Raedt, E. Beyne, and R.P. Mertens, "Accurate modeling of high Q spiral inductors in thin-film multilayer technology for wireless telecommunication applications", IEEE Transactions On Microwave Theory and Techniques, vol. 49, no. 4 , Apr. 2001, pp. 589 – 599.

[Pisani 2003] M.B. Pisani, S. Bantas, C. Hibert, M. Trzmiel, C. Pisela, C. Dehollain, M. Declercq, A. M. Ionescu. "High-Q inductors for 1 – 10 GHz applications: modeling, simulation, design and fabrication", in Proceedings of the 4th Workshop on MEMS for Millimeter-Wave Communications (MEMSWAVE'03), Toulouse, France, July 2003, pp. B7.

[Pisani 2003b] M.B. Pisani, C. Hibert, D. Bouvet, P. Beaud and A. M. Ionescu. "Copper / polyimide fabrication process for above RF IC integration of high quality factor inductors", in Proceedings of the Micro and Nanoengineering Conference (MNE'03), Cambridge, United Kingdom, pp. 292 – 293, Sep. 2003.

[Pisani 2004] M.B. Pisani, C. Hibert, D. Bouvet, P. Beaud and A. M. Ionescu. "Copper / polyimide fabrication process for above RF IC integration of high quality factor inductors", Microelectronics Engineering, vol. 73 – 74, pp. 474 – 479, 2004.

[Pisani 2004b] M.B. Pisani, S. Bantas, C. Hibert, M. Trzmiel, C. Pisela, C. Dehollain, M. Declercq, A. M. Ionescu. "High-Q inductors for 1 – 10 GHz applications: modeling, simulation, design and fabrication", MEMS Technologies for Millimeter Wave Devices and Circuits, Series in Micro and Nanoengineering, 5, Romanian Academy Publishing House (Editura Academiei Romane), 2004, pp. 11 – 19, ed. by R. Plana, A. Muller, and D. Dascalu. (ISBN 973-27-1087-X).

[Pisani 2004c] M.B. Pisani, C. Hibert, M. Pavius, D. Bouvet, P. Beaud, C. Dehollain and A.M. Ionescu, "High-Q copper / polyimide inductors: Fabrication results and electrical performance analysis", in Proceedings of the 5th Workshop on MEMS for Millimeter-Wave Communications (MEMSWAVE'04), Uppsala, Sweden, June-July 2004, pp. I 9 – I 12.

[Pisani 2004d] M.B. Pisani, MLib – RF analysis and Passive Design Toolbox, Matlab® toolbox (http://legwww.epfl.ch/~pisani/mlib).

[Pisani 2005] M.B. Pisani, C. Hibert, D. Bouvet, C. Dehollain, A.M. Ionescu, "High-performance copper / polyimide inductors fabricated using thick double metal layer damascene process", in Proceedings of the Workshop on MEMS for Millimeter-Wave Communications (MEMSWAVE'05), Lausanne, Switzerland, June 2005, pp. 121 – 124.

[Pisani 2005b] M.B. Pisani, C. Hibert, D. Bouvet, C. Dehollain and A.M. Ionescu, "Fabrication and electrical characterization of high performance copper / polyimide inductors", Proceedings of the IEEE PhD Research in Microelectronics and Electronics Conference (IEEE-PRIME'05), Lausanne, Switzerland, vol. 1, pp. 185 – 188, July 2005. (ISBN: 0-7803-9345-7).

[Pisani 2005c] M.B. Pisani, C. Hibert, M. Pavius, D. Bouvet, P. Beaud, C. Dehollain and A.M. Ionescu, "High-Q copper / polyimide inductors: Fabrication results and electrical performance analysis" in Advanced MEMS for RF and Millimeter Wave Communications, Series in Micro and Nanoengineering, no. 7, pp. 214 – 221, edited by A. Müller, A. Rydberg and R. Plana, Romanian Academy of Sciences, Bucharest, 2005 (ISBN 973-27-1110-8).

[Post 2000] J.E. Post, “Optimizing the design of spiral inductors on silicon”, IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing, vol. 47, no. 1, Jan. 2000, pp. 15 – 17.

[Pozar 1998] D.M. Pozar, “Microwave engineering”, John Wiley & Sons, New York, 2nd ed., 1998.

[Ramo 1984] S. Ramo, J.R. Whinnery, and T. van Duzer, “Fields and waves in communication electronics”, John Wiley & Sons, New York, 2nd ed, 1984.

[Rebeiz 2001] G.M. Rebeiz and J.B. Muldavin, “RF MEMS switches and switch circuits”, IEEE Microwave Magazine, vol. 2, no. 4, Dec. 2001, pp. 59 – 71.

[Rebeiz 2003] G.M. Rebeiz, “RF MEMS: theory, design, and technology”, John Wiley & Sons, 2003 (chap. 12: Micromachined inductors).

[Reiha 2003] M.T. Reiha, T.-Y. Choi, J.-H. Jeon, S. Mohammadi, and L.P.B. Katehi, “High-Q differential inductors for RFIC design”. In Proceedings of the 33rd European Microwave Conference, vol. 1, Oct. 20003, pp. 127 – 130.

[Reyes 1996] A.C. Reyes, S.M. El-Ghazaly, S. Dorn, M. Dydyk, D.K. Schroder, and H. Patterson, “High resistivity Si as a microwave substrate”, in Proceedings of the 46th Electronic Components and Technology Conference, May 1996, pp. 382 – 391.

[Rijks 2004] Th.G.S.M. Rijks, J.T.M. van Beek, P.G. Steeneken, M.J.E. Ulenaers, J. De Coster and R. Puers, “RF MEMS tunable capacitors with large tuning ratio”, in Proceedings of the IEEE Conference on Microelectromechanical Systems (MEMS'04), Maastricht, Jan. 25 – 29, 2004. pp. 777 – 780.

[Ritzdorf 1998] T. Ritzdorf, L. Graham, S. Jin, C. Mu, and D. Fraser, “Self-annealing of electrochemically deposited copper films in advanced interconnect applications”, in Proceedings of the IEEE International Interconnect Technology Conference, June 1998, pp. 166 – 168.

[Ritzdorf 1999] T. Ritzdorf, L. Chen, D. Fulton, and C. Dundas, “Comparative investigation of plating conditions on self-annealing of electrochemically deposited copper films”, in Proceedings of the IEEE International Conference Interconnect Technology, May 1999, pp. 287 – 289.

[Rong 2004] B. Rong, J.N. Burghartz, L.K. Nanver, B. Rejaei and M. van der Zwanm "Surface-passivated high-resistivity silicon substrates for RFICs”, IEEE Electron Device Letters, vol. 25, no. 4, Apr. 2004, pp. 176 – 178.

[Ronkainen 1997] H. Ronkainen, H. Kattelus, E. Tarvainen, T. Riihisaari, M. Andersson, and P. Kuivalainen, “IC compatible planar inductor on silicon”, IEEE Proceedings on Circuits Devices and Systems, vol. 144, 1997, pp. 29 – 35.

[Royal 1989] R. Royal (ed), “Monolithic microwave integrated circuits: Technology and design”, Norwood (MA,USA), Artech House, 1989.

[Royet 2003] A.S. Royet, R. Cuchet, D. Pellissier, and P. Ancey, “On the investigation of spiral inductors processed on Si substrates with thick porous Si layers”, in Proceedings of the 33rd European Solid-State Device Research Conference (ESSDERC’03), Sept. 2003, pp. 111 – 114.

[Ruehli 1972] A.E. Ruehli, “Inductance calculations in a complex integrated circuit environment”, IBM Journal of Research and Development, vol. 16, Sept. 1972, pp. 470 – 481.

[Sagkol 2002] H. Sagkol, K. Topalli, M. Unlu, O.A. Civi, S. Koc, S. Demir, and T. Akin, “A monolithic phased array with RF MEMS technology”, in Proceedings of the IEEE International Symposium of the Antennas and Propagation Society, vol. 4, no. 16 – 21, June 2002, pp. 760 – 763.

[Samber 1998] M. de Samber, N. Puslford, M. van Delden, and R. Milsom, “Low-complexity MCM-D technology with integrated passives for high frequency applications”, in Proceedings of the International Multichip Modules Conference, Denver, CO, 1998, pp. 285 – 290.

[Schnieder 2001] F. Schnieder and W. Heinrich, “Model of thin-film microstrip for circuit design”, IEEE Transactions on Microwave Theory and Techniques, vol. 49, no. 1, pp. 104 – 110, 2001.

[Steinbrüchel 1995] C. Steinbrüchel, “Patterning of copper for multilevel metallization: reactive ion etching and chemical-mechanical polishing”, Applied Surface Science, vol. 91, no. 1 – 4, Oct. 1995, pp. 139 – 146.

[Steinbrüchel 2001] C. Steinbrüchel and B. L. Chin. "Copper interconnect technology". SPIE Press, Washington, 2001.

[Sen 1998] B. K. Sen and R. L. Wheeler, “Skin effects models for transmission line structures using generic SPICE circuit simulators”, in Proceedings of the IEEE 7th Topical Meeting on Electrical Performance of Electronic Packaging, Oct. 1998, pp. 128–131.

[Shi 2004] J. Shi, K. Kang, T.-S. Yeo, B. Wu, H. Liao, Y. Z. Xiong and S. C. Rustagi, “Temperature effects on the performance of on-chip spiral inductors Used in RF(MM)ICs”, International Journal of Infrared and Millimeter Waves, vol. 25, no. 10, Oct. 2004.

[Shimoto 1995] T. Shimoto, K. Matsui, and K. Utsumi, “Cu / photosensitive – BCB thin film multilayer technology for high performance multichip modules”, IEEE Transactions on Components, Packaging, and Manufacturing Technology A, vol. 18, pp. 11 – 15, Feb. 1995.

[Shi 2004] J. Shi, K. Kang, T.-S. Yeo, B. Wu, H. Liao, Y.Z. Xiong and S.C. Rustagi “Temperature effects on the performance of on-chip spiral inductors Used in RF(MM)ICs”, International Journal of Infrared and Millimeter Waves, vol. 25, no. 10, Oct. 2004, pp. 1511 – 1522.

[Simons 2001] R.N. Simons, “Coplanar waveguide circuits, components and systems”, John Wiley & Sons, 2001.

[Sonnet] Sonnet Software Inc., Liverpool, NY, www.sonnetusa.com.

[Spiegel 1968] M.R. Spiegel, “Mathematical handbook of formulas and tables”, McGraw Hill, New York, 1968.

[Spirito 2005] M. Spirito, F. M. de Paola, L. K. Nanver, E. Valletta, B. Rong, B. Rejaei, L. C. N. de Vreede, and J. N. Burghartz, “Surface-passivated high-resistivity silicon as a true microwave substrate”, IEEE Transactions on Microwave Theory and Techniques, vol. 53, pp. 2340 – 2347, 2005.

[Steinbrüchel 2001] C. Steinbrüchel and B. L. Chin. "Copper interconnect technology". SPIE Press, Washington, 2001.

[Steyaert 1994] M. Steyaert and J. Craninckx, “1.1 GHz oscillator using bondwire inductance”, Electronics Letters , vol.: 3, no. 3 , Feb. 1994, pp. 244 – 245.

[Stojanovic 2006] G. Stojanovic, T. Ljikar, and R. Sordan, “Scaling meander inductors from micro to nano”, in Proceedings of the International Semiconductor Conference, vol. 1, Sept. 2006, pp. 93 – 96.

[Syms 1993] R.R.A. Syms and E.M. Yeatman, “Self-assembly of three-dimensional microstructures using rotation by surface tension forces”, Electronics Letters, vol. 29, no. 8, Apr. 1993, pp. 662 – 664.

[Tan 2000] H.P. Tan, J. G. Ma, K.S. Yeo, and M.A. Do, "High-Q Si-based inductor shielded with double-layer polysilicon for RF applications", Microwave and Optical Technology Letters, vol. 24, no. 6, Mar. 2000, pp. 366 – 367.

[Tassetti 2003] C.M Tassetti, G. Lissorgues, J.P. Gilles, and J.P. Nicole, "New tunable MEMS inductors design for RF und microwave applications", in Proceedings of the 4th Workshop on MEMS for Millimeter-Wave Communications (MEMSWAVE'03), July 2003, pp. H27 – H30.

[Tassetti 2004] C. Tassetti, G. Lissorgues, and J. Gilles, "Reconfigurable RF systems based on tunable MEMS inductors", in Proceedings of the 34th European Microwave Conference, vol. 3, Oct. 2004, pp. 1165 – 1167.

[Ternent 1999] G. Ternent, S. Ferguson, Z. Borsosfoldi, K. Elgaid, T. Lohdi, D. Edgar, C. D. W. Wilkinson, and I. G. Thayne, "Coplanar waveguide transmission lines and high Q inductors on CMOS grade silicon using photoresist and polyimide", Electronics Letters, vol. 35, pp. 1957 – 1958, 1999.

[Tiemeijer 2001] L.F. Tiemeijer, D. Leenaerts, N. Pavlovic, and R.J. Havens, "Record Q spiral inductors in standard CMOS", in IEEE International Electron Devices Meeting Technical Digest (IEDM'01), 2001, pp. 40.7.1 – 40.7.3.

[Tuncer 1993] E. Tuncer, S.Y. Kim, L.T. Pillage, and D.P. Neikirk, "A new, efficient circuit model for microstrip lines including both current crowding and skin depth effects", Electrical Performance of Electronic Packaging, 1993, 20 – 22 Oct. 1993, pp. 85 – 88.

[Unlu 2006] M. Unlu, T. Akin, H.I. Atasoy, O. Bayraktar, O.A. Civi, S. Demir, I. Istanbulluoglu, S. Koc, E.U. Temocin, and K. Topalli, "A reconfigurable RF MEMS triple stub impedance matching network", in Proceedings of the 36th European Microwave Conference, Sept. 2006, pp. 1370 – 1373.

[Vandamme 2001] E. P. Vandamme, D. M. M.-P. Schreurs and C. van Dinther, "Improved tree-sped de-embedding method to accurately account for the influence of pad parasitics in silicon on-wafer RF test-structures", IEEE Transactions on Electron Devices, vol. 48, no. 4, pp. 737 – 742, Apr. 2001.

[Varadan 2003] V.K. Varadan, K.J. Vinoy, and K.A. Jose, "RF MEMS and their Applications", Wiley, 2003.

[Voorman 1993] J.O. Voorman, "Continuous-time analog integrated filters", IEEE Press, 1993.

[Wadell 1991] B.C. Wadell, "Transmission line design handbook". 1st ed. Boston, Artech House, Norwood (USA), 1991.

[Waldow 1987] P. Waldow and I. Wolff, "Dual bounds variational formulation of skin effect problems", in IEEE Microwave Theory and Techniques Society International Microwave Symposium Digest, Las Vegas, 1987, pp. 333 – 336. (see also [Pettenpaul 1988])

[Watenberg 2002] S.A. Wartenberg, "RF measurements of die and packages", Artech House, Boston, 2002.

[Weeks 1979] W.T. Weeks, L.L Wu, M.F. McAlister and A. Singh, "Resistive and inductive skin effect in rectangular conductors", IBM Journal of Research and Development, vol. 23, no. 6, pp. 652 – 660, 1979.

[Weon 2005] D.-H. Weon, J.-I. Kim, J.-H. Jeon, S. Mohammadi, and L.P.B. Katehi, "High performance micro-machined inductors on CMOS substrate", IEEE Microwave Theory and Techniques Society International Microwave Symposium Digest, June 2005, pp. 701 – 704.

[Wheeler 1928] H.A. Wheeler, "Simple inductance formulas for radio coils", in Proceedings of the Institute of Radio Engineers, vol. 16, 1928, pp. 1398 – 1400.

[WTC] WTC Consulting, http://www.wtcconsulting.com.

[Wu 1992] R.-B. Wu, C.-N. Kuo, and K. K, Chang, “Inductance and resistance computations for three-dimensional multiconductor interconnect structures”, IEEE Transactions on Microwave Theory and Techniques, vol. 40, no. 2, pp. 263 – 270, Feb. 1992.

[Wu 1999] Y. Wu, S. Gamble, B.M. Armstrong, V.F. Fusco, and J.A.C. Stewart, “SiO2 interface layer effects on microwave loss of high-resistivity CPW line”, IEEE Microwave and Guided Wave Letters, vol. 9, no. 1, pp. 10 – 12, Jan. 1999.

[Yao 2000] J.J. Yao, “RF MEMS from a device perspective”, Journal of Micromechanics and Microengineering, vol. 10, no. 4, pp. R9 – R38, Dec. 2000.

[Yeo 2000] K.-S. Yeo, J.-G. Ma and M.-A. Do, “Broadband Q Si-based hybrid inductor for RF applications”, Microwave and Optical Technology Letters, vol. 26, no. 4, Aug. 2000, pp. 216 – 219.

[Yoon 1999] J.-B. Yoon, C.-H. Han, E. Yoon, and C.-K. Kim, “Monolithic high Q overhang inductors fabricated on silicon and glass substrates”, in IEEE International Electron Devices Meeting Technical Digest (IEDM'99), 1999, pp. 753 – 755.

[Young 1997] D. J. Young, V. Malba, J.-J. Ou, A. F. Bernhardt, and B. E. Boser, “Monolithic high-performance three-dimensional coil inductors for wireless communication applications”, in Proc. of the IEEE International Electron Device Meeting (IEDM'97), Dec. 1997, pp. 67 – 70.

[Yu 2000] M.-J. Yu, Y.-J. Chan, L-H. Laih, and J.-W. Hong, “Improved microwave performance of spiral inductors on Si substrates by chemically anodizing a porous silicon layer”, Microwave and Optical Technology Letters, vol. 26, no. 4, Aug. 2000, pp. 232 – 234.

[Yue 1996] C. P. Yue, C. Ryu, J. Lau, et al., “A physical model for planar spiral inductors on silicon”, in Proceedings of International Electron Devices Meeting (IEDM'96), 1996, pp. 155 – 158.

[Yue 1998] C. P. Yue and S. S. Wong, “On-chip spiral inductors with patterned ground shields for Si-based RF IC's”, IEEE Journal of Solid-State Circuits, vol. 33, pp. 743 – 752, 1998.

[Yue 2000] C.P. Yue and S.S. Wong, “Physical modeling of spiral inductors on silicon”, IEEE Transactions on Electron Devices, vol. 47, no. 3, pp. 560 – 568, Mar. 2000.

[Zeland] Zeland Software, Zeland’s IE3D, Freemont, CA (USA), www.zeland.com.

[Zolfaghari 2001] A. Zolfaghari, A. Chan, and B. Razavi, “Stacked inductors and transformers in CMOS technology”, IEEE Journal of Solid-State Circuits, vol. 3, no. 4 , Apr. 2001, pp. 620 – 628.

[Zou 2003] J, Zou, C. Liu, D. R. Trainor, J. Chen, J.E. Schutt-Ainé, and P. L. Chapman, “Development of three-dimensional inductors Using Plastic Deformation Magnetic Assembly (PDMA)”, IEEE Transactions On Microwave Theory And Techniques, vol. 51, no. 4, Apr. 2003, pp. 1067 – 1075.

[Zu 1996] L. Zu, Y. Lu, R.C. Frye, M.Y. Lau, S.-C. Chen, D.P. Kossives, J. Lin, and K. L. Tai, “High Q-factor inductors integrated on MCM Si substrates”, IEEE Transactions on Components, Packaging, and Manufacturing Technology B, vol.19, pp. 635 – 643, 1996.

[Zverev 1967] A.I. Zverev, “Handbook of filter synthesis”, John Wiley & Sons, New York, 1967.

Acknowledgements

Achieving a PhD is a hard work that is only possible with the help of many, many people.

I am particularly grateful to Prof. Adrian Ionescu for the opportunity he gave me to join the LEG team. His guiding, enthusiasm, creativity and confidence were essential to make this work real and in all decisions taken before, during and even after this project. Apart from having always a funny story to tell, he also writes the best article titles, abstracts and conclusions I have seen. He always come up with that idea that make you think "why did I not think about it before", even if sometimes it happens just some hours before or after a critical deadline. I also greatly appreciated the help of Dr. Cyrille Hibert for taking in charge the practical aspects involving the co-orientation of the work, the technological choices decision making, for coordinating, operating and working in my training in the CMI equipments and of course for the nice SEM pictures he took or helped me to take. He also contributed to increase my knowledge of funny French language expressions, good food, cheese and wine.

Thanks to Dr. Xavier Gagnard from ST Microelectronics France, Prof. Gianluca Piazza from the University of Pennsylvania, Prof. Radivoje Popovic from EPFL, MER Jean-Michel Sallèse (replacing Prof. Michel Declercq) from EPFL for being part of the evaluation committee and for the valuable and constructive revisions provided for the final version of this report.

Thanks to Dr. Didier Bouvet and Patrice Beaud who took in charge the hard dirty work of developing slurries and receipts for the CMP of thick copper films. Without their talented skills on the mystic practices of CMP this project would not find its way.

Thanks to Raphaël Fritschi for his friendship, for the great help in the technological choices and design, for his patience in sharing the office with me, for helping with the European Research Project reports, for his incredible humor, for being my primary French teacher, for introducing me typical Swiss stuff like kirsch, tête de moine, Jura Bernois, for the company at Satellite and other social activities, for taking care of some bureaucratic stuff during my moving out of Switzerland, for doing some revision in this report and for lending his apartment during our stay for the PhD defense.

Thanks to Roland Guerre for sharing the same office, for teaching me how to pronounce "e" and "u" in French, for the pleasant time we spent together and for the most animated thesis graduation party I could have.

Thanks to Dr. Catherine Dehollain for her contribution and vision from the circuit and systems perspective. Also to Dr. Norbert Joël for the VCO design, simulation and measurements, Jari-Pascal Curty and Nasser Hefeyne for their help with my first insights in the RF measurement world. I cannot forget the students Abheek Gupta, Supratim Ray, Pooja Agarwal, Huynh Nguyen Trang and Manu Agarwal for some initial embryonic work done in the simulation of spiral inductors.

Thanks a lot to Christine Leroy for taking care of the hard work on the process development and with the quartz embedded inductors and packaging. Thanks to Sébastien Jiguet and Gersteltec SA for the help with the SU-8 resist in the packaging project and for the nice time we spent together appreciating good wine, cheese, raclette Savoyarde and other typical French stuff. Thanks also to Giancarlo Corradini for the wire-bonding of the copper / quartz inductors samples. Thanks to Stephan Metz for the initial development of polyimide-based process steps and for the initial training in the use of this material. Thanks also to Matteo Leonardi and Andre Mercanzinni for the fruitful discussions about polyimide based processing.

Special thanks to Isabelle Buzzi, Marie Halm, Karin Bellardinelli-Borcard, Claudia d'Agostino for the assistance given with all that bureaucratic, administrative and academic stuff. Of course I cannot forget the warm reception of Danielle Gallay in my newbie days at the EPFL campus.

Thanks to my Brazilian or half-Brazilian friends at EPFL and in Lausanne, who helped to find a small piece of my hometown in the middle of the mountains and helped with the bureaucratic steps of the PhD while I was out of Switzerland: Cristiano and Grazieli Niclass, Paulo Augusto and Alexandre dal Fabbro, Marcelo Leite Ribeiro, Rodolfo Rabe, Ana da Costa, Bruno and Luciana, Hanso and Alline, Anderson Maciel, Samya and Marcus, Gherhardt and others. Special thanks to Roland and Neuza dos Santos Margueron for the friendship, for the nice time we spent together, for nice views on Swiss places and culture, for the *feijõeszinhos* and *raclettes*, and for their company during our not so long but intense ride in *El Camino de Santiago*.

Thanks for my family in Brazil for all their support, for taking care of all sort of stuff and small everyday problems we have left behind. Special thanks to my mother Alice (in memoriam) and to my father Oswaldo for their commitment in providing me the background and motivation to find my way: you are my real life heroes.

Thanks to my ex-colleagues in Brazil for the great experience provided, for pushing me forward into a new experience and for keeping me informed about what was happening a few kilometers away, especially to Prof. Patrick Verdonck and Prof. Nilton Morimoto.

Thanks for the European Research Projects Wide-RF (IST-2001-33286), Swiss OFES 01.0308, Mimosa (IST-2002-507045) and AMICOM (IST-2003-507352) for funding and for the colleagues of these projects for the nice interaction, collaboration and exchange of ideas, process parameters, designs, simulations, measurements and pieces of silicon wafers. I have to especially thank Tronic's Microsystems France in the person of Marjorie Trzmiel and Christian Pisella for the exchanges of designs and for providing gold inductor samples and Helic SA Greece for the support provided using VeloceRF simulator. Thanks to the National Institute for Research and Development in Microtechnologies RF design group (IMT, Bucharest, Romania), especially to Andrei Muller, Alexandru Muller and Dan Neculoiu for providing designs of LC filters for the GSM and WLAN applications. Thanks also to Julien Perruisseau-Carrier for the HFSS simulation results and to Prof. Anja Skrivervik and Prof. Juan Mosig from the Laboratory of Electromagnetism and Acoustics at EPFL (LEMA) for the valuable discussions about RF modeling, simulation and measurements.

Thanks to the LEG staff for taking care of basic laboratory infra-structure, especially to Joseph Guzzardi, Raymond Sutter and Roland Jaques.

Many to thanks to the CMI staff: Philippe Flückiger, Georges Brélaz, Roberto Mancini, William Baer, Yrène Magnenat, Philippe Langlet, Yvan and Paulette Deillon, Georges-Andrès Racine, Guy Clerc with the heavy sputtering targets, Michael Pavius, Jan Schildknecht, Pierrick Duvoisin, Faouzi Khechana, and Jean Marie-Voirol for the basic training on almost all machines available in the CMI and for keeping a really nice clean room working like a Swiss clock. Thanks also for the good time we spent together in the annual promenade, fondue and mountain days.

Thanks to Alexandre Mehdaoui for the nice sharing of knowledge when developing common copper / polyimide fabrication process steps, especially for the fabrication and measurement of the filter circuits.

Thanks to the colleagues of LEG for the excellent atmosphere and exchange of ideas: Marco Mazza and his ripe oranges and tomatoes, Kirsten Moselund, Serge Ecofey, Montserat Fernandez-Bolaños, Daniel Grogg, Diana Badila, Julien and Kathy Boucard, Dimitrios Tsamados, Nicolas Abélé and his fast speaking Parisian accent, and especially Vincent Pott for some simulations and for the noise produced in the electrical measurement laboratory.

Thanks for the French teachers at the EPFL Language Learning Center and at "Français en Jeu" Lausanne, especially to Raphaël Noir for the practical lesson on how to prepare a fondue and Anne Monti for the pleasant French conversations and nice Belgium coffee.

Thanks for the medical team of CHUV, especially Dr. Hottinger, for taking care of my (hopefully dead) "*helicobacter pylori*".

Thank you Roberta for accepting to take full part in this adventure, for your effort in finding your way in Switzerland, for the love and patience you provide me in the good and bad times, for the inspiration, for writing letters to complain about heath insurance, credit card, telephone and apartment management and for taking care of revising these acknowledgments.

For many other people that crossed my way and helped this thesis to be real by a series of small but very important actions and have eventually and involuntary forgotten to be included in this small and certainly incomplete list.

Vitae

<u>Marcelo Bento PISANI</u>
Born in Sao Paulo – SP (Brazil), Brazilian Citizen, married

Education

2007 **PhD Thesis in Electrical Engineering and Microsystems**. Ecole Polytechnique Federale de Lausanne (Swiss Federal Institute of Technology - EPFL). Thesis Subject**:** *Copper / Low k Technological Platform for the Fabrication of High-Quality Factor Above-IC Passive Devices.*

2001 **M.Sc. in Electrical Engineering**. Polytechnic School of the University of Sao Paulo - Brazil. Dissertation subject**:** *RF Electrical Measurements and Plasma Processing*.

1996 **B.Sc. in Physics**. Physics Institute of the University of Sao Paulo - Brazil.

1991 **Technician in Electronics**. Federal Technical School of Sao Paulo (ETFSP).

Professional

2006/7 **Post-doctoral researcher, University of Pennsylvania, Electrical and Systems Engineering Department**. Activities: Development and optimization of AlN piezoelectric RF MEMS and NEMS applications (resonators, oscillators, filters and piezoelectric RF switches and variable capacitors). DARPA / Honeywell funded research programs.

2002 **Research Assistant, Swiss Federal Institute of Technology** – École Polytechnique Fédérale de Lausanne (EPFL), Electronics Laboratory (LEG) and Center of Micro and Nanotechnology (CMI). Activities: Development of a new Cu / low κ process module for the fabrication of high quality factor above IC integrated passive devices (inductors and capacitors). EU funded research projects (WideRF, MIMOSA and Amicom). Support to teaching activities.

1998 **Assistant Professor**, **Technology Faculty of Sao Paulo (Fatec-SP)**. Courses: Semiconductor Devices Fabrication Steps and Processes.

1991 **Laboratory Technician**, **Polytechnic School of the University of Sao Paulo, Integrated Systems Laboratory**. Activities: Project, maintenance and operation of scientific electronic equipment. Operation and maintenance of clean-room facilities and material characterization instruments.

Publication List

- **Conference and Journal Papers**

[1] A. Mehdaoui, M.B. Pisani, R. Fritschi, P. Ancey and A.M. Ionescu, “Vertical co-integration of AlSi MEMS tunable capacitors and Cu inductors for tunable LC blocks”, **Microelectronic Engineering**, vol. 84, no. 5 – 8, May – Aug. 2007, pp. 1369 – 1373.

[2] A. Mehdaoui, M.B. Pisani, R. Fritschi, P. Ancey and A.M. Ionescu, “Vertical co-integration of AlSi MEMS tunable capacitors and Cu inductors for tunable LC blocks”, **Proceedings of the MNE 2006 Conference**, Barcelona, Spain, 17 – 20 Sep. 2006.

[3] C. Leroy, M. B. Pisani, C. Hibert, D. Bouvet, M. Puech and A.M. Ionescu, “High quality factor copper inductors integrated in deep dry etched quartz substrates”, **Microsystems Technologies**, vol. 13, pp. 1483 – 1487, July 2007.

[4] C. Leroy, M.B. Pisani, R. Fritschi, C. Hibert and A.M. Ionescu, “High quality factor copper inductors on wafer level quartz package for RF MEMS Applications”, **Proceedings of the 2006 ESSDERC Conference**, Montreux, Switzerland, Sept. 2006.

[5] C. Leroy, M. B. Pisani, C. Hibert, D. Bouvet, M. Puech and A.M. Ionescu, “High quality factor copper inductors integrated in deep dry etched quartz substrates”, **Proceedings of the 2006 Symposium on Design, Test, Integration and Packaging of MEMS / MOEMS** (DTIP 2006), Stresa, Italy, Apr. 2006.

[6] C. Leroy, M. B. Pisani, C. Hibert, D. Bouvet, M. Puech and A.M. Ionescu, “High quality factor copper inductors integrated in deep dry etched quartz substrates”, **Microsystems Technology**, vol. 13, pp. 1483 – 1487, 2007.

[7] A. Mehdaoui, M.B. Pisani, D. Tsamados, F. Casset, P. Ancey and A.M. Ionescu, “MEMS tunable capacitor with fragmented electrodes and rotational electro-thermal drive”, **Proceedings of the 2006 Symposium on Design, Test, Integration and Packaging of MEMS / MOEMS** (DTIP'06), Stresa, Italy, Apr. 2006.

[8] M.B. Pisani, C. Hibert, D. Bouvet, C. Dehollain and A.M. Ionescu, “Fabrication and electrical characterization of high performance copper / polyimide inductors”, **Proceedings of the IEEE 2005 PhD Research in Microelectronics and Electronics Conference** (IEEE-PRIME’05), Lausanne, Switzerland, vol. 1, pp. 185 – 188, July 2005. (ISBN: 0-7803-9345-7).

[9] M.B. Pisani, C. Hibert, M. Pavius, D. Bouvet, P. Beaud, C. Dehollain and A.M. Ionescu, “High-Q copper / polyimide inductors: Fabrication results and electrical performance analysis” in **Advanced MEMS for RF and Millimeter Wave Communications**, Series in Micro and Nanoengineering, no. 7, pp. 214 – 221, edited by A. Müller, A. Rydberg and R. Plana, Romanian Academy of Sciences, Bucharest, 2005 (ISBN 973-27-1110-8).

[10] M.B. Pisani, C. Hibert, M. Pavius, D. Bouvet, P. Beaud, C. Dehollain and A.M. Ionescu, “High-Q copper / polyimide inductors: Fabrication results and electrical performance analysis”, **Proceedings of the 5th Workshop on MEMS for Millimeter-Wave Communications** (MEMSWAVE’04), Uppsala, Sweden, June-July 2004, pp. I 9 – I 12.

[11] M.B. Pisani, C. Hibert, D. Bouvet, C. Dehollain, A.M. Ionescu, "High-performance copper/polyimide inductors fabricated using thick double metal layer damascene process". **Proceedings of the 2005 Workshop on MEMS for Millimeter-Wave Communications** (MEMSWAVE'05), Lausanne, Switzerland, June 2005, pp. 121 – 124.

[12] M.B. Pisani, C. Hibert, D. Bouvet, P. Beaud and A. M. Ionescu. "Copper/polyimide fabrication process for above RF IC integration of high quality factor inductors". **Microelectronics Engineering**, vol. 73 – 74, pp. 474 – 479, 2004. Also published in the **Proceedings of Micro and Nano Engineering Conference** (MNE'03), Cambridge, United Kingdom, pp. 292-293, Sep. 2003.

[13] M.B. Pisani, S. Bantas, C. Hibert, M. Trzmiel, C. Pisela, C. Dehollain, M. Declercq, A. M. Ionescu. "High-Q inductors for 1 – 10 GHz applications: modeling, simulation, design and fabrication", MEMS Technologies for Millimeter Wave Devices and Circuits, Series in Micro and Nanoengineering, 5, Romanian Academy Publishing House, 2004, pp. 11-19. (ISBN 973-27-1087-X). Also published in the **Proceedings of the 4th Workshop on MEMS for Millimeter-Wave Communications** (MEMSWAVE'03), Toulouse, France, July 2003, pp. B 7.

[14] M.B. Pisani, P. Verdonck. Characterization of SF_6 plasmas by RF electrical measurements. In: SYMPOSIUM ON MICROELECTRONICS TECHNOLOGY AND DEVICES, 17., Porto Alegre (RS, Brazil), Sept. 2002. **Proceedings.** São Paulo, Sociedade Brasileira de Microeletrônica (*Brazilian Microelectronics Society*), 2002, n.p.

[15] M.B. Pisani, P. Verdonck. RF electrical measurements in plasma processing reactors. In: INTERNATIONAL CONFERENCE ON MICROELECTRONICS AND PACKAGING, 15., Manaus (AM, Brazil), Sept. 2000. **Proceedings**. São Paulo, Sociedade Brasileira de Microeletrônica (*Brazilian Microelectronics Society*), 2000. pp. 348 – 351.

[16] R.M. de Castro, P. Verdonck, M.B. Pisani, R.D. Mansano, G.A. Cirino, H.S. Maciel, M. Massi. End-point detection of polymer etching using Langmuir probes. **IEEE Transactions on Plasma Science**, v.28, n.3, pp. 1043 – 49, June 2000.

[17] M. Massi, R.D. Mansano, P. Verdonck, H.S. Maciel, G.A. Cirino, R.M. de Castro, M.B. Pisani. Performance characterization of an RIE reactor with built-in excitation antenna. **Journal of Solid-State Devices and Circuits**, v.8, n.1, pp. 1 – 4, Feb. 2000.

[18] R.M. de Castro, P. Verdonck, M.B. Pisani, R.D. Mansano, G.A. Cirino, H.S. Maciel, M. Massi. The applicability of Langmuir probes for end point detection of polymer etching. In INTERNATIONAL CONFERENCE ON MICROELECTRONICS AND PACKAGING, 14., Campinas (SP, Brazil), Aug. 1999. **Proceedings.** São Paulo, Sociedade Brasileira de Microeletrônica (*Brazilian Microelectronics Society*), 1999. pp. 24 – 28.

[19] R.M. de Castro, G.A. Cirino, P. Verdonck, H.S. Maciel, M. Massi, M.B. Pisani, R.D. Mansano. A comparative study of single and double Langmuir probe techniques for RF plasma characterization. **Contributions to Plasma Physics**, v.39, n.3, pp. 235 – 246, 1999.

[20] R.M. de Castro, G.A. Cirino, P. Verdonck, H.S. Maciel, M. Massi, M.B. Pisani, R.D. Mansano. Comparison between single and double Langmuir probe techniques for analysis of inductively coupled plasmas. In INTERNATIONAL CONFERENCE ON MICROELECTRONICS AND PACKAGING, 13. **Proceedings.** Curitiba (PR, Brazil), Sociedade Brasileira de Microeletrônica (*Brazilian Microelectronics Society*), 1998. v.1, pp. 508 – 14. (Also published in **Boletim Técnico da Escola Politécnica da USP** (*Technical Report of the Polytechnic School of the University of São Paulo*)**,** n. BT / PEE / 9824, n.p., 1998.)

- **Abstracts, Posters, Panels and Other Technical Communications**

[1] A. Mehdaoui, R. Fritschi, M. Pisani, F. Casset, A. Ionescu and P. Ancey, “Mixed AlSi-copper technological process for quasi-vertical integration of RF MEMS passive devices”. **Abstracts**. Proceedings of the Conference on MEMS for Millimeter-Wave Communications (MEMSWAVE’05), Lausanne, Switzerland, June 2005, pp. 105.

[2] R. Fritschi, M.B. Pisani, C. Hibert, Ph. Flückiger, A.M. Ionescu, “Technology module for above-IC co-integration of RF MEMS capacitors and inductors”. **Abstracts**. Proceedings of the Conference on MEMS for Millimeter-Wave Communications (MEMSWAVE’05), Lausanne, Switzerland, June 2005, pp. 107.

[3] M.B. Pisani, P. Verdonck. RF electrical measurements in argon and SF_6 discharges. In ENCONTRO BRASILEIRO DE FÍSICA DE PLASMAS – EBFP, 6., Campos do Jordão (SP, Brazil), Dec. 2001. (*6th Brazilian Plasma Physics Meeting*). **Abstracts**. São Paulo, Sociedade Brasileira de Física (*Brazilian Physical Society*), s.d., n.p.

[4] M.B. Pisani, R.M. de Castro, G.A. Cirino and P.B. Verdonck. Single, double and floating Langmuir probe measurement system for RF discharge studies. In ENCONTRO BRASILEIRO DE FÍSICA DE PLASMA – EBFP, 6., Campos do Jordão (SP, Brazil), Dec. 2001. (*6th Brazilian Plasma Physics Meeting*). **Abstracts**. São Paulo, Sociedade Brasileira de Física (*Brazilian Physical Society*), s.d., n.p.

[5] M.B. Pisani, P. Verdonck. Development of an RF electrical measurement system for a plasma etching tool. In WORKSHOP DO SISTEMA BRASILEIRO DE TECNOLOGIA DE INFORMAÇÃO (SIBRATI), 4., São Paulo, Mar. 2001. (*4th Brazilian Information Technology System Workshop*). **Abstracts**. São Paulo, Escola Politécnica da USP, 2001, n.p.

[6] M.B. Pisani, P. Verdonck. Utilização de plasmas indutivos para corrosão de silício. (*The use of inductive plasmas in the silicon etching*). In CONGRESSO BRASILEIRO DE APLICAÇÕES DE VÁCUO NA INDÚSTRIA E NA CIÊNCIA, 20. São Paulo, July 1999. (*20th Brazilian Congress of Vacuum Applications on Industry and Science*). **Abstracts.** Campinas, Sociedade Brasileira de Vácuo (*Brazilian Vacuum Society*), 1999, pp. 65, ref.068.

[7] M.B. Pisani, R.D. Mansano, P. Verdonck. Aplicação de plasmas de baixa freqüência em processos de corrosão de silício e fotorresiste. (*Application of low-frequency plasmas to silicon and photoresist etching*). In CONGRESSO BRASILEIRO DE APLICAÇÕES DE VÁCUO NA INDÚSTRIA E NA CIÊNCIA, 18., Petrópolis (RJ, Brazil), July 1997. (*18th Brazilian Congress of Vacuum Applications on Industry and Science*). **Abstracts.** Campinas, Sociedade Brasileira de Vácuo (*Brazilian Vacuum Society*), 1997. n.p., ref.051.

[8] M. Massi, R.D. Mansano, P. Verdonck, H.S. Maciel, M.B. Pisani, G.A. Cirino. Performance characterisation of an RIE reactor with a built-in RF excitation coil. In NATIONAL SYMPOSIUM OF THE AMERICAN VACUUM SOCIETY, 44., San Jose (CA, USA), Oct. 1997. **Abstracts.** San Jose, American Vacuum Society, 1997, pp. 46.

[9] M.B. Pisani, R.D. Mansano, P. Verdonck. Projeto e caracterização de um gerador de baixas freqüências aplicado à corrosão por plasma. (*Design and characterization of a low-frequency generator applied to plasma etching*). In CONGRESSO BRASILEIRO DE APLICAÇÕES DE VÁCUO NA INDÚSTRIA E NA CIÊNCIA, 16. Brasília (DF, Brazil), July 1995. (*16th Brazilian Congress of Vacuum Applications on Industry and Science*). **Abstracts.** Campinas, Sociedade Brasileira de Vácuo (*Brazilian Vacuum Society*), 1995, n.p., ref.064.

[10] R.M. Franzin, P. Verdonck, R.D. Mansano, N. Ordonez, M.B. Pisani. Projeto e construção de um equipamento de corrosão de alumínio por plasma. (*Design and implementation of an aluminum plasma etching equipment*). In CONGRESSO BRASILEIRO DE APLICAÇÕES DE VÁCUO NA INDÚSTRIA E NA CIÊNCIA, 13., Campinas, July 1992. (*13th Brazilian Congress of Vacuum Applications on Industry and Science*). **Abstracts.** Campinas, Sociedade Brasileira de Vácuo (*Brazilian Vacuum Society*), 1992, n.p., ref.060.

- **Technical reports, Dissertations, Tutorials, Software.**

[1] M.B. Pisani. **Copper / Low k Technological Platform for the Fabrication of High-Quality Factor Above-IC Passive Devices**. Lausanne. 2007. Dissertation (PhD) – Ecole Polytechnique Federale de Lausanne (EPFL). Advisor: Prof. Adrian M. Ionescu. (http://library.epfl.ch/theses/?nr=3831)

[2] M.B. Pisani, **MLib – RF analysis and Passive Design Toolbox**, Matlab® toolbox (http://legwww.epfl.ch/~pisani/mlib).

[3] M.B. Pisani, **Characterization of RF Passive Devices by S-parameter Measurements**, Electronics Laboratory Series of Tutorials, June 2006.

[4] M.B. Pisani, **How to Effectively Measure S-Parameter Data**, Internal EPFL technical report, Oct. 2006.

[5] M.B. Pisani. **Medidas elétricas de RF em reatores de processamento a plasma.** (*RF electrical measurements in plasma processing reactors*). São Paulo. 2001. 128p. Dissertation (Master of Science) – Escola Politécnica da Universidade de São Paulo – Departamento de Engenharia Elétrica (*Polytechnic Scholl of the University of São Paulo – Department of Electrical Engineering*). Advisor: Prof. Patrick B. Verdonck.