FERROELECTRIC GATE ON AlGaN/GaN HETEROSTRUCTURES

THÈSE N^{O} 3821 (2007)

PRÉSENTÉE LE 4 JUIN 2007

À LA FACULTÉ DES SCIENCES ET TECHNIQUES DE L'INGÉNIEUR

Laboratoire de céramique

SECTION DE SCIENCE ET GÉNIE DES MATÉRIAUX

ÉCOLE POLYTECHNIQUE FÉDÉRALE DE LAUSANNE

POUR L'OBTENTION DU GRADE DE DOCTEUR ÈS SCIENCES

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ÉCOLE POLYTECHNIQUE
FÉDÉRALE DE LAUSANNE

Lausanne, EPFL
2007

Abstract

The capability of switching the spontaneous polarisation under an applied electric field in ferroelectric materials can be exploited for the use in low power, non-volatile, re-writable memory devices. Currently available commercially is ferroelectric random access memory, FeRAM, which allows for high speed, low voltage and greater write-erase endurance compared to its two main competitors, Flash and EEPROM, when using the one transistor - one capacitor configuration. However, it is desired to further optimise the configuration in order to obtain better densification, faster access time and better reliability. One way to do such is to pass from the ferroelectric capacitors and develop ferroelectric field effect transistors.

Exploiting the phenomenon of ferroelectricity and integrating ferroelectrics with the semiconductor technology has not been simple. The FeFET has been demonstrated using a silicon-based transistor, however commercial devices are not available. Challenges arise mainly due to the high temperature deposition of perovskite ferroelectrics causing the degradation of the ferroelectric/semiconductor interface due to inter-diffusion. Acquiring long term retention of the transistor behavior has also been problematic due to phenomenons such as charge injection and depolarisation.

In this thesis a new approach to the problem of semiconductor devices with a ferroelectric gate is explored. Instead of using a silicon-based device, semiconductor heterostructures are investigated. Combining the high mobility channel existing in semiconductor heterostructures, with the non-volatile switching of the polarisation in the ferroelectric gate can pave the way to novel future devices.

The AlGaN/GaN semiconductor heterostructure was chosen for two main reasons. The first is a two dimensional electron gas, 2DEG, located at the AlGaN/GaN interface which possesses better transport properties than a single layered semiconductor. Secondly, GaN and its alloys are known to have large chemical and temperature stability making them ideal to withstand the high temperature deposition process of perovskite ferroelectrics.

The deposition of two ferroelectric layers onto the AlGaN heterostructure were investigated. Lead zirconium titanate, PZT, a traditional perovskite ferroelectric deposited at high temperature, was chosen for its high remanent polarisation and low coercive field. An alternative ferroelectric gate, the co-polymer poly(vinylidene fluoride/trifluoroethylene), P(VDF/TrFE)(70:30) was deposited and of interest due its low crystallisation temperature and low dielectric constant. Its remanent polarisation is smaller and coercive field larger than that of PZT, but were determined sufficient to observe the depletion effect in the two dimensional electron gas.

The goals accomplished in this research were:

Development of Ferroelectric Gate Processing: Deposition processes of the ferroelectric layers were developed and optimised in order to obtain a high quality ferroelectric, while maintaining the original transport properties of AlGaNs 2DEG. The processing of HfO_2 and MgO buffer layers were developed and investigated for their effects on limiting unwanted inter-diffusion and charge injection.

PZT Gate on $Al_{0.3}Ga_{0.7}N$: The first successful development and observation of a PZT gate on a $Al_{0.3}Ga_{0.7}N/GaN$ heterostrucutre was accomplished. A (111) oriented PZT(40:60) ferroelectric gate on the $Al_{0.3}Ga_{0.7}N$ heterostructure depleted the sheet resistance of the 2DEG by a factor of three when poling the PZT layer with $-40\,V$ directly to the conductive cantilever used in a piezoresponse force microscope. This decrease in sheet resistance was stable for more than three days.

P(VDF/TrFE)(70:30) Gate on $Al_{0.3}Ga_{0.7}N$: The ferroelectric co-polymer P(VDF/-TrFE) (70:30) was investigated as a gate on the $Al_{0.3}Ga_{0.7}N$ heterostructure. When the P(VDF/TrFE) was poled with $-30\,V$ to a top electrode the sheet resistance was modulated by a factor three, however there was no retention of this modulation.

Ferroelectric Spontaneous Polarisation on a Semiconductor Heterostructure: It was theoretically derived that when depositing a ferroelectric layer onto a semiconductor heterostructure its spontaneous polarisation is dramatically reduced due to the depolarisation field and may be suppressed completely. This decay in spontaneous polarisation can be minimised by using a ferroelectric layer with a small dielectric constant, which justifies the use of ferroelectric polymers as the gate material.

Domain Writing: The technique of domain writing using piezoresponse force microscopy showed that it was possible to create domain patterning on the ferroelectric layers that were deposited onto the $Al_{0.3}Ga_{0.7}N$ heterostructure with sub-micron line resolution, on the order of 300 nm or better.

Using ferroelectrics on semiconductors is not only limited to ferroelectric memory devices. Other applications could be ferroelectric nano-lithography, where a ferroelectric pattern is written with a piezoresponse force microscope, PFM, and this pattern is projected onto the transistors channel, potentially creating quantum/ballistic devices.

The challenge of integrating ferroelectrics with semiconductors has yet to be fully understood. One of the main advancements that was reached with this research is the understanding of the decrease of the spontaneous polarisation when a ferrroelectric layer is deposited onto a semiconductor heterostructure of finite thickness. The maximisation of the ferroelectrics polarisation on 20 nm of $Al_{0.3}Ga_{0.7}N$ can be obtained when minimising the dielectric constant of the ferroelectric layer. The current challenge is to get a better physical understanding of the limitation of the retention of the spontaneous polarisation, while discovering methods for its improvement.

Keywords: ferroelectric gate, AlGaN/GaN heterostructure, two dimensional electron gas, ferroelectric field effect transistor

Version Abrégée

La capacité de changer la polarisation spontanée sous l'application d'un champ éléctrique dans les matériaux ferroélectriques peut être utilisée dans les mémoires de pouvoir bas, non-volatile et ré-inscriptible. Les mémoires ferroélectriques à accès aléatoire, FeRAM, sont actuellement disponibles commercialement. Elles permettent des temps d'accès rapides, une faible consommation et une endurance supérieure d'écriture-effacement en comparison de ses deux principaux concurrents, Flash et EEPROM, en configuration d'un transistor - un capaciteur. Cependant, il est désiré d'optimiser cette configuration afin d'obtenir une meilleure densification, des temps d'accès encore plus rapide et une meilleure fiabilité. Une manière de le faire consiste à remplacer les capaciteurs ferroélectriques directement par des transistors ferroélectriques.

Exploiter ce phénomène en intégrant des ferroélectriques à la technologie des semi-conducteurs n'a pas été simple. Le FeFET a déjà été démontré en utilisant un transistor de silicium, cependant ces dispositifs ne sont pas disponibles commercialement. La principale difficulté est la haute température de déposition des pérovskites ferroélectriques, dégradant l'interface ferroélectrique/semi-conducteur en raison d'interdiffusion. Le comportement de rétention à long terme du transistor a aussi été problématique en raison des phénomènes d'injection de charges et de dépolarisation.

Dans cette thèse, une nouvelle approche des dispositifs semi-conducteur à grille ferroélectrique est abordée. En effet, les dispositiifs basés sur la technologie du silicium sont remplacés par des semi-conducteurs à hétérostructures. La combinaison de la mobilité élevée, présente dans les semi-conducteurs à hétérostructure, et de la commutation non-volatile de la polarisation dans la grille ferroélectrique laisse envisager de nouvelles possibilités de développement pour des dispositifs originaux.

Les semi-conducteurs à hétérostructure d'AlGaN/GaN ont été choisis pour deux raisons principales. Premièrement, un gaz à deux dimensions d'électron, 2DEG, est localisé à l'interface d'AlGaN/GaN. Celui-ci possède des propriétés de transport plus hautes qu'un semi-conducteur mono-couche. Deuxièmement, le GaN, et ses alliages, est connu pour avoir une grande stabilité chimique et thermique, ce qui fait du GaN un candidat idéal pour le procédé de déposition à haute température de la perovskite ferroélectrique.

Deux couches ferroélectriques différentes ont été déposée sur l'hétérostructure de AlGaN. La première, le zirconate de titanate de plomb, PZT, une perovskite ferroélectrique traditionnellement déposée à hautes températures, a été choisie pour sa haute polarisation rémanente et son faible champ coercitif. La deuxième déposition a été celle d'une grille ferroélectrique alternative, à base de co-polymère poly(fluoré/trifluoroethylene de vinylidene) P(VDF/TrFE)(70:30). L'intérêt de ce co-polymère est sa basse température de cristallisation et sa faible constante diélectrique. Malgré sa polarisation rémanente plus faible et son champ coercitif plus élevée que ceux du PZT, ses propriétés ont été jugées

suffisantes pour observer l'effet d'épuisement d'électrons dans le 2DEG.

Les buts atteints dans cette thèse sont :

Dévelopement du Procédé de la Grille Ferroélectrique: Le procédé de déposition des couches ferroélectriques a été optimisé pour obtenir une couche de haute qualité tout en maintenant les propriètes de transport originelles du 2DEG. Deux couches tampon de HfO_2 et de MgO, ont été aussi développées pour limiter l'interdiffusion et l'injection de charge.

Grille de PZT sur $Al_{0.3}Ga_{0.7}N$: L'effet de grille du PZT sur l'hétérostructure d'$Al_{0.3}Ga_{0.7}N$ a pu être observé. Une grille de 130 nm de PZT(40:60), d'orientation préférentiellle (111), a été pulvérisée sur l'hétérostructure de $Al_{0.3}Ga_{0.7}N$. Cette couche de PZT a modulé la résistance surfacique du 2DEG par un facteur trois en polarisant la couche PZT avec une tension de -40 V directement sur le levier quantique conducteur d'un microscope à force atomique utilisé en réponse piézoélectrique, PFM. Cette diminution de la résistance surfacique a été stable pendant plus de trois jours.

Grille de P(VDF/TrFE)(70:30) sur $Al_{0.3}Ga_{0.7}N$: 250 nm du co-polymère ferroélectrique poly(fluoré/trifluoroethylene de vinylidene) P(VDF/TrFE)(70:30) ont été déposé sur l'hétérostructure de $Al_{0.3}Ga_{0.7}N$. Sous l'application d'une tension de -30 V sur cette grille, la résistance surfacique du 2DEG a diminué par un facteur trois, cependant aucune rétention de cette épuisement d'électrons n'a été mesurée.

Polarisation Spontanée Ferroélectrique sur l'Hétérostructure Semi-Conductrice: Il a été théoriquement démontré qu'en déposant une couche ferroélectrique sur une hétérostructure semi-conductrice, la polarisation spontanée de celle-ci sera réduite en raison de la compensation de charge incomplète ou inexistante. Cette réduction de la polarisation spontanée peut être minimisé en utilisant un ferroélectrique à faible constante diélectrique.

L'Écriture des Domaines: La technique d'écriture des domaines utilisant la microscopie à réponse piézoélectrique a montré qu'il était possible de créer des modèles de domaines sur les couches ferroélectriques déposées sur l'hétérostructure de $Al_{0.3}Ga_{0.7}N$ avec une résolution sub-micronique d'environ 300 nm.

L'utilisation des ferroélectriques sur les semi-conducteurs n'est pas seulement limitée à des dispositifs à mémoire ferroélectriques. Les autres applications pourraient être dans le domaine de la nano-lithographie ferroélectrique où une structure ferroélectrique est écrite avec un microscope à réponse piézoélectrique, PFM. Cette structure est ensuite projetée sur une chaîne du transistor, pouvant créer des dispositifs quantique/balistiques.

Le challenge d'intégrer des ferroélectriques et des semi-conducteurs n'est toujours pas entièrement assimilé. Un des avancements principaux qui a été atteint avec cette recherche est la compréhension de la diminution de la polarisation spontanée lorsqu'une couche ferroélectrique est déposée sur une hétérostructure semi-conductrice d'épaisseur finie. La maximisation de la polarisation ferroélectrique peut être obtenue en choisissant une couche ferroélectrique à faible constante diélectrique. Le défi actuel est d'obtenir une meilleur compréhension du système, surtout les limitations de la rétention de la polarisation spontanée et de trouvée des moyens pour l'améliorer.

Contents

Nomenclature

Abbreviations

1T/1C	One transistor/one capacitor
2DEG	Two dimensional electron gas
2DHG	Two dimensional hole gas
2T/2C	Two transistor/two capacitor
AC	Alternating current
AES	Auger electron spectroscope
BL	Bit line
CNT	Carbon nanotube
CP	Cell plate line
C-V	Capacitance voltage curve
DC	Direct current
DRAM	Dynamic random access memory
EDS	Electron dispersive spectroscopy
EELS	Electron energy loss spectrometer
EEPROM	Electrically erasable programmable read only memory
FeFET	Ferroelectric field effect transistor
FEG	Focused electron gun
FeRAM	Ferroelectric random access memory
FET	Field Effect Transistor
FFT	Fast fourier transform
FIB	Focused ion beam
HEMT	High electron mobility transistor
MEMS	Micro-electro-mechanical systems

MFIS	Metal ferroelectric insulator semiconductor
MFM	Metal ferroelectric semiconductor
MFSFET	Metal ferroelectric semiconductor field effect transistor
MFS	Metal ferroelectric semiconductor
MIS	Metal insulator semiconductor
MOSFET	Metal oxide semiconductor field effect transistor
MOSHEMT	Metal oxide semiconductor high electron mobility transistor
MPB	Morphotropic phase boundary
NVRAM	Non volatile random access memory
PFM	Piezoresponse force microscope
PSPD	Position sensitive photodetector
P-V	Polarisation voltage curve
QPC	Quantum point contact
RF	Radio frequency
RHEED	Reflection high-energy electron diffraction
RTA	Rapid thermal anneal
SEM	Scanning electron microscope
SFM	Scanning force microscope
SIMS	Secondary ion mass spectroscopy
SPM	Scanning probe microscope
TEM	Transmission electron microscope
TLM	Transmission line method
VLSI	Very large scale integration
WL	Word line
XPS	Xray photoelectron spectroscopy

Processing Techniques

AVD	Atomic vapor deposition
CSD	Chemical solution deposition
ECR-RIE	Electron cyclotron resonance reactive ion etching
HVPE	Hybrid vapor phase epitaxy

LMBE	Laser molecular beam epitaxy
MOCVD	Metal organic chemical vapor deposition
MOVPE	Metal organic vapor phase epitaxy
PAMBE	Plasma assisted molecular beam epitaxy
PIMBE	Plasma induced molecular beam epitaxy
PLD	Pulsed laser deposition
PVD	Physical vapor deposition

Greek Letters

ϵ_o	Permittivity of free space
ϵ_b	Background dielectric constant not including the soft mode
ϵ_d	Dielectric constant of the dielectric layer
ϵ_f	Dielectric constant of the ferroelectric
μ	Electron mobility
σ_{inj}	Injected charge

Roman Letters

B	Magnetic field
C	Curie Constant
C_f	Capacitance of the ferroelectric layer
C_g	Gate capacitance
C_{IS}	Capacitance of the insulator and semiconductor layers
d	Piezoelectric coefficient
d_d	Dielectric layer thickness
d_f	Ferroelectric layer thickness
E_b	Internal bias field
E_c	Coercive electric field
E_{co}	Coercive field of only the ferroelectric layer
E_d	Electric field in the dielectric layer
E_{dp}	Depolarisation field
e	Electron charge
E_f	Electric field in the ferroelectric layer

E_{th}	Threshold electric field above which charge injection occurs
g_m	Transconductance
h	Planck's constant
I_d	Drain current
I_{DS}	Drain source current
I	Current
I_L	Leakage current
L	Length
n_s	Electron sheet concentration
P_b	Background polarisation of a dielectric layer
P_f	Total polarisation in the ferroelectric layer, except the background contribution
P_m	Maximal polarisation
P	Polarisation
P	Total induced polarisation, for PFM measurements.
P_{PE}	Piezoelectric polarisation in GaN and its alloys
P_r	Remanent polarisation
P_s	Spontaneous polarisation in the ferroelectric layer
$P_{s-active}$	Active spontaneous polarisation of a ferroelectric layer, taking into account charge compensation.
$P_{s-layer}$	Spontaneous polarisation of a ferroelectric layer that is in a structure with a finite dielectric layer, taking into account the depolarisation field and if applicable charge compensation.
P_{SP}	Spontaneous polarisation in GaN and its alloys
P_{total}	Total polarisation of a ferroelectric layer including the background contribution
Q_f	Charge compensated at the electrode/ferroelectric interface
Q	Electrostrictive coefficient
q	Electron charge
R_c	Contact resistance
R_s	Sheet Resistance
S	Strain

T_c	Curie temperature
T	Temperature
V_{DS}	Drain source voltage
V_f	Voltage drop across the ferroelectric layer
V_{GS}	Gate source voltage
V_{gt}	Gate voltage
V_H	Hall voltage
V_{IS}	Voltage drop across the insulator/semiconductor layers
W	Width

Chapter 1

Introduction/Concept of Ferroelectric Gate

Ferroelectric materials have a spontaneous polarisation which has the ability to switch with an applied electric field, greater than its coercive field, E_c. Once this electric field is turned off the last "written" polarisation remains as a stable state. In the simplified case the spontaneous polarisation can be considered either positive or negative. This bistable state has been thought of as an obvious way to represent the Boolean Algebra "1" and "0". The next step involved in exploiting this property is to integrate the ferroelectric layer with the existing semiconductor technology, the most common used being MOSFET. However, this has been by far an easy task to reach since the concept was introduced by Looney [1957], Brown [1957], Ross [1957], and Morton [1957]. Many researchers are still trying to optimise material choices and device design in order to find the optimal ferroelectric memory device.

1.1 The Concept

The main goal of this thesis is to implement an operational ferroelectric gate on a semiconductor heterostructure. The addition of a ferroelectric layer onto a semiconductor can be a benefit for the production of non-volatile memory devices with low power consumption. However, the integration of ferroelectrics and semiconductors is not trivial. The problem of choosing a ferroelectric and a semiconductor to constructively prove the concept of ferroelectric field effect transistor presented by Looney [1957], Brown [1957], Ross [1957], and Morton [1957] is still in process by many researchers.

A classical transistor is shown in figure 1.1. What occurs here is that the current allowed to flow from the source to drain is modulated by a gate voltage. In fact the channel is modified when the gate voltage is applied by an external source. Of interest is that once the gate voltage is turned off the channel goes back to its initial state, there is no memory retention of the last written state.

This is exactly the primary reason for switching to ferroelectric based devices, since ferroelectric materials have the capability of retentaining its polarisation direction after an applied electric field is turned off. This characteristic, unique to ferroelectrics, allows for the creation of non-volatile memory devices that have low power consumption. The

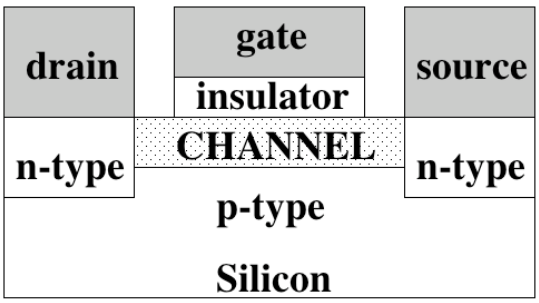


Figure 1.1: A n-channel MOSFET.

ferroelectric layer can be deposited directly onto a semiconductor or be deposited onto a buffer layer in order to avoid diffusion, see figure 1.2 for a cross-section of a device.

The image shown in figure 1.2 illustrates the phenomenon of modulating the channel resistance (the electrons in the channel) through the spontaneous polarisation in the ferroelectric layer. When a negative DC voltage is applied to the ferroelectric layer the spontaneous polarisation should be oriented upwards causing a negative bound charge in the ferroelectric layer at the semiconductor interface. To compensate this negative bound charge the channel in the semiconductor will be depleted of its electrons. Conversely, when a positive DC voltage is applied to the ferroelectric layer the spontaneous polarisation should be oriented downwards causing a positive bound charge in the ferroelectric layer at the semiconductor interface. To compensate this positive bound charge there will be an accumulation of electrons in the channel of the semiconductor.

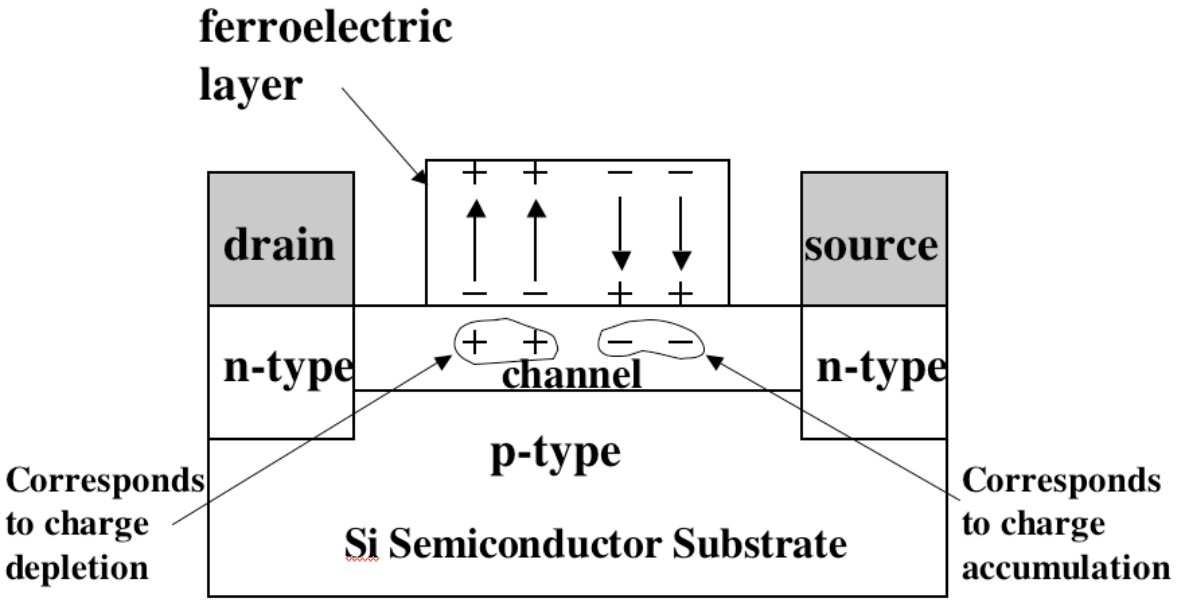


Figure 1.2: An example of the modulation of a semiconductor channels source drain current or channel resistance when it is modulated by poling the ferroelectric layer in either the upwards or downwards direction.

Why ferroelectrics have not been successfully integrated with semiconductors has been addressed by many researchers including Ma and Han [2002]. Who declare that two problems cause poor retention of the ferroelectrics polarisation when it has been deposited onto a semiconductor. The first problem is due to a depolarisation field occurring due

to incomplete charge compensation at the ferroelectric/semiconductor interface which is an increasing problem when the capacitance of the semiconductor layer (that is included in the sandwiched structure) is sufficiently inferior to that of the ferroelectric layer used. The other problem is due to leakage current and charge trapping in the ferroelectric layer due to electron injection at the electrode. However, the biggest challenge to date is that the volatile processing of the perovskite ferroelectric layers lead often to highly diffusive interfaces when being deposited onto semiconductors. This can lead to a severe degradation of the ferroelectric and semiconductor characteristics.

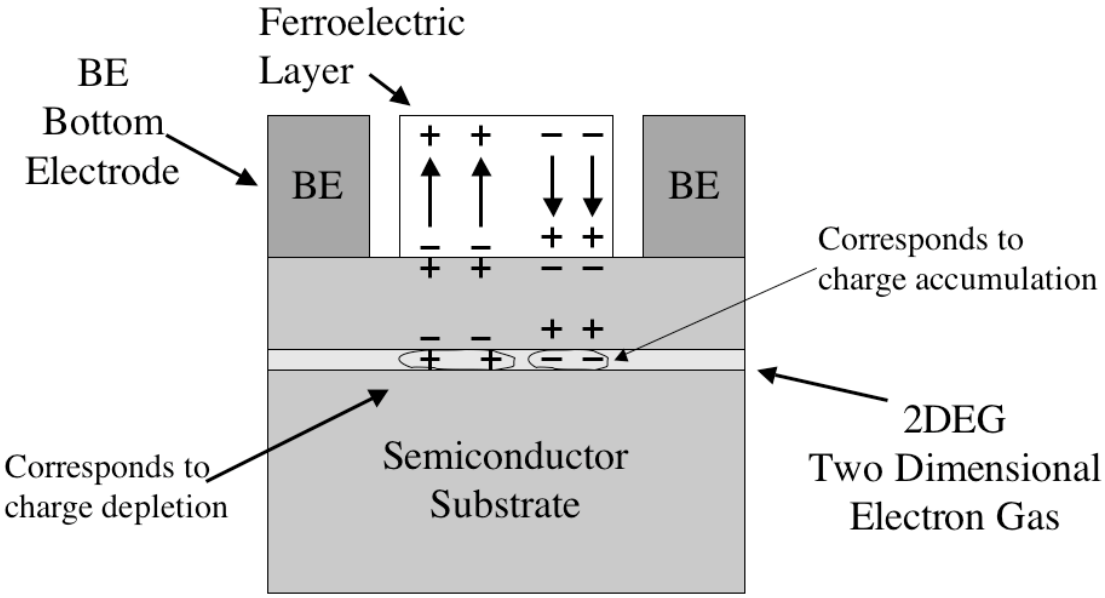


Figure 1.3: An example of the modulation of a semiconductor heterostructures 2DEG when it is modulated by poling the ferroelectric layer in either the upwards or downwards direction.

As mentioned above the problem of integrating the ferroelectric films onto commonly used semiconductors and using the already existing processing technology was not trivial. To prove the concept of ferroelectric field effect transistor it is necessary to investigate a combination of a broader range of ferroelectrics and semiconductors. One possible way of doing this is trying to implement a ferroelectric layer onto a semiconductor heterostructure, that is a semiconductor of multiple layers where the concentration of each semiconductor layer is slightly varied to cause a mismatch of the band-gap at each interface. Semiconductor heterostructures can possess a two dimensional electron gas, 2DEG, that is located at the interface between two of its layers. This 2DEG has transport properties that are superior to single-layered semiconductors, which is beneficial for high frequency devices, low noise devices and quantum transport devices. Figure 1.3 shows an out of scale model of such a structure.

For applied studies the fabrication and measurements of transistor structures is the ultimate way. However, the successful fabrication of a ferroelectric field effect transistors, FeFET, has not been achieved to date so it is of more interest to get a better fundamental understanding of the functioning of ferroelectric/semiconductor devices. Therefore, the approach of this thesis is to study the basic ferroelectric properties of the ferroelectric layer deposited onto a semiconductor. After which, the modulation of the semiconductor channel transport properties with sheet resistance measurements and Hall measurements due to the poling of the ferroelectric layer will be observed. That is to study the change

of sheet resistance R_s, electron sheet concentration n_s and mobility μ as a function of polarisation and the temporarily applied gate voltage. Two configurations were tested one had the ferroelectric layer directly deposited onto a semiconductor and the other used an intermediate buffer layer between the ferroelectric and semiconductor layer.

1.2 Material Integration

To successfully come to such a device important choices need to be made regarding the semiconductor and ferroelectric materials chosen. One of the principal requirements is that the ferroelectric layer is deposited on top of a semiconductor while maintaining the transport properties of the semiconductors channel and the switching, as well as retention, characteristics of the ferroelectric layer. However, one can also decide the converse that the semiconductor needs to be chosen in order to sustain the deposition process of the ferroelectric layer.

Choosing the ferroelectric layer first and choosing the semiconducting heterostructure first were considered because as often is found when fabricating devices multiple parameters need to be optimised in order to fabricate high performance devices. There were multiple reasons to choose the AlGaN/GaN heterostructure. The AlGaN/GaN heterostructure was decided to be the most optimal heterostructure available since at its interface a 2DEG exists which has high mobility, sheet concentration and low sheet resistance. Most importantly, the GaN structure exhibits temperature and chemical stability which will allow it to survive the high temperature, volatile processing of the ferroelectric layer. More details about the properties and the choice of this semiconductor heterostructure will be described in section 4.1.1.

The ferroelectric layer was a variable in this thesis. PZT, lead zirconium titanate, was deposited using both chemical solution deposition, CSD, and multiple target sputtering and P(VDF/TrFE), an organic polymer was deposited with a spin casting technique. It was thought that because the processing temperature of PZT is below 600 °C, for both sputtering and sol gel, that this was not hot enough to induce/invoke diffusion into the temperature stable AlGaN. Also the large polarisation of PZT should be able to build up enough bound charge to modulate the electrons in the channel, which in the case of a heterostructure is the 2DEG. The organic, lead-free, ferroelectric polymer poly(vinylidene fluoride/trifluoroethylene), P(VDF/TrFE), was also tested as it has a crystallisation temperature of 130 °C which should allow for a less volatile deposition onto a semiconductor substrate. However, this advantage of low deposition temperature could also be a disadvantage due to the limitations of the device functionality and limit any high temperature processing techniques. Further details on the ferroelectric materials will be described later on; PZT properties and characteristics in section 4.1.2 and P(VDF/TrFE) in section 4.1.2.

1.3 Applications

The use of a combination of AlGaN and PZT could lead to high frequency, high temperature, and high power devices. These devices would have high mechanical, chemical and thermal stability. Changing the PZT layer to P(VDF/TrFE) results only in the loss

of the high temperature performance since P(VDF/TrFE) has a melting temperature of 150 °C.

These devices have first and foremost possibilities for use as memory storage devices, since the ferroelectric layer retains its polarisation after the bias voltage is turned off. Currently ferroelectrics are used in electronics as non-volatile random access memory, NVRAM, called ferroelectric random access memory, FeRAM. One of the main disadvantages of the current commercially available NVRAM/FeRAM is that the readout is destructive. Each time a memory cell is read it looses the value written and must be re-written. It is important to use the polarisation retention characteristic to its utmost and obtain a ferroelectric memory device with non-destructive readout. To do such the research of the fabrication of ferroelectric field effect transistors, FeFET, is of interest since not only does this structure allow for the non-destructive readout but also allows for the densification of circuitry and high access times.

The applications are not exclusively for memory devices but have also the potential to be extended to low-dimensional semiconductor nano-structuring by scanning force microscopy, SFM, and ferroelectric lithography techniques.

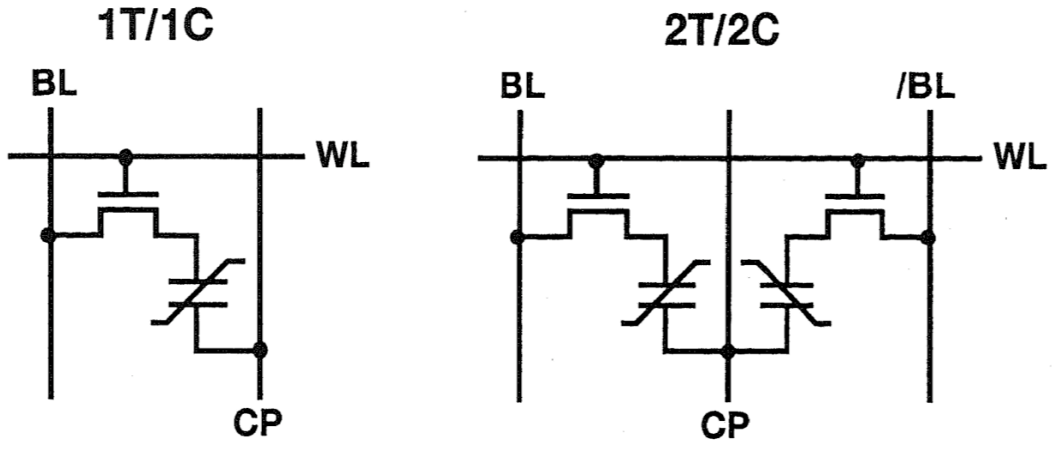
1.3.1 Non-Volatile Ferroelectric Memory

Non-volatile random access memory, NVRAM, is any random access memory where the memory is stored in a way that it can be accessed at random and does not loose the information stored when there is no power. The basics of ferroelectric memories is well summarised by Auciello et al. [1998] and Scott [2000], describing the details of the non-volatile process of switching the memory state. In brief there are two main types of ferroelectric NVRAM, which differ in the reading mechanism being either resistive or charge based memories. Resistive based NVRAM is considered to be Ferroelectric Field Effect Transistor, FeFET, and has a non-destructive readout, where the bit line, BL, is charged via the resistor. Charge based NVRAM is considered to be Ferroelectric Random Access Memory, FeRAM, and has a destructive readout, a charged capacitor is sensed, where the memory cell must be rewritten after reading. Therefore, for the obvious reason of preferring non-destructive readout and densification of the circuitry the FeFET NVRAM configuration is the most ideal.

Two techniques of NVRAM that are competing with FeRAM are Flash and EEPROM, both of which have good integration possibilities, Kohlstedt et al. [2005]. The existing problems with Flash and EEPROM memories such as large programming times, large voltages and limited endurance keep ferroelectric based NVRAM as a running contender for this market.

FeRAM Design

Ferroelectric Random Access Memory, FeRAM, is a charge based NVRAM and has a destructive readout where a charged capacitor is sensed. This technology is already currently in use with embedded memory. FeRAM needs to work with the current transistor technology commercially available and have its circuit design optimised. Two possible circuit configurations are shown in figure 1.4, the 1 Transistor/1 Capacitor (1T/1C) and 2 Transistor/2 Capacitor (2T/2C) configurations.



(a) (b)

Figure 1.4: The schematic diagram of a) one transistor/one capacitor and b) 2 transistors/2 capacitors circuitry, Sumi et al. [1995].

In the 1T/1C configuration a "zero" is written when the cell plate line, CP, is shifted from 0 to a positive DC bias, +VDD, and a "one" is written when the CP is shifted from 0 to -VDD. The bit line, BL, is grounded and a pulse is sent through the word line, WL, to activate the transistor. Sense amplifiers are necessary to sense difference between the "zero" and "one" imprinted values, see Kohlstedt et al. [2005].

To reduce the error in reading the memory a better configuration would be the 2 Capacitor/2 Transistor (2T/2C) configuration where two capacitors have opposite polarisations memorised. A first capacitor is used as a reference and is located directly besides the addressed capacitor and is accessed an equivalent amount of times. Therefore, the referenced capacitor cell fatigues at the same rate as the addressed cell so that the sense amplifier always returns a zero. This is the essential advantage over the 1T/1C configuration that has only one reference cell for the whole memory unit. Hence the reference capacitor fatigues faster and the sense amplifier does not return a zero but a small fraction. This small fraction can lead to errors in reading the memory cells. Although this is a benefit in using the 2T/2C configuration it does not always outweigh the fact that memory cells will have to be twice the size.

Other configurations do exist and are being developed for FeRAM but will not be discussed here as it is not in the scope of this section.

The company Fujitsu currently produce 1 Mbit NVRAM/FeRAM and are researching to create higher density memory chips. Those created by Fujitsu are currently in use in the Sony Playstation3. Fujitsu and the Tokyo Institute of Technology are working on the development of Bismuth Ferrite ($BiFeO_3$ or BFO) for the use in 256 Mbit FeRAM using the 65 nm technology, which will be available in 2009. The switch from the commonly used lead zirconium titanate, PZT, to BFO is an important one since the integration limit of PZT is at the 130 nm node. Not only will BFO be functional at the 65 nm node but it has lower leakage current, and higher polarisation than PZT. Fujitsu will also try to switch towards using the 1T/1C structure for increased circuit densification. Other groups such as Texas Instruments and Ramtron have 512 kbit memories on the market but have produced 4 Mbit memory devices that will soon become commercially available.

FeFET Design

One of the most important advantages of FeFET design is that it allows for the larger densification of circuitry. Using the same notation as above in section 1.3.1 the FeFET can be thought of as a 1 Transistor (1T) cell. This 1T cell is a MOSFET (or other conventional transistor) with a ferroelectric gate dielectric. The benefit of having a reading operation which is nondestructive is negated by the principal challenge for FeFETs, that is insufficient retention. FeFETs also benefit from characteristics such as random access, high speed, low power, high density and non-volatility. The main reason for all of these benefits is that ideally the ferroelectric layer is deposited directly onto the semiconductor, or if necessary with an additional super-thin insulating layer or buffer layer, see figure 1.2. This is what allows for the densification of circuitry and random access as there does not need to be any checking of the reference capacitor with the memory capacitor, such as in the 1T/1C and 2T/2C configuration of FeRAMs. The ferroelectric material can bring with it the two benefits of non-volatility and low power consumption when the processing of the ferroelectric layer is fully optimised on the semiconductor layer.

However, these benefits that can be achieved in obtaining a successful FeFET are only possible after the optimsation of the deposition of ferroelectric layers on semiconductor devices. Already many researchers have tried solving this problem by using a buffer layer without making the task less trivial, Sugibuchi et al. [1975] and Kijima et al. [2001]. Practically this concept leads to the problem of poor retention of the spontaneous polarisation in the ferroelectric gate of the FeFET which is the biggest challenge to date. The details of the problems in implementing FeFET will be presented in more detail in section 2.2 and elaborated upon in the results sections of this thesis. Currently, there are no commercially available FeFET on the market.

1.3.2 Low-Dimensional Semiconductor Nano-Structuring by SFM

Although not dealt with directly during this thesis one must keep in mind the broader picture and the future potential of ferroelectric gated semiconducting devices. Described here is a technique that can potentially lead to the creation of nanostructures using techniques from the scanning probe microscope, SPM, family.

Starting from the nineties a new group of methods for semiconductor nanostructure fabrication by SPM has been developed, by Snow and Campbell [1994]. The SPM techniques presents a number of essential differences compared to all previous techniques. The techniques based on direct SPM writing allow for a single-step process of nanostructure formation with a pattern resolution that is potentially higher than the traditional lithographic process. Snow and Campbell [1994], Matsumoto et al. [1996], and Held et al. [1997] demonstrated the local anodic oxidation of the cap layer in the $GaAs/Al_xGa_{1-x}As$ heterostructure with a 2DEG located tens of nm to the surface with typical writing feature size of 100 nm using SPM techniques. The potential of this method for the fabrication of different semiconductor nanostructures including quantum dots, wires and rings has been demonstrated by Held et al. [1997], Luscher et al. [1999], and Fuhrer et al. [2001].

Ferroelectric lithography

The SPM methods for nanostructure formation possess several essential advantages compared to other techniques. These advantages include the potential of high resolution patterning, the ability to selectively address each individual structural feature and a flexibility of nanostructure design by being capable of drawing any arbitrary-shaped lines with the precise positioning of each feature. A scanning force microscopy, SFM, method is proposed here in which the polarisation domain pattern, controlled by the local application of voltage to the ferroelectric film, is projected onto the 2DEG. This proposed technique offers a possibility for the nondestructive modification or even complete change of a nanostructure pattern with a possibility of high ($< 50\,\text{nm}$) resolution, Paruch et al. [2001]. The key element that could make ferroelectric lithography possible is the integration of a ferroelectric layer with a semiconducting heterostructure and observing the effect of local depletion in the 2DEG due to the poling of the ferroelectric gate. The other interesting feature of this technique is that the ferroelectric gate is normally transparent to visible light, which can facilitate optical experiments.

1.4 Outlook

The main goal of this thesis is to implement an operational ferroelectric gate on the AlGaN/GaN semiconductor heterostructure, using PZT and P(VDF/TrFE) as the ferroelectric material. One of the ways to do such is to show the modulation of the sheet resistance of a channel located in a semiconductor through the bi-stable spontaneous polarisation in a ferroelectric layer. Within the scope of this thesis the intermediate goals that are attempted to be successfully accomplished are listed below:

1. Deposit a ferroelectric layer onto the AlGaN heterostucture without destroying/-degrading the 2DEG.
2. Observe ferroelectricity in the ferroelectric layer by multiple measurement techniques.
3. Pole the ferroelectric layer and observe its polarisation and retention.
4. Pole the ferroelectric layer and measure a change of transport properties of the 2DEG.

The first goal that needs to be accomplished is successfully depositing the ferroelectric layer onto the AlGaN heterostructure. The success of this is characterised by comparing the initial transport properties such as sheet resistance of the 2DEG to these same values after the deposition of the ferroelectric layer. It is possible that a slight degradation of the 2DEGs transport properties can be tolerated, to observe the effect of depletion. Secondly, it is necessary to observe that this ferroelectric layer is indeed switchable with good retention characteristics. Measurements such as C-V curves, and piezoresponse force microscopy, PFM, measurements will be utilised in order to assess whether or not the spontaneous polarisation in this ferroelectric layer can be reversed under voltage and retain its polarisation. Which leads to the third goal, that is to observe the retention of the switched polarisation in the ferroelectric layer. The last and ultimate goal is to

permanently modify the electrons in the 2DEG when poling the ferroelectric layer. That is when the ferroelectric layer is poled with a negative DC gate bias the 2DEG is depleted of electrons and when a positive DC gate bias is applied the 2DEG has an accumulation of electrons.

Chapter 2

State of Art

2.1 Ferroelectrics as Gate Materials

Attempting to implement the concept of ferroelectric gate in field effect transistors has been the goal of many researchers since its introduction by Looney [1957], Brown [1957], Ross [1957], and Morton [1957]. The ferroelectric field-effect transistors, FeFET, have architecture similar to standard FETs but their gates are comprised of a ferroelectric layer that can be poled positively or negatively provoking charge accumulation or depletion, respectively in the transistor channel. One of the major problems of commercialisation of such devices is the integration issue since the high processing temperatures of the ferroelectric perovskite materials are rarely compatible with the standard silicon technology. This makes the selection of materials used of utmost importance.

Six years after the introduction of FeFETs the first successful experiments were performed by Moll and Tarui [1963], in order to implement a solid state variable resistor. A thin triglycine sulfate, TGS, layer was deposited between a gold base electrode and a thin film transistor. The thin film transistor consisted of two counter electrodes covered with a cadmium sulfide, CdS, layer and a silicon monoxide layer with an aluminum electrode on the top. Measured was a change in source drain resistance of 60 kΩ, a stable change of this resistance by a factor 1.25 after poling with $\pm$90 V was observed. Although this is far from the low power memory device described as an advantage for the FeFET in section 1.3.1, it was a step forward towards such a device.

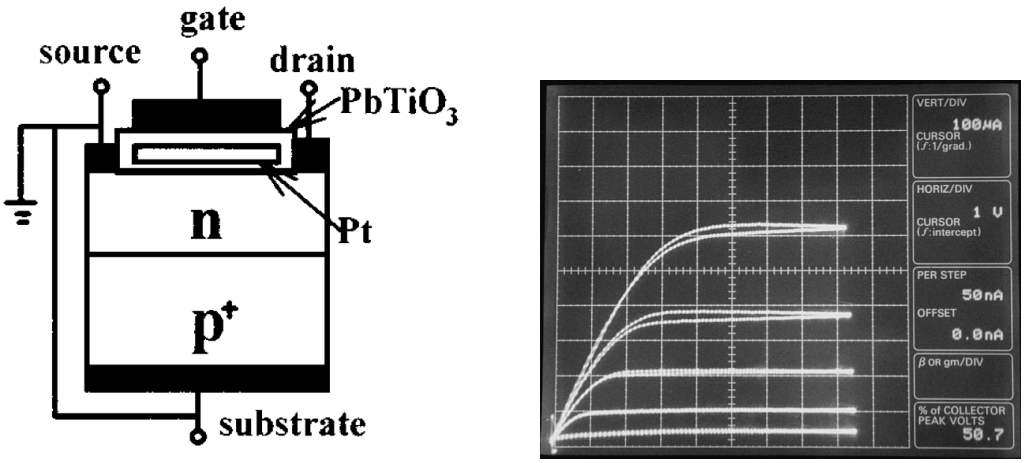
2.1.1 Ferroelectric Gate on Silicon

Some of the first attempts of integrating ferroelectrics and semiconductors to create a metal-ferroelectric-semiconductor, MFS, device were done on the silicon semiconductor. Semiconductors such as silicon were preferred since the processing of silicon based devices was already highly developed.

A ferroelectric layer was deposited onto the silicon in-order to modulate the semiconductors channel properties with the polarisation of the ferroelectric layer. Unfortunately, many problems occurred primarily due to a degradation in the properties due to a diffusive interface between the ferroelectric and the silicon substrate. These samples exhibited poor switching behavior, poor current-voltage curves, large leakage currents and large dif-

fusive interfaces. Some successful attempts at implementing ferroelectric gates on silicon have been achieved by Sugibuchi et al. [1975], Chen et al. [1996] and Kijima et al. [2001], but are far from ideal and need much more optimisation.

Sugibuchi et al. [1975] attempted to fabricate a ferroelectric field effect memory device with bismuth titanate, $Bi_4Ti_3O_{12}$ deposited by RF diode sputtering onto a Si substrate. The 1 μm thick $Bi_4Ti_3O_{12}$ was annealed in air at a temperature of 650 °C for 30 min and had a remanent polarisation of 4 $\mu C/cm^2$. After a few attempts a 50 nm SiO_2 buffer layer was used in order to minimise the charge injection between the ferroelectric and semiconductor layers. Unfortunately, this SiO_2 buffer layer degraded the memory retention of the devices. Switching voltages of ±15 V were used to significantly modulate the drain current of the Si transistor and showed little fatigue with 10^5 write and erase cycles. In order to stably modulate the channel resistance of a semiconductor it was claimed to be a necesssity to use a ferroelectric with a coercive field greater than the depolarisation field.



(a) (b)

Figure 2.1: a) The floating gate $PbTiO_3$/Si structure of the device used. b) The drain source current vs drain source voltage curves measured after applying the gate voltage. Images are taken from Chen et al. [1996].

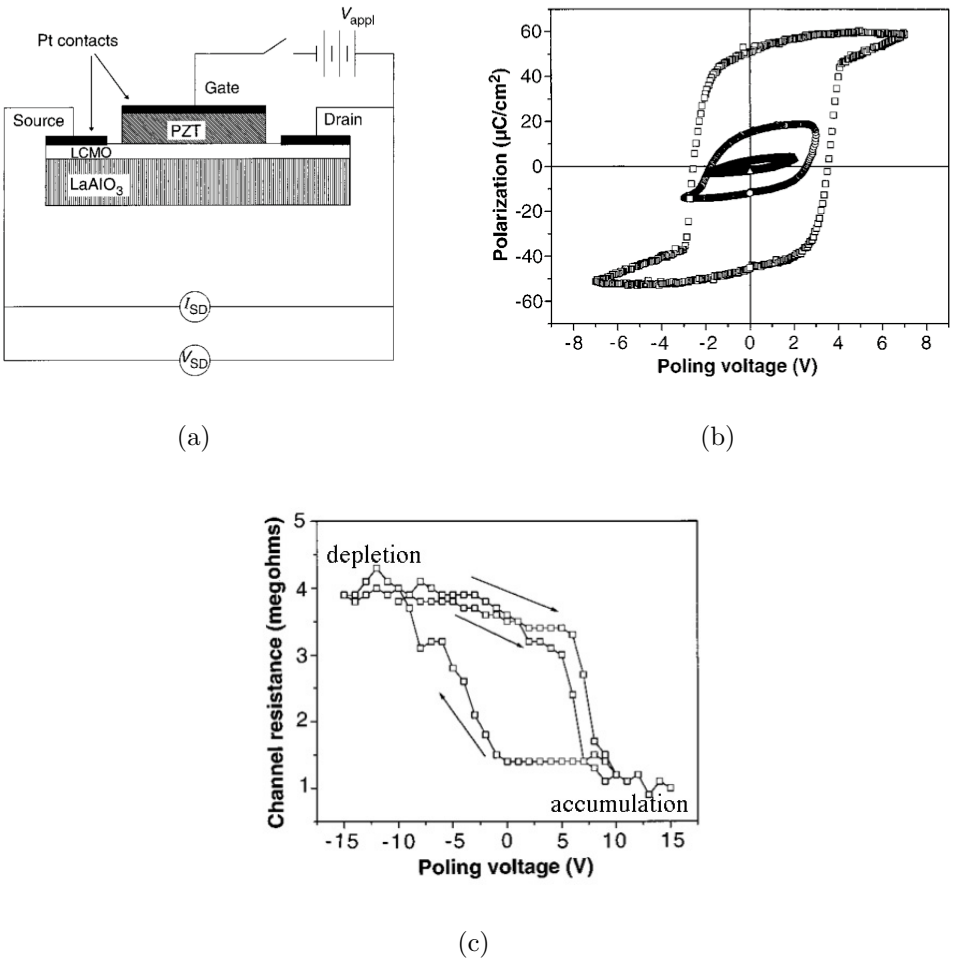
The concept of ferroelectric gate was once more implemented in field effect transistors in the nineteen nineties by Chen et al. [1996]. Where $PbTiO_3$ was used as the ferroelectric floating gate on a n/p^+ doped Si transistor, to control the conductivity in the n-doped layer. To more thoroughly describe this concept of floating gate one can observe in figure 2.1 that on top of the doped silicon a 5 nm layer of lead titanate was deposited, after which the Pt electrode was deposited and then $PbTiO_3$ of 50 nm was deposited finishing with a Au gate electrode. These devices show potential for very large scale integration, VLSI, low voltage ±10 V and fast access time < 160 ns.

Kijima et al. [2001] demonstrated ferroelectric properties of a $Bi_{3.25}La_{0.75}Ti_3O_{12}$, BLT, thin film deposited onto p-type and n-type silicon with a 3 nm thick Si_3N_4 buffer layer. The Si_3N_4 buffer layer was used in an attempt to minimise the diffusion occurring at the ferroelectric/semiconductor interface which severely degraded the ferroelectric and semiconductor performance. Therefore, they switched from the conventional idea of metal ferroelectric semiconductor, MFS, devices and attempted to implement a metal ferroelectric insulator semiconductor, MFIS, device. With capacitive device structures using platinum top electrodes hysteretic capacitance-voltage curves with nearly 100 % retention

were observed on both n-type and p-type silicon substrates, when measured over 3 days.

2.1.2 PZT as Gate Material

A natural selection for the ferroelectric gate material is PZT because of its high remanent polarisation and low coercive field. Unfortunately, the relatively low temperature of crystallisation of perovskite PZT is approximately above 570 °C, making the selection of the semiconductor extremely important to limit diffusion. Therefore, it can be necessary to deviate from the use of the silicon semiconductor to one that has a relatively high breakdown field, good chemical, mechanical and thermal stability while still having good transport properties such as high electron mobility and electron sheet concentration. With this concept in mind Mathews et al. [1997] implemented PZT (20:80) as the ferroelectric gate onto the semiconductor structure of $La_{0.7}Ca_{0.3}MnO_3$, LCMO. They measured a change in the channel conductance of a factor 3 due to the applied gate voltage. Although long retention measurements after poling the PZT were not performed, a retention loss of 3 % after 45 min was measured.



(a) (b)

(c)

Figure 2.2: a) The structure/cross section of the device used for demonstrating the concept of ferroelectric gate, b) polarisation vs poling voltage for different final poling voltages and c) the modulation of the channel resistance of the LCMO semiconductor by the poling voltage of the PZT layer, Mathews et al. [1997].

2.1.3 PZT on GaN and AlGaN Heterostructures

Li et al. [1999] first attempted to use $Pb(Zr_{0.53}Ti_{0.47})O_3$ as a ferroelectric gate material on GaN as a MFS structure instead of the conventional metal-insulator-semiconductor, MIS, structures for the development of metal-ferroelectric-semiconductor field effect transistors, MFSFET. The reason for choosing GaN instead of the traditional Si semiconductor was due to the high chemical and temperature stability of the GaN and its high breakdown voltage. Later on Shen et al. [2002] switched to AlGaN heterostructures due to the fact that at the AlGaN/GaN interface is a 2DEG which has high mobility, electron concentration and low sheet resistance. The above mentioned characteristics make them ideal for high frequency, power and temperature devices. A 400 nm layer of PZT was deposited on the AlGaN/GaN heterostructure and an aluminium contact was used to polarise the PZT film inducing depletion of the 2DEG. A simple C-V technique was used to estimate the electron sheet concentration derived from the basic equation Q=CV, equation 2.1. Where q is the electron charge, C_g is the gate capacitance and V_{gt} is the gate switching voltage. This approximation for the electron sheet concentration in the 2DEG gives an indication of the possibility of local depletion due to the direction of the PZTs polarisation. The C-V curve was measured using a bridge technique described further in section 3.4.2. They demonstrated, using high frequency capacitance voltage measurements at room temperature, the depletion of electron concentration from $1.56\text{x}10^{13}\,\text{cm}^{-2}$ to $5.6\text{x}10^{12}\,\text{cm}^{-2}$ (that is a factor of 2.78) in an n-doped AlGaN/GaN heterostructure with a 2DEG located 78 nm from the PZT interface.

$$n_s = \frac{C_g V_{gt}}{Aq} \tag{2.1}$$

2.2 Existing Problems in Implementing Ferroelectrics

Ma and Han [2002] give one of the most comprehensive papers posing questions about why there are no ferroelectric field effect transistor memory devices already on the market. The main problem limiting the coming to market of ferroeletric transistors is the poor retention time of the written polarisation state, this being far from the required 10 years necessary for a reliable memory device. Instead retention of the written polarisation state and hence the modulation of the channels current has only been shown to be stable for multiple days, Kijima et al. [2001] and Mathews et al. [1997]. Preliminary experiments and research by Wurfel and Batra [1973] stated that the bistability of the spontaneous polarisation in the ferroelectric layer no longer exists in metal ferroelectric semiconductor, MFS, structures.

Below are listed some of the mechanisms that can possibly hinder the operation of a ferroelectric transistor device. The depolarisation field will be studied in depth using the passive dielectric layer model. After which, reducing and increasing this depolarisation field due to charge compensation, charge injection and trapping at the ferroeletric/electrode interface will be discussed. A retention time for the MFS structure will be estimated and a MFIS structure introduced as being the solution for decreasing diffusion at the interface, among other advantages. Finally, the mechanisms behind polarisation fatigue will be briefly mentioned. Although this is beyond the scope of what it is to be studied, these mechanisms are possible failure mechanisms to study for the future.

2.2.1 Depolarisation Field

The depolarisation field is an electric field that opposes the direction of polarisation and is particularly present in thin films. This phenomenon causes the poled state in the ferroelectric film to become unstable. The depolarisation field existing in thin ferroelectric films can be explained by using a layer of low dielectric constant in series with the ferroelectric layer that causes a strong depolarising electric field. Alternatively, it is also possible to think of the depolarisation field existing due to incomplete charge compensation at the ferroelectric/electrode interface which gives rise to a passive dielectric layer. This low dielectric constant layer can be considered as any layer with a dielectric constant inferior to that of the ferroelectric layer. The depolarisation effect also exists in MFS structures where the semiconductor layer can possibly enhance the already existing depolarisation field. The depolarisation field is affected by both the thickness of the ferroelectric film, or layers deposited, and the dielectric constants of the layers deposited. The depolarising field can be minimised by using a thicker ferroelectric film in the MFM structure. For the MFS structure minimising the thickness of the intermediate/semiconductor layer and matching the dielectric constant of the ferroelectric to that of the semiconductor, or vice versa can decrease this depolarisation field.

Passive Dielectric Layer

The depolarisation field can be conceptually viewed using a passive dielectric layer model. The depolarising field existing due to a passive dielectric layer existing in the thin ferroelectric film is described in more detail by Tagantsev et al. [1995]. A ferroelectric film is thought to be divided into two layers, a ferroelectric layer and an ultra thin passive layer, which has become so due to incomplete compensation of the spontaneous polarisation at the ferroelectric/electrode interface. This passive layer can be considered either as a second non-ferroelectric phase at the electrode or a near by electrode layer where the ferroelectric polarisation changes in the layer with distance from the electrode. Recently, the origin of this passive dielectric layer was investigated by Stengel and Spaldin [2006]. They calculated that the decrease in capacitance is an intrinsic property of a metal/insulator interface and not a result of processing issues.

The ultra thin passive layer has a low dielectric constant, and exists when no electric field is being applied to this capacitor, see figure 2.3. Equation 2.2 represents the electric field seen by the whole ferroelectric film, E, by two separate components the electric field in the ferroelectric layer, E_f, and the electric field in the passive dielectric layer, E_d. Where d_d is the thickness of the dielectric layer and d_f that of the ferroelectric layer.

$$(d_f + d_d)E = d_f E_f + d_d E_d \tag{2.2}$$

The depolarisation field in the ferroelectric layer, is determined by E_{dp}=E_f, when there is no applied electric field, equation 2.2 then becomes equation 2.3.

$$0 = E_f + \frac{d_d}{d_f} E_d \tag{2.3}$$

When there is no DC bias applied to the ferroelectric capacitor the electric field in the dielectric is approximately equal to the total polarisation in the ferroelectric layer, P_f,

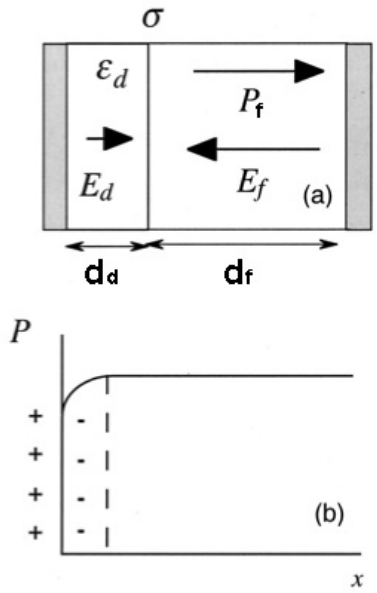


Figure 2.3: Model of the ferroelectric capacitor with a depolarisation field (or a passive dielectric layer). b) Polarisation distribution in this ferroelectric/dielectric capacitor. Image taken from Tagantsev and Stolichnov [1999].

divided by the dielectric constant of the dielectric layer, ϵ_d, and the permittivity of free space, ϵ_o, equation 2.4. This can be derived for when there is no electric field applied across the structure and using the continuity equation at the passive layer/ferroelectric interface. This continuity equation states that the dielectric displacement of the passive layer should equal that of the ferroelectric layer, D_d=D_f. Knowing that the spontaneous polarisation in the ferroelectric film equals the dielectric displacement in the ferroelectric film, P_s=D_f=D_d, when there is no applied electric field across the structure. It is then possible using D_d=$\epsilon_o\epsilon_d E_d$ to derive equation 2.4.

$$E_d \approx \frac{P_s}{\epsilon_o \epsilon_d} \tag{2.4}$$

Substituting equation 2.4 into equation 2.3 it is possible to estimate the depolarisation field in the ferroelectric layer using equation 2.5. When there is no electric field applied across the structure, E=0, then the ferroelectric polarisation is equal to the spontaneous polarisation in the ferroelectric layer, P_f=P_s.

$$E_{dp} = E_f = -\frac{d_d}{d_f}\frac{P_s}{\epsilon_o \epsilon_d} \tag{2.5}$$

Incomplete Charge Compensation at the Electrode

Batra and Silverman [1972] investigated the effects of the depolarisation effect/field in thin ferroelectric films. Wurfel and Batra [1973] state that when the charge in the electrode is not completely compensated the polarisation is accompanied by an electric field, a depolarisation field. This incomplete charge compensation is very important since it decreases the Curie temperature and decreases the total spontaneous polarisation of the

ferroelectric layer. The sample used to confirm this phenomenon was a doped silicon electrode with a triglycine sulphate, TGS, ferroelectric thin film and a gold top electrode. Due to the asymmetry of these electrodes the depolarisation field cannot be eliminated by domain formation. One of their most important observations was that as the thickness of the ferroelectric film decreases, an increase occurred in the depolarisation field.

It is possible to estimate the depolarisation field for a ferroelectric with remanent polarisation $20\,{}^{\mu C}/_{cm^2}$, a dielectric constant of the dielectric layer ϵ_d=10, thickness of the dielectric layer 10 nm and the thickness of the ferroelectric layer 100 nm to be $2.26\,{}^{MV}/_{cm}$, using equations 2.2 and 2.3. This depolarisation is so huge that it does not seem realistic and it is possible to assume that there is charge compensation that allows for stability in the system. For thick ferroelectric films this charge compensation of the depolarisation field is 100 %. Depolarisation fields existing due to incomplete charge compensation will also have a lower phase transition temperature than in thick films. Batra and Silverman [1972] developed the theory to calculate the spontaneous polarsation in a ferroelectric film with and without the depolarisation field, starting from the Ginzburg-Landau, GL, thermodynamic theory, see appendix B. The model is based on the ferroelectric/electrode geometry shown in figure 2.4. The equation of free energy for this model gives equation 2.6.

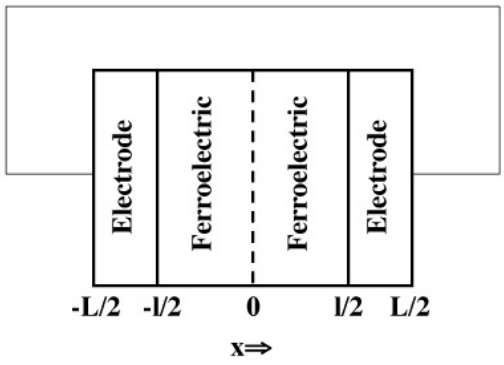


Figure 2.4: Model of the short circuited ferroelectric/electrode geometry used in the model by Batra and Silverman [1972]

$$F(P,T) = F(0,T) + \frac{2\pi}{C}(T - T_c)P_{total}^2 + \frac{1}{4}\zeta P_{total}^4 \tag{2.6}$$

When there is no applied electric field, P_{total}=P_s and the electric field in the ferroelectric layer, E_f, can be easily solved to equation 2.7 by taking the first derivative of equation 2.6 with respect to the polarisation, P_{total}. The main result coming from this is that if there is incomplete charge compensation a reduction of the spontaneous polarisation in the ferroelectric layer, P_s, occurs which is due to a shift in the Curie temperature, T_c. C is the Curie constant, ζ a positive constant and F(0,T) the free energy independent of the polarisation.

$$E_f = \frac{4\pi}{C}(T - T_c)P_s + \zeta P_s^3 \tag{2.7}$$

In the case where there is no depolarisation field, $E_f = 0$, there is 100 % charge compen-

sation and the spontaneous polarisation is calculated to be, equation 2.8.

$$P_s(T) = \sqrt{\frac{4\pi}{C\zeta}(T_c - T)} \tag{2.8}$$

In the case that there is incomplete charge compensation and a depolarisation field exists in the ferroelectric film the spontaneous polarisation was calculated to be equation 2.10. Where, l is the thickness of the ferroelectric layer as is visible from the figure 2.4. T_c^* is the new Curie temperature due to the incomplete charge compensation where $\theta(\lambda, l)$ is a convoluted equation of the screening length, ferroelectric and electrode thicknesses and the electrodes dielectric constant.

$$T_c^* = T_c - C(1 - \theta(\lambda, l)) \tag{2.9}$$

$$P_s(T) = \sqrt{\frac{4\pi}{C}(T_c^* - T)} \tag{2.10}$$

It is possible to see that when θ=1, there is no depolarisation field since $T_c^* = T_c$ and P_f is equivalent in equation 2.8 and 2.10. Equation 2.9 explains that when there is incomplete charge compensation there is a shift in the Curie temperature. The main resultant from this decrease in Curie temperature is the reduction of the spontaneous polarisation which can be especially a disadvantage for ferroelectrics with small remanent polarisations. Although 100% charge compensation is beneficial for MFM structures this might not be the case for the MFS and MFIS structures.

Depolarisation Field due to a Semiconductor Layer

Now that the ferroelectric layer is put onto a semiconductor a question arises: to what impact will the semiconductor affect the ferroelectric layer? Specifically, if the dielectric constant of the semiconductor is substantially lower than that of the ferroelectric layer will there be a large depolarisation field?

An attempt in making a model of this uncompensated charge at the ferroelectric interfaces was presented by Ma and Han [2002]. In assuming a metal ferroelectric insulator semiconductor structure, MFISFET, one can try to estimate the depolarisation field due to incomplete charge compensation when the ferroelectric layer is not sandwiched in-between two identical metallic layers, Ma and Han [2002]. See the schematic diagram, in figure 2.5, where the ferroelectric layer is represented as one capacitor with a certain spontaneous ferroelectric polarisation, P_s, and an amount of charge compensated at the electrodes, Q_f, with a total capacitance, C_f. The hard ferroelectric assumption has been used. The insulator/semiconductor layers are considered together and represent a capacitor, C_{IS}.

These insulating/semiconducting layers actually play exactly the same role as the passive dielectric layer presented above. The only difference is that the thickness of these layers is much thicker than the passive dielectric layer. The theory that is presented below can also be thought of for the passive dielectric layer where all values would be replaced for that of the passive dielectric layer when analysing a MFS structure.

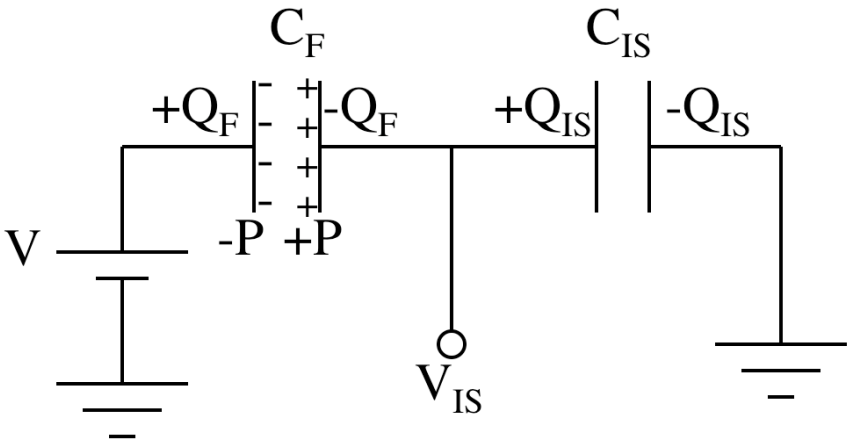


Figure 2.5: A schematic capacitive design of the Metal Ferroelectric Insulator Semiconductor, MFIS, sandwich, Ma and Han [2002].

The voltage drop across the ferroelectric is represented in two terms: one due to its capacitance and the voltage applied across it, V_f, and another due to its internal spontaneous polarisation. That is equation 2.11 and 2.12 have helped to derive equation 2.13 for details of the total voltage applied as a function of the insulator/semiconductor capacitance, C_{IS}, the ferroelectric capacitance, C_f and the spontaneous ferroelectric polarisation, P_s. Note that the equations listed below (2.11-2.15) only hold true when the denoted capacitance is taken as the capacitance per unit area.

$$C_{IS}V_{IS} = P_sA + C_fV_f \tag{2.11}$$

$$V = V_{IS} + V_f \tag{2.12}$$

$$V_f = \frac{C_{IS}V - P_sA}{(C_{IS} + C_f)} \tag{2.13}$$

When the applied field is turned off V =0 V and using Q = CV it is possible to simplify to equation 2.14.

$$Q_f = \frac{P_sAC_{IS}}{C_{IS} + C_f} \tag{2.14}$$

The final depolarisation electric field can then be represented by equation 2.15. This suggests that in order to have a small depolarisation field the ratio of C_{IS}/C_f needs to be maximised. Since the capacitance is directly proportional to the dielectric constant, and inversely proportional to the film thickness there are two parameters that can be varied in-order to control the depolarisation field. In the case of a thick insulating/semiconducting film in comparison to the ferroelectric film there would be a large depolarisation field. However, when the ferroelectric film is much thicker than the insulating/semiconducting film there would be little or no depolarisation field. If the dielectric constant of the

ferroelectric layer is smaller than the insulating/semiconducting layer there is little depolarisation field. So when the dielectric constant of the ferroelectric layer is greater than the insulating/semiconducting layer the depolarisation field must be considered.

$$E_{dp} = \frac{P_s A C_f}{[\epsilon_o \epsilon_f (C_{IS} + C_f)]} = \frac{P_s A}{[\epsilon_o \epsilon_f (\frac{C_{IS}}{C_f} + 1)]} \tag{2.15}$$

Most importantly is that in comparing equation 2.15 to equation 2.3 one can calculate that the two equations derived for depolarisation field are equivalent. Setting the dielectric displacement of the ferroelectric equal to that of the dielectric and substituting in equation 2.3 and the basic equation for capacitance it is possible to write equation 2.15. It can be assumed that the dielectric layer in the passive dielectric layer model is similar to the insulatior/semiconductor, IS, layer.

2.2.2 Charge Injection and Trapping

Electron injection from both the metallic gate and the semiconductor layer can give rise to the trapping of charges in the ferroelectric layer which creates charge compensation. Larsen et al. [1994] introduced the concept of having an additional layer in series electrically with the ferroelectric layer called the blocking layer. Due to the observation made in capacitance measurements which showed an increase in capacitance when the PZT capacitors were annealed in oxygen, that were independent of the PZT thickness. This implied that the annealing reduces the influence of this interface/blocking layer. This layer exists between the electrode and ferroelectric, most likely at the top electrode due to high temperature processing reasons.

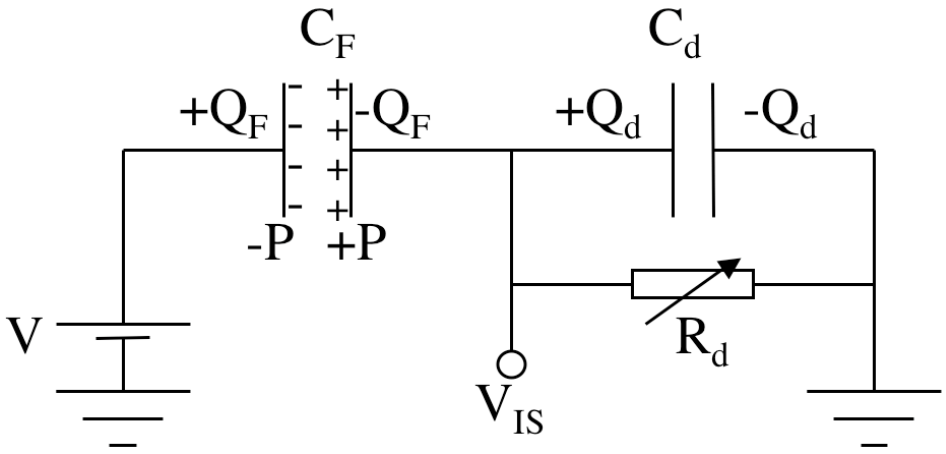


Figure 2.6: A schematic capacitive design of the Metal Ferroelectric Metal, MFM, structure, Cillessen et al. [1997].

They also explain that there is little likelihood that there is charge buildup at the ferroelectric, blocking layer interface due to results from pulse switching measurements. A blocking layer could exist due to non-stoichiometry at the ferroelectric/electrode interface or by poor quality growth of the ferroelectric layer, that is stress induced. However, the electrode/ferroelectric interface is complex; a blocking layer could be used to visualise what occurs there. To incorporate charge injection into the capacitance model, made by

Ma and Han [2002] in figure 2.5, Larsen et al. [1994] added a variable resistance in parallel to the capacitance of the dielectric layer in the capacitor model, see figure 2.6.

Injected Charge Impact on the Coercive Field

Tagantsev and Stolichnov [1999] developed a theoretical model to describe the effects that charge injection had on the coercive electric field, also providing experimental support. Figure 2.6, will also be used to describe the charge injection mechanism with a build up of possible trapped charge due to the injected charge, σ_{inj}, sitting at the dielectric/ferroelectric interface. As is seen in figure 2.3, the polarisation in the dielectric layer is smaller than in the ferroelectric layer and increases in value when moving away from the top electrode, Wurfel and Batra [1973]. Two reasons for this "dead" layer is due to a second-nonferroelectric phase or a near-by electrode layer as described above in section 2.2.1.

There needs to be one modification to equation 2.2 derived for the passive layer model and that is to include the injected charge. This is done by expanding the electric field in the dielectric layer to incorporate this injected charge by using equation 2.16 to represent the electric field in the dielectric layer. Where σ_{inj} represents the injected charge and P_s is the spontaneous polarisation in the ferroelectric layer.

$$E_d = \frac{P_s - \sigma_{inj}}{\epsilon_o \epsilon_d} \tag{2.16}$$

There are three scenarios to approximate the coercive electric field due to charge injection:

1. There is no charge injection due to the ferroelectric capacitor behaving as an insulator and is a classical dielectric where there is no change in the coercive electric field.

2. Charge injection occurs when the electric field is greater than the coercive field and the coercive field is modified as in equation 2.18.

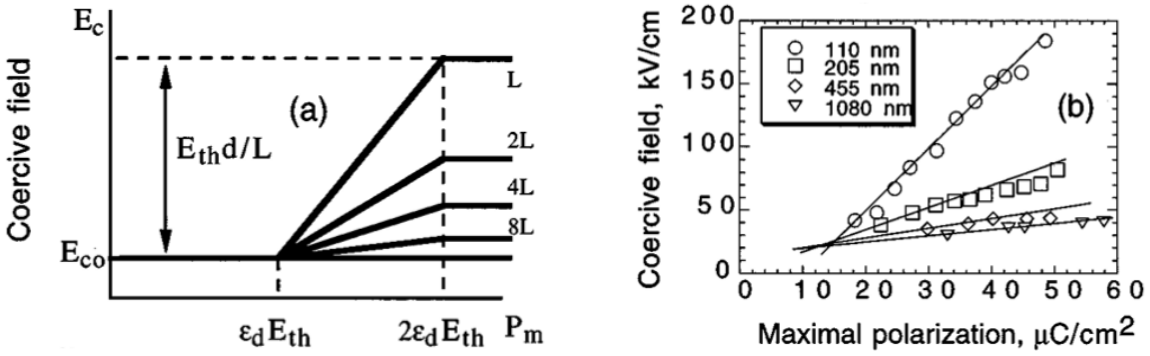
3. Charge injection occurs before reaching the coercive field and the coercive field is modified as in equation 2.19.

When charge injection occurs before the electric field reaches the coercive field then equation 2.16 becomes equation 2.17 due to $\text{E}_\text{d} \approx \text{E}_\text{th}$, the injection threshold electric field, where the polarisation is about its maximal $-\text{P}_\text{m}$.

$$\sigma_- = -P_m + \epsilon_d E_{th} \tag{2.17}$$

Substituting this into equation 2.2 and 2.16, with $\sigma_{\text{inj}}=\sigma_-$, $\text{P}_\text{s}=0$ and $\text{E}_\text{f}=\text{E}_\text{co}$ the equation 2.18 is derived. The coercive film of the ferroelectric film is denoted as E_co whereas that of the complete structure is denoted as E_c. This equation implies that charge injection occurs after the electric field reaches that of the coercive field.

$$E_c = E_{co} + \frac{d_d}{\epsilon_d d_f}(P_m - \epsilon_d E_{th}) \tag{2.18}$$



(a) (b)

Figure 2.7: a) The developed theory showing the increase of coercive field with the total polarisation. b) Experimental results proving this theory with PZT(45:55) capacitors of varying thicknesses. Tagantsev and Stolichnov [1999].

Figure 2.7a is a graph of equation 2.18 to which experimental support was developed. PZT(45:55) capacitors of varying thicknesses, $110, 205, 455, 1080\,\text{nm}$, were deposited by the sol gel method, including an annealing at $600\,^{\circ}\text{C}$. The capacitor structure had both sputtered platinum top and bottom electrodes. The experimental results of the polarisation loops are summarised in figure 2.7b and proves that equation 2.18 correctly models these capacitors. That is the charge injection occurs after the coercive field has been obtained.

When charge is injected before the electric field reaches the coercive field E_{th} is approximately E_d, and one gets equation 2.19, which was also derived by Cillessen et al. [1997].

$$E_c = E_{co} + \frac{d_d}{d_f} E_{th} \tag{2.19}$$

2.2.3 Estimation of the Retention Time of a MFS Structure

If the polarisation state is not stable in the ferroelectric layer then it should have some finite time associated to it that describes how long the polarisation can be maintained before going to the opposite direction, this is called the retention time. Poor retention in ferroelectrics deposited onto semiconductors can be caused due to incomplete charge compensation and charge injection as presented in more detail by Ma and Han [2002]. However, if too much charge trapping occurs to give 100% charge compensation all of the bound charge associated with the spontaneous polarisation of the ferroelectric layer could be completely screened from the channel that is supposed to be modulated.

Oversimplifying the retention time, that is by not considering all of the polarsation retention mechanisms and taking into account only charge leakage and charge trapping, Ma and Han [2002] derived the following simple equation 2.21 for estimating the retention time of the ferroelectic layer on a semiconductor. P_r is the remanent polarisation of the

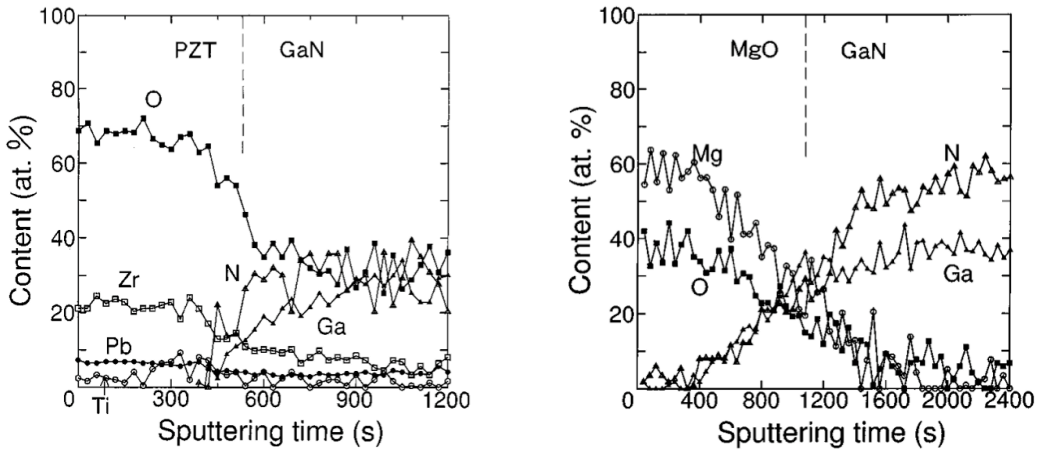
ferroelectric layer, I_L is the leakage current of the sandwiched ferroelectric layer, and t is the retention time. Lastly, α is a factor from 0 to 1 that represents the amount of injection current that becomes trapped charge and hence degrades the polarisation retention.

$$Q(E) = \int I(t)dt \tag{2.20}$$

$$t = \frac{P_r}{I_L \alpha} \tag{2.21}$$

Ma and Han [2002] tried applying the equation 2.21 to estimate the retention time when $P_r = 5\,\mu C/cm^2$ and $I_L = 5x10^{-8}\,A/cm^2$ for different amounts of charge trapping. In assuming the "worse" case scenario that every injected electron is trapped in the ferroelectric layer, α=1 and a retention time of 100 s can be calculated. On the other hand when one electron is trapped for every 10^4 electrons injected, $\alpha = 10^{-4}$, and the retention time would be approximately 10 days. These are rough estimates that oversimplify the scenario of polarisation retention in ferroelectrics deposited on semiconductors, considering only charge trapping due to charge injection and charge leakage. Especially since the phenomenon of charge leakage should not be constant but should decrease with the amount of charge trapped in the ferroelectric layer.

2.2.4 Interface Control



(a) (b)

Figure 2.8: a) XPS depth profile of the interface between 500 nm PZT (52:48) on cubic GaN , b) XPS depth profile of the interface between 200 nm MgO on cubic GaN , Masuda et al. [1998].

The PZT and GaN interface has already been studied using XPS depth profiling by Masuda et al. [1998], see figure 2.8a. The sandwich structure used here is interesting for the use in integrated ferroelectric devices including waveguides and the blue/green diodes. Randomly oriented PZT (52:48) of a thickness of 500 nm was deposited by pulsed laser deposition, PLD, onto cubic GaN. This cubic GaN was grown by metal organic vapor phase epitaxy, MOVPE, onto a (100) GaAs substrate. The initial deposition showed a highly diffusive interface as is shown in figure 2.8a. After which it was decided to use an

MgO diffusion barrier with a thickness of 200 nm directly deposited onto the cubic GaN, in order to minimise the oxygen and metallic diffusion. This intermediate MgO layer also allowed for the growth of a PZT layer with a preferential orientation in the (100) direction. XPS depth profiling was also done at the interface of the sample with 200 nm MgO on cubic GaN, see figure 2.8b. The two XPS depth profiles in figure 2.8 confirm that the diffusion at the MgO/GaN(cubic) interface is inferior to that at the PZT/GaN(cubic) interface.

For the case of this thesis a 200 nm layer of MgO is too thick and can completely reduce the spontaneous polarisation of the ferroelectric layer. Also as can be observed in the two XPS depth profiles, in figure 2.8, is that the interface extends to a thickness greater than 20 nm. This is already too large for the case of working with the AlGaN/GaN heterostructure as it will most likely destroy the 2DEG located at the AlGaN/GaN interface, see section 4.1.1.

2.2.5 Possible Solution with an MFIS Structure

The solution to reduce the leakage current could be simply solved by adding a thin buffer layer, possibly also solving the problem of the diffusive interface. Of importance is that there is not insufficient charge compensation causing a depolarisation effect as described above.

Briefly stated in the section 2.2.4 was that an insulating layer in-between the ferroelectric and semiconductor layers could be used as a buffer layer, working as a diffusion barrier. Watanabe and Masuda [2001] state that the Kittel model explains that when working with metal ferroelectric semiconductor, MFS, structures one ferroelectric state is stable and the other is quasi-stable depending on the effects countering the depolarisation field. This can be further extended to the fact that when the thickness of the ferroelectric film decreases it is expected that one ferroelectric polarisation state is more probable than the other. One way to increase the charge compensation, minimising the depolarising electric field in the ferroelectric layer is by using a metal ferroelectric insulator semiconductor, MFIS. In doing such the ferroelectric film in the MFIS structure has a better chance to exhibit two stable polarisation states. Watanabe and Masuda [2001] were also able to show that a full optimisation of the insulator layer needs to be done to implement a working device. If using too thick of an insulator the ferroelectric polarisation is completely screened to the semiconductor and in the case when too thin an insulator is used not enough charge compensation occurs. Stressing the importance that this buffer layer does not only work as a diffusion barrier but also as a charge barrier.

2.2.6 Polarisation Fatigue

A ferroelectric film in a ferroelectric capacitor with top and bottom electrodes usually exhibits fatigue. Fatigue occurs when the spontaneous polarisation of the ferroelectric layer can only be switched through so many cycles before it no longer can switch. This phenomenon is not the first problem that will be encountered when implementing ferroelectrics on semiconductors, however, this effect could be stronger for ferroelectrics deposited directly onto semiconductors than on metallic films. A well written review pertaining to the mechanisms of polarisation fatigue in polycrystalline ferroelectric thin

films is written by Tagantsev et al. [2001]. In the conclusion five principle mechanisms are given:

- Bulk pinning of domain walls.
- Nearby electrode injection, inhibiting the seeds of opposite domain to nucleate.
- A depolarising field that is caused by the formation of a passive dielectric layer.
- Nearby electrode screening of ferroelectric polarisation with low mobility carriers.
- Reduction of electrode size due to delamination or burning, destruction when applying high DC voltage, of the electrode itself.

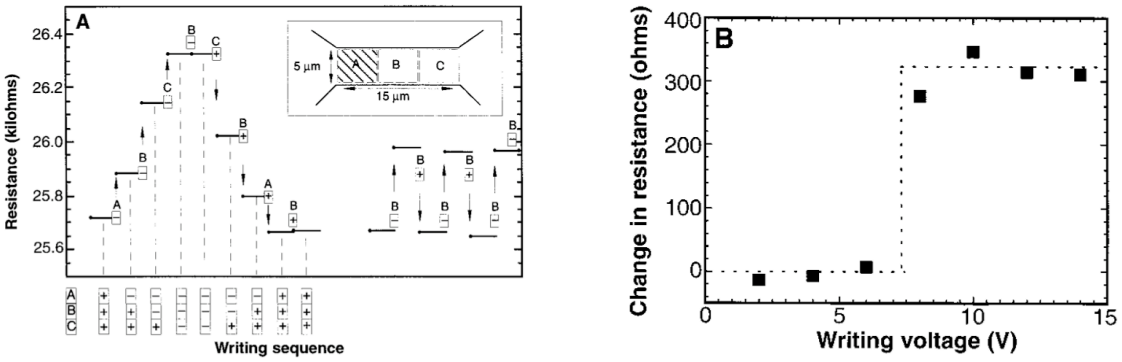
The principle mechanism of fatigue is claimed to be due to the nearby electrode injection. These mechanisms are important for the characterisation of ferroelectric materials when sandwiched between two metal electrodes. In this thesis the ferroelectric layer is deposited on a semiconductor and either has or does not have a top electrode. When developing the mechanisms of polarisation fatigue for ferroelectrics deposited on semiconductors it is important to keep in mind the mechanisms of polarisation fatigue when the ferroelectric layer has a metallic bottom electrode. It is possible that some of the above mentioned mechanisms are disadvantages for ferroelectrics on metallic electrodes but can bring about advantages for ferroelectrics on semiconductors, or vice versa.

2.3 Ferroelectrics for Domain Writing

Using contact scanning force microscopy, SFM, methods it is possible to do domain writing on ferroelectric films by applying a DC voltage to a conductive cantilever. Even more so, it might be possible to write structures on the nano-meter scale when using software designed to accurately control the position of the cantilever. When working with ferroelectrics deposited on semiconductors it is possible to create nano-structures by poling the ferroelectric with a DC bias to the conductive tip which is projected onto the semiconductor. This pattern would then invoke a local depletion or accumulation of electrons depending on the bias applied to the tip. The modulation of the current in the channel can then be observed using appropriate electrical measurements. Using SFM or piezoresponse force microscopy, PFM, it is possible to write domains on the nano-meter scale, paving the way for future possibilities in ferroelectric nano-lithography. The benefits of using ferroelectrics for domain writing is that they allow for the creation of a reversible, non-destructive process.

2.3.1 Ferroelectric Gate Controlled by Scanning Force Microscopy

The possibility to project a ferroelectric domain pattern written onto a channel using scanning probe microscopy techniques has been investigated by, Ahn et al. [1997]. This is a very intersting technique since when using the ferroelectric layer the process is both reversible and non-destructive. A 400 nm epitaxial $Pb(Zr_{0.52}, Ti_{0.48})O_3$ film was deposited onto a 3 nm metallic $SrRuO_3$ layer where poling the ferroelectric induced the effect of



(a) (b)

Figure 2.9: a) The change in the resistance of the metallic $SrRuO_3$ after the poling of each individual square of 5x5 μm^2 of PZT with ± 14 V. (In the insert the 15x5 μm^2 structure used is shown.) b) The resistance vs writing voltage when only square B of 5x5 μm^2 was poled with 0 V to -15 V, Ahn et al. [1997].

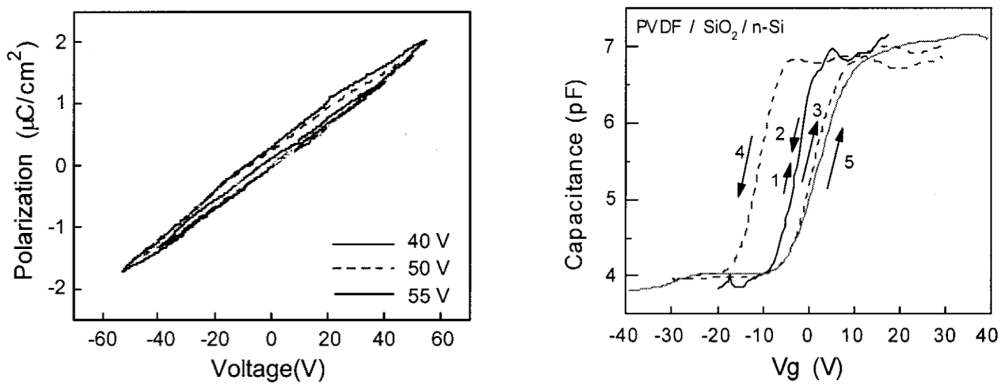
local depletion in the $SrRuO_3$. The benefit of using this structure to show the modulation of the channels resistance due to the poling of the spontaneous polarisation of the PZT layer is that the metallic $SrRuO_3$ and PZT are located in direct contact with each other, and do not suffer from large additional depolarisation fields and charge screening effects. The poling occurred by individually poling three squares of 5x5 μm^2, see figure 2.9a, with ± 14 V applied to a conductive tip on a scanning probe microscope. The resistance was then measured with a two probe technique to observe the modulation of the resistance after the poling of each 5x5 μm^2 square. Figure 2.9b shows explicitly how the resistance changes after the poling of one, the central, 5x5 μm^2 square. The resistance was modulated by a value of 300 Ω, when poling with ± 14 V in one square of 5x5 μm^2. The line resolution when writing domains with the PFM on this structure was measured as 350 nm. The technique of controlling the channels resistance when poling the ferroelectric layer with a PFM technique confirms the future potential of ferroelectric nano-lithography.

2.4 Organic Ferroelectrics

Organic ferroelectrics have gained much interest lately due to their low crystallisation temperatures, and low cost of deposition. Kawai [1969] and Fukada and Takashita [1969] discovered the piezoelectricity in poly(vinylidene fluoride), PVDF, when studying various polymers. Later on Nakamura and Wada [1971], Bergman et al. [1971] and Glass et al. [1971] discovered that this polymer layer, PVDF, also possesses ferroelectric properties. Furukawa et al. [1980] have done much research of the enhanced ferroelectric copolymer, P(VDF/TrFE). Due to the low crystallisation temperature of this group of ferroelectric polymers it was thought of as an ideal ferroelectric layer in the FeFET structure to preserve the semiconductor during the ferroelectric deposition.

2.4.1 P(VDF/TrFE)/Silicon Transistors

Lim et al. [2004] decided to integrate the P(VDF/TrFE), having a low crystallisation temperature, immediately with a silicon semiconductor while using an intermediate SiO_2 insulator layer. A layer of 450 nm P(VDF/TrFE) was deposited by spin casting, and annealed at 145 °C for $30 - 120$ min, on top of a layer of 80 nm SiO_2 grown by wet thermal oxidation at 1100 °C on the n-doped silicon substrate. The silicon had a resistivity of $1 - 10\,\Omega$cm and titanium top electrodes to the ferroelectric were used on a device where the silicon substrate was not etched.



(a) (b)

Figure 2.10: MFIS structure with 450 nm P(VDF/TrFE)/80 nm SiO_2/Si. a) Polarisation vs gate voltage curve. b) Capacitance vs gate voltage curve where line 1 is swept from −20 V to +20 V, line 2 from +20 V to −20 V, line 3 from −30 V to +30 V, and line 4 from +30 V to −30 V, and line 5 from −40 V to +40 V, Lim et al. [2004].

The P(VDF/TrFE)/SiO_2/Si MFIS structure underwent ferroelectric characterisation with both C-V and P-V measurements. The polarisation vs gate voltage curve in figure 2.10a is typical of a lossy capacitor that is not a good insulator and is a linear dielectric with linear conduction, Jaffe et al. [1971]. For a non ferroelectric insulator the polarisation vs voltage curve would result in a straight line, Jaffe et al. [1971]. It is also not so trivial to assume ferroelectricity from the capacitance vs voltage curve in figure 2.10b.

Gerber et al. [2006] also tried to develop the P(VDF/TrFE)/silicon transistor, where the silicon had a resistivity of $1 - 10\,\Omega$cm. A gold gate made a schottky contact to a 36 nm P(VDF/TrFE) film deposited on a 10 nm SiO_2 insulating layer on a p-type silicon substrate. The main change of results from Lim et al. [2004] is that the applied gate voltage did not need to be so large since the ferroelectric and insulator thickness was more than one order of magnitude smaller. This is due to using the Langmuir-Blodgett deposition process for the P(VDF/TrFE) film which allows for the deposition of thinner films than using spin casting. The polarisation vs gate voltage of this structure was similar to that shown in figure 2.10a, however they were able to show C-V curves with better defined ferroelectric retention in the counterclockwise curve. Figure 2.11 shows the retention of the structures capacitance after having been poled ±4 V.

Neither groups showed measurements on the change of the channels transport properties by transistor or transport measurements, including retention of the written state. The concept of P(VDF/TrFE)/SiO_2/Si FeFET or MFIS transistor has yet to be completely demonstrated.

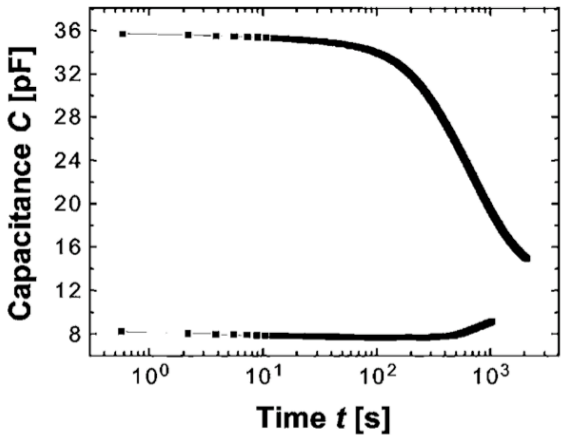
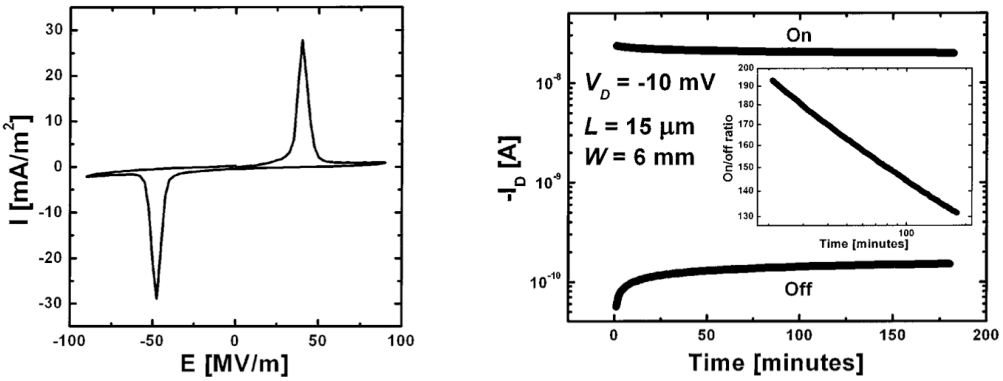


Figure 2.11: A 36 nm P(VDF/TrFE) film with a 10 nm SiO_2 insulating layer on a p-type silicon transistor showing the retention of the capacitance after having been poled ±4 V, Gerber et al. [2006].

2.4.2 P(VDF/TrFE) Organic Transistors

Naber et al. [2005] spin coated P(VDF/TrFE) polymer ferroelectric thin films onto the high mobility semiconducting polymer, regio-regular poly-(3-hexylthiophen)-(rr-P3HT). This device is 100% bio-degradable, organic transistors and ferroelectrics are the wave of the future as they are extremely beneficial for creating environmental friendly electronic circuits.



(a) (b)

Figure 2.12: a) Current vs gate electric field demonstrating ferroelectric hysteresis with ±18 V in a P(VDF/TrFE) ferroelectric organic capacitor. b) The retention characteristics of a P(VDF/TrFE) ferroelectric organic transistor, the drain current is observed after having applied ±18 V, Naber et al. [2005].

The P(VDF/TrFE) was deposited to a thickness of 200 nm and gold gate electrodes with an area of 1 mm^2 were used. First capacitor structures were tested in which it was possible to observe ferroelectric behavior, Naber et al. [2004], after which transistor devices were fabricated. In figure 2.12a the drain source current, I_{DS}, vs gate voltage, V_G, curve from a P(VDF/TrFE) ferroelectric organic capacitor not only demonstrates the modulation of the I_{DS} with V_G but also shows ferroelectric behavior. A P(VDF/TrFE) ferroelectric

organic transistor exhibited ferroelectric retention from the I_{DS} vs V_G curve at a constant $V_G = -1\,V$ since this curve can be transformed to a counterclockwise C-V curve. Retention measurements were then performed on this transistor in the on and off states for 180 min, using a programming voltage of $\pm 18\,V$, the results of which are shown in figure 2.12b. An extrapolation of the retention measurement was done and is shown in the inset graph of figure 2.12b, estimating the lifetime of the ferroelectric transistor as 10^8 min.

2.5 Recent Progress

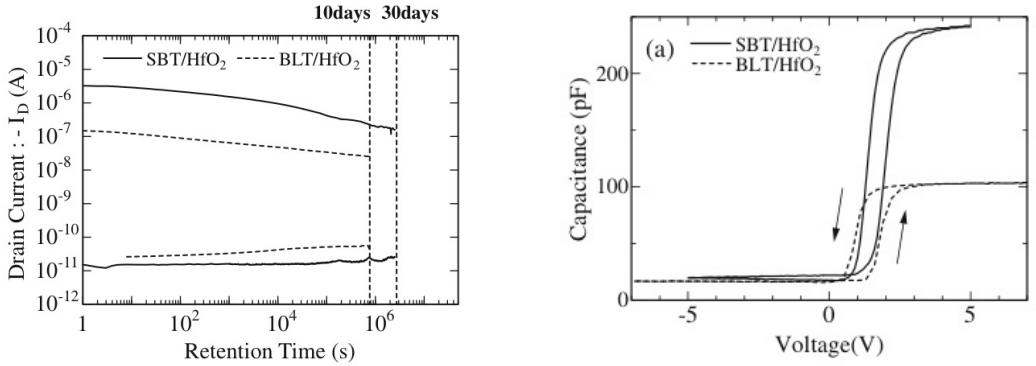
During the elapsed time of this thesis many other researchers, laboratories and companies were also investigating the improvement of FeFET structures. Therefore, other papers were published during the course of this thesis. Most of these papers confirm the line of direction that this research also used. Briefly will be presented some of the major developments in this field during the years 2004 to 2006.

2.5.1 HfO_2 Buffer Layer

The HfO_2 layer can serve as the gate dielectric, helping surface passivation and decreasing any gate leakage current. The dielectric constant of HfO_2 is $\epsilon_{HfO_2} \sim 23$ and it has a large bandgap of $E_g = 5.67\,eV$. The high dielectric constant is of utmost importance so that there will be little voltage drop across this layer in the sandwich structure.

Ferroelectric/Silicon Transistor

More recently in the field of MFISFETs (metal-ferroelectric-insulator-semiconductor field-effect transistors) strong results have been presented by Takahashi et al. [2005], and Aizawa et al. [2004]. They investigated the $Pt/SrBi_2Ta_2O_9(SBT)/HfO_2/Si$ structure and at the same time a $Pt/(BiLa)_4Ti_3O_{12}(BLT)/HfO_2/Si$ structure.



(a) (b)

Figure 2.13: $SBT/HfO_2/Si$ and the $BLT/HfO_2/Si$ MFIS-FETs, Takahashi et al. [2005]. a) Drain source current, I_D, vs time, showing the retention characteristics of the in the accumulated, poled $+10\,V$, and depleted, poled $-10\,V$, states. b) C-V curves performed at 1 MHz show hysteretic ferroelectric behavior for both structures.

The ferroelectric films were approximately of 400 nm thickness, grown by sol-gel methods and then annealed in oxygen at 750 °C for $1 - 30$ min. The HfO_2 films were 8 nm thick and grown by ultra high vacuum electron-beam evaporation. Immediately after poling the source to drain current on(poled -10 V)/off(poled $+10$ V) ratio was 10^5, after 30 days this ratio decreased to 10^3, see figure 2.13a. In figure 2.13b it is possible to observe from the C-V curves done at 1 MHz on both SBT/HfO_2/Si and BLT/HfO_2/Si diodes that the switching mechanism behind the depletion and accumulation of electrons in the Si channel is in fact from the ferroelectric polarisation.

These results are so spectacular that it would be assumed that the problem is solved here, especially since it involved the integration of a ferroelectric with the most commonly used semiconductor, silicon. However, as of now they are the only group to have had published such sound results and the FeFET in this configuration is not being commercially produced.

HfO_2/Hf Buffer Layer

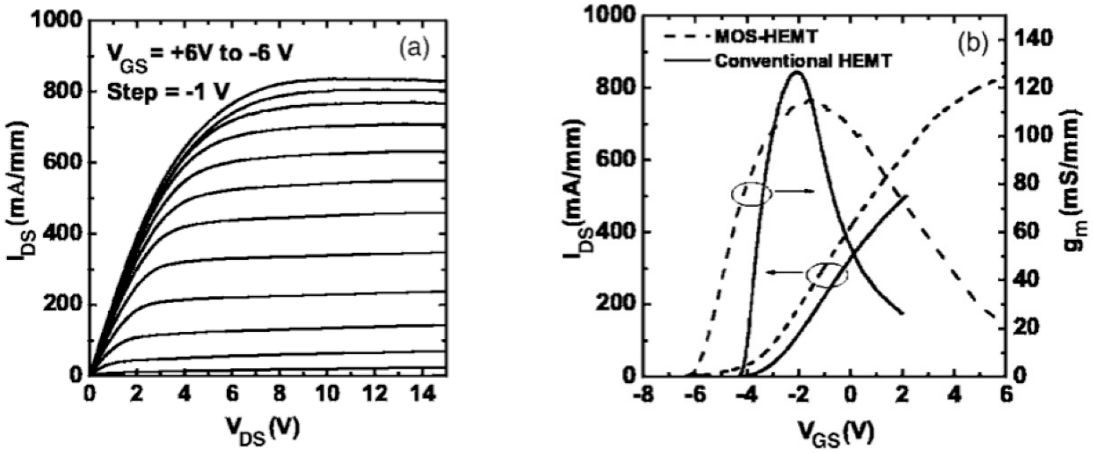
Lu et al. [2006] decided to optimise the growth of HfO_2 on silicon by minimising the low dielectric hafnium interfacial layer that is usually initially grown on the silicon, before the HfO_2 is deposited. They tried to do this by optimising the oxygen partial pressure and developing a two-step process using auger electron spectroscopy, AES, to help analyse the resulting layer deposited. The optimised HfO_2 layer was done by first depositing a 3 nm thick layer of pure Hf after which the HfO_2 was deposited. This thin metal layer efficiently suppressed the diffusion of O_2 into the Si. HfO_2 was grown by laser molecular beam epitaxy (LMBE) for the development of a high dielectric insulator layer in MOSFETs.

AlGaN MOSHEMT

If the HfO_2 buffer layer can suppress the diffusion occurring at a feroelectric/silicon interface why could it not suppress the diffusion at the ferroelectric/AlGaN interface. Already HfO_2 is being used as the oxide layer in a AlGaN/GaN metal-oxide-semiconductor high electron mobility transistors, MOS-HEMTs by Liu et al. [2006]. Showing the potential for the integration of HfO_2 and AlGaN.

The device structure had a 2DEG located at a distance 20 nm below the HfO_2/AlGaN interface. The AlGaN heterostructure was grown by MOCVD with a undoped GaN cap layer of 2 nm on 18 nm layer of undoped $Al_{0.26}Ga_{0.74}N$. HfO_2 of 3 nm, 23 nm and 60 nm was sputtered onto this heterostructure using a hafnium target in O_2. The transistor design had a length of 1.5 μm and source to drain spacing of 6 μm. This HEMT with HfO_2 charge passivation oxide layer shows excellent transistor curves, see figure 2.14a.

They claim that HfO_2 passivates the surface traps thus increasing the electron sheet concentration in AlGaN. This is supposed to be due to the fact that the maximum current source current, I_{DS}, of a HEMT is 500 $^{mA}/_{mm}$ at V_{GS}=2 V but is 830 $^{mA}/_{mm}$ at V_{GS}=6 V in the MOS-HEMT. Even more so is that the I_{DS} of MOS-HEMTs is superior to that of HEMTs at equivalent gate source voltage, V_{GS}, see figure 2.14b. Less decrease in the transconductance, g_m, will occur in comparison to using an oxide with a low dielectric constant. The transconductance is one of the most important parameters to measure



(a) (b)

Figure 2.14: MOS-HEMT characteristics with a 23 nm oxide layer a) I_{DS} vs V_{DS} at varied V_{GS} for b) I_{DS} and g_m vs V_{GS} at V_{DS} = 8 V, Liu et al. [2006].

since it tells us how much the V_{GS} can control the I_{DS} at a specific drain source voltage, V_{DS}, see equation 2.22.

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}}|_{V_{DS}} \tag{2.22}$$

2.5.2 PZT Gate with Si_3N_4 Buffer Layer

Several months after our own publication, Stolichnov et al. [2006], showing the modification of the sheet resistance in the 2DEG by a factor of three due to the poling the PZT layer, Kang et al. [2006] published similar results while using a Si_3N_4 buffer layer.

Si_3N_4 is another possibility as a buffer layer with a dielectric constant, $\epsilon_{Si_3N_4} \approx$ 7.5. However, this dielectric constant is smaller than oxides such as MgO, $\epsilon_{MgO} \approx$ 9.7, and HfO_2, $\epsilon_{HfO_2} \approx$ 25. Si_3N_4 which has a bandgap, E_g, of approximately 5 eV matches better the bandgaps of $Al_{0.3}Ga_{0.7}N$ (4.3 eV) and PZT (3.7 eV), than MgO and HfO_2 do. Among other reasons for using this interfacial buffer layer is that it could improve the ferroelectric/semiconductor interface, allowing the channel to keep its good transport properties.

Kang et al. [2006] decided to use a Si_3N_4 buffer layer of 10 nm thickness between the AlGaN and the gate ferroelectric in order to limit the diffusion occurring at this interface by chemical isolation, see figure 2.15. This Si_3N_4 layer was grown by plasma enchanced chemical vapor deposition (PECVD) onto a 180 nm thick layer of Si-doped $Al_{0.3}Ga_{0.7}N$ grown by plasma assisted molecular beam epitaxy, PAMBE. The 2DEG transport properties were measured as having a sheet concentration of $2.3 \text{x} 10^{13}\,\text{cm}^{-2}$ and a mobility of $467\,^{\text{cm}^2}/_{\text{Vs}}$ at room temperature before PZT deposition. The PZT was grown by a single target ($Pb_{12}(Zr_{0.52}Ti_{0.48})O_3$) RF magnetron sputtering process to a thickness of 120 nm. A ferroelectric field effect transistor was then designed and structured with width 7 μm and length 95 μm. With this structured device they were able to measure a modulation in the drain source current I_{DS} with V_{GS} by at least a factor four. Figure 2.16b shows a

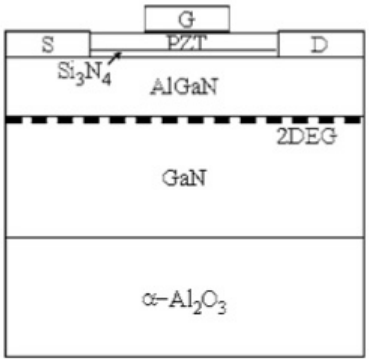
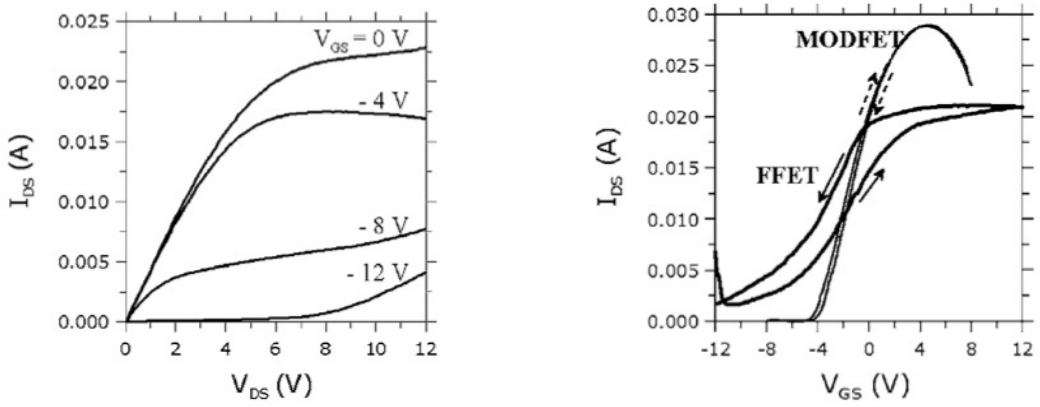


Figure 2.15: Cross section of the device used by Kang et al. [2006]. A 10 nm Si_3N_4 buffer layer was used to limit the diffusion of the PZT grown by a single target ($Pb_{12}(Zr_{0.52}Ti_{0.48})O_3$) RF magnetron sputtering process.



(a) (b)

Figure 2.16: PZT/Si_3N_4/$Al_{0.3}Ga_{0.7}N$/GaN ferroelectric field effect transistor of width 7 μm and length 95 μm. a) I_D vs V_{DS} transistor characteristics for different values of V_{GS}, showing the modulation of the I_{DS} with the V_{GS} by at least a factor four. b) I_D vs V_{GS} indicating retention of the switched polarisation. Kang et al. [2006]

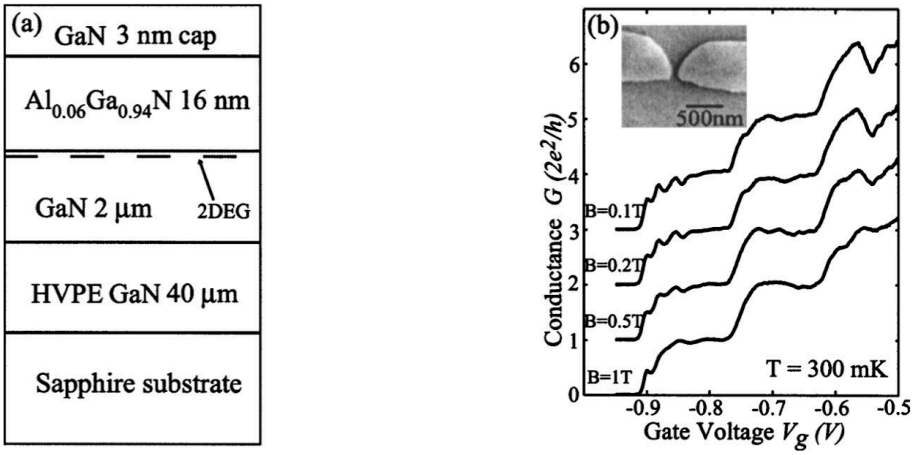
typical transistor curve with I_{DS} varying with V_{DS} and modulated by V_{GS}. When increasing V_{DS} above 8 V, I_{DS} had problems of gate leakage for $V_{GS} \geq -8$ V. The depletion effect observed could be more substantial if the gate leakage problems are reduced with a higher crystalline quality PZT layer that was deposited here. They suppose that their PZT quality is poor since the usual post-annealing treatment was omitted. Counterclockwise current voltage curves were also produced with these structures indicating the retention of the switched polarisation; shown in figure 2.16.

2.5.3 GaN/AlGaN/GaN Quantum Point Contact

The techniques based on direct SPM writing can allow for the formation of a nanostructure in a single-step with a pattern resolution that is potentially higher than the traditional lithographic processes. Snow and Campbell [1994], Matsumoto et al. [1996], and Held et al. [1997] demonstrated the local anodic oxidation of the cap layer in the

$GaAs/Al_xGa_{1-x}As$ heterostructure with a 2DEG located tens of nm to the surface with typical writing feature size of 100 nm using SPM techniques. The projection of the ferroelectric polarisation pattern onto the 2DEG of the AlGaN/GaN heterostructure could also allow to make and measure quantum dots, wires and rings. However to do so it is of interest to first observe the creation of quantum devices and ballistic transport by patterned electroded AlGaN heterostructures.

To date there has only been one report of a quantum device in a AlGaN heterostructure. The quantum point contact, QPC, structure has been successfully demonstrated by Chou et al. [2005]. The heterostructure used is shown in figure 2.17a and consists from top to bottom of 3 nm GaN, 16 nm $Al_{0.06}Ga_{0.94}N$, 2 μm GaN, 40 μm hydride vapor phase epitaxy, HVPE, GaN and a sapphire substrate. At 4.2 K the 2DEG in this heterostructure has a electron sheet concentration of $1x10^{12}$ electrons/cm^2 and a mobility of 56000 cm^2/Vs. As shown in the inset of figure 2.17b nickel electrodes were deposited by evaporation and patterned with electron beam lithography to be in as close proximity as possible. The QPC exhibits one dimensional transport between two electrodes that are narrowly spaced. The conductance (dI/dV_{sd}) flowing between these two electrodes can be tuned by an electron each of a quantised conductance, of $2e^2/h$ at low magnetic fields and e^2/h at higher magnetic fields. The constant e is the electron charge ($1.602x10^{-19}$ C) and h is Planck's constant ($6.626x10^{-34}$ Js). The functional QPC is shown in figure 2.17b, and shows the two quantised conductance plateaus at $2e^2/h$ and $4e^2/h$ for low magnetic fields. When the magnetic field is increased to 1 T a third quantised conductance appears. They claim that the resonances observed in the conductance vs gate voltage at magnetic fields close to zero tesla are due to backscattering effects, since the mean free path of the electrons is 700 nm which is about the same order of magnitude of the largest spacing between the two electrodes in the QPC.



(a) (b)

Figure 2.17: a) Cross section of the device used. b) Demonstration of the functionality of the quantised conductance, by $2e^2/h$, in the quantum point contact at 300 mK. The inset shows the top view of the device. Chou et al. [2005].

At 300 mK Schmult et al. [2006] observed that the Shubnikov de Haas oscillations begun at a magnetic field of 0.6 T. This observation was found out on a modified heterostructure from the one discussed above where the mobilty of the 2DEG had been improved to 167000 cm^2/Vs with a electron sheet concentration of $9.1x10^{11}$ electrons/cm^2 at 300 mK. The

integer quantum Hall effect was visible for magnetic fields greater than 3 T. The Shubnikov de Hass oscillations and the quantum Hall effect were previously observed at 50 mK by Knap et al. [2004] on a AlGaN heterostructures where the 2DEG had a mobility of $60000\,^{\mathrm{cm}^2}/_{\mathrm{Vs}}$ at 4 K.

The fact that ballistic transport devices have not been so successfully achieved without using the ferroelectric gate concept implies that it will be extremely difficult to do so with one. The fact is that even in the best case scenario the complete depletion of electrons from the channel is not expected.

Chapter 3

Measurement Techniques

3.1 Transport Measurements

Transport measurements are necessary in order to monitor the electron sheet concentration, mobility and sheet resistance of the two dimensional electron gas, 2DEG. The simplest method to control the sheet resistance, is using the van der Pauw technique which is most accurate for square structures but can also be used for samples of arbitrary shapes. For more detailed analysis Hall effect measurements allow for controlling the additional values of the electron sheet concentration and mobility in the 2DEG. Both of these techniques will be described in this section.

3.1.1 Hall Measurements

The basic principle standing behind Hall measurements is observing the Hall voltage produced when electrons flowing from one end of the channel to the other are slightly deviated in the direction perpendicular to their flow with the application of a magnetic field. The phenomenon that causes an electron to move in a direction that is perpendicular to its direction of motion and the applied magnetic field is is known as the Lorentz force, see figure 3.1. From this force it is possible to measure the Hall voltage, V_H. Then with the known values for the current, I, the magnetic field, B, and the electron charge, q=1.602x10^{-19} C it is possible to calculate the electron sheet concentration, n_s, equation 3.1. The Hall effect is usually used to measure a three dimensional channel, however since we are concerned with the two dimensional 2DEG, all of the equations listed in this section will be for two dimensional channels.

$$n_s = \frac{IB}{q|V_H|} \tag{3.1}$$

If the sheet resistance R_s of the semiconductor is known it is then possible to calculate the carrier mobility, μ, with equation 3.2.

$$\mu = \frac{|V_H|}{R_S IB} = \frac{1}{qn_s R_s} \tag{3.2}$$

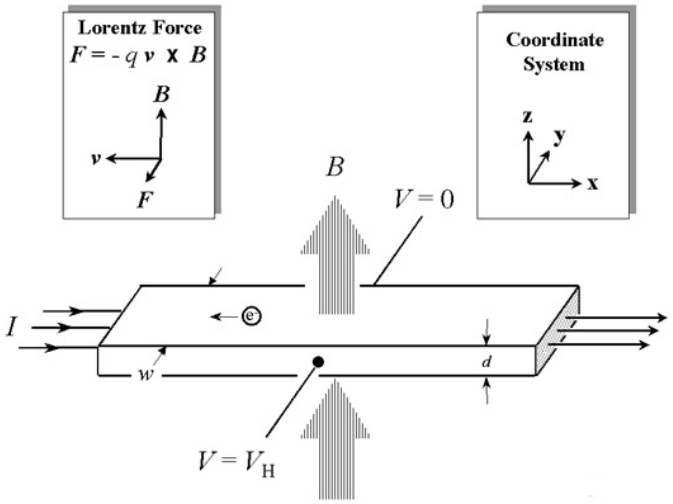


Figure 3.1: Hall Measurements. Image is taken from http://www.eeel.nist.gov/812/effe.htm.

The sheet resistance, R_s, for a Hall bar structure is calculated by equation 3.3, where I_c is the current applied to the extremities, W the width of the Hall bar, L the length of the Hall bar and V the voltage drop across the Hall bar. Equation 3.3 is a two dimensional measurement and is valid for the resistance describing the two dimensional electron gas. If it is necessary to measure R_s for a sample without the Hall bar patterned onto it or a arbitrary shape sample one must follow the method described by Pauw [1958/59].

$$R_s = \frac{VW}{I_c L} \tag{3.3}$$

3.1.2 The van der Pauw Technique

For this thesis the van der Pauw technique was useful in preliminary measurements of determing the sheet resistance of the 2DEG and observing its change during the ferroelectric deposition process. This measurement technique was less cumbersome than preparing structure samples for Hall effect measurements. Using the van der Pauw technique the sheet resistance R_s can be calculated easily for arbitrary shaped samples, equation 3.5, Pauw [1958/59]. This is done by applying a voltage across two neighbouring electrodes and measuring current across the other two neighbouring electrodes, see figure 3.2 where 1, 2, 3, and 4 denote the four corner electrodes. This is done in two different orientations to allow for the calculation of R_A and R_B using the equations 3.4.

$$R_A = \frac{V_{43}}{I_{12}} \qquad R_B = \frac{V_{14}}{I_{23}} \tag{3.4}$$

$$e^{\frac{-\pi R_A}{R_S}} + e^{\frac{-\pi R_B}{R_S}} = 1 \tag{3.5}$$

If wanting to do more accurate measurements for R_A and R_B one needs to take into account the a-symmetrical effects produced by the sample to do so more current-voltage needs to be done.

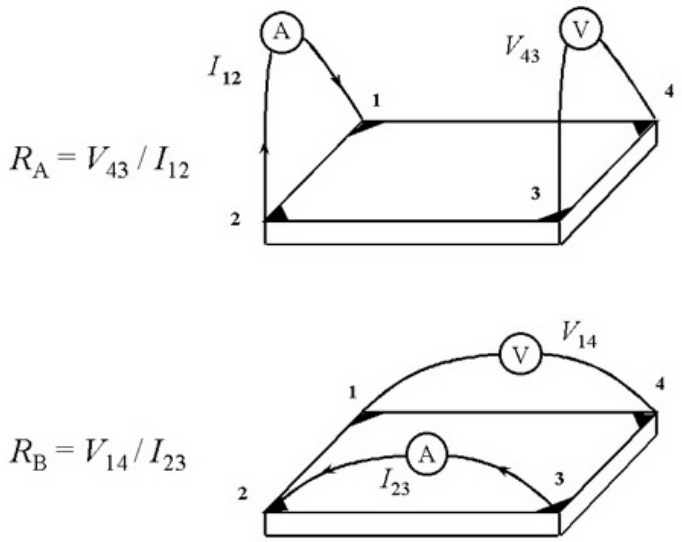


Figure 3.2: Van der Pauw measurements. Image is taken from http://www.eeel.nist.gov/812/effe.htm.

$$R_A = (\frac{V_{34}}{I_{21}} + \frac{V_{43}}{I_{12}} + \frac{V_{12}}{I_{43}} + \frac{V_{21}}{I_{34}})/4 \tag{3.6}$$

$$R_B = (\frac{V_{41}}{I_{32}} + \frac{V_{14}}{I_{23}} + \frac{V_{23}}{I_{14}} + \frac{V_{32}}{I_{41}})/4 \tag{3.7}$$

Where due to symmetry the following equations 3.8 - 3.10, must be true within a 5% margin of error.

$$\frac{V_{41}}{I_{32}} = \frac{V_{14}}{I_{23}} \qquad \frac{V_{34}}{I_{21}} = \frac{V_{43}}{I_{12}} \qquad \frac{V_{12}}{I_{43}} = \frac{V_{21}}{I_{34}} \qquad \frac{V_{23}}{I_{14}} = \frac{V_{32}}{I_{41}} \tag{3.8}$$

And due to reciprocity the following equations must hold true, equations 3.9 and 3.10.

$$\frac{V_{41}}{I_{32}} + \frac{V_{14}}{I_{23}} = \frac{V_{23}}{I_{14}} + \frac{V_{32}}{I_{41}} \tag{3.9}$$

$$\frac{V_{34}}{I_{21}} + \frac{V_{43}}{I_{12}} = \frac{V_{12}}{I_{43}} + \frac{V_{21}}{I_{34}} \tag{3.10}$$

Using the van der Pauw resistivity measurements the carrier mobility and the carrier concentration can also be measured. As seen in figure 3.3, the current is applied to two terminals opposite from each other and the voltage is measured from the other two terminals. This voltage labeled V_{24P} is equivalent to the Hall voltage as measured in the Hall measurements. Afterwards the same equations as for Hall measurements are used to calculate the carrier mobility and concentration. These techniques can allow for the studying of the 2DEG properties in the ferroelectric/heterostructure device as a function of ferroelectric polarisation, however n_s and μ are more accurate when using a Hall bar structure.

In fact when measuring the Hall effect for an arbitrary shape it is also important to check for symmetry. The most accurate results will thus be obtained by taking measurements when the magnetic field is applied in both polarities and reversing the current/voltage configuration. In this manner one will have an averaged value for the Hall voltage. This is explicitly done by applying a positive magnetic field and then: apply I_{13} and measure V_{24P}, apply I_{31} and measure V_{42P}, apply I_{24} and measure V_{13P} and apply I_{42} and measure V_{31P}. Then the same needs to be done for a negative magnetic field: apply I_{13} and measure V_{24N}, apply I_{31} and measure V_{42N}, apply I_{24} and measure V_{13N} and apply I_{42} and measure V_{31N}. Then it is possible to calculate V_C, V_D, V_E and V_F, see equation 3.11, to calculate the Hall voltage of the sample with equation 3.12. It is then possible with the known values for V_H and R_s to calculate the electron sheet concentration with equation 3.1 and the mobility with equation 3.2.

$$V_C = V_{24P} - V_{24N} \qquad V_D = V_{42P} - V_{42N} \qquad V_E = V_{13P} - V_{31N} \qquad V_F = V_{31P} - V_{31N} \tag{3.11}$$

$$V_H = \frac{V_C + V_D + V_E + V_F}{8} \tag{3.12}$$

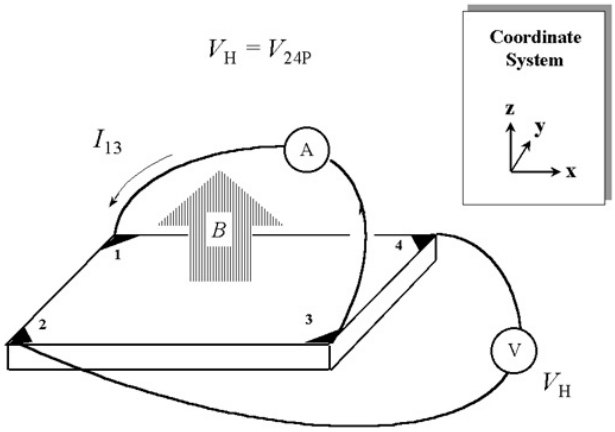


Figure 3.3: Measuring the Hall effect by the van der Pauw technique. Image is taken from the website http://www.eeel.nist.gov/812/effe.htm.

3.2 Scanning Force Microscope

The idea of scanning force microscopy, SFM, was discovered in 1986 by Binnig et al. [1986], as a topographical technique. A constant force is maintained between a cantilever and the sample, or in some cases a constant sample-cantilever tip distance is used, to measure the change in distance or force, respectively, hence having a topographic map of a sample. To measure these forces and distances a laser beam is focused onto the cantilever and is reflected onto a position sensitive photodetector, PSPD. The reflected signal is compared to the set point value chosen and the difference is used for calculating both the topographical data and to control the z position of the scanner, see figure

3.4. This is a versatile and non-destructive technique for making mappings of insulators, conductors, semi-conductors and also used for biological applications. Cantilever shape and dimensions can strongly impact the quality of the image due to properties such as the mechanical resonance frequency and force constant. Specifically, the resolution of the image obtained can be controlled, along with other factors, by the tip radius.

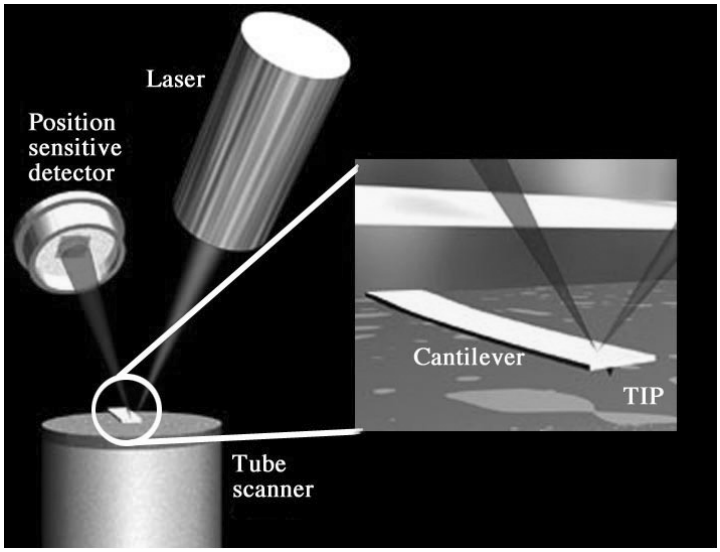


Figure 3.4: Principle of SFM. Baselt [1993]

There are three modes in SFM: contact, non-contact, and tapping(intermittent) mode. In contact mode a repulsive van der Waals force is measured from the reflected laser signal as the cantilever tip is in close proximity $(1 - 10)$ nm to the sample. Ideally, the cantilever should have a spring constant slightly lower than the effective spring constant holding the atoms of the sample together. In using a force too great in between the cantilever and sample any particles lying on the surface will be dragged around. However, if one uses too small of a force the cantilever will not follow the topography. In general, this technique is good for large, non-uniform areas. In non-contact mode the cantilever is never in contact with the sample and the cantilever-sample forces are attractive, therefore the mechanical stiffness of the cantilever should be greater than those used for contact mode so that it does not get pulled into the sample. Here the cantilever is a distance of $(1 - 100)$ nm above the sample, implying that the cantilever will have a longer life and that there is less potential for surface damage. In this method the cantilever is driven by a piezoactuator at a frequency just a bit higher than its mechanical resonance frequency, afterwards using amplitude modulation the topographical signal is extracted. Intermittent or tapping mode is similar to non-contact mode in many ways, however, the cantilever is vibrating $(1 - 10)$ nm above the sample, where at the lowest point of its cycle the tip intermittently touches the sample. A frequency just lower than the mechanical resonance frequency of the cantilever is used and again the topographical signal is extracted using amplitude modulation. Tapping mode at ambient temperature is possible, however non-contact operation is easier in vacuum where air damping of cantilever oscillations is negligible, due to a much sharper mechanical resonance peak of the cantilever and hence higher sensitivity while measuring the shift in resonance frequency, Abplanalp [2001].

3.3 Piezoresponse Force Microscope

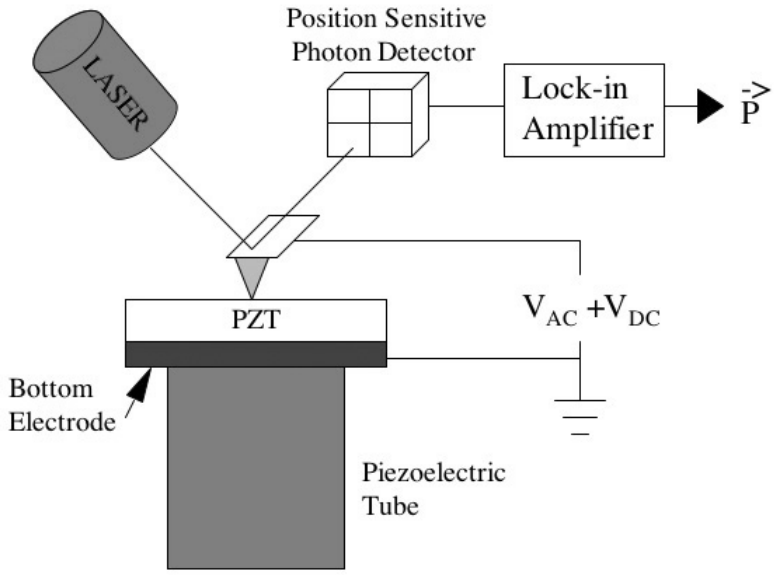


Figure 3.5: PFM measurement setup

The first measurements of piezoresponse force microscopy, PFM, were done by Güthner and Dransfeld [1992]. They observed ferroelectricity by first applying a DC voltage between a conductive SFM tip, acting as top electrode, and a bottom electrode, hence poling the ferroelectric vinylidene-fluoride trifluoroethylene copolymer film (VDF-TrFE). The converse piezoelectric effect was then measured by applying an AC signal between the cantilever and bottom electrode, using a lock-in amplifier, amplitude modulation, to observe the phase and amplitude of the polarisation. This converse piezoelectric effect forces a ferroelectric film to contract or expand under applied voltage depending on the orientation of polarisation, see figure 3.5. The resolution in these first experiments was limited to 1 μm, where higher resolution was obtained with topography. They claim that this is due to the fact that van der Waals forces decay much faster with distance than do the electric field forces generated by the AC voltage applied to the cantilever.

With improvements to this technique it was later possible to observe ferroelectric domain patterns on the nano-scale by taking images of amplitude and phase of the local piezoelectric response, Colla et al. [1998] and Gruverman et al. [1996]. Alexe and Gruverman [2004] give a thorough description of PFM and other SFM techniques. Hong et al. [1999] and Hong et al. [2001] give a thorough description of the system we used and modified in this thesis. It is important for the frequency of the applied AC signal to be smaller than the mechanical resonance frequency of the cantilever and the AC voltage must be smaller than the coercive voltage in order to measure the converse piezoelectric effect. The phase shift of this piezoelectric vibration with respect to the phase of the applied AC signal will be around 0 ° or around 180 ° depending on the polarisation orientation. Since in thin ferroelectric films the amplitude of the piezoelectric vibration is extremely small, on the

order of Ås, for correct phase detection a lock-in amplifier is indispensable.

The method of local piezoresponse imaging allows for direct visualisation of the polarisation distribution across the scanned area. Repetitive scans of this area can deliver information about stability of the created pattern and polarisation losses due to back switching and other ferroelectric phenomenon.

3.3.1 Choice of Top Electrode

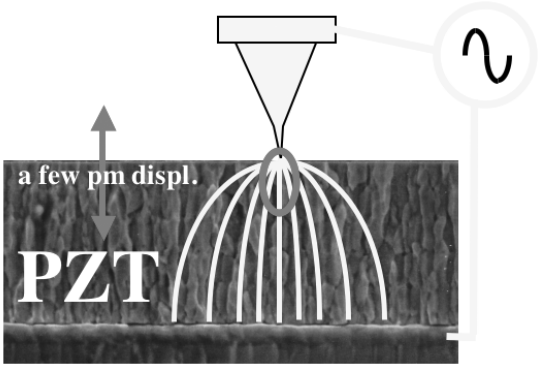


Figure 3.6: The electric field distribution when using a conducting cantilever tip is more difficult to model. This system emits a large field directly underneath the tip, but still can penetrate the ferroelectric film not directly in contact with the AFM tip. (Image courtesy of E. Colla)

There are two different ways to study the piezoresponse of ferroelectric films. The original experiments by Güthner and Dransfeld [1992] were using the configuration as noted in figure 3.6. That is the AC modulation voltage used was applied directly to the cantilever tip and the tip scanned directly the ferroelectric film. When using the configuration of poling the ferroelectric layer directly with the conducting AFM tip care must be taken in analysing these results. This is because the emanating electric field from the conducting cantilever might not penetrate the whole ferroelectric film, Durkan et al. [1999]. Also the electric field distribution from the conducting cantilever is not trivial and can affect areas not directly in contact with the tip, Abplanalp [2001].

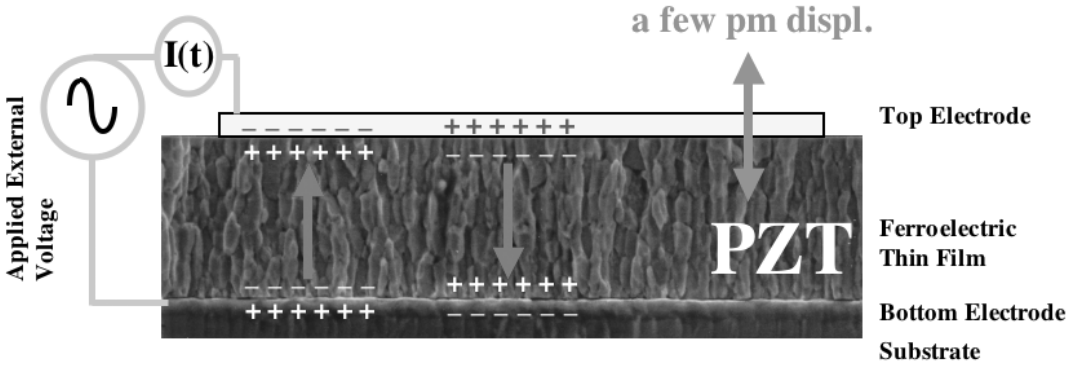


Figure 3.7: The electric field distribution when studying the ferroelectricity through a deposited top electrode is simpler computationally. As it should exhibit a uniform electric field distribution from top electrode to bottom electrode. (Image courtesy of E. Colla)

Later on Colla et al. [1998] wanted to gain further insight into ferroelectric capacitors, that is Pt/PZT/Pt capacitors, and changed the original configuration to that viewed in figure 3.7. In this configuration the AC modulation voltage is still applied directly to the cantilever tip, however the tip is now scanning the top electrode of the ferroelectric layer. Using this setup it was possible to confirm that polarisation suppression occurs region by region, or grain by grain. Also after cycling the capacitor with opposite fields it was possible to observe the fatigue or frozen regions, of dimensions 100 nm-1 μm. When capacitors are designed to such small dimensions this could become important.

When applying the AC modulation voltage to the conductive cantilever tip the voltage seen locally by the ferroelectric layer is much higher than when studying a capacitor structure through its top electrode. Also the electric field distribution in the ferroelectric layer is non-uniform when scanning directly the ferroelectric layer, unlike when studying the capacitor structure which has a uniform linear electric field distribution. Therefore it is not possible to directly compare the poling voltages when poling with the PFM directly on the ferroelectric layer and through a top electrode.

3.3.2 Converse Piezoelectric Effect

The mechanism allowing for the observation of the piezoresponse in a piezoelectric layer with the PFM technique is the converse piezoelectric effect. The converse piezoelectric effect is that an induced strain, S, will be produced in a piezoelectric film with the application of an electric field, E, equation 3.13. Where the constant d_{33} is the converse piezoelectric constant in the vertical direction giving the linear relationship between the electric field and the induced strain.

$$S = \pm d_{33} E \tag{3.13}$$

This strain can be noted in mechanical terms as being equal to the sample deformation in the direction perpendicular to the sample, ΔL, in regards to the sample thickness, L. As all piezoelectric materials exhibit electrostriction, that is a strain is induced with the application of an electric field it is also fitting to express this total strain as the electrostrictive constant, Q, times the square of the total induced polarisation, P, equation 3.14.

$$S = \frac{\Delta L}{L} = Q \times P^2 \tag{3.14}$$

It is important to remember that this change in strain due to the applied electric field has no retention characteristics, that is the film looses this change in strain once the electric field is turned off. PFM imaging can allow for the determining whether a material is piezoelectric or not, but if one wants to investigate if the material is ferroelectric it is important to study the retention characteristics by domain writing, see section 3.3.4.

When making PFM images there is an AC voltage applied, $\mathrm{V} = \mathrm{V}_0 \sin(\omega \mathrm{t} + \theta)$. This alternating voltage induces a small alternating strain in the film which gives rise to a alternating polarisation, δP. Therefore, the total induced polarisation measured can be expressed as in equation 3.15, where $\mathrm{P_f}$ is the total polarisation of the piezoelectric layer.

$$P = P_f + \delta P \tag{3.15}$$

Substituting this expression of the polarisation into equation 3.14 allows to express the induced strain in the piezoelectric layer as in equation 3.16.

$$S = Q({P_f}^2 + 2P_f\delta P + (\delta P)^2) \tag{3.16}$$

A lock-in amplifier is programmed to consider only the first harmonic signal and one is left with equation 3.17. With the help of electronic circuitry and a Labview program it is thus possible to extract a value proportional to the total polarisation and allow for amplitude and phase mapping of this piezoelectric signal.

$$S' = 2QP_f\delta P \tag{3.17}$$

3.3.3 Three Dimensional Measurements

It is possible to make three dimensional polarisation mapping using a four quadrant position sensitive photodetector, PSPD. In the vertical direction of the PSPD it is possible to measure the out of plane polarisation, see figure 3.8a. Also in the vertical direction of the PSPD it is possible to measure the in plane polarisation that lies perpendicular to the horizontal scanning direction of the cantilever, see figure 3.8b. Then in the lateral direction of the PSPD it is possible to measure the in plane polarisation that lies parallel to the horizontal scanning direction of the cantilever, see figure 3.8c. It is possible to create a three-dimensional mapping of this polarisation as has been shown successfully by Eng et al. [1999b] and Rodriguez et al. [2004].

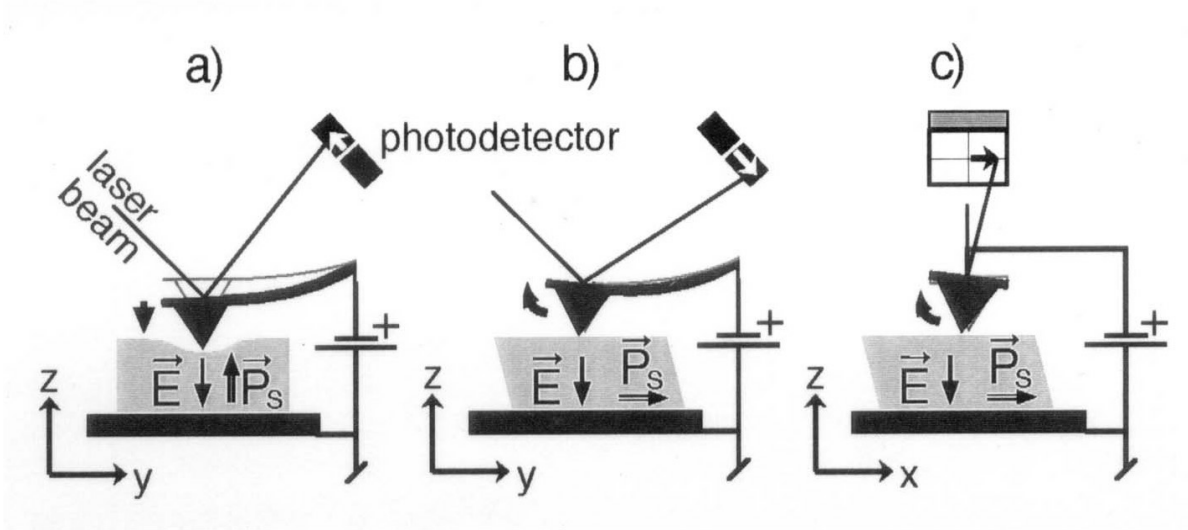


Figure 3.8: Concept of 3D-PFM a) out of plane polarisation can be measured in the vertical PSPD b) in plane polarisation perpendicular to the scan direction can be measured in the vertical PSPD c) in plane polarisation parallel to the scan direction can be measured in the lateral PSPD, Abplanalp [2001].

3.3.4 Domain Writing

The great benefits of using ferroelectrics for domain writing is that they allow for the creation of a reversible, non-destructive process. It is possible in using the Scanning Force Microscope, SFM, to modulate the spontaneous ferroelectric polarisation by using a conductive cantilever with which a biasing DC voltage of either positive or negative is applied locally to the ferroelectric layer. The ferroelectric regions in which the tip of the cantilever has contact with will be poled with the according polarity. The poling of the spontaneous polarisation in the ferroelectric layer can lead to the modulation of the current/resistance in a semiconductor channel. Reading of the modulation of the current in the channel can then be done using electrical measurements. Using the SFM or PFM it is possible to write domains on the nano-meter scale, paving the way for future possibilities in ferroelectric nano-lithography.

3.3.5 Resolution

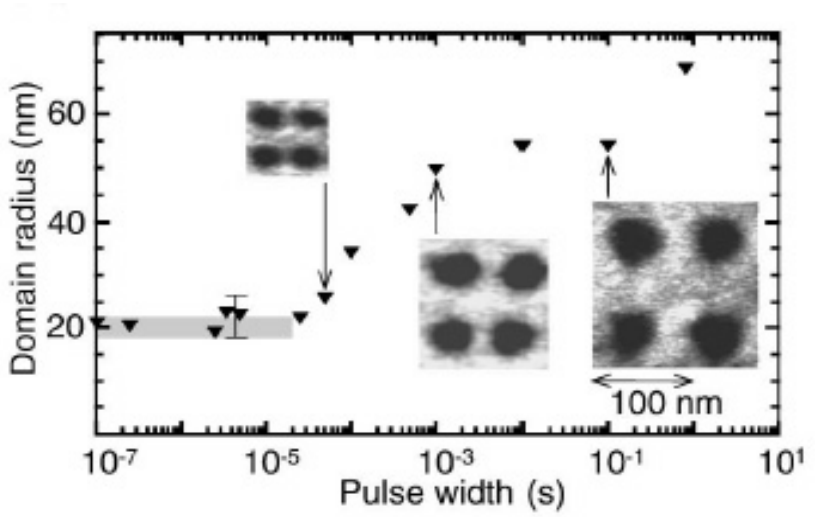


Figure 3.9: The time of the voltage pulse applied to the conductive SFM tip limits the resolution of poling. Once the duration of the voltage pulse is minimised the next factor limiting the resolution is the tip radius, Tybell et al. [2002].

As with the SFM there are many factors contributing to the quality and resolution of the piezoresponse image taken or the domain size written. The piezoresponse image and domain writing depends on the tip radius, frequency of the AC voltage, magnitude of the AC voltage, scanning rate, humidity, pressure and the tip/sample force. Written domain size depends on additional factors such as the sample thickness, transition temperature, crystallography, applied DC electric field, switching time, and cantilever/tip properties, such as the metal coating. Shown in figure 3.9 is that the time of the voltage applied to the conductive SFM tip is one of the limits in writing resolution demonstrated by Tybell et al. [2002]. Epitaxial c-axis oriented $Pb(Zr_{0.2}Ti_{0.8})O_3$ 37 nm thin films were magnetron sputtered onto conducting (100) Nb-doped $SrTiO_3$, the minimum feature size capable of being locally written was the tip radius. To do so a DC voltage of +12 V was used as a biasing voltage. So not only the duration of the biasing voltage pulse was a factor in limiting the minimum feature size but also the radius of the conductive tip radius.

However, the tip radius can be a trade off, not only does it limit the line poled but a larger tip radius gives a larger resistance and therefore a larger field can be applied also the electric field will be more homogeneous. A balancing of many contributing factors is needed in order to obtain the minimum resolution for the sample being measured.

One of the main factors limiting the resolution of both domain imaging and domain writing is the tip radius of the conductive tip. Since usually a non conductive cantilever/tip is micro-fabricated after which a conductive coating is deposited onto it. The use of carbon nanotubes, CNTs, for the use as the scanning tip in conductive SFM methods is being highly researched. The CNTs can be grown in the metallic state possessing conductive properties. Of most importance is that the radius of the CNTs is $0.5 - 3\,\text{nm}$ much less than the traditional conductive SFM tips being used now, Arai et al. [2002], Hudspeth et al. [2002] and Nguyen et al. [2002].

3.3.6 The Setup

A Veeco CP Research atomic force microscope was modified in order to measure the converse piezoelectric effect and apply a large DC bias between the cantilever and a bottom electrode on the sample, figure 3.10. To do this additional circuitry and a Labview program were both designed and developed. This setup was tested with a conventional CSD PZT thin film grown on platinum. It was demonstrated with this sample that it is possible to observe the converse piezoelectric effect, and to locally pole the ferroelectric, PZT, layer, figure 3.11. Piezoresponse measurements will depend on thickness of ferroelectric film, grain size, scanning rate, tip dimensions, tip-sample force, AC modulation voltage and frequency, Abplanalp [2001], Likodimos et al. [2000]. It is assumed that a lower quality of PZT will be deposited on AlGaN/GaN than with PZT deposited on platinum, hence it will be more difficult to observe the converse piezoelectric effect.

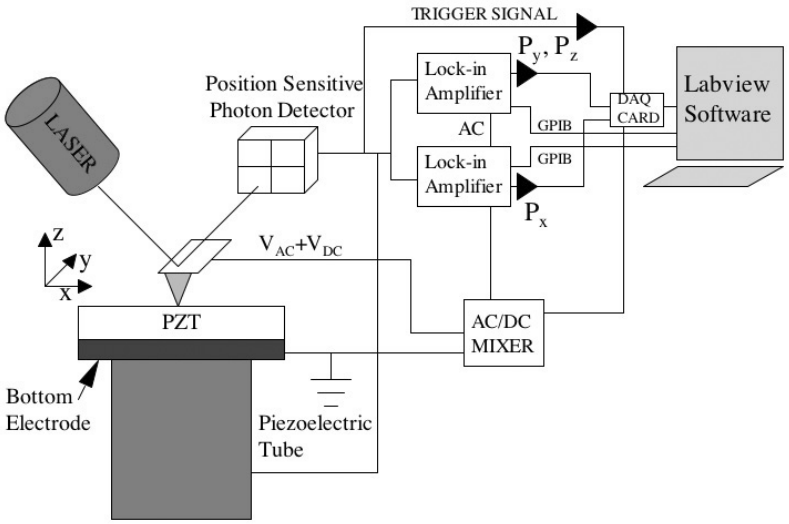


Figure 3.10: PFM setup including most circuitry.

The two ways in which the PFM will be used in this thesis is to show that the polarisation in the ferroelectric film is switchable, capable of retaining the switched polarisation and by

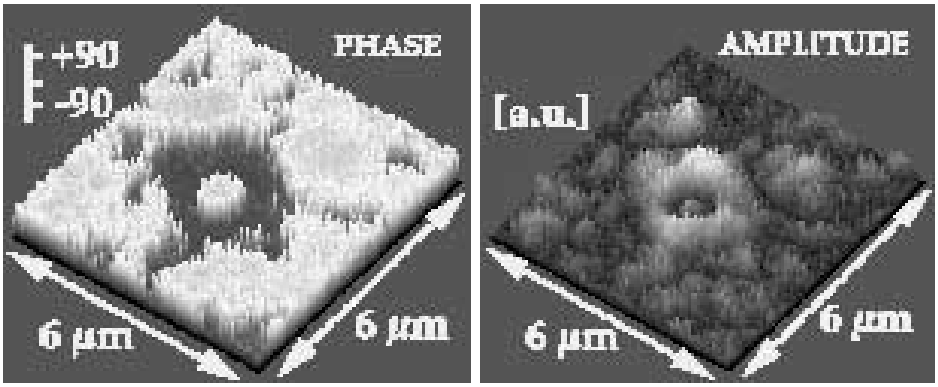


Figure 3.11: Phase and amplitude of the local piezoelectric response measured on the sol gel PZT film after domain writing (data from LC-EPFL, non-published).

poling the active area in the ferroelectric device. Figure 3.12 represents this last scenario of a ferroelectric device structure where the poled region of a PZT film plays the role of gate depleting the 2DEG underneath. This method is advantageous in that no top electrode needs to be deposited onto the PZT creating an electric field distribution that is higher and more local than when using the top electrode configuration. The main concept behind this is that when poling the PZT in the bottom to top orientation a local depletion of the electrons occur. Using directly the PZT layer as the gate could allow for writing of nano-scale patterns in the PZT, these nano-patterns would thus be transferred to the 2DEG in the AlGaN heterostructure. In the case of a bi-stable switchable PZT layer this phenomenon could extend to quantum structure devices, as described in section 1.3.2. Probably the most important obstacle in achieving this is the optimisation of the necessary processing steps and their compatibility.

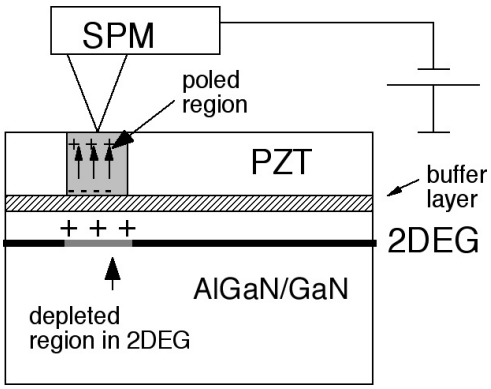


Figure 3.12: The PZT/AlGaN/GaN structure used in this thesis that demonstrates a second method for poling the ferroelectric layer without using a top electrode. This PFM technique allows the PZT layer to be the direct gate to the device and can be used for the local depletion of the 2DEG.

3.4 Ferroelectric Characterisation

3.4.1 P-V Measurements

MFM structure

Polarisation switching can be observed in a ferroelectric hysteresis loop when measured by using a Sawyer-Tower circuit, Sawyer and Tower [1930]. The polarisation is measured by the change in current when applying an AC voltage, at a small frequency, that is varied from 0 V to voltages greater than the coercive field of the ferroelectric being measured. Figure 3.13 shows a typical ferroelectric hysteresis curve for a PZT thin film deposited with the same multiple target magnetron sputtering technique used in this thesis. The remanent polarisation, P_r, is the polarisation at which there is no applied electric field and the coercive field, E_c, is the coercive field in which there is zero net polarisation. For the ideal ferroelectric these values are expected to be symmetric, $+P_r$=-(-P_r) and $+E_c$=-(-E_c). However, there are many factors that do not allow for this symmetry such as film thickness, charged defects, mechanical stresses, and deposition conditions, Damjanovic [1998]. For example in thin films this hysteresis loop is often tilted due to the depolarisation field, Tagantsev et al. [1995]. The PZT film shown in figure 3.13 is not symmetric and has an internal bias field, E_b.

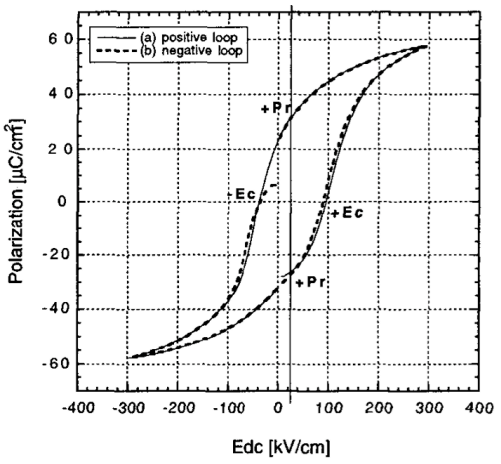


Figure 3.13: Ferroelectric hysteresis loop of 300 nm PZT(45:55) (111) oriented, where the curve is started with a) a positive DC bias and b) a negative DC bias, Hiboux [2002].

Jaffe et al. [1971] summarise very well the fact that ferroelectric hysteresis loops can often be misinterpreted due to assuming that the layers resistance is linear and that its capacitance is non linear. The P-V curve can prove that a layer is ferroelectric: by showing that it is possible to switch the dipole moment of the structure and have it retain this net polarisation. However, it is much better to compliment this measurement with another measurement technique such as observing the Curie temperature, the high dielectric constant and domain structure with PFM. Determining if a layer is ferroelectric or not would be easy if the layer was an insulator due to the fact that all charges are capacitive. However, when the layer is not an insulator it is necessary to determine if the layer possesses non-linear or linear capacitive and dielectric behavior.

MFS structure

The ferroelectric hysteresis curve is instrumental for observing the ferroelectric properties of a ferroelectric sandwiched between two electrodes. However, this is not the case for the samples used in this thesis where it is possible to think of the configuration as metal - ferrroelectric - semiconductor - metal. With this configuration it is no longer so straightforward to observe the ferroelectric switching behavior as the semiconductor impacts this measurement. This is due to the fact that it becomes more difficult to associate what current is a result of the polarisation switching in the ferroelectric layer. If the semiconductor is highly doped and the channel is directly in contact with the ferroelectric layer maybe it would be possible to measure the change in current flow and thus get a ferroelectric hysteresis loop.

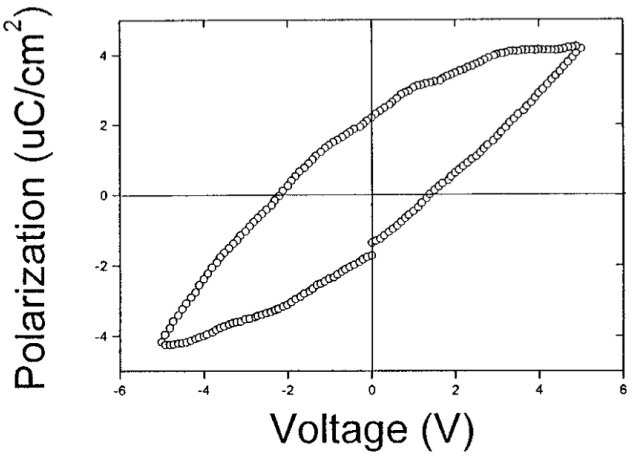


Figure 3.14: Ferroelectric hysteresis loop of 130 nm PZT(53:47) on a n-doped GaN with an electron density of approximately 1x10^{17} electrons/cm^3, Li et al. [1999].

Li et al. [1999] were able to measure a ferroelectric hysteresis loop on a PZT/GaN structure. 130 nm of PZT(53:47) which was deposited by pulsed laser deposition, PLD, onto a thick n-doped GaN layer with a final annealing step at 600 °C. The n-doped GaN layer had an electron density of approximately 1x10^{17} electrons/cm^3 that was directly in contact with the PZT which allowed for making a polarisation hysteresis curve, shown in figure 3.14. However, Jaffe et al. [1971] give a thorough description of when it is necessary to be careful in interpreting the P-V hysteresis curve. Since, if a lossy linear capacitor, with linear dielectric and conduction behavior, is measured it will give the same ellipsoidal curve shown in figure 3.14.

3.4.2 C-V Measurements

MFM structure

Capacitance-Voltage, C-V, curves can also be represented as the relative dielectric permittivity, ϵ_{33}, vs the DC electric field E_{dc}. The C-V curve of a typical PZT thin film deposited with the same magnetron sputtering technique as used in this thesis is shown in figure 3.15, Hiboux [2002]. The butterfly shape that this C-V curve makes is characteristic of ferroelectric films and shows that it is possible to separate intrinsic lattice and extrinsic domain contributions. The maximum capacitance occurs at the coercive field.

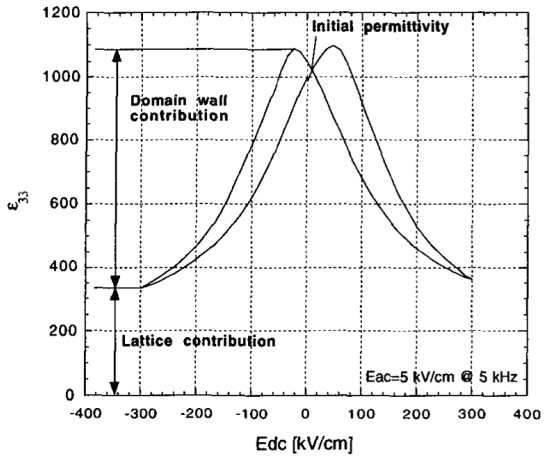


Figure 3.15: Relative permittivity vs gate electric field characteristic of a PZT thin film, Hiboux [2002].

These experiments will be useful in determining if the layer is ferroelectric, whether it switches and partly retains the polarisation when switched. Capacitance-Voltage, C-V, Measurements were performed using a Hewlett Packard 4284A precision LCR meter with an AC voltage frequency range of 20 Hz to 1 MHz. The external DC bias was also applied through this LCR meter. The AC voltage was smaller than the coercive field and the additional DC poling voltage was switching the ferroelectric.

This measurement technique is complementary to the ferroelectric polarisation hysteresis loop measurement, since it is not always possible to apply equation 3.18 to the ferroelectric hysteresis curve in order to obtain the C-V curve, Damjanovic [1998]. This is due to the fact that the dielectric constant is frequency dependent and the P-V curve is usually done at a much smaller frequency than the C-V curve. Also problems in domain switching occur when making C-V measurements due to applying the large DC field that can permanently block the ferroelectric domains, where the AC field supplied by the lock amplifier is not capable to sense them. Only if the sample being measured is a ideal single crystal, will it be possible to apply equation 3.18 and observe equivalent results in the C-V and P-V measurement techniques.

$$\epsilon_f \epsilon_o = \frac{\partial P_f}{\partial E} \tag{3.18}$$

MFS structure

Unlike the ferroelectric hysteresis loops it is possible to measure the C-V curves of ferroelectrics deposited onto semiconductors that are not highly conducting. Shen et al. [2002] pulsed laser deposited, PLD, 400 nm PZT(53:47) onto 75 nm $Al_{0.22}Ga_{0.78}N$/ 3 nm $Al_{0.22}Ga_{0.78}N$/ GaN heterostructure. The C-V curve of this structure while using an aluminium top electrode is shown in figure 3.16. Note that it is not similar to the C-V curve of the ferroelectric layer sandwiched between two metal electrodes as in figure 3.15, but exhibits counter clockwise behavior. The reason for the change in the capacitance is due to the modulation of the electron sheet concentration in the 2DEG with the gate voltage, explained by the simple equation 2.1.

The C-V measurement technique is thus a useful method that allows for both observing if

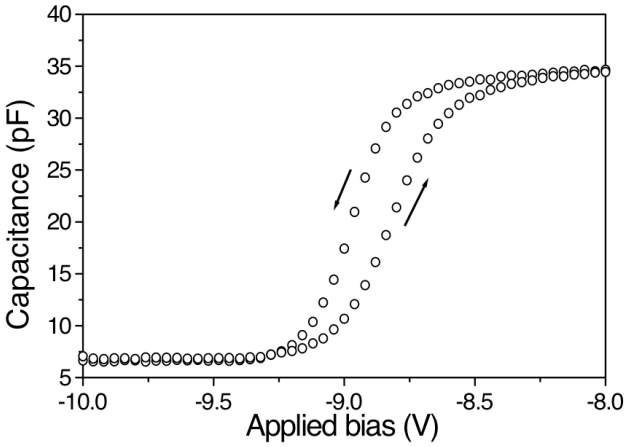


Figure 3.16: Counterclockwise capacitance vs gate voltage curve in a PZT(53:47)/ $Al_{0.22}Ga_{0.78}N$/GaN heterostructure exhibiting ferroelectric behavior, Shen et al. [2002].

the ferroelectric layer is indeed so and if the polarisation induced when the ferroelectric/semiconductor is poled modulates the electrons in the channel or 2DEG. The depletion of electrons is observed by comparing the capacitance at the largest positive applied electric field to the largest negative applied field. If there is a difference in this capacitance it is assumed that there is a depletion of electrons in the 2DEG. The ferroelectricity of the film should be visible from C-V curves, as in figure 3.16 where the curve is counterclockwise due to a retention of the capacitance, when the capacitance is either increased or decreased after obtaining the maximum negative and positive electric field, respectively, see Sze [1985]. If this curve was clockwise this would be an indication of no ferroelectricity in the film due to the observation of absolutely no retention. If a depletion in the channel occurs for a positive DC bias then what was stated above will be reversed: clockwise curves will indicate retention and ferroelectricity, whereas counterclockwise curves indicate no retention and ferroelectricity. C-V curves that do not show a complete cycle of the DC poling voltage do not contain enough information to determine if the thin film is ferroelectric or not, but only indicates if it is possible to modulate the channel with the application of a DC bias. The voltage gap at the average capacitance value in the C-V curve can be considered the memory window of the ferroelectric device, which gives an indication to the retention of the ferroelectric device. This memory window is often dependent on factors as the thickness of the ferroelectric film, largest electric field applied and frequency used for the C-V measurement.

3.5 Material Characterisation

3.5.1 SEM

A high resolution, low accelerating voltage scanning electron microscope, SEM, the Phillips XL30 FEG was used in this thesis. The low voltage functionality is important for measuring the ferroelectric material which has a large band gap, and can lead to a charged surface when the voltage used is too high.

3.5.2 TEM

The Philips CM 300 was used for transmission electron microscope, TEM high resolution images and energy dispersive spectrometry, EDS analysis.

The peaks studied during EDS analysis were:

- Nitrogen peak: 7-N Kα 0.3924 keV
- Oxygen peak: 8-O Kα 0.5249 keV
- Aluminium peak: 13-Al Kα 1.4866 keV
- Titanium peak: 22-Ti Kα 4.5089 keV
- Gallium peak: 31-Ga Lα 1.0979 keV
- Zirconium peak: 40-Zr Kα 15.7473 keV
- Lead peak: 82-Pb Lα 10.5517 keV

3.5.3 X-ray Diffraction

X-ray diffraction was done with a Siemens D500 diffractometer with CuKα radiation source, with a wavelength of 0.15405 nm. The spectra were then compared with the JCPDS file database, the most important files for this thesis are summarised in appendix C.

3.5.4 XPS

X-ray photoelectron spectroscopy, XPS, surface analysis and depth profiling was done with a Kratos AXIS Ultra, XPS spectrometer with monochromator.

3.6 Measurement Flow Diagram

The following list is a description of the task or challenge that needed to be achieved with an appropriate measurement technique to achieve the challenge. The list is in chronological order, that is, the first task was done first and the seventh task last. It was not always possible to follow this measurement flow, however, it is a good guideline for the device verification methods that were needed to be done in order to have a functional working device. As the processing of the ferroelectric/AlGaN devices was highly complicated the failure in one of the earlier steps would eventually lead to the failure of the final device. It is of interest to follow this measurement flow diagram in order to assess any failures of the device fabrication as they occur and not in the last step.

STEP	CHALLENGE	TECHNIQUE
1	Measure the 2DEG before the PZT deposition.	Van der Pauw technique or Hall effect measurement.
2	Observe the survival of the 2DEG after the PZT deposition.	Van der Pauw technique or for Hall bars with the current/voltage, IV, measurement.
3	Observe that the structure, composition and topography of the ferroelectric layer deposited onto AlGaN.	SFM and x-ray diffraction.
4	Observe that the ferroelectric layer deposited onto AlGaN is indeed so.	PFM and C-V measurements.
5	Transport properties of the 2DEG before poling experiments.	Van der Pauw or Hall effect measurement.
6	Switch the ferroelectric layer.	Scanning the active area with the PFM conducting cantilever with a DC bias or for a top electrode a DC voltage is directly applied.
7	Measure the modulation of the transport properties in the 2DEG after poling.	Hall effect and sheet resistance measurements.

Chapter 4

Materials and Processing

The key idea standing behind this project is the local depletion of the electrons in a 2DEG due to the spontaneous polarisation induced in a ferroelectric material. The two principal components required for this system is a semiconductor with one or more heterojunctions and a ferroelectric layer. The first issue to be resolved is the selection of the optimal combination of the heterostructure with the 2DEG and then the selection of the ferroelectric layer. After which, multiple processing techniques need to be chosen and combined constructively in order to optimise the fabrication and design of the ferroelectric/heterostructure device. See figure 4.1 for a cross section of the device, where the ferroelectric layer and top electrode are the two principal layers which will be modified in this thesis.

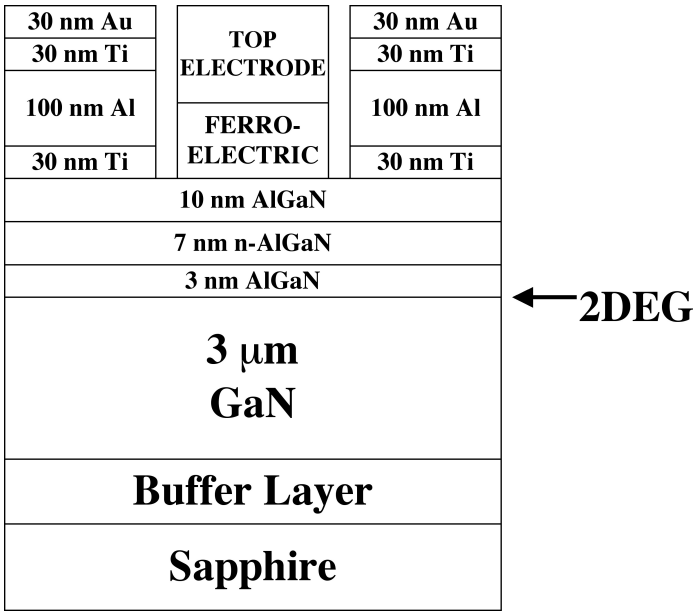


Figure 4.1: Cross Section of the Ferroelectric/Heterostructure Structure

4.1 Material Selection

Discussed here are the materials chosen for this project. The semiconductor heterostructure system AlGaN/GaN was chosen for its temperature and chemical stability. It was also chosen for the transport properties that its 2DEG possess, including a high electron sheet concentration. For the ferroelectric material both conventional lead zirconium titanate, PZT, and the organic polymer poly(vinylidene fluoride/trifluoroethylene), P(VDF/TrFE) were chosen. PZT has the benefits of having a large spontaneous polarisation, approximately $20\,\mu C/cm^2$, to modulate the 2DEG and can be used for devices operating at high temperature. P(VDF/TrFE) has a smaller spontaneous polarisation, $10\,\mu C/cm^2$, but could still be sufficient to modulate the 2DEG, small dielectric constant and a low crystallisation temperature that can possibly better preserve the characteristics of the 2DEG. The characteristics, functionalities, advantages, and disadvantages of the materials chosen will be further discussed.

4.1.1 AlGaN/GaN Heterostructure

In this project the semiconductor heterostructure investigated was chosen to be the system of AlGaN/GaN/sapphire. The choice of the AlGaN/GaN heterostructure presents an important advantage of being a very robust material compared to other semiconductors. The processing temperature of the AlGaN/GaN heterostructure is above 1000 °C, so that the processing temperature of the ferroelectric layer should be less of an issue in this case. The advantage of using a heterostructure with 2DEG over traditional semiconductors is that the 2DEG has higher mobility allowing for the fabrication of high frequency devices. Additionally, in the AlGaN/GaN heterostructures the 2DEG can be formed as close to the surface as 20 nm, see figure 4.1, which could be an important factor for modulating the transport properties of the 2DEG. This could also be a benefit for high-resolution patterning since there is more of a chance that the electric field distribution due to the nano-patterned ferroelectric layer has less chance of extending or broadening its pattern when the distance from the ferroelectric polarisation to the 2DEG is the smallest. AlGaAs/GaAs heterostructures have the advantage that the processing is more developed and more readily available than for GaN and AlGaN. Also they have a 2DEG that exhibits better transport properties than AlGaN/GaN due to a better crystalline quality with better lattice match, fewer dislocations and cleaner interfaces, Schmult et al. [2006]. However, the important thing to note here is that AlGaAs does not have as good chemical and temperature stability as the AlGaN does. Due to the knowledge that the perovskite ferroelectric processing is highly volatile AlGaN is the better choice for this application and high temperature devices.

Gallium Nitride

GaN can have two crystallographic structures: hexagonal-wurtzite structure grown on SiC or sapphire substrates and cubic-zincblende structure grown on Si(001). The structure is either gallium or nitrogen terminated due to growth conditions which can change its chemical and physical properties, but is not an intrinsic property of the structure. For example, Ga-faced GaN can have higher structural quality than N-faced GaN under certain deposition conditions. Ga-faced indicates that the crystallographic direction perpendicu-

lar to the surface is (0001) and when N-faced the crystallographic direction perpendicular to the surface is $(000\bar{1})$. Although this is not always the case, Rodriguez et al. [2002a] used an AlN seeding layer to ensure Ga-faced GaN and when GaN is grown directly on sapphire N-faced GaN was grown, see figure 4.2a.

Piezoelectricity

GaN, in the hexagonal-wurtzite structure is a piezoelectric material, Shur et al. [2000], since the wurtzite structure is non-centrosymmetric. It also possesses spontaneous polarisation, however it does not possess ferroelectric properties since its spontaneous polarisation cannot be reversed. The fact that this crystal structure has a spontaneous polarisation implies that GaN is pyroelectric which is understandable due to the fact that wurtzite is a polar structure where the unit cell possesses a dipole.

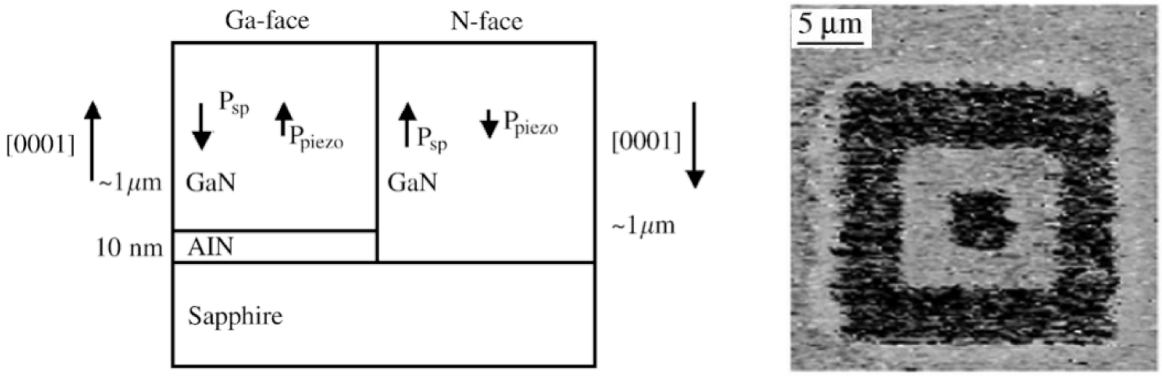


Figure 4.2: a) Cross section of the sample used in order to observe the difference of spontaneous and piezoelectric polarisation in Ga-faced (using AlN seeding layer) and N-faced GaN. b) PFM phase image of the structured GaN where Ga-faced and N-faced GaN are out of phase by approximately 160 °, Rodriguez et al. [2002a].

Rodriguez et al. [2002a] studied GaN samples with PFM, piezoresponse force microscopy (see section 3.3 for more details on this technique). Patterned GaN was grown by PIMBE, plasma induced molecular beam epitaxy using a patterned AlN seeding layer to have both Ga-faced and N-faced structures, see figure 4.2a. According to Rodriguez et al. [2002b] the piezoresponse of the N-faced GaN was measured to be 0.6 pm/V and that of Ga-faced to be 0.3 pm/V. See figure 4.2b for the confirmation, using PFM, that the spontaneous polarisation is in opposite directions depending on whether the GaN is Ga-faced or N-faced.

The values for the spontaneous and piezoelectric polarisations of AlN, GaN and its alloys have been measured and derived by Ambacher et al. [1999]. Using the measured spontaneous polarisation for AlN as $-8.1\,\mu C/cm^2$, and that of GaN as $-2.9\,\mu C/cm^2$, a linear extrapolation gave equation 4.1 for the spontaneous polarisation, P_{SP}, where x is the fraction of aluminium, allowing for the calculation of $Al_{0.3}Ga_{0.7}N$ as $-4.5\,\mu C/cm^2$. In the case of using a $Al_{0.3}Ga_{0.7}N$/GaN heterostructure, where the AlGaN layer is under tensile strain (the case for the sample used in this thesis) the piezoelectric polarisation was calculated to be $-1.1\,\mu C/cm^2$, by Ambacher et al. [1999].

$$P_{SP}(x) = -5.2x - 2.9 \quad [\mu C/cm^2] \tag{4.1}$$

Existence of the 2DEG

It is possible to create a 2DEG in AlGaN/GaN heterostructures through the correct optimisation of the polarity, alloy composition, strain, thickness and doping of the AlGaN barrier, Ambacher et al. [2000]. A two dimensional hole gas can also be created depending on the layering of the nitride layers, and crystalline structure. A 2DEG, is a 2 dimensional surface area of electrons that are quantised in the direction perpendicular to the sample and have random motion in the other two planar directions. The electrons in the 2DEG can then be described by the sheet resistance, R_s, the mobility, μ, and the sheet carrier concentration, n_s. The mobility is the mean drift velocity per unit applied electric field. The current mechanism that is limiting the improvement of AlGaN heterostructures, to have higher mobility, is scattering due to charged surface states, background impurities and charged dislocations, Schmult et al. [2006]. At high temperature this scattering is caused by thermal vibrations whereas at low temperature the scattering is caused by defects in the structure.

Band Bending

The 2DEG can be described in terms of the band bending of the conduction band at the AlGaN/GaN interface, Dimitrijev [2000]. When an AlGaN is deposited onto GaN a triangular potential is always formed at the interface, as seen in figure 4.3. This triangular well is formed due to the ionisation of the electrons in the conduction band of the AlGaN which are attracted and accumulated at the AlGaN/GaN interface due to the induced charge associated with the polarisation of the AlGaN layer. The population of the 2DEG with electrons then forces the fermi energy to be larger than that of the electrons

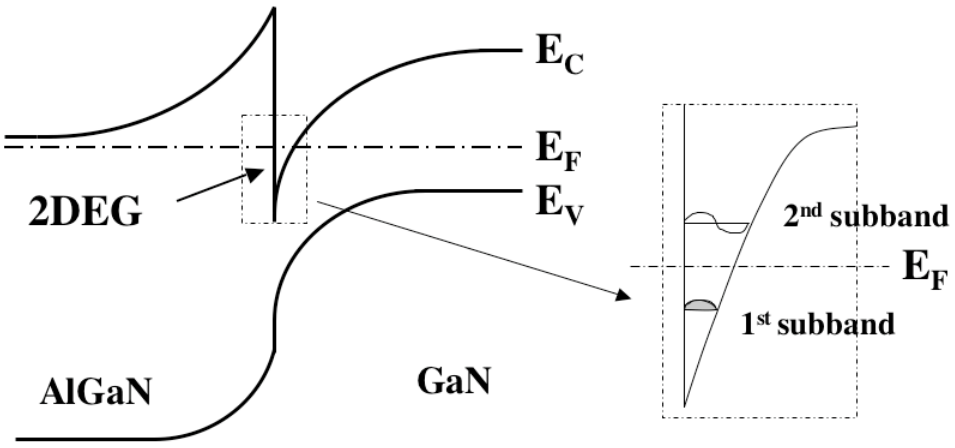


Figure 4.3: Energy band diagram at the AlGaN/GaN interface. In accommodating for the differences in band-gap, and the polarisation of each layer, a well is created that has a high concentration of electrons known as the two dimensional electron gas, 2DEG. Where the electrons are quantised in the direction perpendicular to the sample growth, and populate only the first energy state, of half a wavelength, which is forced to be less than the fermi energy.

The quantisation of the electrons, in the one direction perpendicular to the direction of growth, can be described using this triangular well. In the 2DEG the allowed energy states are quantised where the first energy state is populated with electrons of half a wavelength, the second energy state are populated with electrons of a full wavelength, the third energy state is populated with electrons of three halves of a wavelength and so on. The n_{th} energy state is proportional to n times half a wavelength. However, for a 2DEG only the first energy sub-band is populated by electrons which is forced to have an energy less than the fermi energy of GaN. This implies that there is no need for an electric field to populate the triangular well, or 2DEG. The creation of the 2DEG in the AlGaN/GaN structure, or the quantisation of the electrons in the out of plane direction, exists due to the induced charge associated with the spontaneous and piezoelectric polarisation of each layer. It is important to keep in mind that in the 2DEG the electron is quantised in the one direction however, in the other two planar directions the electrons exhibit random motion.

Polarisation Induced 2DEG

The piezoelectric and spontaneous polarisation of the AlGaN/GaN are thought to be the two mechanisms that create the 2DEG and determine its electron sheet concentration (which changes to a maximum of ±5% with a decrease in the temperature). The spontaneous polarisation is determined by the direction of growth of the GaN-based layers. However, AlGaN and GaN layers can be found in three different strain or piezoelectric polarisation scenarios, Ambacher et al. [2000]. The first is when there is absolutely no strain in the film, therefore no piezoelectric polarisation will be present. When the GaN film is under tensile strain the piezoelectric polarisation will be in the same direction as the spontaneous polarisation of the film. Conversely, when the film is under compressive strain the piezoelectric polarisation is in the direction opposite to the spontaneous polarisation of the film. For the heterostructure used in this thesis where AlGaN is grown on a GaN buffer layer it is under tensile strain, Ambacher et al. [1999], and the piezoelectric polarisation is added to the spontaneous polarisation, see equation 4.2. This forces the direction of the piezoelectric and spontaneous polarisation to be the same (ie. pointing towards the N-face layer), see figure 4.4.

Ambacher et al. [2000] state that the creation of the 2DEG is due to induced charge density, σ, from the spontaneous and piezoelectric polarisation. When σ is positive, free electrons will compensate the induced charge leading to a 2DEG at the AlGaN/GaN interface. Alternatively, when σ is negative free holes will compensate the induced charge leading to a two dimensional hole gas, 2DHG, at the AlGaN/GaN interface. The total induced charge by the spontaneous, P_{SP}, and piezoelectric, P_{PE}, polarisation, equation 4.3 can be thought of in the case of the sample structures shown in figure 4.4. This would lead to equation 4.3 where the total induced charge, $\sigma(P_{PE} + P_{SP})$, is equal to the total polarisation of the bottom layer, $P_{BottomLayer}$, (in our case GaN) minus the total polarisation of the top layer, $P_{TopLayer}$, (in our case AlGaN).

$$P = P_{PE} + P_{SP} \tag{4.2}$$

$$\sigma(P_{PE} + P_{SP}) = P_{BottomLayer} - P_{TopLayer} \tag{4.3}$$

Two cases illustrating the effects of piezoelectric and spontaneous polarisation in the AlGaN/GaN heterostructures are shown in figure 4.4. When the GaN/AlGaN/GaN grown is Ga-faced with tensile strain in the AlGaN layer the crystal structure appears as in figure 4.4a. Since the structure is Ga-faced there is a downward orientation of the spontaneous polarisation, the piezoelectric polarisation is also downward due to tensile strain, and the 2DEG is created at the lower AlGaN/GaN interface, figure 4.4b. Growing an N-faced GaN/AlGaN/GaN structure with tensile strain in the AlGaN layer the crystal structure is shown in figure 4.4c. Figure 4.4d illustrates that the 2DEG for N-faced structures is thus formed at the upper GaN/AlGaN interface. This is due to the upwards orientation of spontaneous polarisation in N-faced GaN and the upwards piezoelectric polarisation in the AlGaN layer under tensile strain. Keep in mind that these two structures are only two possible scenarios of a multitude of combinations that can be deposited.

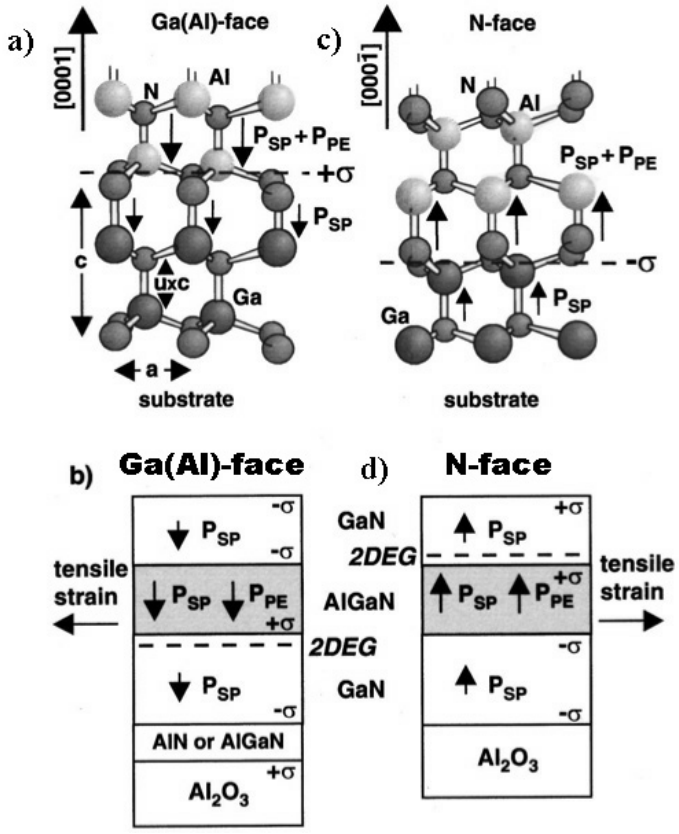


Figure 4.4: The piezoelectric and spontaneous polarisation of the AlGaN/GaN creates the 2DEG, Ambacher et al. [2000]. a) The crystal structure of a Ga-faced wurtzite structure where it is shown in b) that it was Ga-faced due to the AlN seeding layer. c) The crystal structure of a N-faced wurtzite structure where it is shown in d) that it was N-faced due to depositing the GaN directly on the sapphire substrate.

Stutzmann et al. [2002] describe once more the derivation of the 2DEG due to the spontaneous and piezoelectric polarisation in the AlGaN and GaN layers. This concept further extended to explain any charge build up occurring at the GaN/sapphire interface. It is thought that the GaN buffer layer which is normally quite thick, in these experiments $3\,\mu$m, is an effective screening layer due to its intrinsic charge carriers. It can be possible, nevertheless to have accumulation of bound charge at the GaN/sapphire interface due to GaNs spontaneous polarisation. However, an AlN seeding layer can be used to ensure a Ga-faced structure which has better structural qualities than the N-faced structure, possibly limiting this unwanted charge at the sapphire substrate.

Transport Properties

It is important to choose both the heterostructure and the ferroelectric layers in a way that the bound charge associated with the remanent polarisation of the ferroelectric layer is sufficient to influence the electrons in the 2DEG of the heterostructure. To determine this very simple calculations were performed where the sheet concentration, n_s, is equal to the bound charge created by the remanent polarisation of the ferroelectric layer, $\sigma(P_r)$, divided by the electron charge constant, q, see equation 4.4. Which is a simplification to the equation used for n_s by Ambacher et al. [2002] who also take into account the conduction band offset, the fermi level positioning and the Schottky-Barrier contact of the top electrode.

$$n_s = \frac{\sigma(P_r)}{q} \tag{4.4}$$

For example, if using a heterostructure with an electron sheet concentration of $10^{13}\,\mathrm{cm}^{-2}$ in the 2DEG this would correspond to a charge density of $1.6\,\mu\mathrm{C}/\mathrm{cm}^2$, using equation 4.4. The minimum requirement could be considered as using a ferroelectric layer where its remanent polarisation is greater than $2\,\mu\mathrm{C}/\mathrm{cm}^2$, in order to impact the transport properties of the 2DEG. If this remanent polarisation is equivalent to the charge density of the 2DEG there could be a risk that not enough charge associated with the ferroelectric polarisation is available to modulate the transport properties of the 2DEG. It is not fully understood at this point what are the exact requirements on the remanent polarisation of the ferroelectric layer, and thus will be of interest to explore in this thesis.

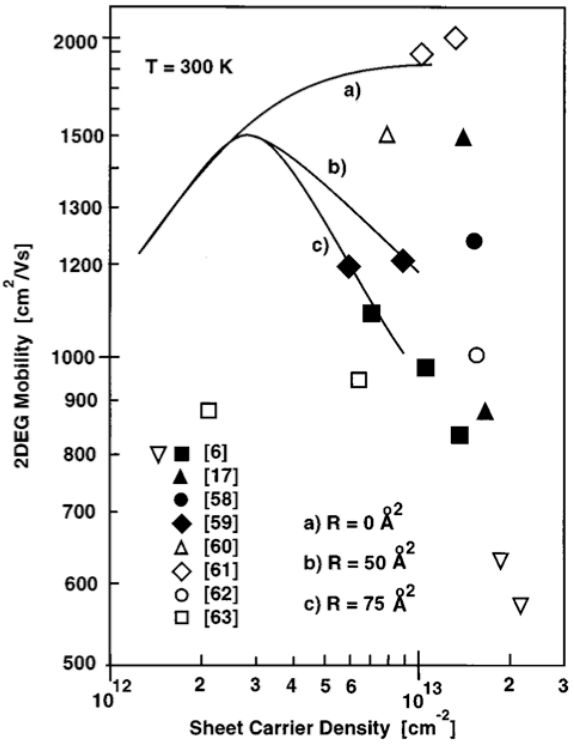


Figure 4.5: Oberhuber et al. [1998] showed the change in μ with n_s for various roughness of the GaN surface, modified image taken from Ambacher et al. [1999].

It has been shown that the mobility of the 2DEG in the AlGaN/GaN heterostructures

depends on many factors, but in general on the crystalline quality of the films. This includes the dependence of the mobility on the surface roughness as shown by Oberhuber et al. [1998], see figure 4.5. Figure 4.5 also includes literature values for μ and n_s of various AlGaN heterostructures; see Ambacher et al. [1999]. Zhong et al. [2002] showed that the mobility of the 2DEGs in their AlGaN heterostructures was constrained not by the rms surface roughness of the film but by the domain size. Zhong et al. [2002] used a sample grown by MOCVD with the following structure 5 nm AlGaN, 10 nm Si doped AlGaN, 3 nm AlGaN, GaN with sapphire substrate with an Al concentration of 33.5 % had transport properties of n_s=1.07x10^{13} cm^{-2} and μ=5000 $^{cm^2}/_{Vs}$ at RT. It has been stated by Zhong et al. [2002] that the mobility is dependent on the dislocation density in the AlGaN and GaN films.

More recently there has been improvement of the deposition of AlGaN and an increase in the mobility of its 2DEG. Some of these samples are summarised in table 4.1, all were grown with plasma assisted molecular beam epitaxy, PAMBE, where the buffer layer of GaN grown on sapphire was deposited with a vapor phase epitaxy technique (HVPE or MOVPE). The best transport properties were observed independently by Schmult et al. [2006] and Manfra et al. [2004] at 300 mK using a magnetic field of 0.6 T. They measured on a $Al_{0.06}Ga_{0.94}N$/GaN heterostructure a 2DEG with mobility of 167000 $^{cm^2}/_{Vs}$ and a electron sheet concentration of 9.1x10^{11} $^{electrons}/_{cm^2}$ at 300 mK. Skierbiszewski et al. [2005] have observed a AlGaN heterostructure where the 2DEG had a electron sheet concentration of 1x10^{12} $^{electrons}/_{cm^2}$ and a mobility of 100000 $^{cm^2}/_{Vs}$ at 4.2 K. It doesn't appear as if these transport properties follow the same trend as was outlined above by Oberhuber et al. [1998], but it is possible for the mobility of the 2DEG to be constrained by multiple factors.

Table 4.1: Literature review of the mobility and sheet concentration of the 2DEG of GaN/AlGaN/GaN/sapphire and AlGaN/GaN/sapphire heterostructures. All samples are grown with PAMBE, except for that by Zhong et al. [2002] which is grown by MOCVD.

Paper	**Al (x)** %	**Temperature** [K]	μ [cm^2/Vs]	$\mathbf{n_s}$ [electrons/cm^2]
Skierbiszewski et al. [2005]	10	RT	2510	2.6x10^{12}
Zhong et al. [2002]	33.5	77K	5000	1.07x10^{13}
Skierbiszewski et al. [2005]	10	4.2	109000	2x10^{12}
Chou et al. [2005]	6	4.2	56000	1.0x10^{12}
Manfra et al. [2004]	6	0.3	167000	9.1x10^{11}
Schmult et al. [2006]	6	0.3	167000	9.1x10^{11}

AlGaN heterostructures have great potential for use in high frequency and high power devices, improving its transport properties increases its multipurpose functionality. Therefore, it is of enormous importance to improve the quality of the 2DEG and increase its transport properties to have larger μ and n_s with lower R_s.

HEMT

The High Electron Mobility Transistor, HEMT, is a transistor that operates at high frequencies with low noise. HEMT's are transistors with a carrier channel of high concen-

tration of electrons that are constrained in the direction perpendicular to the substrate and have random motion in the two planar directions. This carrier channel is known as a two dimensional electron gas, 2DEG, and makes them ideal for some high frequency applications such as satellite receivers and mobile/wireless applications. The 2DEG located at the interface of AlGaN/GaN possess lower mobility than AlGaAs heterostructures, but AlGaN is preferred for high temperature HEMT's, see figure 4.6 for a cross section of an AlGaN/GaN HEMT.

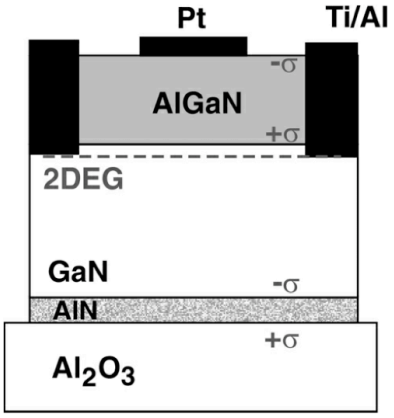


Figure 4.6: The polarisation surface charge induced at the interface of the GaN buffer layer and sapphire substrate should be screened due to the intrinsic charge carriers in the buffer layer, Stutzmann et al. [2002].

Figure 4.6 shows that Ti/Al bottom electrodes are directly deposited onto the AlGaN where the Al of the electrode diffuses down to make an ohmic contact with the 2DEG. These two electrodes can be considered the source and drain electrodes. Then there is a Schottky contact referred to as the gate electrode. When a negative bias is applied to the gate electrode a depletion occurs in the 2DEG which is measured through the current flowing from the source to drain electrodes. This could be thought of as a depletion field effect transistor, FET.

Stutzmann et al. [2002] explain in detail that the conductivity of the 2DEG, or its transport properties, should be highly sensitive to the changes in the surface charge concentration. Therefore, modulation of the electrons from a gate electrode located on the AlGaN surface occurs when applying different bias voltages.

Heterostructure Used

The main problem with the first samples received was that parallel conduction existed at the GaN/sapphire interface. This parallel conduction exists due to the fact that the polarisation surface charge induced at the interface of the GaN buffer layer and sapphire substrate is not completely screened by the intrinsic charge carriers in the buffer layer, Stutzmann et al. [2002], figure 4.6. This parallel current or incomplete screened charge was measured by observing the current flow between etched structures, with depths up to $2\,\mu$m. When there was little current flow between etched structures it was assumed that these samples were good for our experiments. But when the current flow between etched structures was of the same order of magnitude as that flowing through the actual individual device it was deduced that there was parallel conduction at the GaN/sapphire

interface. Due to the fact that this parallel conduction was of the same order of magnitude as the current flowing in the 2DEG it was determined that these samples were insufficient for controlling the changes occurring in the 2DEG as it is not known if one is measuring the 2DEG or the parallel conduction. This parallel conduction was not found in the commercial Cree samples purchased later.

A detailed cross section of the Cree AlGaN/GaN heterostructure used in the following experiments is shown in figure 4.1. All samples used in the following experiments were purchased from Cree, Inc. A two inch (0001) sapphire substrate of 330±50 nm was used. Onto which was deposited by MOCVD, metal-organic chemical vapor deposition, a special thin AlN composite buffer layer, 3 μm un-doped GaN, 3 nm un-doped $Al_{0.3}Ga_{0.7}N$, 7 nm of Si doped $Al_{0.3}Ga_{0.7}N$ (n=3x10^{18} electrons/cm^3), and then a top layer of 10 nm un-doped $Al_{0.3}Ga_{0.7}N$. The structure was Ga-faced.

The Cree Inc. samples came with calibrated sheet resistance values done at room temperature ranging from 410±5 Ω/□ or 417±5 Ω/□. On average all the films provided have an average of 415±10 Ω/□ before processing. Also Cree Inc. states that the 2DEG should have transport properties with $n_s > 1x10^{13}$ electrons/cm^2 and $\mu > 1000$ cm^2/Vs at room temperature. The properties of this 2DEG would correspond to a charge density of 1.6 μC/cm^2 implying that the regular ferroelectrics could be used to modulate this charge as the ferroelectric PZT has a remanent polarisation of 20 μC/cm^2. As discussed above in section 4.1.1 the sheet concentration in this AlGaN heterostructure has the potential to be modulated.

4.1.2 Ferroelectric Layer

The two ferroelectric materials that were investigated are PZT and P(VDF/TrFE). PZT has the benefits of having a large spontaneous polarisation, approximately 20 μC/cm^2, to modulate the 2DEG and can be used for devices operating at high temperature. P(VDF/TrFE) has the benefit of a smaller spontaneous polarisation of 10 μC/cm^2 but could still be sufficient to modulate the 2DEG, and a low crystallisation temperature that can possibly better preserve the characteristics of the 2DEG. Its small dielectric constant of 13 is beneficial in minimising the depolarisation field.

PZT

As for the ferroelectric material, $Pb(Zr_x,Ti_{1-x})O_3$ (PZT) was a straightforward choice since it has relatively low processing temperatures, approximately 570 °C, high remanent polarisation, approximately 20 μC/cm^2, and low coercive field. PZT exhibits nucleation controlled growth, therefore, it is grown using a TiO_2 buffer layer of $2-4$ nm thickness to promote (111) growth of PZT on platinum bottom electrodes, Muralt et al. [1998].

PZT was deposited with two different techniques, initial depositions were done with the chemical solution deposition, CSD, method and final depositions were done using a multiple target sputtering technique. In choosing AlGaN as the heterostructure it was thought that it would sustain the high temperature deposition process of ferroelectrics. Therefore, in choosing the ferroelectric material it was thought to be possible to heat the sample to relatively high temperatures. The crystallisation temperature of PZT is around 600 °C to 700 °C and it was initially thought that the AlGaN could sustain these temperatures without any degradation of its structure and the transport properties of the 2DEG. It was

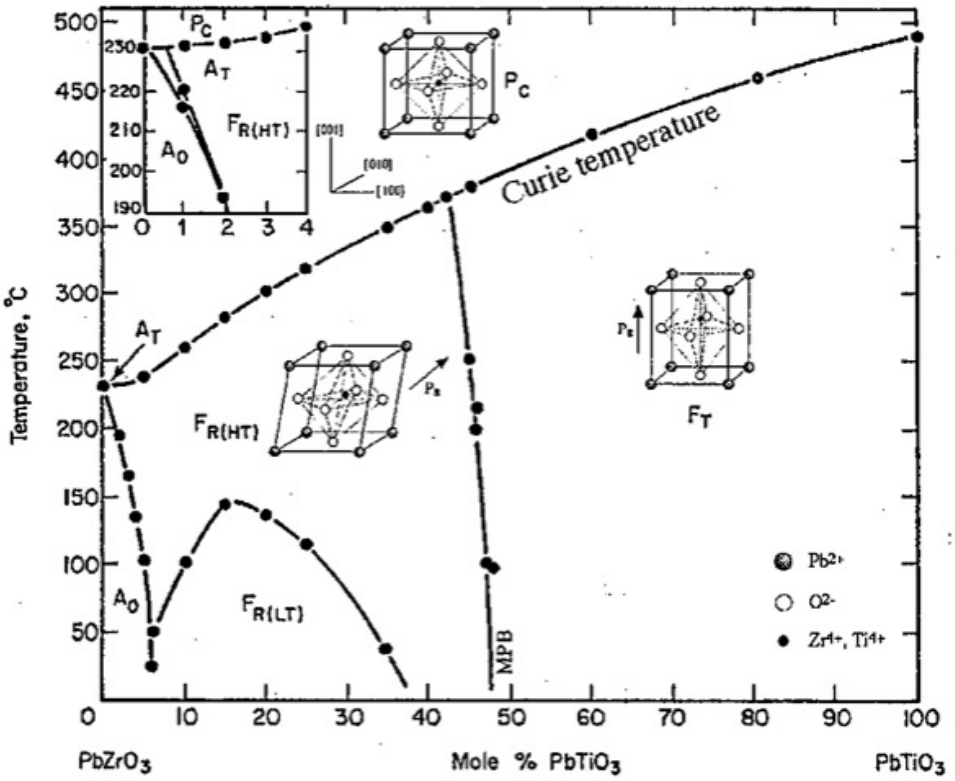


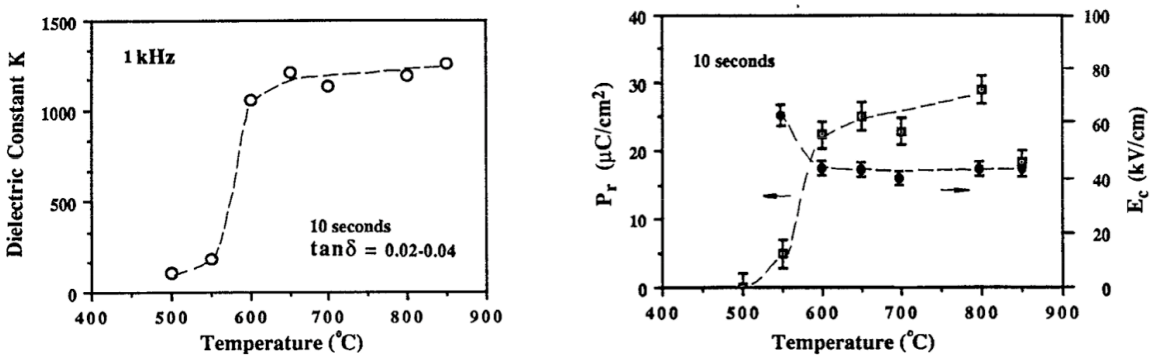
Figure 4.7: Phase diagram of $Pb(Zr_x,Ti_{1-x})O_3$, Jaffe et al. [1971]. The morphotropic phase boundary, MPB, is noted at a composition of 48 % Zr and 52 % Ti at room temperature.

also assumed that there was little need to have a diffusion barrier between AlGaN and PZT, and that the ferroelectric layer could be grown directly on the AlGaN/GaN sample.

PZT was usually deposited at a composition of 40 % Zr and 60 % Ti just below the morphotropic phase boundary, MPB, shown in figure 4.7, due to superior ferroelectric properties. PZT was initially deposited using sol gel methods, however limitations were imposed by the film thickness, high temperature annealing profiles and the large grain size. It was therefore of interest to investigate the growth of PZT on AlGaN by multiple target reactive magnetron sputtering. Sputtering produces thinner PZT films with smaller grain diameters and has less volatile temperature conditions, in comparison to previously developed sol gel methods; both are benefits for high-resolution patterning and the later for the survival of the 2DEG.

CSD PZT

As a reference for CSD PZT thin films one can consult the paper by Chen et al. [1992] who deposited PZT onto a platinum bottom electrode and used a silicon substrate. In this paper they discussed the change of piezoelectric properties of a 400 nm PZT (52:48) layer due to the change in rapid thermal annealing, RTA, parameters. Firstly, the annealing time was optimised at 700 °C to be 10 s when consulting the dielectric constant, remanent polarisation and coercive field measurements. After which, when keeping the annealing time constant at 10 s the minimal temperature for crystallisation of the ferroelectric layer was observed to be 600 °C, see figure 4.8.



(a) (b)

Figure 4.8: Annealing the sol gel PZT thin film for 10 s needs to be done at temperatures above 600 °C. a) The dielectric constant/remanent polarisation vs temperature. b) The coercive field vs temperature. Chen et al. [1992].

CSD PZT Deposition Technique

The PZT layer was deposited for some of the experiments in this thesis with the chemical solution deposition, CSD, technique for PZT(40/60) films. The solution consisted of a specific combination of 2-methoxy ethanol, lead-acetate trihydrate, titanium tetraisopropoxide and zirconium tetraisopropoxide that allowed for the deposition of PZT with composition (40/60). The thickness of about $260 - 280$ nm was ensured with a deposition that was done with 4 spin coatings at 2500 rpm, for 40 s. Pyrolisis took place at 350 °C to remove the solvent. With a final annealing process in a rapid thermal annealer, RTA, occuring at 660 °C for $0.5 - 6$ min in an ambient atmosphere. The annealing step allowed for the crystallisation to the perovskite phase. Further descriptions of the sol gel experiments can be found in section 5.2, where the traditional sol gel deposition method was modified for successful deposition onto the AlGaN heterostructure.

Sputtered PZT

The sputtering system used for depositing the PZT and TiO_2 layers was a multiple target magnetron system imaged in figure 4.9. This multiple target system allows for the deposition of TiO_2 with a direct current, DC, source when the substrate holder is static above the Ti target and sufficient heating is used. In order to deposit PZT the sample holder rotates at a continuous speed while DC biases are applied to both the Zr and Ti target and a radio frequency, RF, bias is applied to the Pb target. It is possible that benefits could be seen if depositing the PZT layer with a single target thus decreasing the maximum temperature needed.

Hiboux [2002] improved the deposition of PZT with the same multi-target RF sputtering technique used in this thesis and shown in figure 4.9. Some of his results will be shown below with a PZT layer of 300 nm. At Zr:Ti ratios of 10:90 and 20:80 the polarisation hysteresis loops did not exhibit normal ferroelectric properties so those results can not be considered since there was no full switching of the PZT layer.

The remanent polarisation increases until the Zr ratio is of 40 % after which the remanent

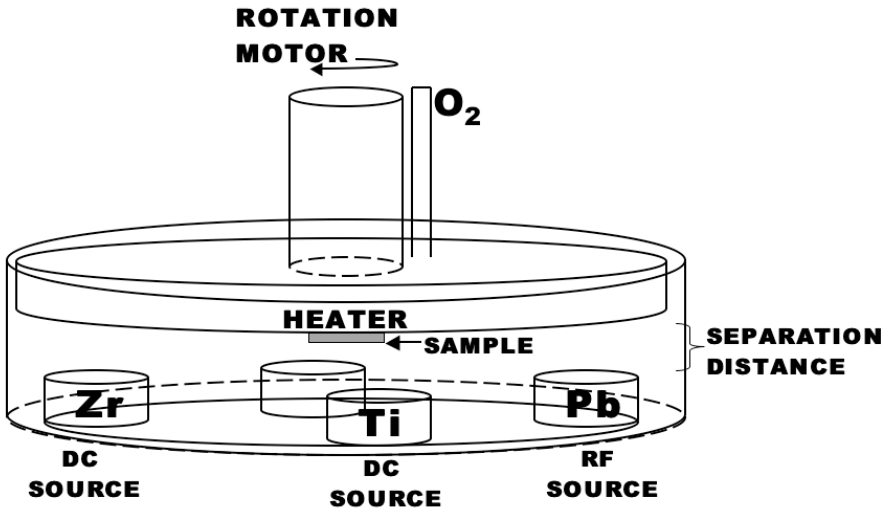
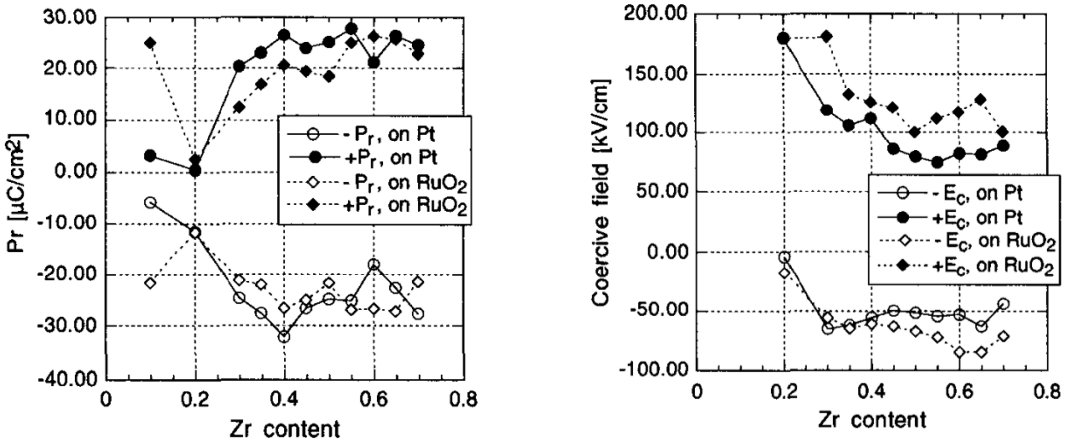


Figure 4.9: Schematic diagram of the multiple target magnetron sputtering machine used for the deposition of PZT and TiO_2, only three of the possible four targets were used.

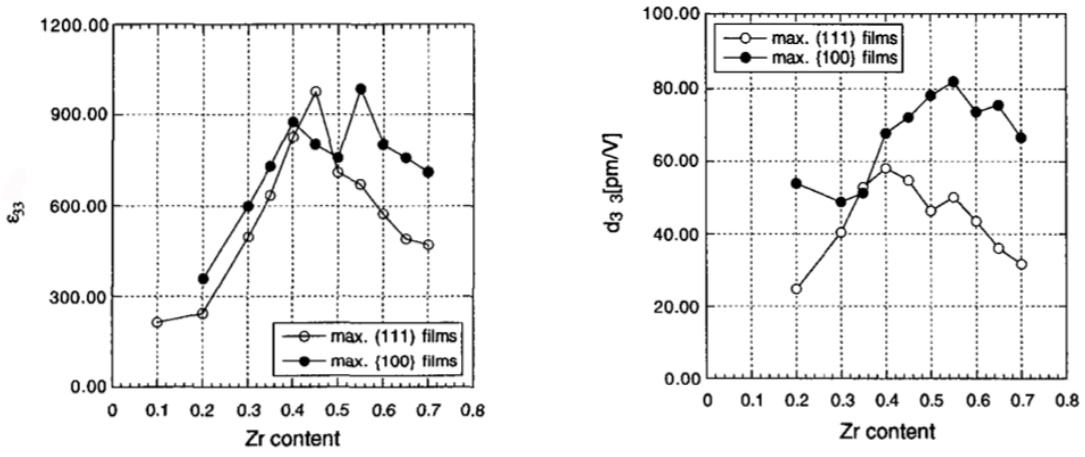
polarisation remains constant, see figure 4.10a. In figure 4.10b the coercive field is minimised when the Zr ratio is of $50 - 55\,\%$ after which it remains constant. The ferroelectric results are superior when using a Pt bottom electrode rather than RuO_2. The relative permittivity is maximised when the Zr ratio is $40 - 45\,\%$, depending on the bottom electrode used, thus indicating where the MPB, morphotropic phase boundary is, see figure 4.11a.



(a) (b)

Figure 4.10: Variations of remanent polarisation and coercive field with Zr:Ti composition when using both Pt and RuO_2 bottom electrodes, Hiboux [2002].

In figure 4.11a it is observed that the relative permittivity is higher in (111) films whereas the saturation polarisation is higher in (100) films. Which implies that higher polarisation can be achieved in (100) films but that the back-switching is stronger than (111) films. The values in figure 4.11 were measured around the coercive field. In figure 4.11b one can observe that d_{33} values are always higher for (100) PZT than for (111) PZT. In summary this implies that PZT films oriented (111) with Zr:Ti composition 40:60 exhibits the



(a) (b)

Figure 4.11: Measured around the coercive field are: a) Variations of ϵ_{33} with Zr:Ti composition. b) Variations of d_{33} with Zr:Ti composition. Hiboux [2002].

best/strongest ferroelectric properties.

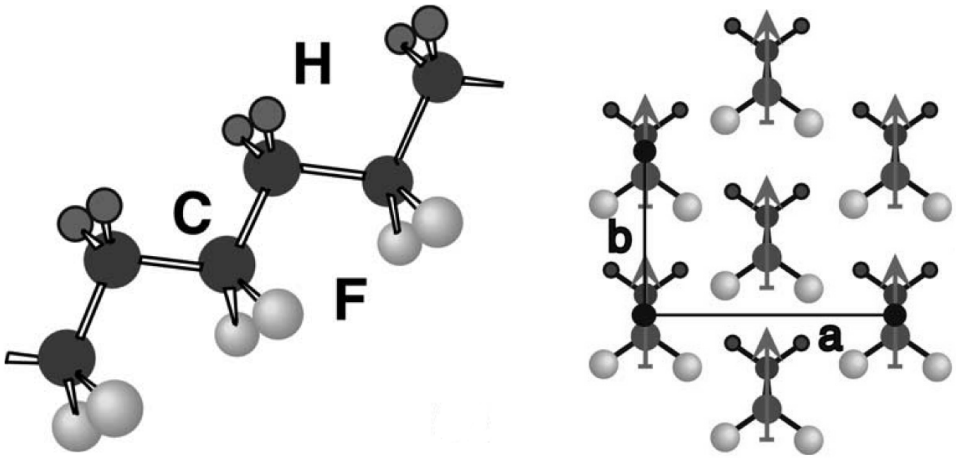
The PZT deposition process used for this thesis is described in detail has been included in appendix A.

P(VDF/TrFE)

Kawai [1969] and Fukada and Takashita [1969] discovered the piezoelectricity in poly(vinylidene fluoride), PVDF, when studying various polymers. Later on Nakamura and Wada [1971], Bergman et al. [1971] and Glass et al. [1971] discovered that this polymer layer, PVDF, also possesses ferroelectric properties. The combination of the ferroelectric polymer PVDF, $[C_2H_2F_2]_n$, with trifluorethylene, TrFE, $[(C_2H_2F_2)_x(C_2HF_3)_{1-x}]_n$, allows for the creation of high quality co-polymer ferroelectric films.

Ducharme et al. [2005] summarises very extensively the advantages and disadvantages of using polymer ferroelectric thin films instead of the more traditional perovskite ferroelectrics. Among the advantages are the low production costs with the ease and flexibility to fabricate various forms of thin film. The polymers also possess such characteristics such as being lead free, high chemical stability and resistance to degradation due to strain defects. The low temperature of crystallisation is one of the largest advantages for combining ferroelectrics with semiconductor and still have a reasonable polarisation of approximately $10\,{}^{\mu C}/_{cm^2}$. However, there also exist disadvantages due to the low melting temperature, low stiffness and the polymorphous structure of solvent-formed samples. Additionally, a disadvantage for the process of devices with PVDF is that it is soluble in organic solvents, of concern is acetone which is commonly used to clean samples after a processing step.

Hasegawa et al. [1972] stated that the PVDF crystal structure is usually orthorhombic but has some tendencies to the hexagonal structure, see figure 4.12. Where the orthorhombic lattice spacings are a=8.58 Å, b=4.91 Å and c(fiber axis)=2.56 Å in the space group Cm2m(C_{2v}^{14}). Ferroelectricity exists due to the net dipole going from the electro-negative fluorine atoms to the electro-positive hydrogen atoms. When an electric field is applied



(a) (b)

Figure 4.12: Structural representation of P(VDF/TrFE) showing a) the carbon chain with attached fluorine and hydrogen atoms and b) the β phase orthorhombic structure with a tendency to the hexagonal structure, Ducharme et al. [2005].

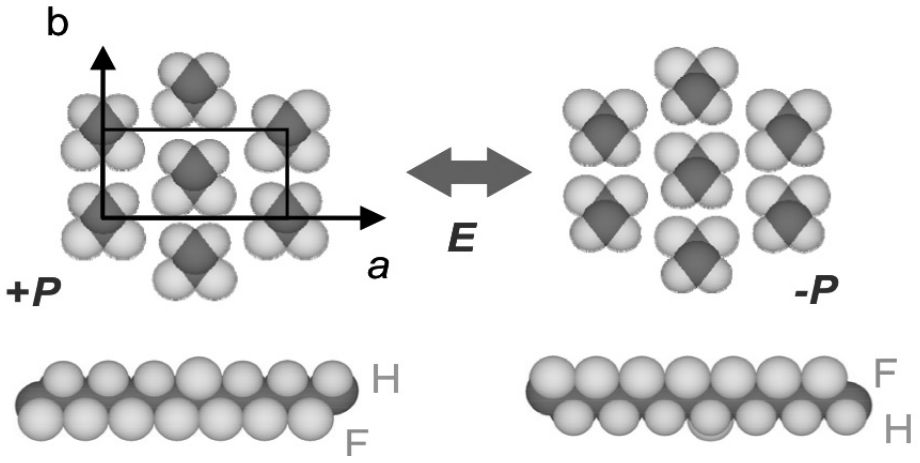


Figure 4.13: Showing the structural change in the P(VDF/TrFE) structure after the application of an electric field causing polarisation reversal, Furukawa et al. [2006]. Viewed in the ab-plane.

the hydrogen and fluorine atoms switch and remain switched (or mirrored in the a-plane) as is shown in figure 4.13.

Kepler and Anderson [1992] describe in detail that a polymer usually crystallises when spherulites are formed by the 10 nm thick lamellae, that are formed by the polymer molecules. Figure 4.14 shows how the polymer molecules are folded so that they penetrate the lamellae many times, while having an orientation perpendicular to the lamellaes surface. The phase of PVDF ferroelectric thin films can be up to one half amorphous and the rest being crystalline.

The technique to deposit the P(VDF/TrFE) in this thesis will be used is the spin casting technique. Another technique to deposit the P(VDF/TrFE) is the Langmuir-Blodgett process which grows thinner films than the spin casting method. However, in regards to this project the thicker films are preferred since they will generate more bound charge to deplete the 2DEG in the AlGaN/GaN heterostructure. Therefore, a summary of current

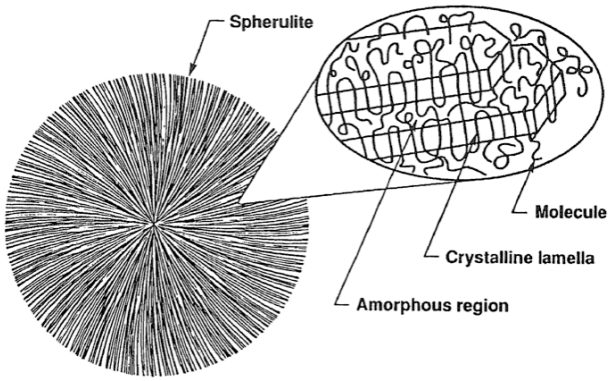


Figure 4.14: Spherulitic morphology showing the crystalline lamella and the amorphous regions, Kepler and Anderson [1992].

results in spin casting P(VDF/TrFE) thin films near room temperature has been done and is summarised in table 4.2.

Table 4.2: P(VDF/TrFE) literature values for coercive field and remanent polarisation at around room temperature.

Paper	**PVDF** [%]	**TrFE** [%]	**thickness** [nm]	P_r [$\mu C/cm^2$]	E_c [MV/cm]
Furukawa et al. [1980]	55	45	11 000	4.5	0.35
Furukawa et al. [1983]	52	48	20 000	7.0	0.40
Kimura and Ohigashi [1986]	75	25	60	10	1.25
Naber et al. [2004]	65	35	65	6.5	0.80
Furukawa et al. [2006]	75	25	260	8.5	0.50
Furukawa et al. [2006]	75	25	27 000	10	0.50

Many different groups have worked on optimising the metal-ferroelectric-metal, MFM, structure in order to obtain the ideal ferroelectric capacitor. Much improvement has been done by Furukawa et al. [2006] since some of their earlier results Furukawa et al. [1980] and Furukawa et al. [1983]. It has been noticed that the use of different electrode materials provide a range of ferroelectric characteristics. One of the main improvements is that the ferroelectric coercive field is now not order of magnitudes larger when using thinner films Naber et al. [2004]

P(VDF/TrFE) Deposition Technique

The P(VDF/TrFE) in this thesis was deposited with a spin casting technique in cyclohexanone with a volume ratio of (1:20). The spin parameters for the deposition were spin speed of 1500 rpm for a time of 1 min. After the spin, crystallisation of the P(VDF/TrFE) was induced in an annealing process on a hot plate at a temperature of $128 - 130\,^{\circ}C$ for 3 min in ambient conditions. The measured thickness of these films is 250 ± 10 nm. Thinner P(VDF/TrFE) ferroelectric films can be deposited using the Langmuir-Blodgett approach, Ducharme et al. [2005], which have a smaller operational voltage that is more suitable for integration with CMOS based devices. However, for the use in this thesis the

thicker P(VDF/TrFE) ferroelectric layer was used as a large enough polarisation is needed in order to accumulate enough bound charge at the semiconductor interface in order to deplete the 2DEG of its electrons. The pellets that were dissolved in cylclohexanone were purchased from Solvay-Solexis, its characteristics are summarised in table 4.3. What will be extremely important in the future processing of devices is that the melting temperature is quite low at 154.5 °C, which could impede the use of negative photoresists.

Table 4.3: P(VDF/TrFE) data sheet provided from Solexis.

VF2	70 % mol.
TRFE	30 % mol.
Melt Flow Index at 230 °C and 5 kg	(1.9 $^{g}/_{10min}$)
melting temperature	154.5 °C
ΔH_f	30 $^{J}/_{g}$
$T_{crystallisation}$	129 °C
T_{curie}	106 °C
Tensile Modulus	1350 MPa
ϵ_r at 50 °C and 1000 Hz	13

4.2 Processing

4.2.1 Ohmic Bottom Electrode

Ohmic/Schottky electrodes were deposited to make contact with the 2DEG in the AlGaN/GaN heterostructure. Using a Ti/Al/Ti/Au sandwich, Motayed et al. [2003] successfully had ohmic contact with the 2DEG after annealing at high temperatures. Annealing of the electrodes is not possible in our configuration and might not be necessary. Here 30/100/30/30 nm electrodes, deposited by electron beam, created good quality Schottky contacts without annealing at high temperatures.

The best way to assess the quality of the electrodes to the 2DEG in the AlGaN heterostructure is to use the transmission line method, TLM, setup as shown in figure 4.15. This setup allows the contact resistance R_c to be extrapolated after making a series of IV curves, Reeves and Harrison [1982]. A resistance versus electrode separation distance curve is plotted and extrapolated to a distance of zero. The resistance calculated here is equal to twice R_c.

A Hall bar structure was designed without PZT to observe the transport properties of the 2DEG in the AlGaN heterostructure, see section 3.1 for more details on this technique. That is a Hall bar structure was etched using the electron cyclotron resonance reactive ion etching, ECR-RIE, technique described in section 4.2.4 and Ti/Al/Ti/Au electrodes were deposited and annealed at 700 °C for 30 s. The Hall bar measurements gave values of $R_s = 431\ ^{\Omega}/_{\square}$, $n_s = 1.15\text{x}10^{13}\ ^{electrons}/_{cm^2}$ and $\mu = 1260\ ^{cm^2}/_{Vs}$. These values are within experimental error of the data supplied to us from Cree, Inc., therefore since the AlGaN samples are extremely expensive no TLM measurements were done in order to minimise the contact resistance.

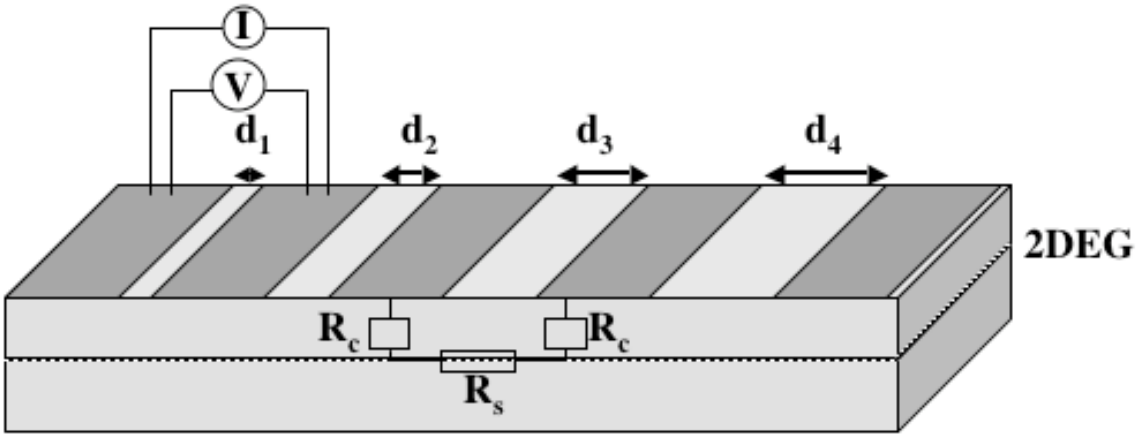


Figure 4.15: Transmission Line Measurements are done with multiple electrodes in series on a rectangular etched semiconductor.

The PZT can henceforth be deposited first and then the annealing of the bottom electrodes can be done, see figure 4.16.

4.2.2 Gate Electrode

Gate Electrode for PZT

Since top electrodes for PZT has already been investigated, Baborowski [2004], thus making the choice for the optimal top electrode for this device simple. Standard Pt electrodes usually give the best results, however there are many inconveniences to using them for this device. The main problem is due to the fact that they are deposited using PVD, magnetron sputtering technique after which a high temperature annealing is necessary in order to restore the Pt/PZT interface and to re-crystallize the Pt. It is absolutely critical that all unnecessary annealing steps are reduced since annealing in oxygen will cause the bottom electrodes to oxidise and lose their ohmic contact properties with the 2DEG, also high temperature processes can cause the PZT to further diffuse into the AlGaN and potentially into the GaN reducing the transport characteristics of the 2DEG. Also an additional processing step of dry etching needs to be done in order to pattern the electrodes, further damaging the side walls of the PZT by ion bombardment, making again the post-annealing treatment an important fabrication step. Therefore it was chosen to use Au(100 nm/Cr(10 nm)) electrodes due to the fact that these two metals can be deposited using electron-beam evaporation, making it possible to get high resolution structures in a one processing step by lift-off technique. Most importantly is that during the electron-beam evaporation there is no ion bombardment of our sample making a post-annealing treatment unnecessary.

Gate Electrode to P(VDF/TrFE)

There were different electrodes used as the gate contact to the P(VDF/TrFE) ferroelectric layer. Firstly, chrome electrodes of 100 nm were used but this did not create a good external contact. Therefore both Au/Cr 100/10 nm electrodes deposited by electron beam

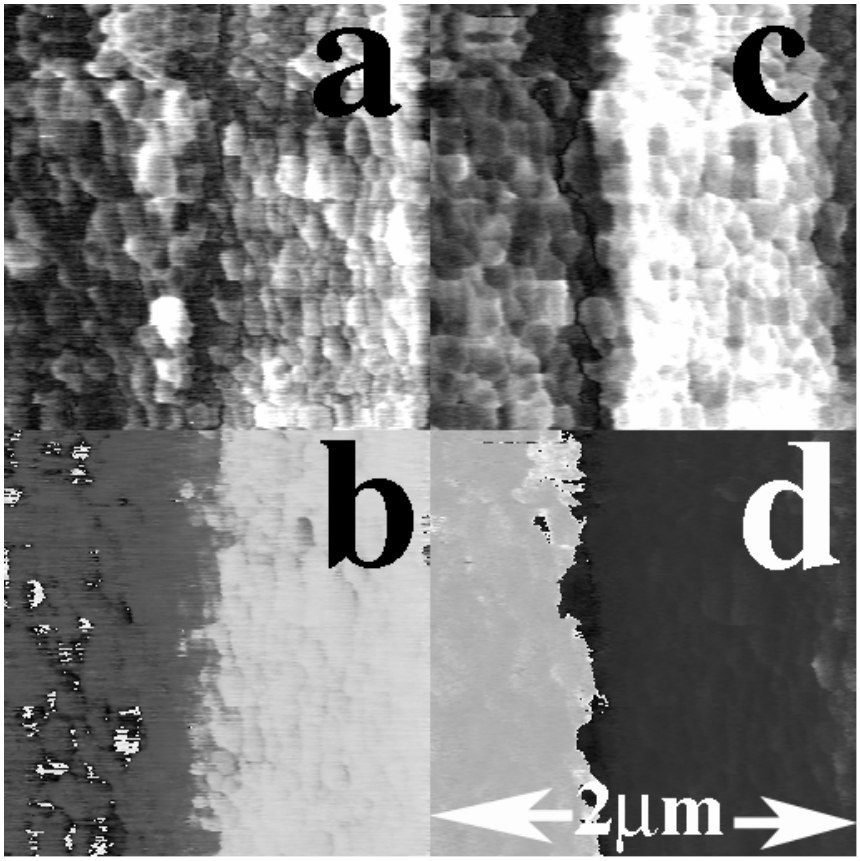


Figure 4.16: a) Vertical amplitude, b) vertical phase, c) lateral amplitude, and d) lateral phase of the PFM images when poled −30 V on the left side and +30 V on the right side with the conducting cantilever. This poling shows retention and concludes that the PZT can sustain nitrogen annealing.

evaporation and 100 nm Au electrodes deposited by joule effect evaporation. The Au electrodes could be easily structured with a wet etching solution of KI, I_2 and H_2O. Aluminium electrodes, of 100 nm, deposited by electron beam evaporation were also tried as they are reported to make a chemical reaction with the fluoro-polymer, P(VDF/TrFE), preventing diffusion, Wu et al. [1994], Chen and Mukhopadhyay [1995] and Xia and Zhang [2004]. The aluminium electrodes could easily be patterned with a wet etching solution of ANP. Where ANP is a chemical solution of the ratio 5:3:75 of acetic acid, CH_3COOH 100%, nitric acid, HNO_3 70%, phosphoric acid, H_3PO_4 85%.

4.2.3 Wet Etching of PZT

The techniques of both dry and wet etching of the PZT grown on AlGaN/GaN were investigated. Both techniques are well developed and successfully used in the laboratory of ceramics. Wet etching produced problems in lateral over-etching as the solution is isotropic; this is difficult to compensate in mask design. Wet etching of PZT is used to etch out holes in the PZT layer to create a window in order to deposit ohmic electrodes to the 2DEG. For the mesa structure a new technique was developed to simultaneously etch both PZT and AlGaN/GaN in one step, see the below sub-section for further details. The wet etching solution used is 30 mL of 32 % hydrochloric acid, HCl, 5 drops of 40 % hydrofluoric acid, HF, and 70 mL of water, H_2O. It can also be said that the final solution

has a concentration of 9.4 % HCl, and 1 % HF and 89.6 % H_2O.

4.2.4 Dry Etching of PZT/AlGaN/GaN

AlGaN/GaN dry etching has been done successfully by Kao et al. [2004] using inductively coupled plasma reactive ion etching. In this study it was shown that it is possible to anisotropically etch AlGaN/GaN with an etched surface root mean square roughness value of about 0.2 nm. Also shown was that there was an increase of surface roughness (due to ion bombardment) above the saturated bias power of 200 W where the dislocation density and the number of pits increased.

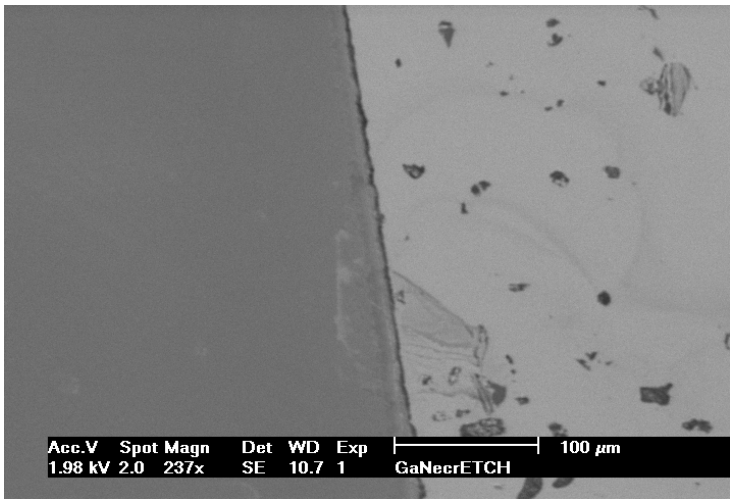


Figure 4.17: A SEM top view of the AlGaN/GaN heterostructrure after having been etched and PZT removed, where a clear step is visibly etched into the semiconductor.

Although the above method might give high etching rates and small aspect ratios, it is necessary also to optimise our device design. Therefore, the same dry etching electron cyclotron resonance reactive ion etching, ECR-RIE, setup, as previously used for PZT by Baborowski et al. [2000], was tested in its etching capabilities of AlGaN/GaN. Previous attempts to etch GaN with ECR-RIE were done with plasma chemistries of: $Cl_2/CH_4/H_2/Ar$, BCl_3/Ar, Cl_2/H_2, Cl_2/H_2, Cl_2/SF_6/ HBr/H_2 and HI/H_2, see Pearton et al. [1997] for a review of such methods. These methods have etching rates from $40 - 310\,^{\mathrm{nm}}/_{\mathrm{min}}$.

Table 4.4 gives a summary of multiple etching conditions used to etch a 300 nm PZT/AlGaN structure. The best etching conditions with which to etch the PZT/AlGaN/GaN structure, in the ECR-RIE, is with a plasma chemistry of $Ar{:}CCl_4 : CF_4$ at a ratio of 2:3:3 and a total flow rate of 20 sccm. The overall etching rate of this structure is approximately $30\,^{\mathrm{nm}}/_{\mathrm{min}}$. The main advantage of this technique is one step processing (i.e. one mask/alignment) improving the alignment of the sidewalls of the PZT layer to the AlGaN/GaN structure. The main drawback of this technique is a large aspect ratio of 1:1, this could imply that PZT does not cover all of the 2DEG which could create channels for leakage current.

Table 4.4: Dry etching conditions for PZT/AlGaN/GaN structure at an RF power of 50 W and an accelerating voltage of 200 V and a beam voltage of 200 V.

Ar [sccm]	CCl_4 [sccm]	CF_4 [sccm]	O_2 [sccm]	**Etch Rate** [nm/min]	**Side Walls** [°]
3.75	7.5	7.5	0	27.4	no
5	7.5	7.5	1	30	45.9
5	15	15	0	26.7	45
5	15	0	0	30.6	60.2
5	0	15	0	26.7	64.8
5	0	0	0	0	0
15	15	15	1	26	36.9
10	15	15	0	33.7	38.7
0	15	15	1	24.4	31.3

4.2.5 Focused Ion Beam, FIB

Preliminary experiments showed that it is possible to finely structure PZT/AlGaN/GaN devices through focused ion beam with a resolution of approximately 130 nm, see figure 4.18. This is an option to create a pattern of nano-resolution with sidewalls of good aspect ratio. Previous experiments done by Stanishevsky et al. [2002] investigated the radiation damage in PZT after using FIB. For their experiments a focused beam of 50 keV Ga^+ ions was used to pattern 100 nm square capacitors. The surface layer was significantly damaged due to the loss of lead and oxygen. A substantial increase in leakage current was found after FIB patterning, this leakage current could be reduced by annealing in oxygen for 30 min at 400 °C. Unfortunately, the ferroelectric hysteresis loops were significantly degraded with the FIB; these properties could not be restored with annealing but only slightly improved, see figure 4.19. To continue using the FIB technique to nano-structure devices, further experiments to reduce surface degradation need to be done.

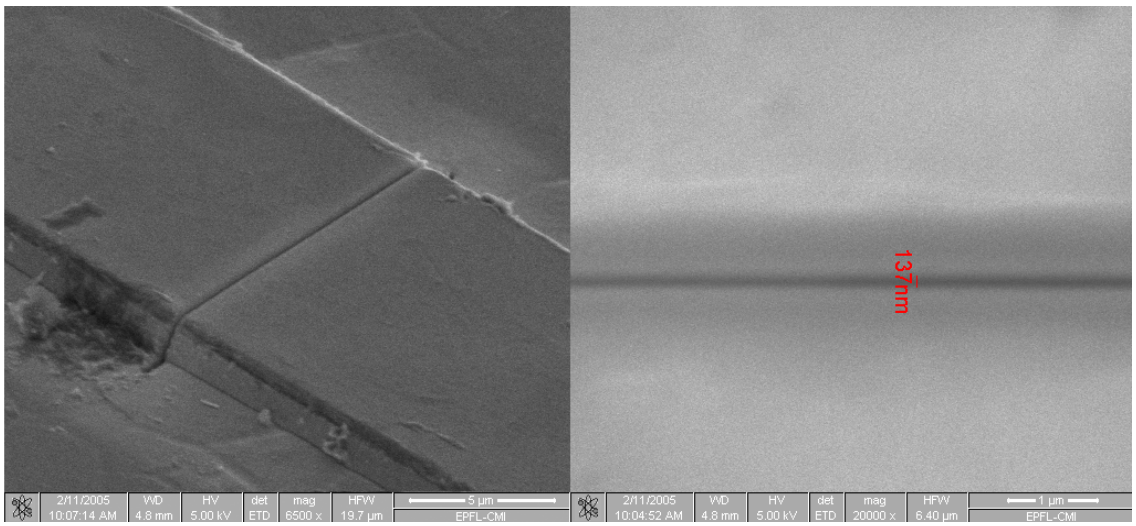


Figure 4.18: FIB cut in the PZT/AlGaN/GaN structure.

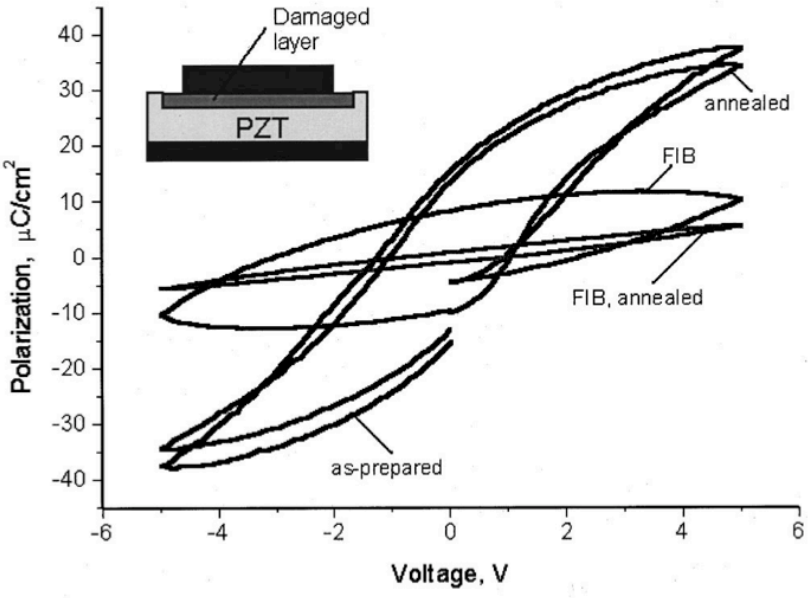


Figure 4.19: Showing the hysteresis loops of a PZT layer as deposited, after annealing, after FIB and after a final annealing, Stanishevsky et al. [2002]. Permanent degradation of the hysteresis characteristics occur after FIB processing.

4.3 Device Fabrication

The biggest challenge in obtaining a ferroelectric gate or ferroelectric transistor is the optimisation of each and every processing step. However, it is also necessary to be able to combine all of these steps in-order to preserve the characteristics that each material has in its optimal conditions. Such as maintaining the ferroelectric characteristics that the ferroelectric layer has on a metallic bottom electrode when depositing the ferroelectric layer onto AlGaN. Also important in this project is to maintain the excellent transport properties of the 2DEG at the AlGaN/GaN interface and the capability to measure the 2DEG with good ohmic contacts.

Three different structures were fabricated. A Hall bar structure of 200x50 μm^2 for direct poling with the PFM. A Hall bar structure of 1000x200 μm^2 for poling with a top electrode. Also a van der Pauw structure of 1x1 cm^2 with top electrode was fabricated with a top electrode to facilitate processing.

The processing steps for PZT deposited by the sputter method and the sol gel method are similar except for the process unique to their methods.

4.3.1 PZT Device Fabrication

Initially, the annealing of the bottom electrodes in nitrogen was not thought necessary. Unfortunately, when using the AlGaN sample with 30 % aluminum content annealing of the electrodes in nitrogen at 700 °C for 30 s was necessary in order to minimise the contact resistance that the electrodes made to the 2DEG. It is due to this that these samples were made in following the fabrication steps listed below, as the annealing had to be done in retrospect. If chance were to come to remake some devices, annealing of the electrodes in nitrogen would come as one of the first steps as described later in section 4.3.2.

STEP 1

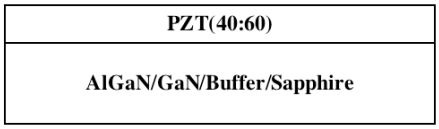


Figure 4.20:

The first step as shown in figure 4.20 is the deposition of the PZT ferroelectric layer including the ultra-thin TiO_2 seeding layer. PZT is deposited uniformly on the AlGaN layer.

STEP 2

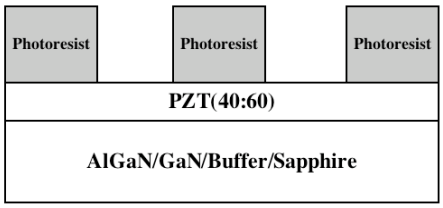


Figure 4.21:

The positive photoresist was deposited and exposure was done such to leave windows open large enough for where the bottom electrodes will be deposited, see figure 4.21.

STEP 3

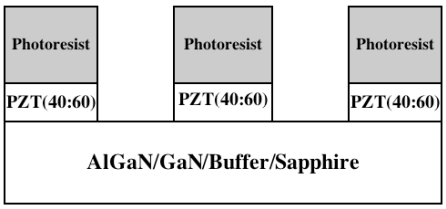


Figure 4.22:

However, as is obvious from figure 4.21 the PZT was first wet etched in order to make an access to the AlGaN layer. The PZT wet etch solution as described in section 4.2.3 also removes the TiO_2 seeding layer. Most importantly is that AlGaN and GaN are not chemically affected by the wet etching solution of PZT, see figure 4.22. The PZT is wet etched where the bottom electrodes will be deposited.

STEP 4

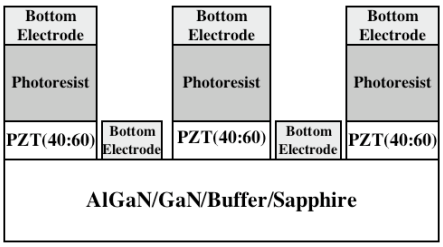


Figure 4.23:

Now that access to the AlGaN layer has been made the bottom electrodes were deposited and the lift-off technique was used, see figure 4.23. The benefit of this technique is that multiple processes were able to be done with one positive photoresist layer. Allowing for a great accuracy and precision that would be un-accomplishable with the use two separate photoresist processes.

STEP 5

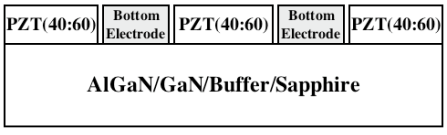


Figure 4.24:

The end of the lift-off process for the bottom electrodes. In figure 4.24 one sees the cross section after the completion of the lift-off process. Annealing of the electrodes was not done here but at a later step.

STEP 6

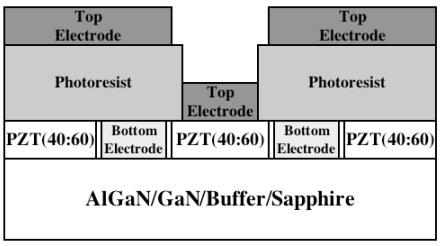


Figure 4.25:

Figure 4.25 demonstrates the 2nd lift-off process, this one for the top electrode. The positive photoresist is put on ready for the lift off process of the top electrode.

STEP 7

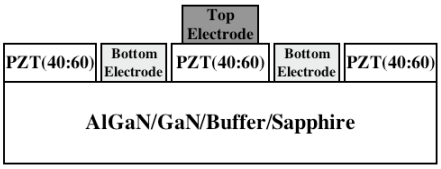


Figure 4.26:

At the completion of the lift-off process for the top electrode to the PZT the structure is as appears in figure 4.26.

STEP 8

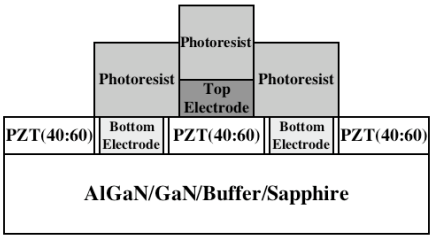


Figure 4.27:

Now the final positive resist is deposited, illuminated and developed for the MESA structure or Hall bar structure used in these experiments, see figure 4.27.

STEP 9

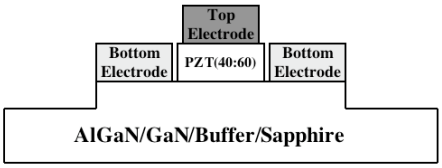


Figure 4.28:

Finally the last step of etching the Hall bar structure is done, all photoresist is removed in acetone and one is left with what is seen in figure 4.28. This step is beneficial in that the dry etching recipe used etches both the PZT, AlGaN and GaN at an acceptable rate. Minimising once more the amount of alignment steps that are necessary for obtaining a final device structure.

4.3.2 Possible Ideal Fabrication of PZT Device

In retrospect a processing scheme such as the one presented in this section could be the most beneficial for the fabrication of PZT gate devices. The reason for this is that the PZT has no chance to degrade since it is not annealed in nitrogen at 700 °C and the bottom electrodes are annealed using the optimal condition of annealing in nitrogen at 700 °C for 30 s as one of the first steps. Unfortunately, it was not possible to follow this sequence of process steps since the magnetron sputtering machine had technical problems. It would be interesting to see if it is possible to obtain superior results than those obtained and mentioned in the results section. Of most importance would be to check that the bottom electrodes are still as ohmic after the PZT deposition process as before. Keep in mind that the ohmic contact is created by the diffusion of the aluminium to the 2DEG and the gold layer is for external contact only. Now if PZT is deposited on top of this electrode in an oxygen atmosphere how will it affect this bottom electrode? This is the important question that would need to be answered.

STEP 1

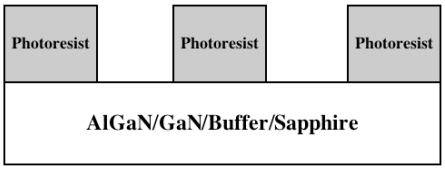


Figure 4.29:

Positive photoresist is spun on, illuminated and developed such that holes are left for the deposition of the bottom electrodes, see figure 4.29.

STEP 2

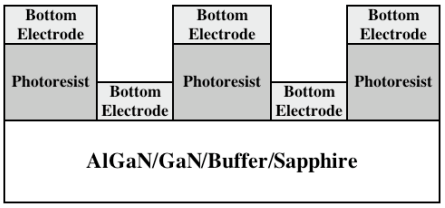


Figure 4.30:

Bottom electrodes are deposited using the lift-off process, see figure 4.30. Keeping the area that will have the ferroelectric layer on it untouched, more specifically without any unwanted aluminium diffusion.

STEP 3

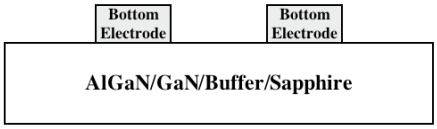


Figure 4.31:

The lift off process of the bottom electrodes is completed, see figure 4.31. After which an anneal in nitrogen is done at 700 °C for 30 s that allows for the aluminum to diffuse and create an ohmic contact to the 2DEG.

STEP 4

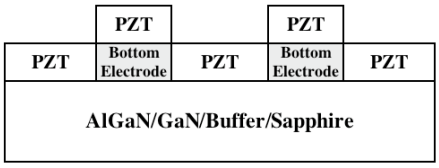


Figure 4.32:

A blanket layer of PZT is deposited, see figure 4.32.

STEP 5

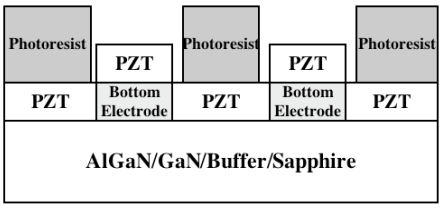


Figure 4.33:

The positive photoresist is applied and illuminated in order to leave openings where the bottom electrodes are located, see figure 4.33.

STEP 6

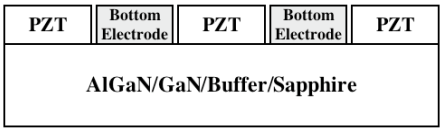
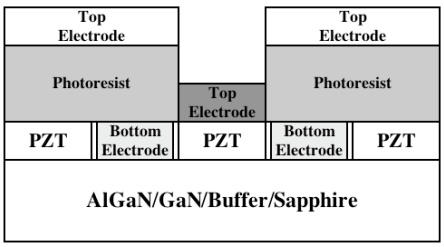


Figure 4.34:

The PZT is wet etched in those openings to create a passage way to the bottom electrodes. After which the photoresist is removed, see figure 4.34.

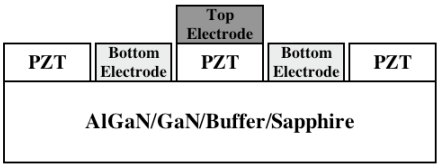
STEP 7



The photoresist is spun on and illuminated for the top electrode step. The top electrodes are deposited using the lift-off technique, see figure 4.35.

Figure 4.35:

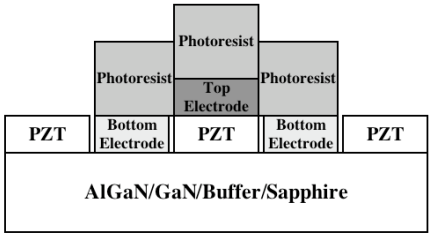
STEP 8



All of the unwanted photoresist is removed and what is to be left is seen in figure 4.36.

Figure 4.36:

STEP 9



Positive photoresist is applied, illuminated and developed to create the MESA structure which will be dry etched, see figure 4.37.

Figure 4.37:

STEP 10

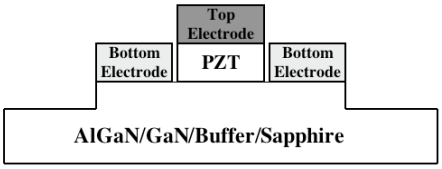


Figure 4.38 represents the final structure after the final dry etching of the MESA and the removal of the photoresist with acetone.

Figure 4.38:

4.3.3 P(VDF/TrFE) Device Fabrication

The main difficulty in passing from PZT ferroelectric gates to P(VDF/TrFE) ferroelectric gates is the modification of the processing steps. Mostly, attention needs to be paid to the steps that involve acetone and organic solvents, especially the removal of photoresist in acetone. This is due to the fact that the thin film layer of P(VDF/TrFE) is dissolved when put in a bath of acetone. The temperature also needs to be taken into consideration as the melting temperature of the P(VDF/TrFE) used in these experiments is 154.5 °C and the crystallisation temperature 129 °C. Therefore, all processing steps cannot involve the heating of the P(VDF/TrFE)/AlGaN structure to temperatures above approximately 120 °C. A challenge in the processing that still remains in step 9 is the removal of the P(VDF/TrFE) that is covering the bottom electrodes, currently this is being done by mechanical scratching. A more optimal way to access the bottom electrodes would be to deposit a chrome mask leaving holes where the bottom electrodes are, removing the P(VDF/TrFE) by oxygen plasma ashing. After the ashing step the chromium mask would be removed by wet etching. Although this process has already been tested it was not used for the processing of the devices in this thesis.

STEP 1

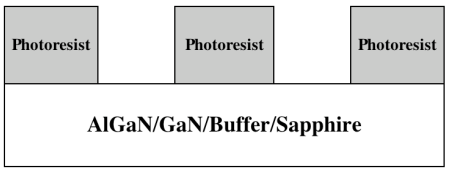


Figure 4.39:

Positive photoresist is spun on, illuminated and developed such that holes are left for the deposition of the bottom electrodes, see figure 4.39.

STEP 2

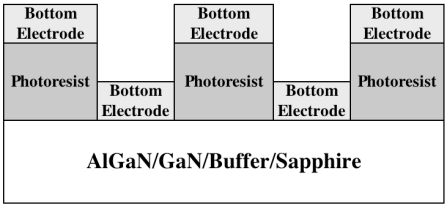


Figure 4.40:

Bottom electrodes are deposited using the lift-off process, see figure 4.40. Keeping the area that will have the ferroelectric layer on it untouched, more specifically without any unwanted aluminium diffusion.

STEP 3

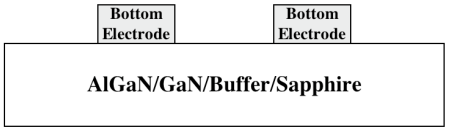


Figure 4.41:

The lift off process of the bottom electrodes is completed, see figure 4.41. After which an anneal in nitrogen is done at 700 °C for 30 s that allows for the aluminum to diffuse and create an ohmic contact to the2DEG.

STEP 4

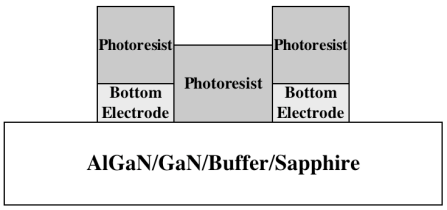


Figure 4.42:

Positive photoresist is applied and illuminated to create the MESA structure which will be dry etched, see figure 4.42.

STEP 5

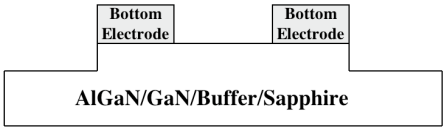


Figure 4.43:

Figure 4.43 represents the structure after the dry etching of the MESA and the removal of the photoresist with the positive photoresist developer.

STEP 6

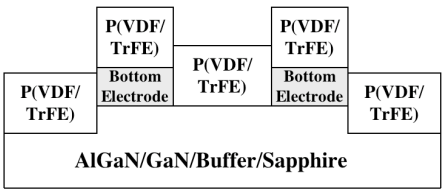


Figure 4.44:

A blanket layer of P(VDF/TrFe) is then deposited, see figure 4.44.

STEP 7

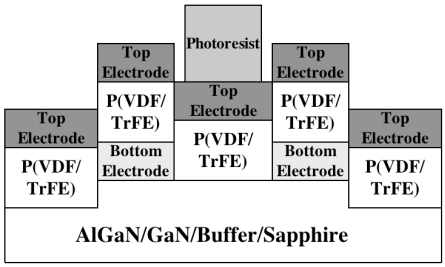


Figure 4.45:

A blanket layer of the top electrode is then deposited, see figure 4.45. Positive photoresist is then spun on and illuminated leaving photoresist covering the area of the active top electrodes.

STEP 8

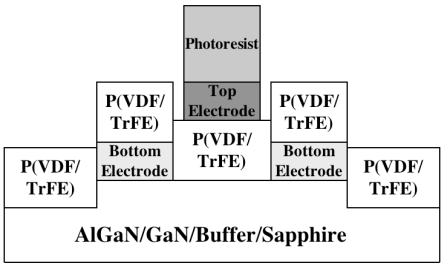


Figure 4.46:

The undesired top electrode is then wet etched to leave only the top electrode covering the active area in the Hall bar structure, see figure 4.46.

STEP 9

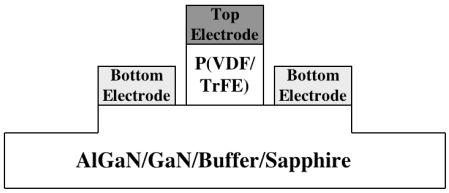


Figure 4.47:

The final photoresist is then removed by the positive photoresist developer, see figure 4.47. The P(VDF/TrFE) covering the bottom electrodes, is removed by mechanical scratching.

Chapter 5

PZT Deposition and Characterisation

This chapter will describe in detail the deposition of the lead zirconium titanate, PZT, layer onto the AlGaN/GaN heterostructure and its characterisation. The PZT layer is deposited both directly onto the AlGaN heterostructure or using an intermediary buffer layer. Listed below are the different ferroelectric and ferroelectric/buffer layers whose depositions were investigated in this chapter:

- TiO_2 nucleation layer for (111) PZT
- Chemical solution deposition, CSD, PZT
- CSD PZT with a MgO buffer layer deposited by pulsed laser deposition
- Sputtered PZT

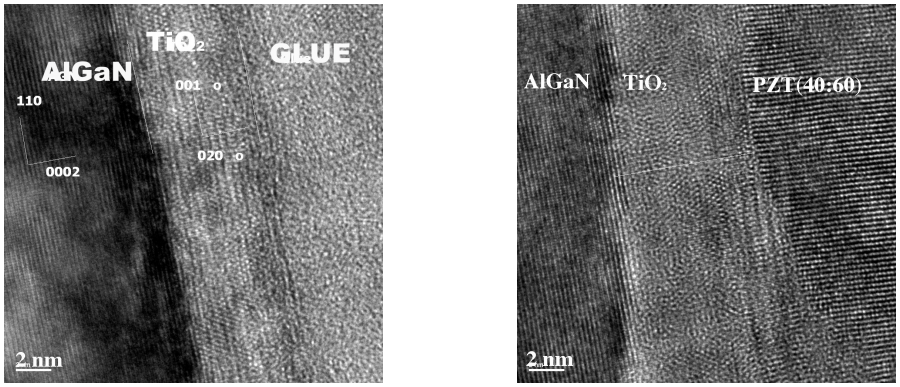
After the ferroelectric layer was deposited various tests were done in order to characterise the ferroelectric thin film and determine if the 2DEG retained its great transport properties. The experimental investigations of the ferroelectric and ferroelectric/buffer layers that was done in this chapter are listed below. When the results were positive it was possible to further proceed with capacitance voltage measurements and the fabrication of Hall bar and van der Pauw structures.

- XRD spectra
- AFM topography
- SEM topography
- Quick resistance and sheet resistance measurements of the 2DEG
- HRTEM and TEM-EDS at the ferroelectric/semiconductor interface
- PFM poling, and retention measurements
- XPS surface analysis and depth profiling

5.1 TiO_2 Nucleation Layer for PZT

To ensure for the (111) textured growth of PZT on platinum Muralt et al. [1998] determined that it was beneficial to use an "ultra-thin" seeding layer of TiO_2. This TiO_2 seeding layer might not necessarily be needed for the growth of PZT on the AlGaN heterostructures and it is thus of interest to investigate the deposition of this layer. TiO_2 was grown on AlGaN/GaN by DC magnetron sputtering with a titanium target. During deposition the sample was held static at a constant distance from the target with a continuous oxygen flow of 20 sccm, see appendix A for more details on the process conditions.

The thickness of the TiO_2 seeding layer on AlGaN was controlled by a HRTEM image, figure 5.1a, as 7.5 nm for a deposition time of 3 min. Using this known thickness for a deposition time of 3 min it was possible to make a linear extrapolation to determine the thickness of the future layers deposited, but not measured, according to the time of deposition.



(a) (b)

Figure 5.1: a) HRTEM image of the TiO_2/AlGaN interface, showing a TiO_2 thickness of 7.5 nm for a deposition time of 3 min. b) HRTEM image of the PZT/TiO_2/AlGaN interface showing that when using too thick of a TiO_2 seeding layer it remains as is and is not converted to PZT during the PZT deposition process.

Performing a fast fourier transform, FFT, of the HRTEM image, in figure 5.1a, the lattice spacings, of the TiO_2 layer, were measured a=b=4.72 Å and c=2.941 Å and tetragonal structure was deduced using the XRD file database (JCPDS file no. 86-147, see appendix C). There would be tensile stress in the in-plane direction due to the fact that this database file of TiO_2 has a crystal structure of rutile with a=4.594 Å and c=2.9586 Å. Figure 5.1b is a HRTEM image of the PZT/TiO_2/AlGaN interface, from right to left, using a TiO_2 layer of 7.5 nm. What is interesting to see here is that not all of the TiO_2 is consumed to create PZT during the PZT deposition process and possibly an ultra-thin "dead" or un-switchable layer remains of TiO_2 or a inferior, to PZT, $PbTiO_3$ layer. The FFT of the AlGaN structure of the HRTEM image, in figure 5.1b, was measured with c=5.12 Å. This value is similar to the values of the lattice spacings of hexagonal GaN taken from the XRD database file (JCPDS file no. 2-1078, see appendix C), where a=b=3.186 Å and c=5.178 Å. At the interface where the PZT growth is assumed to start a lattice constant of a=b=4.65 Å is measured. This result is within the experimental error of the lattice constant of rutile tetragonal TiO_2 listed above. Since the lattice constant of tetragonal $PbTiO_3$ taken from the XRD database as a=b=3.90440 Å and c=4.15220 Å,

see appendix C, the transitional zone is not $PbTiO_3$. Therefore, it is assumed that when using too thick of a TiO_2 seeding layer on AlGaN remains, since it is not completely consumed during the PZT deposition process.

It is known from the deposition of PZT on platinum that the TiO_2 seeding layer needs to be of a thickness greater than 2 nm in order to have full coverage, Muralt et al. [1998]. Also no more than 3 nm of TiO_2 needs to be deposited since excess TiO_2 will not be converted into PZT. Figure 5.2 shows that the relative permittivity of the PZT layer is optimised/maximised for a TiO_2 seeding layer of approximately 2 nm. Although Hiboux [2002] made a two seeding layer system, including a second $PbTiO_3$ seeding layer, and the PZT is grown on platinum, figure 5.2 illustrates the effect of the TiO_2 seeding layer.

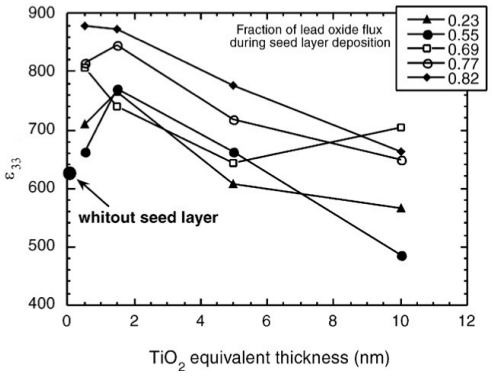


Figure 5.2: Relative permittivities of (111) PZT when deposited onto a TiO_2 layer of varying thickness when using a second seeding layer of $PbTiO_3$ of various concentrations of PbO. See the inset in the figure which denotes the fraction of lead oxide flux during the second seeding layer deposition. A critical thickness of 2 nm is observed after which the permittivity decreases when increasing the thickness of the first seeding layer, Hiboux [2002].

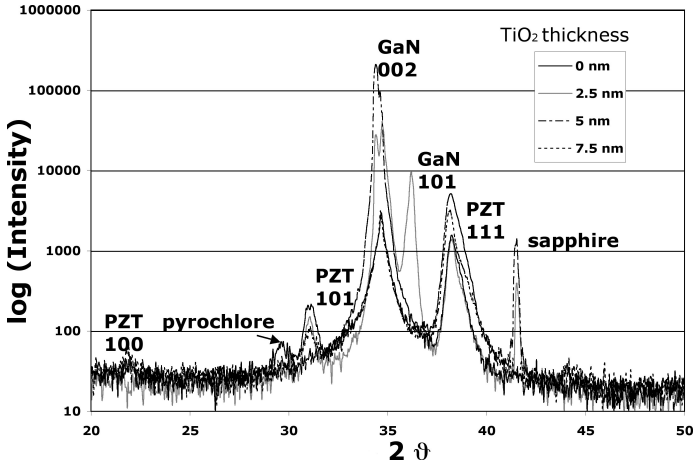


Figure 5.3: XRD spectra showing the change of the orientation of the PZT layer with the TiO_2 thickness. All samples have a PZT layer of thickness 65 nm with a 40(Zr):60(Ti) orientation.

However, very few experiments of depositing PZT on AlGaN or GaN have been done. Therefore, four samples were deposited in the same manner with a varying thickness of the TiO_2 layer to see the influence of its thickness on the orientation of the PZT layer. Both the TiO_2 and PZT(40:60) were deposited with magnetron sputtering described in more detail in section 4.1.2 and 5.4. The TiO_2 layer had thicknesses of 0 nm, 2.5 nm,

5 nm, and 7.5 nm where the PZT layer had a constant thickness of 65 nm with a ratio of 40(Zr):60(Ti). These depositions and measurements were only performed once and should be done once more in order to confirm the trend. However, importance can be given in the fact that they are similar to the same results obtained by Muralt et al. [1998]. The XRD results of these four samples can be seen in figure 5.3, where the orientation of the PZT layer shows its dependence on the thickness of the TiO_2 layer. It is clear that pyrochlore phase is slightly present when not using the TiO_2 layer and that it is necessary not only to encourage (111) textured growth but also to help crystallisation. Also it is possible to see that when the thickness of the TiO_2 layer is 5 nm and 7.5 nm (100) and (101) oriented PZT of the perovskite phase are present. Whereas, when the TiO_2 layer is 2.5 nm (111) oriented PZT is the only orientation. The XRD spectra thus aid in concluding that it is easiest to obtain textured (111) PZT when using a TiO_2 seeding layer of 2.5 nm. The rutile structure of TiO_2 is preferred on (001) AlGaN, as also observed later on by Hansen et al. [2005].

5.2 CSD PZT

Many trials were done in order to optimise the CSD deposition process of the PZT(40:60) layer, see section 4.1.2 for details of the deposition technique. Most variables were held constant during the deposition process. The only two parameters varied were the annealing temperature and the time of annealing. These two parameters were determined instrumental in the crystallisation of the PZT perovskite layer of uniform grain structure without destroying the transport properties of the 2DEG in the AlGaN heterostructure. The CSD PZT deposited for these experiments was adjusted to have a Zr/Ti ratio of 40/60. Pyrolisis took place at 350 °C, allowing for the decomposition of the organic solvents. The final process was in a rapid thermal annealer, RTA, occurring at a temperature range of $620 - 700$ °C for a time varying from 30 s to 6 min in oxygen.

The temperature profile used for the RTA, annealing process was a ramp increase during 15 s to the programmed temperature. Then a hold occurred at the programmed temperature and time, where an overshoot of $9 - 15$ °C occurred during $10 - 15$ s. The final step was a cool down to room temperature, all of which occurred in air at ambient pressure.

No TiO_2 nucleation layer was used when trying to optimise the deposition parameters as it was assumed that it was not of utmost importance if or if not the PZT had random or textured orientation. Of priority was to observe that a perovskite PZT layer was deposited with a uniform grain structure and that the transport properties of the 2DEG in the AlGaN heterostructure were maintained. So for the initial process optimisation the PZT layer exhibited random orientation due to the fact that no seeding layer was used.

Some of the first and most important measurements to be done after the deposition of the ferroelectric layer are listed below. AFM topography imaging was done to observe a grain structure typical of perovskite films. Xray diffraction, XRD, spectrum was taken to observe the perovskite peaks characteristic of PZT. Lastly, simple resistance measurements or precise sheet resistance measurements were done to observe if the 2DEG survived the high temperature air annealing process without any degradation. These were the first measurements that were necessary in order to decide on continuing with this deposition process.

The critical step in this CSD process was determined to be the high temperature annealing process, therefore the two variables chosen for the preliminary experiments were the annealing temperature and time. The temperature and time of annealing were varied from $620 - 660\,^{\circ}\mathrm{C}$ and $1 - 6\,\mathrm{min}$ respectively. After which AFM, XRD and two probe resistance measurements were made to confirm or not if the annealing parameters were sufficient or to grow perovskite PZT on AlGaN without severely degrading the 2DEG. Conduction was evaluated with a two probe resistance measurement technique. Two indium electrodes were used, of approximately 1x1 mm^2, with a separation distance of approximately 4 mm. The resistance measured between these two electrodes was then used to monitor any degradation of the transport properties of the 2DEG due to the processing of the PZT layer. The results of these experiments are summarised in table 5.1.

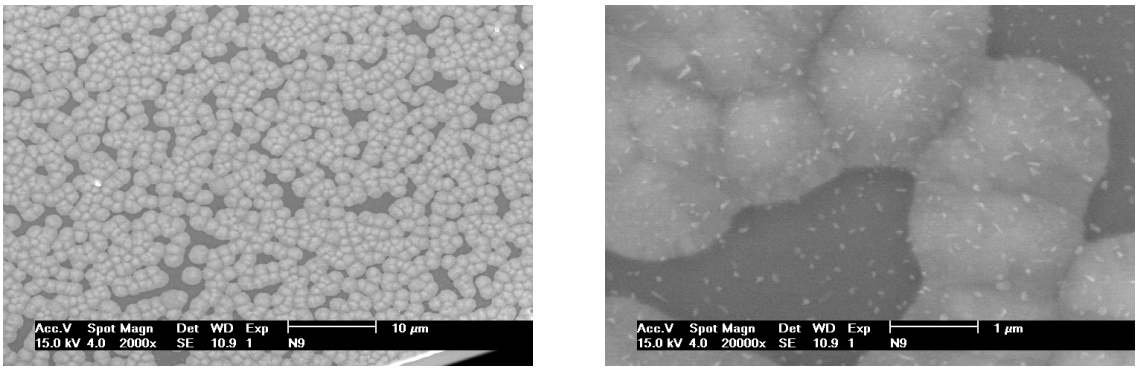
Table 5.1: The annealing temperature and time were modified in the CSD PZT deposition process in order to have a uniform grain structure in the AFM image, perovskite phase in the XRD spectra and small resistance in the 2DEG. Below is a summary of the preliminary experiments.

Anneal Temp [°C]	**Anneal Time** [min]	**AFM**	**XRD**	**Two Probe Resistance** [kΩ]
620	1	Amorphous	Amorphous	6-10
	3	Amorphous	Amorphous	6-10
	6	Island Like Grains	Small Perovskite Peaks	25
640	1	Island like Grains	Amorphous	10
	3	Grains	Predominantly Perovskite	15
	6	Grains	Predominantly Perovskite	200
660	1	Grains	Small Perovskite Peaks	20
	3	Grains	Predominantly Perovskite	35-40
	6	Grains	Predominantly Perovskite	> 1000

What can be observed from the experiments listed in table 5.1 is that in order to deposit a PZT thin film of sufficient quality the annealing temperature and time must be properly optimised. To grow perovskite PZT when annealing for 1 min it is important to use an annealing temperature greater than 660 °C. However, when the annealing occurs for 6 min the annealing temperature has only to be greater than 620 °C. In summary it was more likely to observe perovskite XRD peaks when annealing at high temperatures for long time.

Having a perovskite PZT XRD spectrum is not the only requirement in having a successful PZT layer on AlGaN, but also having a uniform grain like structure. This involves in optimising the RTA step to get rid of any secondary phases, as is visible in figure 5.4 when the annealing was done for 1 min at 600 °C. These SEM topography images show a non-uniform grain like structure with many holes as can be seen in the zoomed out image in figure 5.4a and in figure 5.4b secondary phases are visible typical of the pyrochlore phase. When using too low of an annealing temperature for too short of a time the PZT layer deposited had a SEM image as that shown in figure 5.4.

Also of importance is maintaining the low resistance of the 2DEG. Analysing the two probe resistance measurements of table 5.1 informed us on the fact that the 2DEG was ultra-sensitive to the annealing time and only slightly sensitive to the annealing temperature.



(a) (b)

Figure 5.4: PZT(40:60) annealed for 1 min at 600 °C. a) Zoomed out SEM image and b) a zoomed in SEM image showing holes where no grains existed and the small dots characteristic of the secondary/pyrochlore phase.

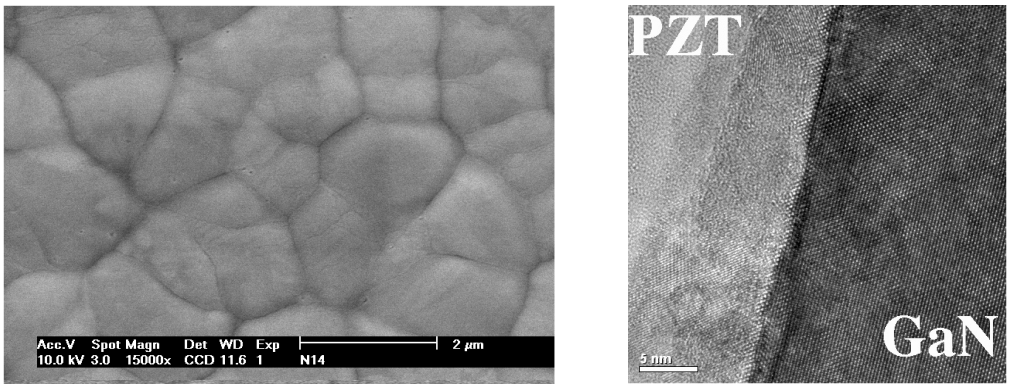
A slight degradation of the 2DEG by an increase of its sheet resistance can be tolerated, however in the most volatile annealing processes the 2DEG can be destroyed completely. It is necessary therefore to observe the resistance of the 2DEG after any high temperature processing step.

Attempts to grow PZT on AlGaN/GaN heterostructures by conventional CSD deposition techniques were not trivial. What was observed from the results in table 5.1 was that the 2DEG was most sensitive to the annealing time and not the annealing temperature. The depositions that followed were not monitored as closely as those used to create table 5.1 as the same trends were also noted in them. From this the sample used to study the change in transport properties due to the change in the spontaneous polarisation of the ferroelectric layer was grown as such. Initially, a $2-4$ nm TiO_2 layer was deposited by magnetron sputtering using a Ti target and depositing at a sample holder temperature of approximately 570 °C. After which PZT 40:60 was deposited in 4 layers, see section 4.1.2. To provoke perovskite phase rapid thermal annealing was done at 700 °C for 30 s, at lower temperatures pure pyrochlore phase remained and at longer times the 2DEG was destroyed.

Using the AFM the thickness of the film deposited was measured as 350 nm. The grain size of approximately $1-2\,\mu$m was observed by the SEM image in figure 5.5a. Figure 5.5b, shows a good epitaxial interface when the PZT was annealed for 30 s at 700 °C when using the TiO_2 seeding layer. Unfortunately, from the XRD spectra it was observed that it was very difficult to get rid of all traces of pyrochlore phases for pure perovskite growth without the reduction of the 2DEGs transport properties. This includes the samples that were annealed at 700 °C for 30 s. Whether or not this small percentage of pyrochlore phased PZT impedes the investigation of the impact of the ferroelectric gate on the 2DEG is not known here and needs to be investigated by further characterisation of the structure.

5.2.1 Poling and Retention with PFM

The use of the piezoresponse force microscope, PFM, in characterising the ferroelectric film on AlGaN/GaN heterostructures was instrumental in determining the stability of



(a) (b)

Figure 5.5: PZT(40:60)(111) annealed for 30 s at 700 °C. a) SEM image showing a uniform grain structure and b) HRTEM image of the PZT/GaN interface showing an almost epitaxial interface.

the switched polarisation. Section 3.3 gives a full description of PFMs functionalities, advantages, and disadvantages. This technique was particularly useful in observing if the ferroelectric layer deposited onto AlGaN was or was not capable of retaining its switched polarisation.

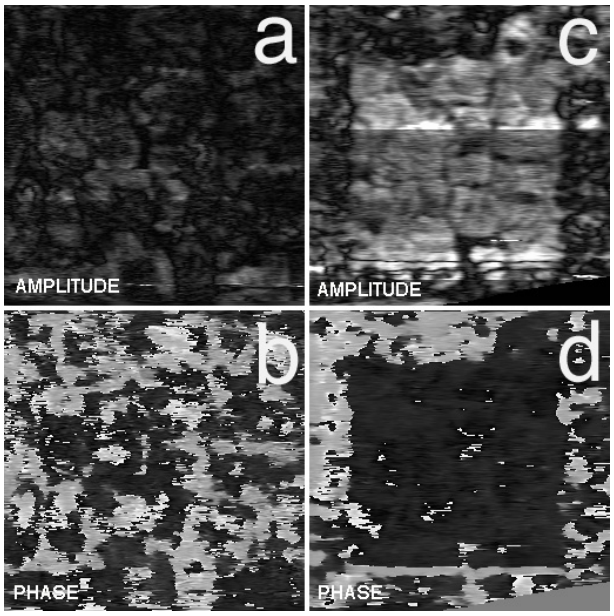


Figure 5.6: PFM measurements of a 3x3 μm^2 are on a PZT CSD sample annealed for 30 s at 700 °C. a) The vertical amplitude and b) the vertical phase of the as deposited state. c) The vertical amplitude and d) the vertical phase 22 hrs after an area of 2x2 μm^2 was poled with -45 V to the conducting cantilever.

It was observed that the PZT grown by the CSD method on AlGaN/GaN heterostructures can be poled in both directions and retain the written polarity. The CSD sample shown in figure 5.6 was annealed for 30 s at 700 °C. Firstly, the piezoresponse imaging was done for a PZT sample just deposited in an area of 3x3 μm^2, and exhibits random orientation in the vertical amplitude of the piezoresponse, figure 5.6a and the vertical phase of the piezoresponse in figure 5.6b. These images are useful in comparing the piezoresponse images after poling processes in order to observe the preferential orientation of the polarisation.

The poling was done in an area of 2x2 μm^2 which was completely poled with -45 V to the conducting cantilever. After which the vertical amplitude, figure 5.6c, and the vertical phase, figure 5.6d, piezoresponse images were taken in an area of 3x3 μm^2. This poling was stable for a few days after which no further measurements were done. Similar tests were done with DC poling voltages of the opposite polarities and it was confirmed that it was possible to switch the polarisation and have it retain its polarisation.

5.2.2 PZT(30:70) on GaN

Gruverman et al. [2004] deposited sol-gel PZT(30:70) films of varying thicknesses (100 nm, 200 nm, 300 nm) onto a GaN/sapphire sample. For crystallisation of the PZT to the perovskite phase the samples were annealed at a temperature of 700 °C for a time of 5 min in oxygen. It was only possible to grow partially textured (111) and (100) as no seeding layer was used. The effective piezoelectric coefficients were estimated to be $2, 5, 9$ pm/V for the different thicknesses ($100, 200, 300$ nm), that of GaN being 2 pm/V. In the 100 nm film most of the piezoresponse signal was in the in-plane (100) direction, possibly due to the tensile stress from the lattice mismatch between the PZT and GaN films. In the films with a thickness greater than 200 nm this stress was relieved and eliminated. Shown below in figure 5.7 is a piezoresponse hysteresis loop performed through a conducting AFM tip sitting stagnantly in contact with the PZT. The strain relaxation in the thickest 300 nm film allows for observing clear ferroelectric properties.

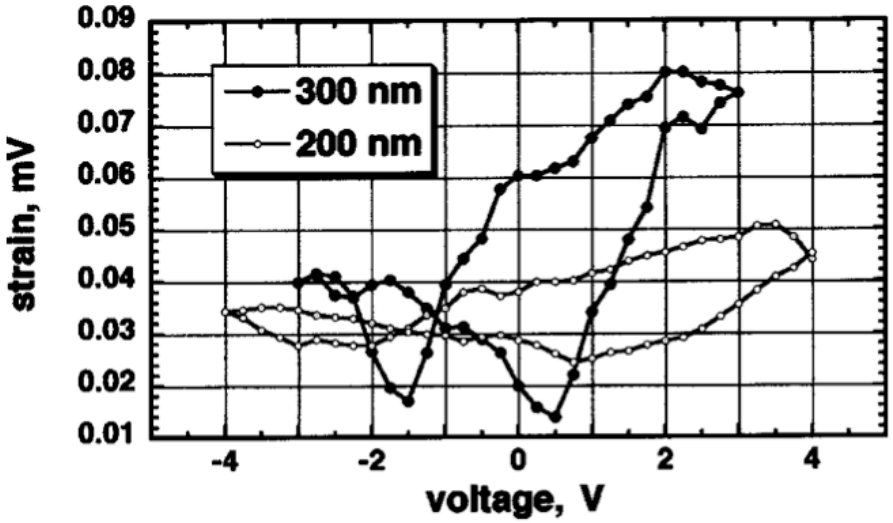


Figure 5.7: Piezoresponse hysteresis loop performed using a stagnant conductive AFM tip on a PZT/GaN structure with PZT of varying thickness, Gruverman et al. [2004].

What is important to note here is that the research of Gruverman et al. [2004] involved only a GaN/sapphire sample, that is there was no 2DEG and it was not an AlGaN heterostructure. The system of pure GaN allows for more forgiveness in the case of diffusion occurring at the PZT/GaN interface. This diffusion occurring due to the deposition process of the PZT, ferroelectric, layer at high temperatures or due to volatile chemical reactions.

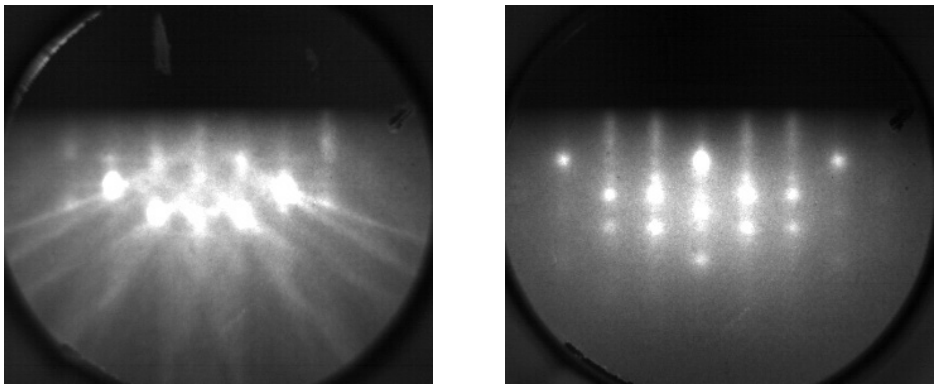
In the case of depositing PZT on AlGaN heterostructures, such as is done in this project, the 2DEG is located 20 nm below the PZT/AlGaN interface or at the AlGaN/GaN inter-

face. This 2DEG is contacted by Schottky indium bottom electrodes which allow for the controlling of its transport properties or resistance. If diffusion does occur changing the composition or structure of the AlGaN or GaN layers and hence reducing the conductivity of the 2DEG. This will be measured by the two point probe resistance measurement, as done for the results shown in table 5.1 or for more precise analysis by measuring the sheet resistance. The advantage of having the 2DEG is that this is an ultra-sensitive way to monitor if any diffusion does occur. Which means that a lot of time needs to be consecrated towards the optimisation of processing conditions of the ferroelectric layer in order for the 2DEG to maintain its transport properties.

5.3 CSD PZT with MgO Buffer Layer

One of the main difficulties in depositing ferroelectrics on semiconductors is the reactions and inter-diffusion occurring at their interface. To avoid or minimise this problem of inter-diffusion it is possible to use a barrier layer, as described in section 2.2.5. The criteria for this buffer layer is that it is of minimal thickness in order not to screen the ferroelectric polarisation from the semiconductor and that the voltage drop across it is minimised hence a high dielectric constant is optimal, and lastly a conduction band offset of at least 1 eV is ideal in order to minimise gate leakage current. MgO is a possible candidate for a buffer layer between the PZT and AlGaN layers, since it has a band gap of 8 eV, which is suitable to reduce leakage current. MgO has a dielectric constant of 9.65, which is sufficient but not ideal for a buffer layer. Finally, MgO has only a relatively smalll lattice mismatch of ≈6.5 % with the AlGaN layer allowing for a possible epitaxial interface with minimal diffusion.

5.3.1 MgO Deposition



(a) (b)

Figure 5.8: RHEED diffraction patterns of a) the AlGaN before deposition and b) at the end of the MgO deposition by pulsed laser deposition, PLD.

The MgO layer was deposited by PLD, pulse laser deposition, from a MgO target. Processing was done at a temperature of 400 °C, with a pressure of $1x10^{-7}$ Torr for 100 s. The laser was tuned to the following settings: laser energy 350 mJ, laser repetition 5 Hz,

laser voltage 20 kV, and laser pressure 3300 mbar. The AlGaN layer was cleaned with 3 % HF and 12 % HCl at room temperature for 1 min to remove all oxides at the surface before the deposition. Reflection high-energy electron diffraction, RHEED, patterns of the AlGaN surface were taken before the deposition process started, see figure 5.8a. During the deposition process the RHEED diffraction pattern was used to control the presence of the growth of the MgO layer, the final pattern in figure 5.8b demonstrates the successful deposition of the MgO layer with cubic structure. Unfortunately, with the PLD system used it is not possible to control the thickness of this layer grown to a better accuracy than 10 nm ± 5 nm. Therefore, it is not possible to further optimise the deposition conditions in order to grow a thinner MgO layer. For the implementation of a buffer layer it is important to have an "ultra-thin" buffer layer in order not to completely screen the polarisation, if the MgO layer is 15 nm there is a risk of doing such.

5.3.2 PZT/MgO/AlGaN Characterisation

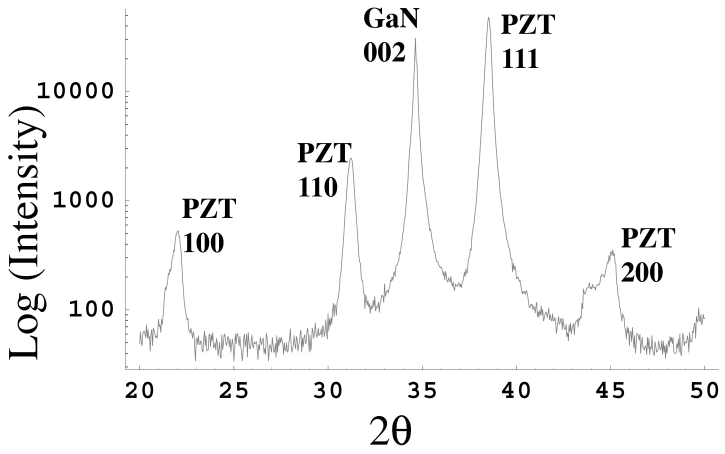


Figure 5.9: XRD spectrum of CSD PZT on AlGaN/GaN with an approximately 10 nm thick MgO buffer layer.

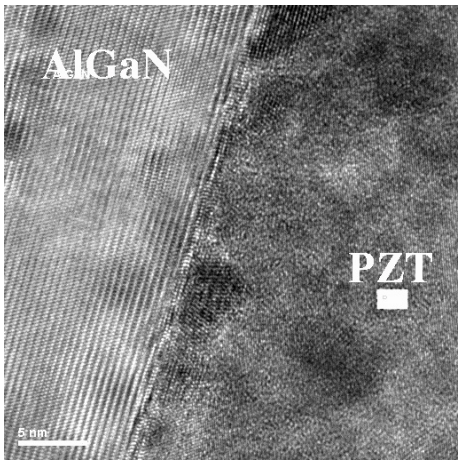


Figure 5.10: HRTEM image of the CSD PZT onto an AlGaN heterostructure with an approximately 10 nm thick MgO buffer layer.

PZT was deposited by the CSD technique on the AlGaN heterostructure while using an

MgO buffer layer of approximately 10 nm ± 5 nm. No seeding layer was used since MgO is textured (111), so it was assumed that this will help grow the PZT in the (111) direction. As one can see from the XRD spectrum, the PZT has preferential (111) growth, however other orientations are also present, see figure 5.9. Notice that there are no unwanted phases such as pyrochlore. The high resolution TEM image taken of the PZT/MgO/AlGaN interface shows that it is possible that a complete MgO layer was not deposited, see figure 5.10. Where it is possible to observe small islands of a cubic structure on the AlGaN layer that do not consist of a continuous layer. It is assumed then that a non-continuous film of MgO will not work efficiently as an inter-diffusion barrier for the high temperature annealing necessary for CSD PZT.

5.4 Sputtered PZT

After making multiple trials of depositing PZT by CSD it was decided to attempt the PZT deposition by multiple target magnetron sputtering. This technique could be advantageous due to the fact that the processing occurs at a lower temperature than that required in the RTA, annealing, step when using the CSD technique. The physical vapor deposition, PVD, or magnetron sputtering set up used in these experiments was already described in section 4.1.2. To ensure the (111) textured growth of the PZT layer a thin TiO_2 seeding layer was always first deposited onto the AlGaN, as described in section 5.1. After which the PZT process was optimised in order to have pure perovskite growth of (111) PZT without any presence of the unwanted amorphous pyrochlore phases.

The original recipe of depositing PZT onto $Pt/SiO_2/Si$ structures was used as an initial starting point. However, it was quickly determined that this recipe only resulted in growing a mixture of both pyrochlore and perovskite phases. The first change to this program was to allow a long enough heating time so that the AlGaN could obtain the minimal critical temperature for the nucleation of perovskite PZT of approximately 570 °C, Kao et al. [2003]. The reason for increasing the warm-up heating time was due to the large band gap of both the sapphire substrate and the GaN semiconductor. In this magnetron sputtering setup the source of sample heating is a lamp on the backside of the sample holder. This implies that the sample is primarily heated through the absorption of photons in the infra red spectrum. The sapphire substrate has a wide band-gap (8.8 eV) as do AlGaN and GaN (3.4 eV) which do not easily allow for the absorption of photons in the visible spectrum. This concept was confirmed due to the fact that this warm-up heating time had to be increased for larger samples to ensure perovskite growth. For these initial experiments a PZT layer of ratio: 40% Zr and 60% Ti, PZT(40:60), was deposited.

After increasing the heating time it was possible to eliminate all pyrochlore phases and have pure perovskite growth on AlGaN. The first successful depositions of pyrochlore free (111) PZT(40:60) were thus deposited, see figure 5.11 for an SFM topography of an area of 2x2 μm^2. The film deposited to a thickness of 65 nm shows uniform grain structure with a uniform grain size of 100 nm in the SFM topography image. The first depositions were done on small samples only to observe that perovskite PZT could be deposited with uniform grain structure. After which the warm-up heating time of the deposition process was proportionally scaled for the deposition onto larger samples, since for device fabrication reasons it was better to work with larger samples. When increasing the size of the AlGaN/GaN/sapphire sample on which the PZT was deposited on to one sixth of a two inch wafer the transition was successful by uniquely increasing the warm-up heating

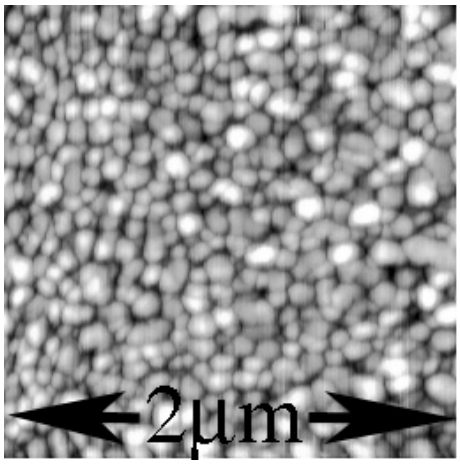
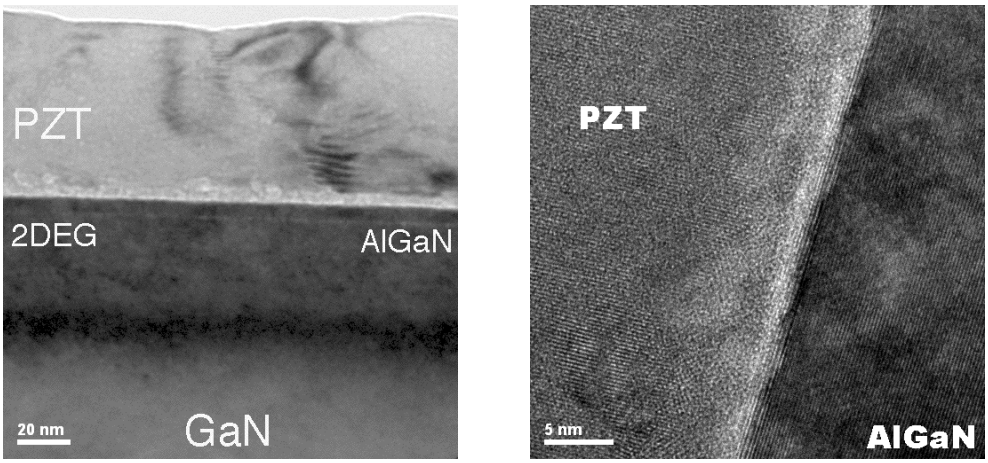


Figure 5.11: SFM topography of a 2x2 μm^2 square for a PZT(40:60) layer of 65 nm with uniform grain structure and grain size of 100 nm.



(a) (b)

Figure 5.12: High resolution transmission electron microscope, HRTEM, cross section of a 65 nmPZT (40:60)(111) /AlGaN interface. a) HRTEM image showing the thickness of the PZT layer and b) HRTEM image showing the details of the PZT/AlGaN interface.

time. Figure 5.12 is a HRTEM image of the PZT/AlGaN interface on the larger sample, with PZT thickness 65 nm. This HRTEM image shows a fairly clean interface, where after a few nanometers from the interface epitaxial PZT is grown.

The 2DEG was also monitored in order to observe any degradation in the transport properties due to the PZT deposition process. It was observed that the original sheet resistance of $R_s = 431\,\Omega/\square$ increased by a factor three to, $R_s = 1270\,\Omega/\square$. This small degradation should still allow for the observation of depletion when poling the PZT layer.

5.4.1 XRD Analysis

Two different thicknesses of PZT were thus deposited: 65 nm and 130 nm. This is shown in the XRD spectra for 65 nm thick samples in figure 5.13 and for 130 nm thick samples

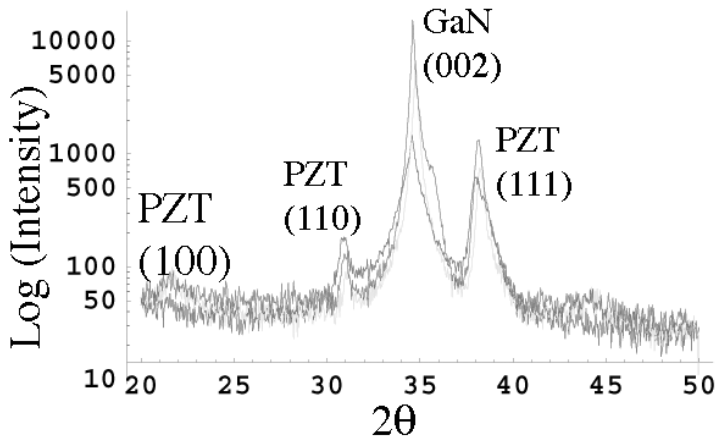


Figure 5.13: XRD spectra of three identically magnetron sputtered samples of 65 nm PZT(40:60).

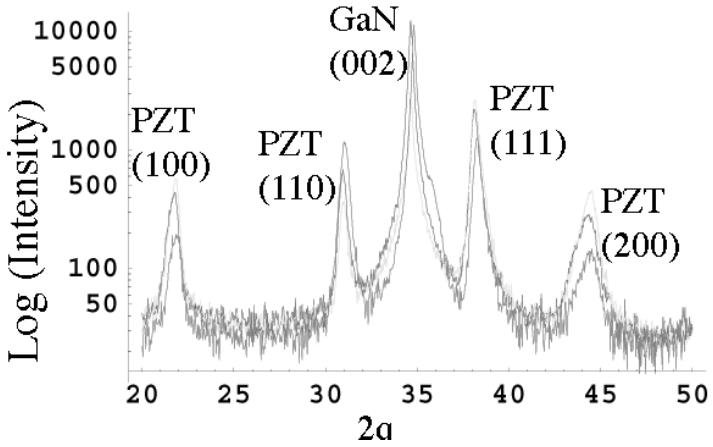


Figure 5.14: XRD spectra of three identically magnetron sputtered samples of 130 nm PZT(40:60).

in figure 5.14. From these spectra it is possible to see that in using the TiO_2 seeding layer it was possible to obtain highly textured (111) growth. In calculating the texture index, equation 5.1, of the three PZT peaks it is possible to calculate an approximation of the orientation of the thin films.

The texture index, shown in equation 5.1, is used in order to quantify the preferred crystallographic orientation with T=1 indicating a pure single crystallographic direction. I(hkl) is the intensity of the XRD peak, T(hkl) is the texture index and a(hkl) is the scaling factor obtained from the XRD peak in a randomly oriented, powder, sample from a JCPDS file described in detail in appendix C. Where for a PZT(44:56) sample the scaling factors are: a(100)=18, a(110)=100 and a(111)=37.

$$T_{100} = \frac{\frac{I_{100}}{a_{100}}}{\frac{I_{100}}{a_{100}} + \frac{I_{110}}{a_{110}} + \frac{I_{111}}{a_{111}}} \tag{5.1}$$

Since three identical depositions, using the same deposition conditions, were done for the two thicknesses it was observed that the depositions are reproducible. For the 65 nm thick films there was an average texture index in the (111) direction of 0.917, which decreases for the 130 nm thick films to 0.657. These results are supported by similar results for

growing PZT on platinum, that is (111) growth is more prominent for thinner films when the thickness of the PZT film increases the amount of the other PZT orientations also increases due to the preferential growth.

Table 5.2: Texture index of the 65 nm and 130 nm thick magnetron sputtered PZT(40:60) samples whose XRD spectra were shown above in figure 5.13 and 5.14.

Sample Name	**thickness** [nm]	**T(100)**	**T(110)**	**T(111)**
TG1-N112	65	0	0.07532	0.92147
TG1-N113	65	0.06767	0.01121	0.92112
C3-N118	65	0.03642	0.05594	0.90765
TG1-N114	130	0.25782	0.07018	0.67200
TG2-N115	130	0.29257	0.03195	0.67548
C3-N119	130	0.16562	0.21034	0.62404

After this more PZT films were sputtered onto the AlGaN heterostructure and it was determined that the orientation of the PZT layer was highly sensitive to any contamination existing on the chambers walls. It was thus determined to be very important to clean all the walls of the chamber by sand blasting before each series of depositions. In doing such it was possible to grow thicker PZT films with a higher degree of orientation in the (111) direction and minimal PZT of the (100) and (110) directions. In figure 5.16 is the XRD spectrum of a 195 nm thick PZT(40:60) sample which exhibits approximately PZT of T(111) =0.99 with no traces of pyrochlore phases and only a small peak for the (100) PZT. This results shows the importance of cleaning the chamber, especially its walls, before the deposition in order to be able to control most accurately what is being deposited onto the AlGaN layer.

To better confirm these results more depositions were done and it was observed that in cleaning the chamber it was possible to obtain pure (111) textured PZT for varying thicknesses and compositions. Already the XRD spectrum of the 195 nm PZT(40:60) exhibited (111) textured PZT, shown in figure 5.15. After which depositions were done for 65 nm PZT(40:60), 130 nm PZT(40:60) and 65 nm PZT(30:70) and their XRD spectra were measured, see figure 5.16. All of these XRD spectra are relatively the same, that is a PZT layer with approximately T(111) =1 with no traces of pyrochlore phases or other PZT orientations.

It has been successfully shown that in using magnetron sputtering it is possible to deposit (111) textured PZT on AlGaN/GaN heterostructures for thicknesses ranging from $65 - 195$ nm for PZT(40:60) and PZT(30:70). It is interesting to note that in the spectrum of the 195 nm PZT(40:60) in figure 5.15 there was a small trace for (100) PZT. However, in the 65 nm and 130 nm PZT(40:60) there was absolutely no presence of (100) PZT. Indicating the same theory that was mentioned above that it is more difficult to obtain perfectly textured (111) PZT for thicker films, as the other orientations have preferential growth.

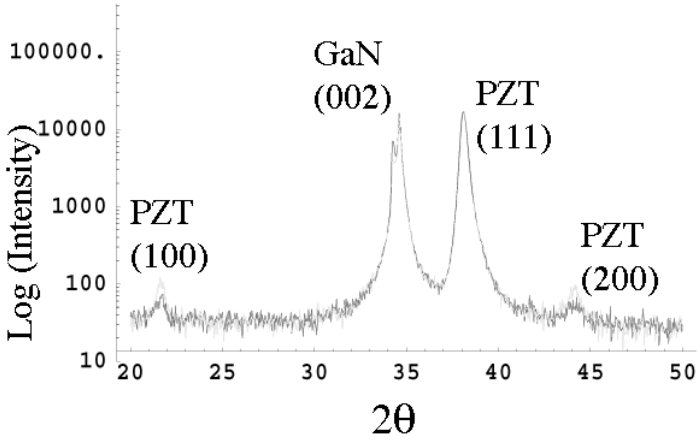


Figure 5.15: XRD spectrum of a PZT(40:60) 195 nm showing good reproducibility and highly preferred (111) orientation.

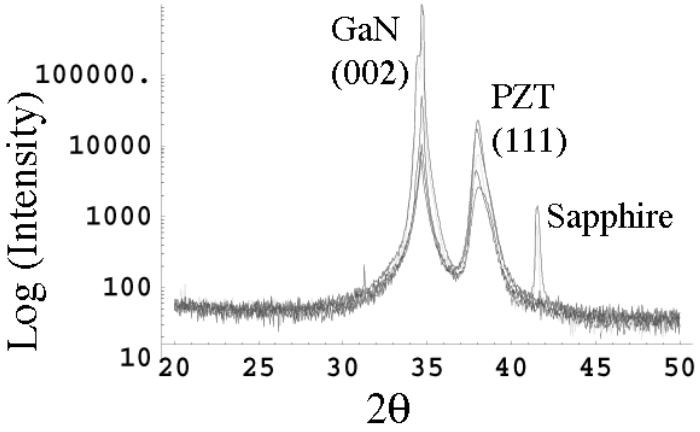


Figure 5.16: XRD spectra of three samples 65 nm PZT(40:60), 130 nm PZT(40:60) and 65 nm PZT(30:70). All of which showed highly preferred (111) orientation.

5.4.2 Poling and Retention with PFM

As in section 5.2.1, PFM, was used to characterise the sputtered PZT film that was deposited on the AlGaN/GaN heterostructure. Not only was this technique used to determine whether the ferroelectric layer could be poled and retain this written polarisation, but it was also possible to determine the maximum resolution with which it was possible to pole the ferroelectric layer when the conducting cantilever was scanning directly the ferroelectric layer.

PZT(40:60)(111) sputtered thin films, with a thickness of approximately 130 nm, on AlGaN/GaN heterostructures were tested with the PFM and the converse piezoelectric effect was observed. In figure 5.17, is an example where an area of 2x2 μm^2 was poled and its piezoresponse image of its retention is also shown. Firstly, an area of 2x2 μm^2 was poled with the a bias of -40 V applied to the conducting cantilever. After which 2 out of the 256 lines were poled with $+40$ V, these 2 lines would represent a line covering less than 1% of 2 μm or approximately 0.02 μm. The piezoresponse images immediately after poling are shown with the vertical amplitude in figure 5.17a, the vertical phase in figure 5.17b, the lateral amplitude in figure 5.17c and the lateral phase in figure 5.17d. The piezore-

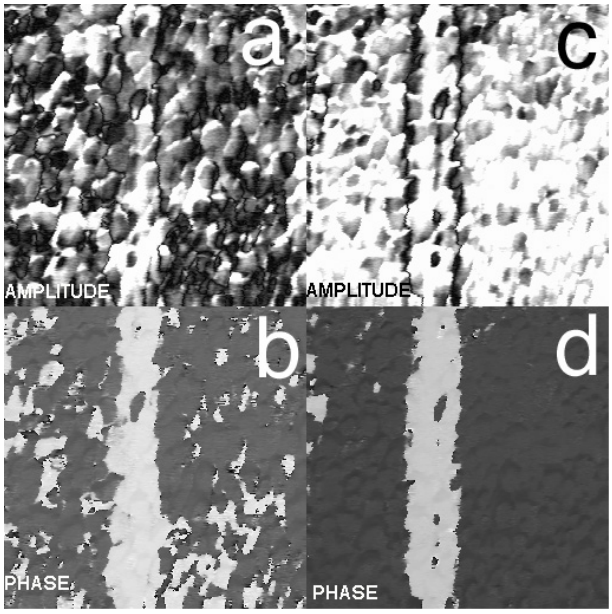


Figure 5.17: Sputtered PZT(40:60)(111) of 130 nm on AlGaN/GaN. An area of 2x2 μm^2 was first poled with -40 V to the conducting cantilever after which a line covering less than 1% of 2 μm (that is 2 out of the 256 lines) was poled with with $+40$ V. The piezoresponse images after this poling process are a) the vertical amplitude, b) the vertical phase, c) the lateral amplitude and d) the lateral phase.

sponse imaging was done with an AC voltage of 3 V_{pp} far below the coercive field of the ferroelectric layer in the MFS structure.

From figure 5.17 it can be observed that it was only possible to write a line with a line resolution of 350 nm. Possible limitations for this resolution are tip radius, electric field distribution, film thickness, grain size, applied voltage, surrounding environment, such as humidity, pressure, and scanning speed. However, it was not the goal of this thesis to optimise all poling and scanning conditions in such a way to observe the minimal writing feature size but to show to what extent the applications of ferroelectric gates can be extended to in the future.

Direct Writing of Stable Domain Configurations

It is imperative to develop the technique for direct writing of stable domain configurations on the PZT/AlGaN/GaN sample using SPM methods in order to write/implement semiconductor nanostructures by artificially created ferroelectric domain patterns. Direct domain writing with nanoscale resolution by SPM attracted much attention in recent years as a potential method of high-density data storage, Paruch et al. [2001], Eng et al. [1999a], Durkan et al. [2000]. It was demonstrated that poled regions with sizes smaller than 50 nm can be produced in a PZT thin film by application of a DC voltage through the tip of a conductive SPM cantilever. The required voltage and poling time vary considerably depending on the structure of the sample.

For the ferroelectric/heterostructure device the problem of writing stable poled regions is expected to be more challenging compared to the traditional case where the ferroelectric film is deposited on top of the metallic layer which acts as the bottom electrode. This is

partly due to the use of the 2DEG as bottom electrode where a Ti/Al/Ti/Au structure makes ohmic contact to it which will not be as stably conducting as a metallic layer. Also it is expected that the PZT layer deposited directly onto AlGaN is of inferior quality in comparison to when it is deposited onto platinum, and will exhibit polarisation fatigue (section 2.2.6) much earlier. Lastly the 20 nm layer of AlGaN is expected to increase the depolarisation field (section 2.2.1) seen in the ferroelectric film after the switching of its polarisation state.

The major problem provoking the short term retention of the polarisation is the depolarisation electric field which originates from the incomplete compensation of the polarisation charge, Tagantsev and Stolichnov [1999], Tagantsev et al. [1995]. This depolarisation field, which always exists in systems with spontaneous polarisation provokes polarisation loss due to back-switching and is larger when including the 20 nm layer of AlGaN. This detrimental effect can be reduced by increasing conduction in the near-by interfacial layer, Stolichnov et al. [2000]. When studying the films with PFM it is possible to overcome this problem by using a relatively high voltage in combination with slow scanning rate.

An attempt to create a stable polarisation domain pattern with the CP research scanning probe microscopes nano-lithography software was attempted. The shape that was programmed was a circle of diameter 3 μm in the opposite polarity than the area had already been poled in. The sample used to do such was a sputtered PZT(40:60)(111) of 130 nm on AlGaN/GaN.

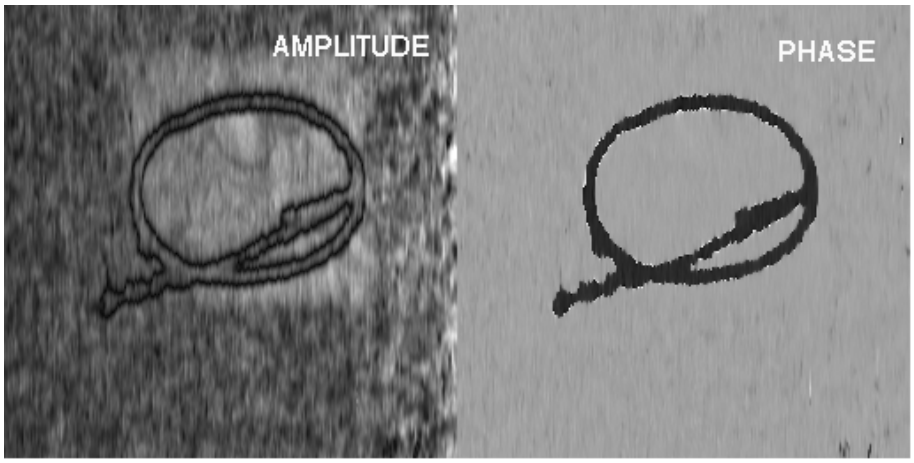


Figure 5.18: Sputtered PZT(40:60)(111) of 130 nm on AlGaN/GaN. An area of 5x5 μm^2 was first poled with +45 V to the conducting cantilever after which a circle of diameter 3 μm was written with a bias of−45 V applied to the conducting cantilever. The piezoresponse images after this poling process were done on an area of 10x10 μm^2 a) the vertical amplitude and b) the vertical phase.

For the first attempt an area of 5x5 μm^2 was first poled with +45 V to the conducting cantilever after which a circle of diameter 3 μm was written with a bias of−45 V applied to the conducting cantilever. The piezoresponse images after this poling process were done on an area of 10x10 μm^2 figure 5.18a shows the vertical amplitude and figure 5.18b shows the vertical phase. The line resolution of the circle written was 350 nm, similar to the line resolution obtained in figure 5.17 where the resolution of the poling was for a bias of +40 V.

The second attempt was on an area of 10x10 μm^2 which was first poled with −45 V to the conducting cantilever after which a circle of diameter 3 μm was written with a bias of

+45 V applied to the conducting cantilever. The piezoresponse images after this poling process were done on an area of 10x10 μm^2, figure 5.19a shows the vertical amplitude and figure 5.19b shows the vertical phase. This process decreased the line resolution to 600 nm due to the use of the opposite polarity for the biasing voltage.

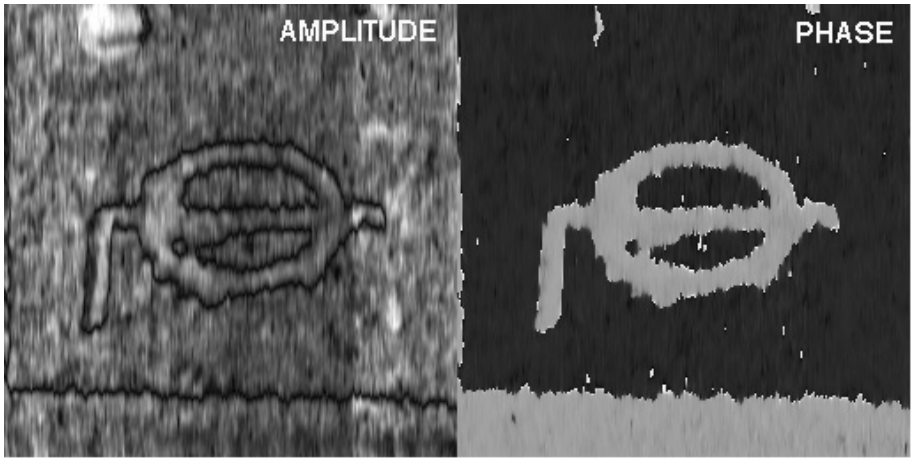


Figure 5.19: Sputtered PZT(40:60)(111) of 130 nm on AlGaN/GaN. An area of 10x10 μm^2 was first poled with -45 V to the conducting cantilever after which a circle of diameter 3 μm was written with a bias of+45 V applied to the conducting cantilever. The piezoresponse images after this poling process were done on an area of 10x10 μm^2 a) the vertical amplitude and b) the vertical phase.

In order to induce a quantum dot one needs to define in the 2DEG an island surrounded by a depleted region. This could possibly be accomplished using the SPM domain writing technique described in section 3.3.4. Both figure 5.18 and figure 5.19 show two examples of a polarisation domain pattern defined on the PZT sputtered film on AlGaN/GaN. Where a circle of radius 3 μm was written with $\pm$45 V onto an already poled area by $\mp$45 V. The difference in the line resolution of these two images from 350 nm to 600 nm is due to the poling with reversed polarities. Our experience as well as data by other researchers Paruch et al. [2001], Eng et al. [1999a], Durkan et al. [2000] shows that features with much smaller sizes than shown in figure 5.18 and 5.19 (down to 50 nm) can be produced by SPM domain writing. The optimisation of the allowed shapes and line resolution of domain patterning could be improved by further optimisation of both the processing of the devices and the poling technique.

5.5 PZT/AlGaN Interface Control

One problem of integrating the perovskite ferroelectrics with semiconductors is due to the inter-diffusion occurring at this interface due to the high temperature processing of the ferroelectric layer. Even though AlGaN is supposed to exhibit chemical and mechanical stability, it could be possible that N_2, O_2 and Ti diffuse through the PZT/AlGaN interface. The most detrimental possibilities of this is that this diffusion leads to the creation of a "dead", un-switchable, layer at the interface or that the diffusion into the heterostructure causes the permanent degradation of the transport properties in the 2DEG. This diffusion could be one of the reasons why there is not a perfect epitaxial interface between the PZT and the AlGaN, but rather that there is a thin amorphous layer before the PZT becomes

epitaxial, as seen in the TEM image figure 5.12. The other reason for not having a "perfect" interface is of course due to the large mismatch in the in-plane lattice constants for the PZT and AlGaN layers.

5.5.1 Diffusion

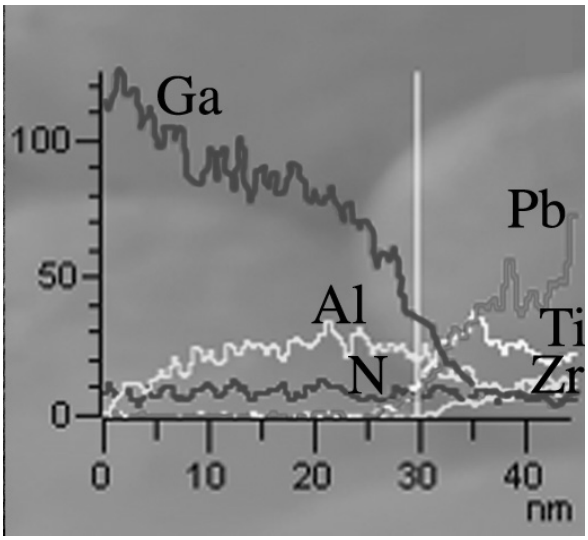


Figure 5.20: TEM-EDS analysis of a 65 nm PZT(40:60)(111) showing a diffusive interface of approximately 7 nm, due to the diffusion of the elements possible to measure with this technique (Pb, Zr, Ti).

It was thus of interest to analyse the PZT/AlGaN interface with both energy dispersive spectroscopy, EDS, TEM analysis and X-ray Photoelectron Spectroscopy, XPS, depth profiling. Ideally it would have been most beneficial to use a technique that could measure all of the elements concerned (Pb, Zr, Ti, O_2, Al, Ga, N_2) with a superior resolution. The technique to do this is called secondary ion mass spectroscopy, SIMS, unfortunately, this technique was not attempted.

TEM-EDS analysis allows for the accurate direct measurement of (Pb, Zr, Ti, Ga) in a carefully prepared cross section of a sample. This will give some information about the diffusion occurring at the interface, but it is of interest to observe the two light elements O_2 and N_2 which are not measurable by this technique. The TEM-EDS analysis of a 65 nm PZT sample demonstrates that it takes Pb, Zr and Ti about 7 nm from the interface before they stabilise, figure 5.20. This implies that there are some strong reactions at the PZT/TiO_2/AlGaN interface.

Another technique that will allow to measure all the elements necessary in this structure is by using XPS depth profiling. In this technique each measurement occurs on the surface of the sample after which the sample is vertically etched with ion bombardment for a predefined amount of time before the next measurement occurs. The disadvantage of this technique is that the etching rate of all the elements in question is not equivalent, therefore when performing thick depth profiles the uncertainty of the measurement is increased.

It was possible to qualitatively analyse the diffusion at the interface by using XPS depth profiling for a 65 nm PZT(40:60) sample as seen in figure 5.21. Knowing that the PZT layer is 65 nm the diffusive interface is calculated as approximately 26 nm. This same

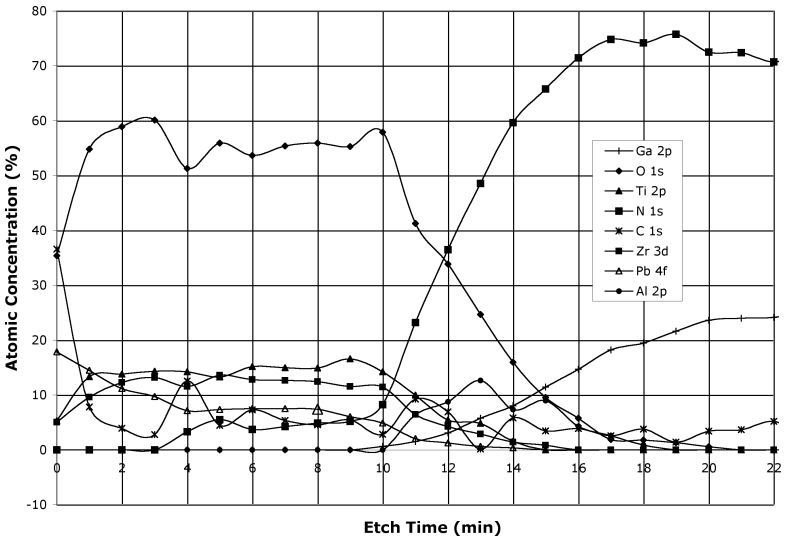


Figure 5.21: XPS depth profile of a 65 nm PZT(40:60)(111). It is possible to facilitate the reading of the x-axis by thinking that the etching time of 1 min is approximately 6.5 nm.

sample also had TEM-EDS analysis at the interface, see figure 5.22. Knowing that the ten data points are taken along a line of approximately 65 nm, the diffusive interface is determined to be approximately 13 nm. This information is more reliable since the elements analysed Ti, Ga, Zr and Pb can all accurately be measured by the EDS and due to the fact that if the interface had diffusion occurring for distances greater than 20 nm the 2DEG would be completely destroyed. The XPS depth profiling results are also a bit ambiguous, since the etching process that occurred before each analysis has different etching rates for each element. As it is known that the 2DEG only slightly degrades due to the PZT deposition process it is concluded that the EDS results are more accurate and that a 13 nm diffusive interface exists.

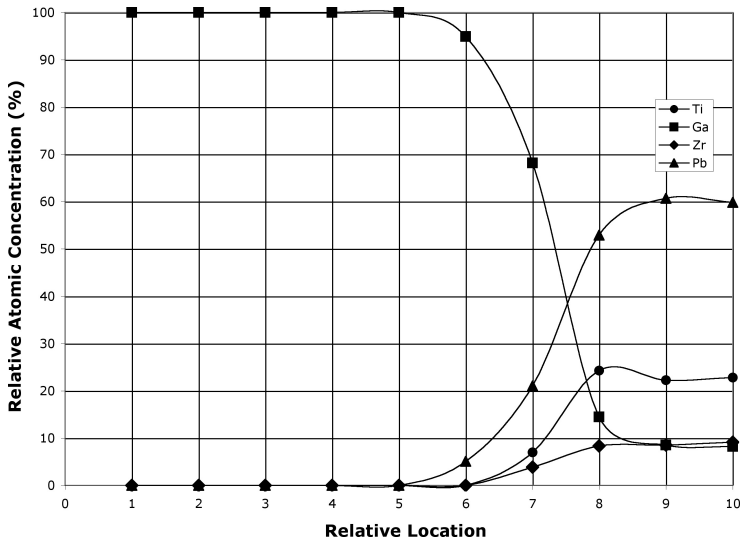


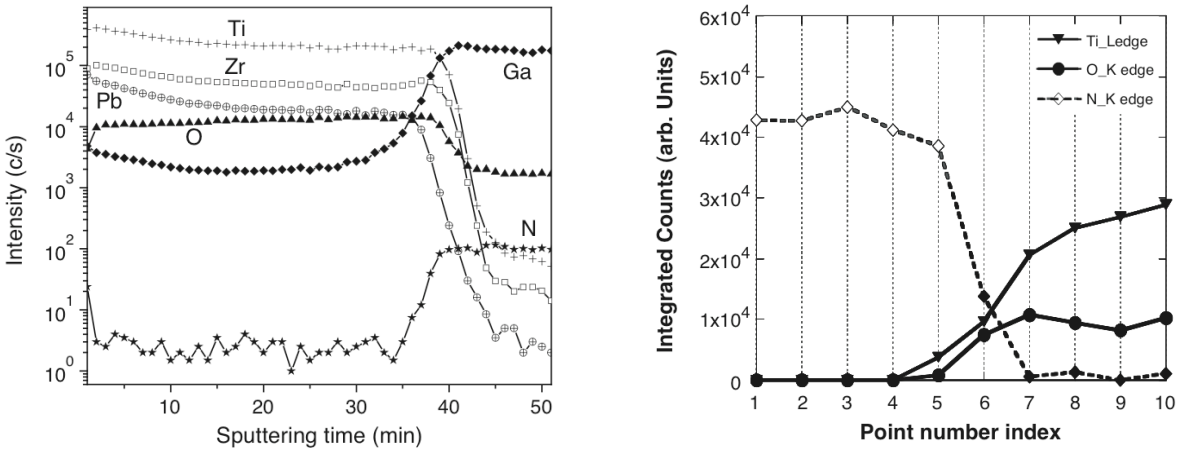
Figure 5.22: TEM-EDS depth analysis of a 65 nm PZT(40:60)(111). It is possible to facilitate the reading of the x-axis by thinking that "1" relative location is approximately 6.5 nm.

Another way to control whether or not diffusion occurred at the interface was to measure the transport properties of the 2DEG from a known reference sample and compare it to

the transport properties after the PZT deposition. This is not a way to determine which elements diffuse but to determine if the processing steps lead to the degradation of the 2DEG and to which factor. The Hall bar measurements on a reference Hall bar structure without having had any PZT deposited onto it but having an etched Hall bar mesa gave transport values of $R_s = 431\,\Omega/\square$, $n_s = 1.15\text{x}10^{13}\,\text{electrons}/\text{cm}^2$ and $\mu = 1260\,\text{cm}^2/\text{Vs}$. Measuring these transport properties on a non-poled PZT Hall bar structure the transport properties change to $R_s = 1270\,\Omega/\square$, $n_s = 6\text{x}10^{12}\,\text{electrons}/\text{cm}^2$ and $\mu = 820\,\text{cm}^2/\text{Vs}$. There is therefore a slight degradation in the 2DEG with an increase in the sheet resistance by a factor three, a decrease in the electron sheet concentration by a factor of two and a decrease in the mobility by a factor of 1.5. This method is much simpler than doing any type of chemical analysis and is more useful for the purposes of this thesis. It is not in the interest of this thesis to analyse the PZT/AlGaN interface but to deposit successfully PZT onto AlGaN without destroying the 2DEG.

5.5.2 PZT on GaN

Cao et al. [2005] deposited PZT by a CSD technique onto GaN and observed the interface by secondary ion mass spectrometry, SIMS, and electron energy loss spectrometry, EELS, see figure 5.23. The sample used in figure 5.23a had been annealed in a RTA in oxygen for 10 min at 700 °C and that in figure 5.23b had been annealed in a RTA in oxygen for 5 min at 700 °C. In observing figure 5.23a and knowing that the PZT layer deposited is 300 nm it is possible to calculate that the diffusive interface is approximately 125 nm. Whether this is due to diffusion occurring during the RTA annealing step or to the unequal etching rates of the different elements to the ion bombardment is not known. In figure 5.23b the EELS data could be determined more precise and gives a diffusive interface of approximately 6 nm. Unfortunately with EELS it is only possible to measure the light elements such as titanium, oxygen and nitrogen, whereas with SIMS it is possible to observe all the elements in the structure.



(a) (b)

Figure 5.23: Cao et al. [2005] deposited PZT by CSD technique onto GaN and observed the interface a) on a sample annealed in an RTA with oxygen for 10 min at 700 °C with secondary ion mass spectrometry, SIMS. and b) on a sample annealed in an RTA with oxygen for 5 min at 700 °C with electron energy loss spectrometry, EELS.

Keep in mind that an annealing procedure as rigorous as $5 - 10$ min at 700 °C in oxygen would result in the complete destruction of the 2DEG in the AlGaN/GaN heterostructures located 20 nm below the PZT layer. The annealing profile that was possible to use in this thesis on the AlGaN/GaN heterostructures at 700 °C could not exceed a time of 30 s without the destruction of its 2DEG, see section 5.2 for further details.

Therefore, it is important to note here that the system being worked with in this thesis is not the GaN/sapphire structure, but the more complicated AlGaN/GaN/sapphire structure. That is there was no 2DEG in the samples of Cao et al. [2005]. This has already been mentioned in more detail in section 5.2.2 regarding the research of Gruverman et al. [2004] with PZT(30:70)/GaN/sapphire sample. However, it will be mentioned quickly again that in the case of depositing PZT on AlGaN heterostructures, such as is done in this project, the 2DEG is located 20 nm below the PZT/AlGaN interface or at the AlGaN/GaN interface. This 2DEG is contacted by ohmic electrodes which allow for the controlling of its transport properties or resistance. If diffusion does occur, changing the composition or structure of the AlGaN or GaN layers, a reduction in the conductivity of the 2DEG will be observed. The advantage of having the 2DEG is that it is an ultra-sensitive way to monitor if any diffusion does occur. The disadvantage of the 2DEG is that a lot of time needs to be consecrated towards the optimisation of processing conditions of the ferroelectric layer in order for the 2DEG to maintain its transport properties.

5.6 Summary

PZT was deposited onto the AlGaN/GaN heterostructure and then tested for ferroelectricity. The use of the additional MgO buffer layer was also investigated. The samples that successfully underwent testing in this chapter that will be used for future experiments in chapter 7 are:

- CSD 400 nm PZT gate
- CSD 300 nm PZT gate with 10±5 nm MgO buffer layer
- Sputtered 130 nm PZT gate
- Sputtered 195 nm PZT gate

5.6.1 TiO_2 Seeding Layer for (111)PZT

The deposition of a 2 nm TiO_2 seeding layer by magnetron sputtering favored the (111) growth of PZT on AlGaN. Without this nucleation layer random oriented PZT was grown.

5.6.2 CSD PZT

Depositing PZT by CSD methods proved highly destructive to the 2DEG due to the rapid thermal annealing process in oxygen. The best annealing process was for a time of 30 s at 700 °C, allowing for the preservation of most of the 2DEGs properties. However, this PZT(40:60) layer was not of optimal quality, since the complete elimination of all

pyrochlore phases was not possible. The PZT that is in the pyrochlore phase will act as a "dead" layer, that is it will not have the switching and retention of the spontaneous polarisation that the perovskite phase possesses.

5.6.3 PLD MgO Buffer Layer

An attempt to minimise the diffusion was done by the addition a MgO buffer layer. The deposition of MgO by pulsed laser deposition, PLD, onto AlGaN was successful since they have a small lattice mismatch. There was little degradation to the 2DEG, from conductance measurements, after the CSD deposition of randomly oriented PZT(40:60).

5.6.4 Sputtered PZT

Due the volatility of the CSD deposition process the PZT(40:60) deposition process was changed to multiple target RF magnetron sputtering. After the optimisation of this method it was possible to deposit 100% (111) textured PZT with absolutely no unwanted pyrochlore phases. This process still degraded the 2DEG but only increased the sheet resistance by a factor of three, decreased the electron sheet concentration by a factor two and decreased the mobility by a factor of two thirds.

5.6.5 Outlook

After these measurements it would have been interesting to do more depositions of sputtered PZT on AlGaN/GaN: minimising the temperature and pre-heating time of the deposition, minimising the diffusion at the interface, preserving the transport properties of the 2DEG, trying different compositions and thicker PZT films. Also of interest would have been to see how these parameters directly influence the modulation of the transport properties of the 2DEG. Especially of interest is the observation of the correlation of the PZT thickness, the Zr:Ti composition in the PZT to the modulation of the transport properties. However, it was extremely unfortunate that after the first series of successful experiments the magnetron sputtering machine had a series of mechanical and electronic failures which did not allow for further depositions of PZT.

Is PZT really the most optimal ferroelectric to be used as the gate on the AlGaN heterostructures? The combination of the two materials allow for the use in applications that have demands for high temperature and high frequency. However, for commercial use there is probably no use for lead based electronics due to environmental reasons. So for the sole reason of attempting to research towards a commercial ready device it would be more interesting to study organic ferroelectrics such as the P(VDF/TrFE) ferroelectric polymer as will be done in the following chapter 6.

The integration of PZT with GaN for the use in RF micro-electro-mechanical systems, MEMS, for bandpass filters is also being currently investigated, Dey et al. [2004]. In this configuration the switching of the spontaneous polarisation in the PZT layer is not being used but its capability of coupling with the RF signal while maintaining a stable large polarisation.

Chapter 6

P(VDF/TrFE) Deposition and Characterisation

The ferroelectric layer of poly(vinylidene fluoride/trifluoroethylene), P(VDF/TrFE), was also tried as the gate ferroelectric on the AlGaN/GaN heterostructure. It has multiple interesting characteristics, one of which being a smaller spontaneous polarisation, than PZT, of 8.5 $^{\mu C}/_{cm^2}$, which should be still sufficient to modulate the 2DEG. Another advantage is its small dielectric constant, $\epsilon_{P(VDF/TrFE)}$=13, so that when it is sandwiched with the AlGaN, $\epsilon_{Al_{0.3}Ga_{0.7}N}$=10.29, Ambacher et al. [2000], a significant amount of the voltage drops across the ferroelectric layer and not the semiconductor layer, and the depolarisation field is minimised. Lastly, and possibly most importantly P(VDF/TrFE) has a low crystallisation temperature, of 130 °C that can better preserve the great transport properties of the 2DEG, than the higher temperature processing of PZT.

This chapter will describe in detail the deposition of the co-polymer ferroelectric layer, poly(vin-ylidene fluoride/trifluoroethylene), P(VDF/TrFE), onto the AlGaN/GaN heterostructure and its characterisation. Also described will be the optimisation of the deposition process for a HfO_2 buffer layer to limit charge injection between the P(VDF/TrFE) and AlGaN layers. Listed below are the different ferroelectric, and buffer layers whose depositions were investigated in this chapter.

- Spin casted P(VDF/TrFE)(70:30)
- Sputtered HfO_2 buffer layer
- Sputtered HfO_2/Hf buffer bi-layer

After the ferroelectric and/or insulator layer was deposited various tests were done in order to characterise the ferroelectric thin film and determine if the 2DEG retained its great transport properties. The experimental investigations of the P(VDF/TrFE) and HfO_2 layers that were done in this chapter are listed below. When these results were positive it was then possible to further proceed with capacitance-voltage measurements and the fabrication of Hall bar and van der Pauw structures.

- XRD spectra
- AFM topography

- Quick resistance and sheet resistance measurements of the 2DEG
- HRTEM at the buffer/semiconductor interface
- PFM poling, retention and d_{33} hysteresis measurements
- Ferroelectric hysteresis loops

6.1 P(VDF/TrFE) MFM Structure

The full introduction to P(VDF/TrFE) and the deposition technique used here can be found in more detail in section 4.1.2. All of the films described here are deposited with the same technique and in the same manner. To induce crystallisation of the film after the spin coating, there was an annealing process on a hot plate at a temperature of $128 - 130\,^{\circ}$C for 3 min in air at atmospheric pressure. The measured thickness of these films is 250 nm. For the use in this thesis the thicker P(VDF/TrFE) ferroelectric layer grown by spin casting was preferred, compared to the Langmuir-Blodgett technique which grows thinner films, as a large enough polarisation is needed in order to accumulate enough bound charge at the semiconductor interface in order to deplete the 2DEG of its electrons.

First, the solution made by the pellets purchased from Solvay-Solexis were deposited as a layer and tested in the MFM capacitor configuration. That is the standard $Pt/TiO_2/SiO_2$/-Si substrate was used onto which was spin coated a P(VDF/TrFE) layer of approximately 250 nm. Either Cr(10 nm)/Au(100 nm) or Au(100 nm) top electrodes of diameter 200 μm were deposited using a shadow mask with joule effect evaporation. XRD diffraction spectra were taken, and polarisation-voltage, P-V, hysteresis curves were measured to characterise the ferroelectric layer.

6.1.1 XRD Analysis

XRD spectra were taken using the diffractometer described in section 3.5.3. Found in the file databases were only reference spectra for PVDF. One PVDF spectrum is referenced in appendix C and has four peaks of interest $2\theta(020)$ =18.392 °, $2\theta(110)$ =20.119 °, $2\theta(130)$ =33.194 °, and $2\theta(040)$ =37.281 °.

Literature value for XRD spectra of the co-polymer P(VDF/TrFE)(70:30) were helpful in obtaining a better understanding. All literature values for the 2θ peaks of P(VDF/TrFE) (70:30) were done with a θ-2θ XRD diffractometer with CuKα radiation. Gil et al. [1998] studied the P(VDF/TrFE)(70:30) polymer casted onto thick glass plates and measured a 2θ peak at 18.9 °. Macchi et al. [1990] studied the P(VDF/TrFE)(70:30) polymer deposited onto a Si wafer and measured a 2θ peak at 19.8 °. Lastly, Fang et al. [2005] studied the P(VDF/TrFE) (68:32) polymer casted onto thick glass plates and measured a 2θ peak at 19.9 °.

The XRD spectrum, shown in figure 6.1, was taken of P(VDF/TrFE)(70:30) with platinum bottom electrode and gold top electrode. The spectrum shows one distinct peaks to P(VDF/TrFE) at 2θ=19.72 °, which is probably the (020) peak. The fact that the peak at 2θ=19.72 ° is similar to the above literature values for P(VDF/TrFE) (70:30) gives a first positive indication of the success of the deposition process.

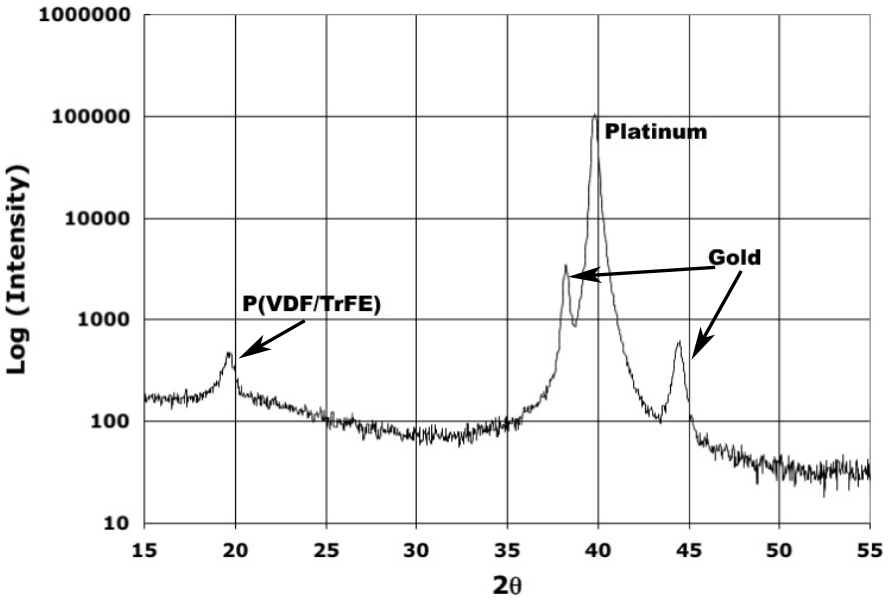
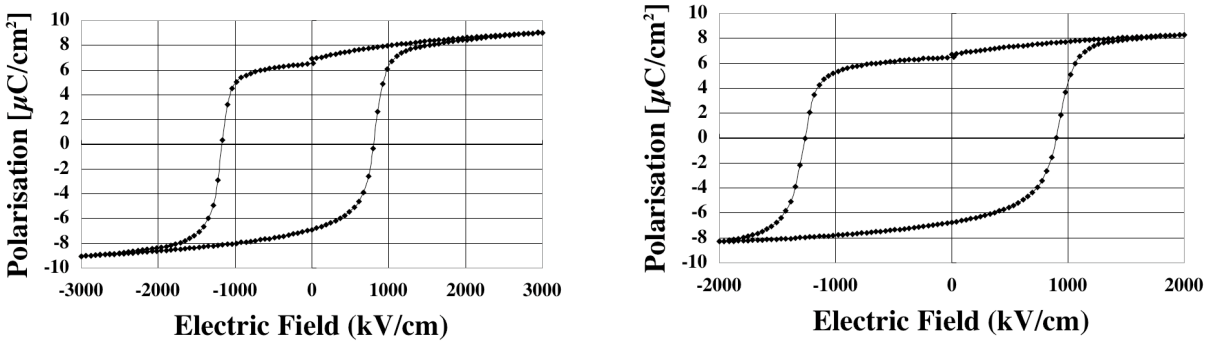


Figure 6.1: XRD spectrum of the MFM structure consisting of a Pt bottom electrode, 250 nm P(VDF/TrFE) and a Au top electrode.

6.1.2 Ferroelectric Hysteresis Loops

With Au(100 nm) top electrodes ferroelectric hysteresis loops were done with a polarisation-voltage, PV, curve in order to positively confirm the ferroelectricity of this film. The details of this measurement technique is summarised in section 3.4.1. Many polarisation voltage curves were performed on this structure while varying the maximum applied electric field and the sampling rate, the results of which are summarised in table 6.1. Two of these polarisation-voltage, P-V, curves are shown in figure 6.2. That in figure 6.2a was done at a sampling rate of 50 Hz for ±75 V and in figure 6.2b for a sampling rate of 150 Hz and ±50 V.



(a) (b)

Figure 6.2: Polarisation - electric field hysteresis loop taken of the MFM structure, Au/250 nm P(VDF/TrFE)/Pt a) with a sampling rate of 50 Hz and a maximum applied field of ±75 V and b) with sampling rate of 150 Hz and a maximum applied field of ±50 V

What can be observed from these curves is that they are all tilted a characteristic attributed to the depolarisation field, Tagantsev et al. [1995]. Also the curve is not sym-

Table 6.1: Summary of the ferroelectric (P-V) hysteresis loops shown in figure 6.2a and 6.2b on a Au/250 nm P(VDF/TrFE)/Pt/TiO_2/SiO_2/Si structure.

Frequency [**Hz**]	**Maximum E** [**kV/cm**]	**-P_r** [μ**C/cm^2**]	**+P_r** [μ**C/cm^2**]	**+E_c** [**kV/cm**]	**-E_c** [**kV/cm**]
50	3000	-6.90	6.89	796	-1163
100	3000	-6.87	6.82	877	-1242
150	3000	-7.04	6.93	980	-1286
50	2500	-6.84	6.87	817	-1173
100	2500	-6.95	6.85	919	-1275
150	2500	-6.93	6.85	969	-1326
50	2250	-6.88	6.84	827	-1193
100	2250	-6.90	6.83	919	-1240
150	2250	-6.86	6.75	919	-1285
50	2000	-6.81	6.77	817	-1183
100	2000	-6.83	6.77	857	-1224
150	2000	-6.75	6.73	898	-1265

metric that is $+P_r \neq -(-P_r)$ and $+E_c \neq -(-E_c)$. The details of the remanent polarisation and coercive field for the three polarisation vs voltage curves are summarised in table 6.1. Due to the fact that $+E_c \neq -(-E_c)$ implies that the ferroelectric film has an internal bias field, E_b which is do to some imprint in the ferroelectric film.

The XRD spectra of the P(VDF/TrFE) MFM structure and the ferroelectric hysteresis loops were two positive indications of the success of the layer deposited. With this base knowledge it was possible to advance in studying the same P(VDF/TrFE) layer in a MFS configuration.

6.2 P(VDF/TrFE) MFS Structure

Due to the success of the P(VDF/TrFE) layer in the MFM structure it was possible to continue and deposit this same ferroelectric layer onto the AlGaN/GaN heterostructure. Exactly the same deposition conditions were used as the low crystallisation temperature of $128 - 130\,^{\circ}C$ was assumed to provoke absolutely no diffusion and thus have no effect on the 2DEG. However, the first measurement done after deposition was to observe any change in the resistance of the 2DEG and the results concluded that it had no effect of permanently degrading the 2DEG. After which XRD spectra were taken and compared to that of the MFM structure in figure 6.1. Finally, the ferroelectric was characterised by PFM and piezoelectric hysteresis loops.

6.2.1 XRD Analysis

XRD spectra were taken using the diffractometer described in section 3.5.3. Section 6.1.1 gives a detailed description of the 2θ peaks that are being investigated when observing the XRD spectra of the co-polymer P(VDF/TrFE)(70:30). The XRD spectrum of the

P(VDF/TrFE) layer deposited onto the AlGaN heterostructure is shown in figure 6.3. The measured peak corresponding to the P(VDF/TrFE) layer is 2θ=19.84 °, the (020) peak. This 2θ peak has a small deviation from the XRD spectrum of the P(VDF/TrFE) layer in the MFM structure, figure 6.1, and is similar to the literature values by Gil et al. [1998], Macchi et al. [1990], and Fang et al. [2005]. The XRD spectrum of the P(VDF/TrFE) layer, figure 6.3, is a positive indication of having deposited a high quality ferroelectric layer onto the AlGaN heterostructure.

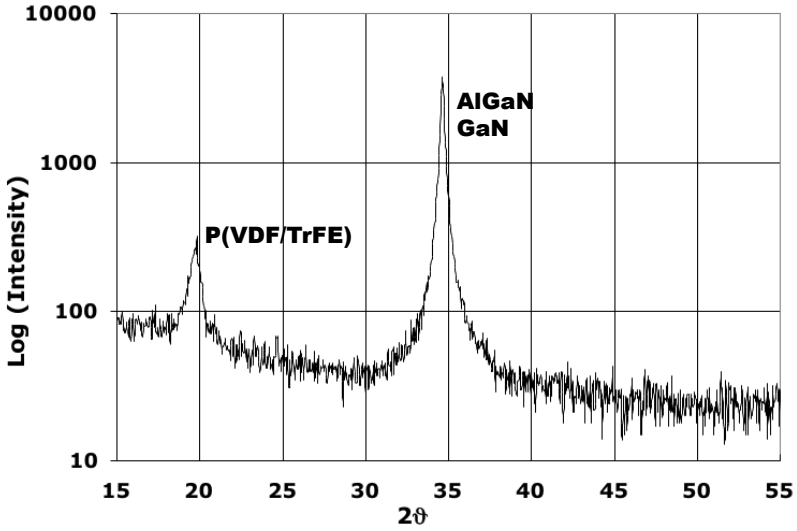
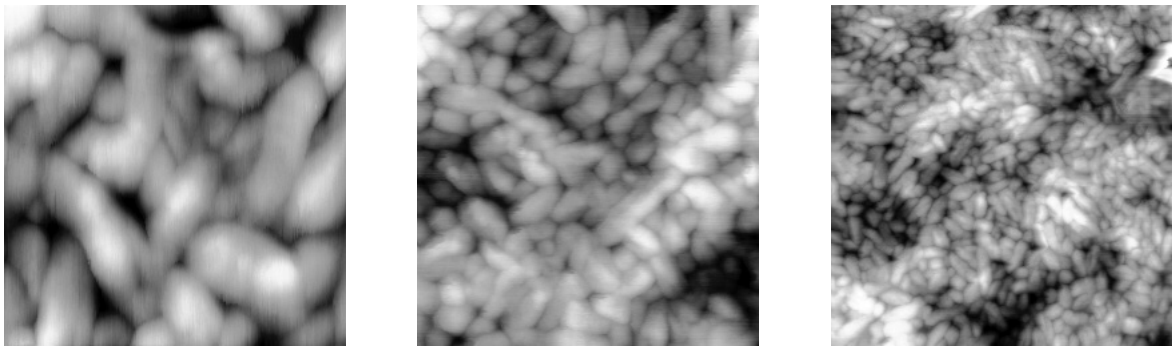


Figure 6.3: XRD spectrum of 250 nm P(VDF/TrFE) deposited onto AlGaN.

6.2.2 Topography

The topography was done with an AFM in the non contact mode to ensure the best quality imaging with no scratching of the soft polymer layer. Topographies, showing the cylinder grain structure, of different areas were obtained: figure 6.4a 0.5x0.5 μm^2, figure 6.4b 1x1 μm^2 and figure 6.4c 2x2 μm^2.



(a) (b) (c)

Figure 6.4: SFM topographies, done with non contact imaging, of 250 nm P(VDF/TrFE)/AlGaN of areas a) 0.5x0.5 μm^2 b) 1x1 μm^2 c) 2x2 μm^2.

6.2.3 Poling and Retention with PFM

The use of the piezoresponse force microscope, PFM, in characterising the ferroelectric film on the AlGaN/GaN heterostructure was useful, since no device processing was necessary. This technique was particularly helpful in observing if the P(VDF/TrFE) layer deposited onto the AlGaN/GaN heterostructure was or was not capable of being poled and retaining its polarisation. The initial test of a 250 nm thick P(VDF/TrFE)/AlGaN/GaN structure gave a positive indication of efficient poling with long term retention.

The initial state of the polarisation in the P(VDF/TrFE) polymer film was random, this random orientation is visible in the non poled regions of the PFM image in figure 6.5. The first poling test consisted of poling an area of 1x1 μm^2 which was scanned in the y-direction and a line covering less than 1% of 1 μm (that is 3 out of the 256 lines, or 0.01 μm) was poled with +30 V. PFM piezoresponse images were then taken of an enlarged area of 2x2 μm^2, immediately after poling. The piezoresponse vertical phase signal is shown in figure 6.5a and the piezoresponse vertical amplitude signal is shown in figure 6.5b. The line resolution of these two images was approximately 700 nm.

The retention of this polarisation pattern was tested after 20 hrs showing little decay or relaxation of the written pattern. The piezoresponse images, after 20 hrs, are shown with the vertical phase signal in figure 6.5c and that of the vertical amplitude in figure 6.5d.

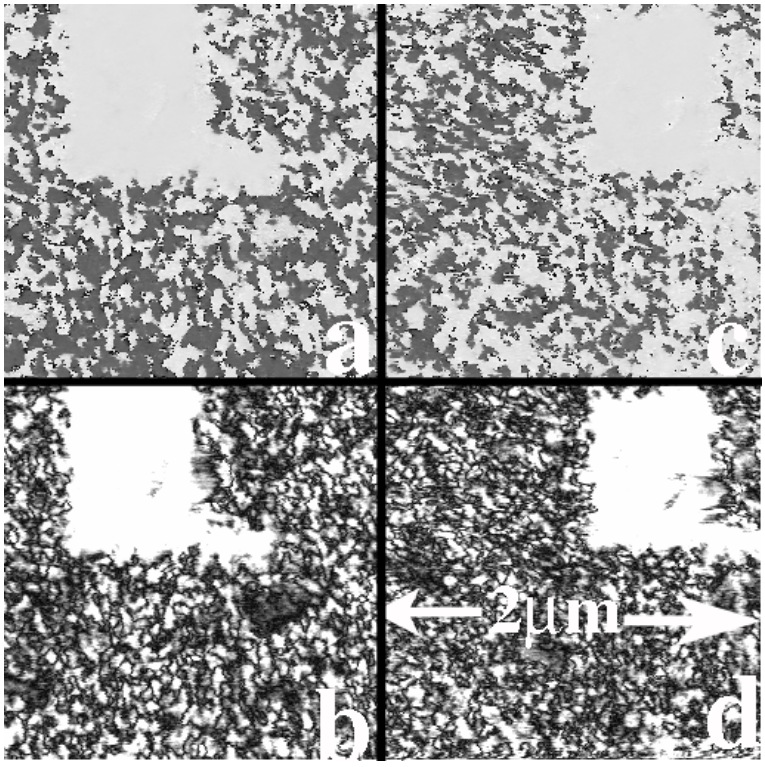
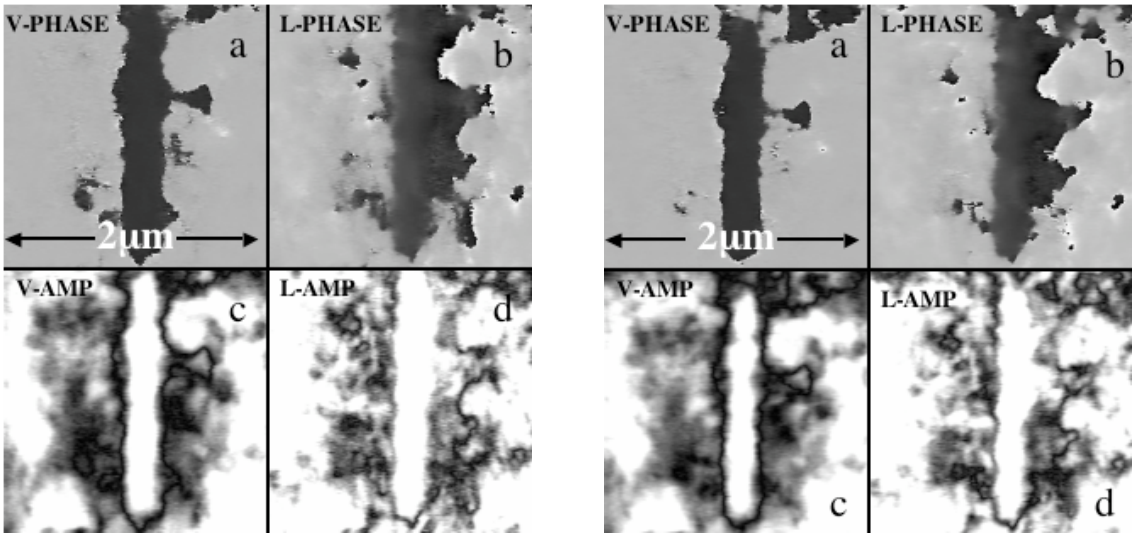


Figure 6.5: A P(VDF/TrFE)/AlGaN structure where the area of 1x1 μm^2 was scanned in the y direction and a line covering less than 1% of 1 μm (that is 3 out of the 256 lines) was poled with with +30 V. PFM piezoresponse images were then taken of an area of 2x2 μm^2 immediately after poling a) the vertical phase and b) the vertical amplitude and 20 hrs after poling c) the vertical phase and d) the vertical amplitude.

Since the line resolution, of the image, in figure 6.5, was approximately 700 nm the scanning parameters were changed; primarily an increase in the scanning area to improve this

resolution. The same sample was used and was poled with −30 V to the complete area of 2x2 μm^2. After which a line covering less than 1% of 2 μm (that is 2 out of the 256 lines, or 0.02 μm) was poled with with +30 V. PFM piezoresponse images were then taken of an area of 2x2 μm^2 immediately after the poling, figure 6.6a. The retention of this poled state 116 hrs after poling was also measured and is shown in figure 6.6b. The abbreviations: V-PHASE is the vertical phase, V-AMPLITUDE is the vertical amplitude, L-PHASE is the lateral phase and L-AMPLITUDE is the lateral amplitude. It was possible to minimise the line resolution of the written pattern to 300 nm with which it was possible to pole the ferroelectric layer when the conducting cantilever was scanning directly the ferroelectric layer.



(a) (b)

Figure 6.6: The 250 nm spin casted P(VDF/TrFE)/AlGaN structure was poled with −30 V in an area of 2x2 μm^2 after which a line covering less than 1% of 2 μm (that is 2 out of the 256 lines) was poled with with +30 V. PFM piezoresponse images were then done of an area of 2x2 μm^2 a) immediately after poling and b) 116 hrs after poling. The piezoresponse signal is divided into: V-PHASE is the vertical phase, V-AMPLITUDE is the vertical amplitude, L-PHASE is the lateral phase and L-AMPLITUDE is the lateral amplitude.

These PFM images and measurements allowed for confirming that this P(VDF/TrFE) was indeed ferroelectric with long term retention. Even though the retention was only measured for 116 hrs after poling, it is assumed that the real retention is much longer since there was no decrease in the amplitude of the piezoresponse signal immediately after poling to 116 hrs after poling. Therefore, it was possible to observe with these measurements that under the ideal conditions it is possible to almost permanently switch the polarisation. However, it does not allow for the observation of the modulation of the electrons in the 2DEG, for this more comprehensive electrical resistance and transport measurements need to be performed.

6.2.4 Piezoelectric Hysteresis

Piezoelectric hysteresis loops were done on a capacitor structure, that is a non etched sample with top electrodes of diameter 200 μm deposited on 250 nm of P(VDF/TrFE).

These piezoelectric hysteresis loops were done with the PFM setup with a special software designed to observe the piezoresponse of the film after the application of a DC bias. The signal received from the lock-in amplifier is proportional but not equal to the piezoelectric coefficient, d_{33}, and can thus be calibrated to be approximately equal to d_{33}.

The top electrode Cr/Au, 10/100 nm, was deposited by joule effect evaporation. The size of top electrodes used was a circular shape of diameter 200 μm, and the bottom electrode used was indium. The piezoresponse measurements were then made by keeping the AFM tip static and varying the DC voltage applied to the bottom electrode, the AC modulation voltage was also applied to the bottom electrode. The top electrode was grounded, as was the conductive AFM tip.

The calibration of the piezoresponse measured by the PFM was taken from previous measurements by Buhlmann [2004] who used exactly the same PFM setup as is used in these experiments and thesis. They measured a 600 nm epitaxial PZT sample on conductive Nb-doped $SrTiO_3$ (100) with platinum top electrodes quantitatively with a double-beam interferometer, Kholkin et al. [1996]. These values then allowed for a conversion of the separated piezoresponse signal from the lock in amplifier to a quantitative piezoresponse measurement. The approximation of the d_{33} coefficient was done by taking the vertical amplitude response from the lock in amplifier (in μV) and modifying it by a calibration factor.

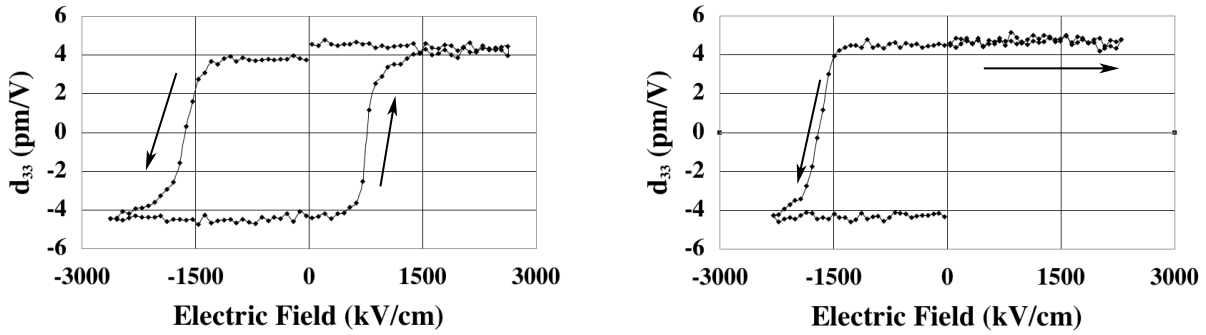


Figure 6.7: PFM hysteresis loop of a 250 nm P(VDF/TrFE)/AlGaN structure. a) The negative voltage is applied first. b) The positive voltage is applied first, observe the retention.

For the reason of continuity in the thesis the electric field noted in figures 6.7a and b, and the text that discusses them, is in such a way that a negative electric field is such as the negative DC bias is applied to the top electrode and there is a depletion of electrons in the 2DEG.

The measured piezoelectric hysteresis curves are antisymmetric and give coercive fields of $-0.8\,^{\mathrm{MV}}/_{\mathrm{cm}}$ and $1.65\,^{\mathrm{MV}}/_{\mathrm{cm}}$ indicating the presence of a internal bias field. In the case of a depolarisation field due to an passive layer in series with the ferroelectric layer, a tilting of the polarisation vs electric field hysteresis loop is expected, Tagantsev et al. [1995]. As the passive layer increases so does the depolarisation field and with it so increases the tilt in the hysteresis loop. In figure 6.7a, and 6.7b there is no tilting in the piezoelectric loops, implying that there is no depolarisation field. This could be so do to the slow measuring of the total polarisation in the system allowing for the increase of charge compensation which eliminates the depolarisation field. Due to the small measuring cycling

used for piezoelectric loops the total polarisation of the P(VDF/TrFE)/AlGaN structure is measured and can reduce measuring injected charge and spontaneous polarisaiton.

Table 6.2: Summary of the piezoelectric (d_{33} vs electric field) hysteresis loops shown in figure 6.7a and 6.7b on a Au/250 nm P(VDF/TrFE)/AlGaN/GaN structure. E_c is calculated by using the total thickness of the ferroelectric and AlGaN layers.

Figure [No.]	**-d_{33} [pm/V]**	**+d_{33} [pm/V]**	**+E_c [kV/cm]**	**-E_c [kV/cm]**
6.7a	-4.5	4.5	750	-1650
6.7b	-4.6	4.7	n/a	-1650

6.3 HfO_2 Buffer Layer

HfO_2 has great potential as a buffer layer in ferroelectric/semiconductor structures because it has a high dielectric constant, ϵ=25 and a large band-gap 5.7 eV. Takahashi et al. [2005], and Aizawa et al. [2004] have used HfO_2 as a inter-diffusion barrier layer for silicon semiconductor substrates before the deposition of the ferroelectric gates $SrBi_2Ta_2O_9$ and $(BiLa)_4Ti_3O_{12}$. The initial idea standing behind the development of the HfO_2 deposition process was also to use it as a buffer layer for limiting the diffusion between the ferroelectric, PZT, and AlGaN layers. A secondary concept is to implement HfO_2 or another buffer layer in order to passivate the surface traps at the interface, which can increase the electron sheet concentration in AlGaN/GaN, metal-oxide-semiconductor high electron mobility transistors, MOS-HEMTs, Liu et al. [2006]. The final reason for optimising the HfO_2 deposition process on AlGaN was to see how this layer operates in limiting injected charge when using a P(VDF/TrFE) ferroelectric layer. Ideally the large band gap of HfO_2 should allow for less charge leakage, possibly improving the bi-stability of the spontaneous polarisation, resulting in better polarisation retention.

6.3.1 HfO_2 Deposition

HfO_2 was deposited with RF magnetron sputtering using a hafnium target with a constant flow of both the reactive gas oxygen and the inert gas argon. When sputtering oxide layers it is more beneficial to use a metal target for multiple reasons. The metal targets are easier to produce, with a larger thermal conductivity than an oxide target allowing for larger power densities, the target can be used for depositions of multiple materials (i.e. pure metal, oxide, nitride...), and the deposition rate is larger. The disadvantages of using a metal target is that it may be difficult to control the composition and to have good uniformity on large surfaces, Muralt [1995-2005]. RF sputtering was used in order to avoid charge build up on the hafnium target and anode after covering these parts with the insulating HfO_2 layer.

Lu et al. [2006], Chien et al. [2003] and Takahashi et al. [2005] attempted to deposit HfO_2 by various methods such as atomic vapor deposition, AVD, electron beam evaporation and laser molecular beam epitaxy, LMBE. The important point is that the deposition temperature was always higher than 400 °C, or a high temperature post-deposition RTA

annealing process was done in oxygen and nitrogen, in order to assure for the growth of a high crystalline quality HfO_2 layer with a high dielectric constant. One of the main problems in their depositions was the diffusion of oxygen into the silicon substrate creating a low dielectric constant intermediate layer of SiO_2 which consumes a large part of the voltage that is applied across the sandwiched ferroelectric/insulator/semiconductor structure. The maximum temperature of the setup used here, 300 °C, was chosen in hope that this temperature was sufficient for the crystallisation of the HfO_2 layer. This left the two parameters of RF power and the oxygen gas flow rate as variables to optimise the deposition process. The post-deposition annealing steps performed by Chien et al. [2003] and Takahashi et al. [2005] are most likely too volatile, since it was learned when depositing CSD PZT that the 2DEG is extremely sensitive to the final step of high temperature annealing in oxygen.

To optimise the deposition of crystalline oxides by sputter deposition it is usual to locate the best flow of oxygen in the return curve of the total oxygen flow vs voltage hysteresis loop, right inside the hysteresis loop where the voltage takes the dramatic decrease to metallic deposition. This DC voltage is auto biasing between the same cathode and anode to which the RF is applied and depends highly on the interactions of the ions in the chamber. The reason why these conditions are chosen is that the deposition rate is usually at it's highest for a stoichiometric film. However, due to the small flow of oxygen there could be insufficient oxygen leading to oxygen vacancies and being located inside the hysteresis loop allows for less stable deposition conditions, implying that the deposition parameters could fluctuate. For the growth of HfO_2 as buffer layer the effect of certain growth properties can be considered negligible. As the buffer layer thickness will be on the order of approximately 5 nm the deposition rate is not important for the speed of production. Using a larger oxygen flow outside of the hysteresis loop will lead to a decreased amount of oxygen vacancies, also the deposition will be more stable when located outside of the hysteresis loop. The RF power and oxygen flow parameters will be the two variables in the following experiments.

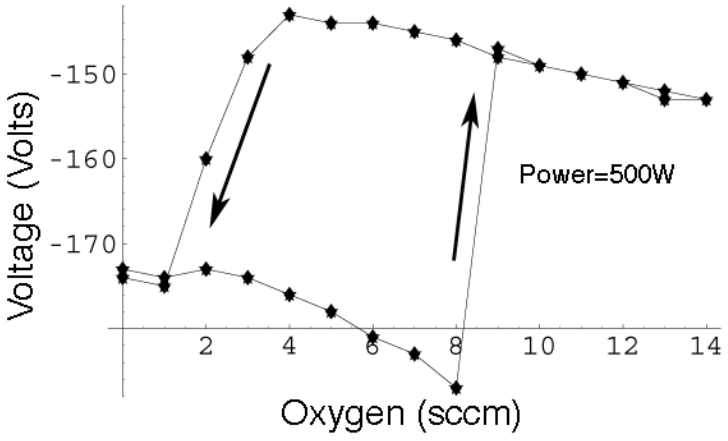


Figure 6.8: At an RF power of 500 W, temperature 300 °C and a flow of 33 sccm of argon the voltage vs. oxygen flow hysteresis. A minimal oxygen flow rate of 4 sccm was necessary to ensure the deposition of an oxide layer.

There is a preference to minimise the RF power used in the deposition of thin oxide films for the main reason that it is possible to deposit an oxide at smaller oxygen pressures. The use of a low RF power allows for the deposition to be done with a larger DC voltage

and with oxygen ions of low energy. This can be clearly seen in figure 6.8 and figure 6.9. With the RF sputtering system used it was possible to vary the RF power from 500 W to 1000 W, these two extreme settings were thus chosen in helping to determine what oxygen flow rate and RF power to use. The hysteresis, voltage vs oxygen flow, curve in figure 6.8 is done at an RF power of 500 W and shows a transition from the deposition of an oxide to a metal at an oxygen flow rate of approximately 4 sccm. Whereas, figure 6.9 measured at a RF power of 1000 W shows a transition from the oxide to metallic phase at an oxygen flow rate of approximately 6 sccm. The graphs shown in figure 6.8 and 6.9 were instrumental in determining the oxygen flow necessary in order to deposit an oxide. It was determined to use an RF power of 500 W and vary the oxygen flow rate to further optimise the deposition process.

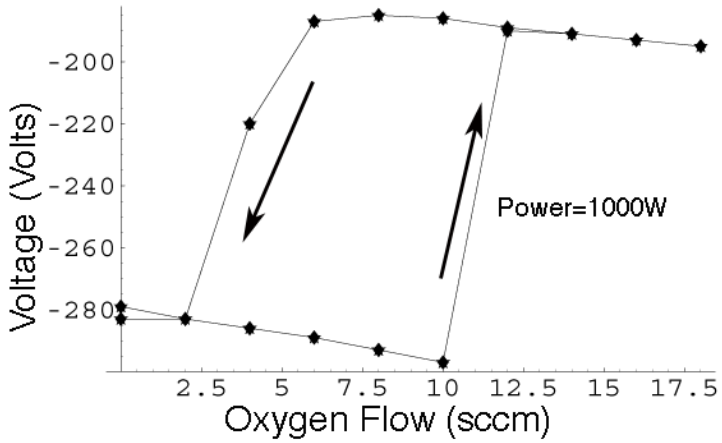


Figure 6.9: At an RF power of 1000 W, temperature 300 °C and a flow of 33 sccm of argon the voltage vs. oxygen flow hysteresis. A minimal oxygen flow rate of 6 sccm was necessary to ensure the deposition of an oxide layer.

6.3.2 HfO_2/AlGaN Characterisation

Table 6.3: Deposition conditions of HfO_2 on AlGaN at a constant pressure of $4.4x10^{-3}$ Torr, 500 W and 300 °C. Including the deposition rate and an indication of a positive XRD diffraction spectrum.

Sample	**Oxygen** [sccm]	**Ar** [sccm]	**Voltage** [V]	**Rate** [Å/min]	**XRD**
C6B1588	18	14	-171	5.8	Yes
C7B1594	4	28	-152	6.67	Yes
C7B1595	8	24	-150	8.33	Yes
C7B1596	12	20	-148	11.67	Yes

Some of the depositions done are summarised in table 6.3, with an RF power of 500 W, at a constant pressure of $4.4x10^{-3}$ Torr, and at 300 °C. The oxygen flow was varied and the argon flow was adjusted in order to guarantee a constant pressure. The deposition rate was determined by measuring the thickness with an alpha step profilometer, for the

known deposition time. Since the HfO_2 layer is only to be a few nanometers thick the deposition rate is not of importance other than controlling the deposited amount. The fastest deposition rate was measured as $11.67\,\text{Å}/\text{min}$ with an oxygen flow rate of 12 sccm, however this characteristic alone does not allow for the best quality of film deposited. It was more important to study the composition of the layer deposited using XRD to observe the appropriate peaks corresponding to HfO_2. Although in table 6.3 it is noted Yes to the XRD spectrum more anlaysis of these spectra are necessary for a complete understanding.

XRD Spectra

The XRD spectra in figures 6.10 to 6.13 show the same peaks representing HfO_2 deposited on the AlGaN/GaN/sapphire substrates, but vary between each other. In general the films are of sufficient quality to use as a buffer layer for the growth of ferroelectric layers. The XRD spectra were matched to the database file no. 34-104, described in further detail in appendix C. The three peaks of interest were 2θ(-111) =28.366 °, 2θ(-222) =58.635 ° and 2θ(311) =61.759 °.

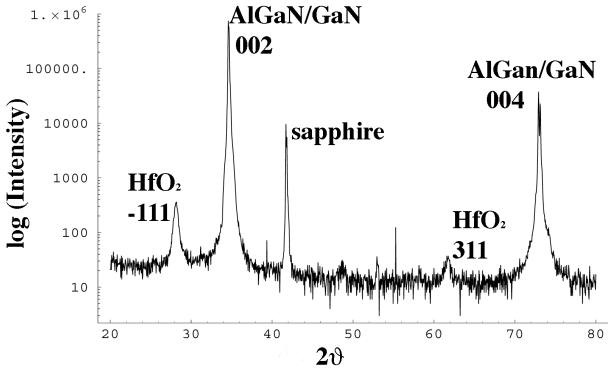


Figure 6.10: XRD spectrum of HfO_2 grown on AlGaN/GaN heterostructure with a total flow of oxygen 4 sccm.

Since all of these samples were deposited at the same conditions only varying the oxygen it is possible to see the importance of the oxygen flow rate has during deposition. There

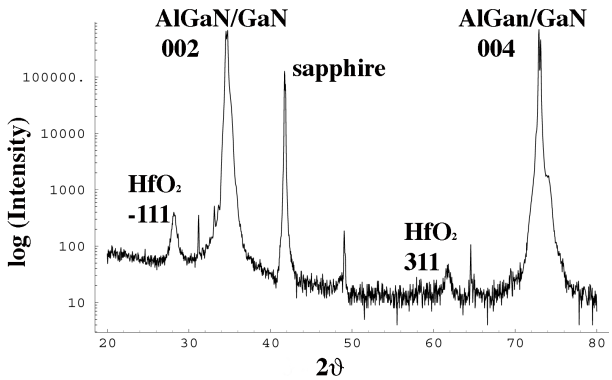


Figure 6.11: XRD spectrum of HfO_2 grown on AlGaN/GaN heterostructure with a total flow of oxygen 8 sccm.

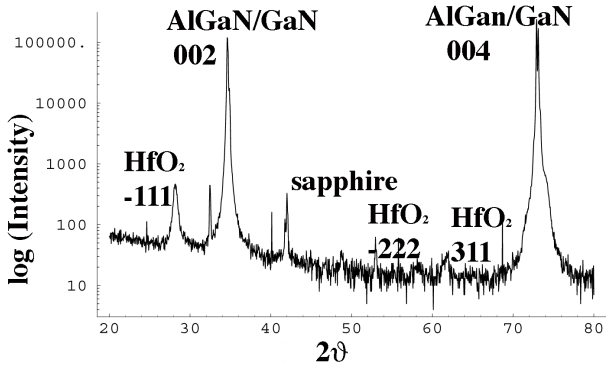


Figure 6.12: XRD spectrum of HfO_2 grown on AlGaN/GaN heterostructure with a total flow of oxygen 12 sccm.

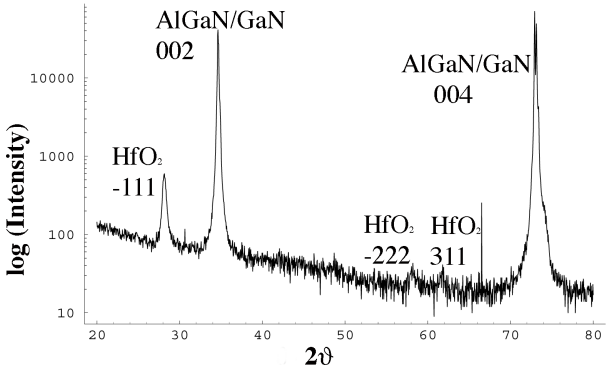


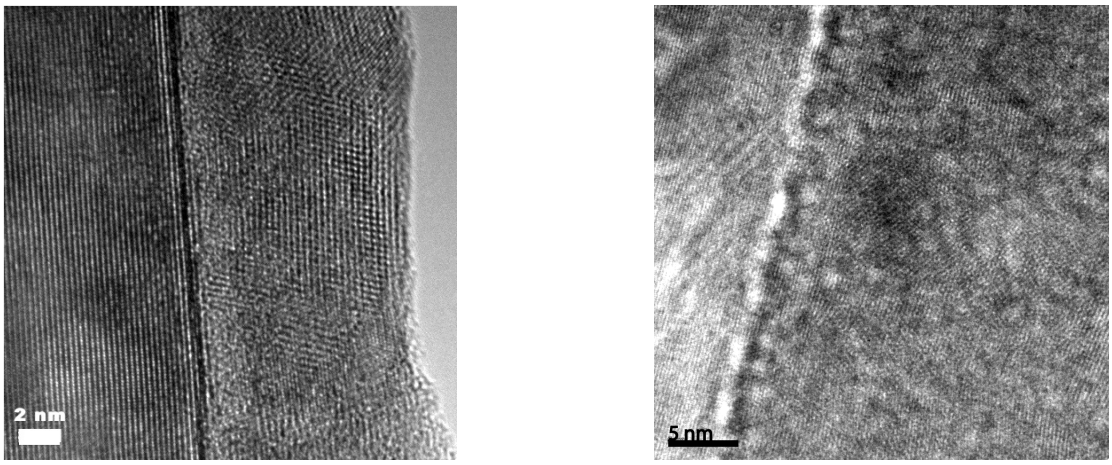
Figure 6.13: XRD spectrum of HfO_2 grown on AlGaN/GaN heterostructure with a total flow of oxygen 18 sccm.

is some presence of amorphous states due to the gentle decline of the intensity at the small angles in all spectra. This is most present and visible in the samples that were prepared with large oxygen flow rates, figures 6.11 to 6.13. The XRD spectrum in figure 6.10 deposited with an oxygen flow of 4 sccm exhibits the cleanest xray spectrum of the four samples deposited.

The sample deposited with an oxygen flow of 12 sccm had the fastest deposition rate which led to a thick layer, however it was observed in its XRD spectrum that the crystallinity of this film was of poor quality. The sample deposited with an oxygen flow of 4 sccm gave the cleanest spectrum, with little tilting at small angles due to amorphous phases, and possesses a respectable deposition rate.

HRTEM imaging

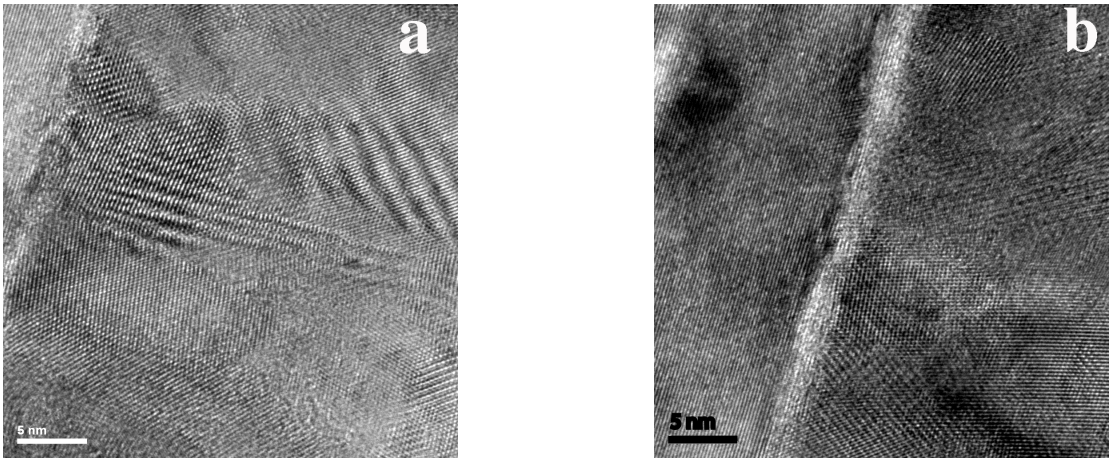
The HRTEM images of the samples deposited with oxygen flow rates of 4 sccm and 8 sccm are shown in figure 6.14. In figure 6.14a is the HRTEM image of the HfO_2/AlGaN interface where the HfO_2 was deposited with a total oxygen flow rate of 4 sccm. This sample exhibited the least amount of defects compared to the samples deposited with higher oxygen flow rates. The sample deposited with a flow rate of 8 sccm of oxygen shows relative good crystallinity in 6.14b. However, one can already see from this image that dislocations start to exist that propagate through the whole thickness of the film.



(a) (b)

Figure 6.14: HRTEM of HfO_2 grown on AlGaN/GaN heterostructure with a) a total flow of oxygen 4 sccm and b) a total flow of oxygen 8 sccm.

The sample deposited with an oxygen flow rate of 18 sccm has its HRTEM image shown in figure 6.15. This image shows even more dislocations than is observed in figure 6.14b when using an oxygen flow rate of 8 sccm.



(a) (b)

Figure 6.15: Two HRTEM images of the same HfO_2 grown on AlGaN/GaN heterostructure with a total flow of oxygen 18 sccm.

The HRTEM analysis at the HfO_2/AlGaN interface allowed for the observation of less dislocations, better crystallinity, and a cleaner interface when depositions occurred using the smallest oxygen flow rate of 4 sccm. Combining the results from the alpha step, XRD spectra and HRTEM imaging it was possible to determine the best deposition conditions for the RF sputtering machine used. The deposition at a flow rate of 4 sccm oxygen, occurring at 300 °C, with RF power 500 W, produces the highest quality HfO_2 with a deposition rate sufficient for the deposition of "ultra"-thin films.

6.3.3 Wet Etching of HfO_2

It was difficult to process samples with HfO_2 since it was not possible to determine a wet etching process for it, being unsuccessful with a HF solution of concentration greater than 20%. Chen et al. [2006] investigated the wet etching properties of Hf materials and HfO_2 materials with different deposition techniques and different chemical etching solutions. In regards to HfO_2 the etching rate was faster for those grown by physical vapor deposition, PVD, techniques in compared to those grown by chemical vapor deposition, CVD, techniques. The fastest etching rates being with the chemical solution composing of hydrofluoric acid, with the fastest etching rate of $30\,^{nm}/_{min}$ being for the PVD HfO_2 sample etched with a chemical solution with 10% hydrofluoric acid. So a question is left here to as why the samples of Chen et al. [2006] were able to be etched even with a chemical solution of 10% of hydrofluoric acid whereas the samples deposited here were unaffected by a chemical solution of 20% hydrofluoric acid. It is uncertain why it was not possible to wet etch the HfO_2 layer.

6.3.4 Survival of 2DEG

Van der Pauw structures of 1x1 cm^2 were grown with shadow masks with the standard annealed Ti/Al/Ti/Au bottom electrodes. Two samples were deposited with different oxygen flow rates in order to determine if there was a change in the sheet resistance of the 2DEG due to the HfO_2 deposition. First approximately 5 nm of HfO_2 was deposited with a oxygen flow rate of 8 sccm, at 300 °C with RF power 500 W. The sheet resistance increased due to this processing and was measured to be 2540 Ω/□ showing a degradation in the 2DEG. Another AlGaN sample had 5 nm of HfO_2 deposited onto it at a oxygen flow rate of 4 sccm at 300 °C with RF power 500 W. The sheet resistance in the 2DEG of this AlGaN sample also increased and was measured to be 2266 Ω/□ showing a degradation in the 2DEG that is larger than when PZT is deposited onto it. Using this magnetron sputtering setup it has been shown that the HfO_2 deposition process is volatile to the 2DEG in the AlGaN heterostructure.

It is assumed that there is oxygen diffusion during the deposition process which leads to the degradation of the 2DEG since it is known that the PVDF process does not affect the 2DEG. However, it is interesting that an oxygen deposition at 300 °C does destroy the 2DEG. Clearly the HfO_2 deposition process is more volatile than that of depositing PZT, where the sheet resistance increases only to 1270 Ω/□.

As mentioned in section 2.5.1, HfO_2 was successfully used as a buffer layer for SBT/HfO_2/Si and BLT/HfO_2/Si FeFETs by Takahashi et al. [2005], and Aizawa et al. [2004]. The HfO_2 was annealed in oxygen at 800 °C for 1 min. Does an intermediary SiO_2 layer really allow for the silicon substrate to sustain such a high temperature annealing process in oxygen?

6.3.5 Bi-Layered HfO_2/Hf Buffer Layer

Assuming that it was the initial oxygen flow that degraded the AlGaN layer and its 2DEG, it was of interest to try the two step deposition process presented by Lu et al. [2006] done on silicon. That is deposit approximately 3 nm of pure Hf and then a few nanometers of HfO_2, in an attempt to minimise the degradation of the 2DEG.

To determine the deposition rate of the hafnium layer, a layer of pure hafnium was RF sputtered at 300 °C with a constant flow of 33 sccm argon for 60 min. The measured thickness deposited with an alpha step profilometer was 201 nm giving a deposition rate of 3.35 $^{nm}/_{min}$. The XRD diffraction pattern of this sample was representative of hexagonal (001) hafnium, only one peak was present at 32.7 ° which is similar enough to the database file summarised in appendix C. The capability to deposit such a high quality hafnium layer can not be surprising as there is only a small in-plane lattice mismatch between it and AlGaN, that of hafnium being 3.32 Å and that of GaN being approximately 3.186 Å, see appendix C.

A trial deposition was done in order to observe this possibility with a layer of hafnium deposited by RF sputtering for 60 s for a thickness of 3.35 nm onto the AlGaN layer at 300 °C with a constant flow of 33 sccm of argon. After which oxygen was quickly introduced for 2 s at 33 sccm and reduced to the deposition flow rate of 4 sccm for the HfO_2 layer. The deposition was done for 180 s (approximately 2 nm) at 300 °C, 500 W and an argon flow rate of 28 sccm. The benefits of this method was evident as there was no increase in the two point probe resistance measurements using this double layer deposition process, making it the ideal buffer layer for AlGaN based devices.

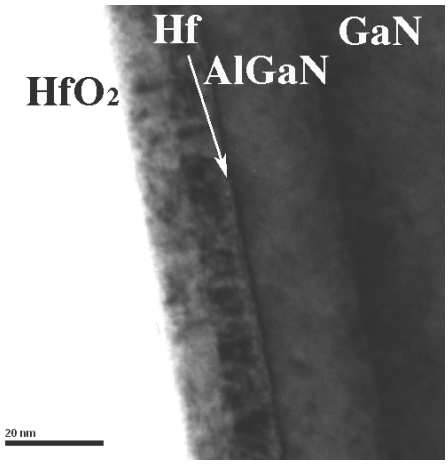
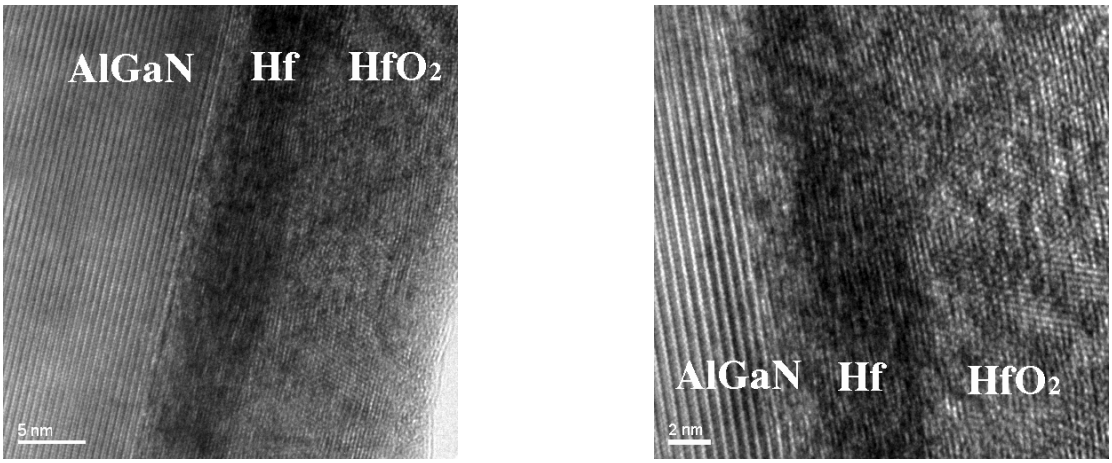


Figure 6.16: TEM image of HfO_2/Hf/AlGaN/GaN interfaces. Where at constant pressure, 4.4x10^{-3} Torr, and temperature, 300 °C, hafnium was deposited by RF sputtering for 60 s and HfO_2 was deposited by RF sputtering for 180 s with a total oxygen flow of 4 sccm.

Making a linear extrapolation to estimate the thickness of the hafnium layers deposited was not accurate as can be seen in the TEM image in figure 6.16. From the TEM image it is possible to measure the hafnium layer as approximately 8 nm and the HfO_2 layer as 9 nm. The hafnium layer alone was too thick and will most likely act as a metallic layer and screen all of the polarisation from the 2DEG. The HfO_2 layer was also too thick to act as an efficient buffer layer. The hafnium layer is being deposited to limit the diffusion of oxygen into the AlGaN heterostructure, but should ideally be consumed with oxygen during the HfO_2 deposition process so that there is absolutely no metallic layer in the buffer layer. It is thought possible that in figure 6.16 that the arrow is pointing to a layer of hafnium that did not get at all affected by oxygen and is left to screen the polarisation from the 2DEG. The HRTEM images confirm this, figure , in that it is possible to use the layer of hafnium still existing, as it was not consumed with oxygen. It is possible to observe a layer of approximately 6 nm of hafnium that remains to screen the 2DEG from the ferroelectric polarisation. This is noted since the hafnium layer has a higher

density than HfO_2, which is observed from the darker contrast in the HRTEM image. It is possible to observe in figure 6.17b that the layers deposited are of high crystalline qualitty, however it is possible that the HfO_2 deposited on Hf is not the same as when it is deposited directly on AlGaN. It would thus be of interest to deposit a thicker layer and observe its XRD diffraction spectrum. The experiments involved in optimising this buffer layer is not exhausted and it is of interest to minimise both these layers while preserving the transport properties of the 2DEG.



(a) (b)

Figure 6.17: Two HRTEM images of the same HfO_2/Hf layer grown on AlGaN/GaN heterostructure. Where at constant pressure, $4.4x10^{-3}$ Torr, and temperature, 300 °C, hafnium was deposited by RF sputtering for 60 s and HfO_2 was deposited by RF sputtering for 180 s with a total oxygen flow of 4 sccm.

Another two layered attempt was done with a deposition time of approximately 30 s to deposit a thinner layer hafnium, 4 nm. After which an oxygen flow of 4 sccm was introduced and the argon flow reduced to 28 sccm for the deposition of approximately 2 nm(180 s) of HfO_2. To control the 2DEG two point probe resistance measurements were done, with the Ti/Al/Ti/Au electrodes annealed in nitrogen, the resistance changed from 0.56 kΩ to 0.7 kΩ showing a small and unsubstantial degradation. The important thing to note here is that this sample had no visible metallic look due to the deposition of a thinner hafnium layer, while the above sample with 8 nm of hafnium showed a metallic appearance.

6.4 Summary

P(VDF/TrFE)(70:30) was deposited onto the AlGaN/GaN heterostructure and then tested for ferroelectricity. The use of an additional HfO_2 buffer layer was also investigated to reduce charge leakage. The samples that successfully underwent testing in this chapter and will be used for depletion experiments in chapter 7 are:

- Spin casted 250 nm P(VDF/TrFE) gate
- Spin casted 250 nm P(VDF/TrFE) gate with a 5 nm HfO_2 buffer layer

- Spin casted 250 nm P(VDF/TrFE) gate with a 9 nm HfO_2/8 nm Hf buffer layer
- Spin casted 250 nm P(VDF/TrFE) gate with a 9 nm HfO_2/4 nm Hf buffer layer

6.4.1 P(VDF/TrFE)

P(VDF/TrFE)(70:30) was successfully deposited onto AlGaN. As its crystallisation temperature is 130 °C it was possible to deposit it without any change to the transport properties of the 2DEG. Ferroelectric retention was also observed in poling experiments using the PFM showing no decrease in the piezoresponse signal 116 hrs after switching.

6.4.2 HfO_2 Buffer Layer

A technique for the deposition of HfO_2 on AlGaN was implemented for possible use as a buffer layer. Unfortunately, the sheet resistance measurements done showed a larger degradation of the sheet resistance than when depositing PZT by sputtering. After the deposition of 5 nm of HfO_2 the sheet resistance increase by a factor six. It would thus be used as a buffer layer to decrease injected charge and reduce the leakage charge instead of being a buffer layer to conserve the properties of the 2DEG.

The optimal way to cause absolutely no degradation to the sheet resistance of the 2DEG in the AlGaN/GaN heterostructure was to use a two step deposition process of hafnium and then HfO_2. The hafnium layer deposited was 4 nm and the HfO_2 layer was 9 nm. With this technique it was possible to deposit a buffer layer without destroying the transport properties of the 2DEG. It is of interest to minimise further both the Hf and HfO_2 layers to possibly obtain better retention of the depletion effect due to the ferroelectric polarisation. Investigating this buffer bi-layer for limiting the diffusion when depositing PZT on AlGaN can be informative.

Chapter 7

Ferroelectric Gate Operation

The final goal in investigating the ferroelectric/heterostructure device is to study the sheet resistance, electron concentration, and mobility in the 2DEG as a function of polarisation in the ferroelectric layer. This is to be done with sheet resistance measurements and detailed Hall measurements at room temperature as well as at lower temperatures. Measurements have been done using the PFM to pole the active area, inducing the depletion of electrons in the 2DEG and by poling directly a top electrode deposited on the ferroelectric. Top electrodes facilitate transport measurements but the deposition process of the metal layer can create a dead layer in-between the ferroelectric and electrode. With a top electrode it is also possible to make C-V measurements which can give an insight to the capabilities of depletion and the retention of this depletion without extensive processing of devices.

By controlling the polarisation orientation in the PZT layer we show that it is possible to deplete the 2DEG of electrons in the AlGaN/GaN heterostructure, exploiting the concept of field effect transistor with ferroelectric gate. The major difference between this device and the conventional transistor is the gate consisting of a ferroelectric thin film, see figure 7.1. When the ferroelectric is poled, positive or negative bound charge is induced at the interface, provoking accumulation of compensating charge in the semiconductor and resulting in the depletion or accumulation of the charge in the channel depending on the poled state. The principal benefit of this structure in comparison to the traditional metal oxide semiconductor transistors is that the modulation of the channels current also occurs after the gate voltage is turned off, giving a transistor with memory retention.

7.1 Method

There are two different methods that are used in this thesis to prove the depletion effect in the 2DEG with a ferroelectric gate. The simplest is to make C-V measurements, section 3.4.2, from which it is possible to estimate the electron sheet concentration in the 2DEG, Shen et al. [2002]. The benefit of using C-V measurements is that less device processing is necessary and it allows for the estimation/understanding of how a ferroelectric layer depletes the 2DEG and the retention possibilities of this depletion. For more fundamental knowledge, structures are fabricated with which it is possible to make transport measurements, consult section 3.1. With these methods it is possible to control the change in sheet resistance, mobility and electron sheet concentration after applying a DC gate voltage to

the ferroelectric layer.

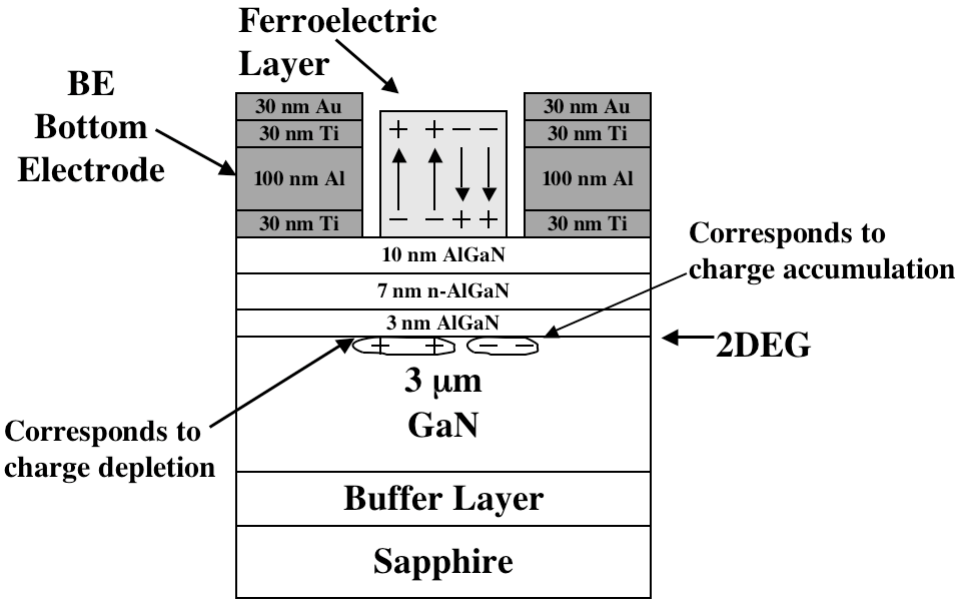


Figure 7.1: Ferroelectric gate on the AlGaN/GaN HEMT: showing the case of depletion and accumulation in the channel.

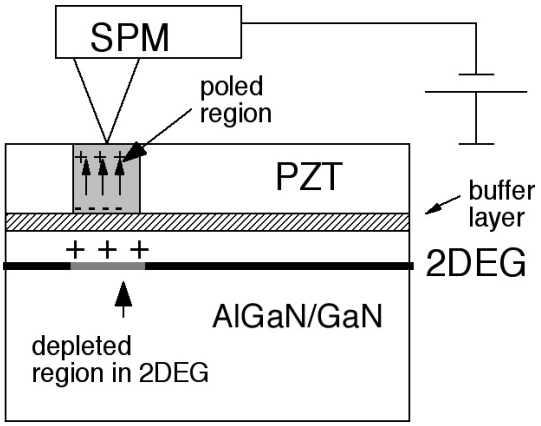


Figure 7.2: The explicit PFM setup used for poling the PZT/AlGaN/GaN structure with a conductive cantilever in contact with the ferroelectric layer and the 2DEG acting as the bottom electrode.

Poling of the ferroelectric layer can be done with two different methods. One of which is to use a top electrode directly deposited onto the ferroelectric layer, the other uses SFM techniques to pole directly the active area in the ferroelectric device. Figure 7.2 represents this last scenario of a ferroelectric device structure where the poled region of a PZT film plays the role of gate, depleting the 2DEG underneath it. This method is advantageous in that no top electrode needs to be deposited onto the PZT creating an electric field distribution that is higher and more local than when using the top electrode configuration. The main concept behind this is that when poling the PZT in the bottom to top orientation a local depletion of the electrons occurs. Using directly the PZT layer as the gate could allow for writing of nano-scale patterns in the PZT, these nano-patterns would thus be transferred to the 2DEG in the AlGaN heterostructure. In the case of a bi-stable, switchable PZT layer this phenomenon could extend to quantum structure

devices, as described in section 1.3.2. Probably the most important obstacle in achieving this is the optimisation of the necessary processing steps and material compatibility.

The PZT samples were predominantly deposited and processed as Hall bar structures where the active area was poled with the conductive cantilever from the PFM. Whereas, the testing of P(VDF/TrFE) was done on capacitor structures, after which more information was obtained from top electroded Hall bar structures.

7.2 CSD PZT Gate

The GaN sample used for the development of the chemical solution deposited, CSD, PZT had a different structure than that used for the other experiments. From top to bottom the structure was as follows: 8 nm of GaN n-doped, 12 nm AlGaN n-doped with 15% Al, $1.5-3\,\mu$m GaN n-doped on a sapphire substrate. The most important difference with this heterostructure and the one used throughout the thesis, is the low aluminium concentration in the upper AlGaN layer. The transport properties of its 2DEG are noted in table 7.2. At 300 K its 2DEG had transport properties of $n_s = 4x10^{12} - 3x10^{13}\,{}^{\text{electrons}}/_{\text{cm}^{-2}}$ and $\mu = 280 - 1000\,{}^{\text{cm}^2}/_{\text{Vs}}$. At 77 K its 2DEG had transport properties of $n_s = 1.6x10^{12} - 2.7x10^{13}\,{}^{\text{electrons}}/_{\text{cm}^{-2}}$ and $\mu = 9000 - 16000\,{}^{\text{cm}^2}/_{\text{Vs}}$.

Table 7.1: Mobility and electron sheet concentration of the 2DEG in the GaN/AlGaN/GaN structure used for the experiments with CSD PZT.

	$\mathbf{n_s}$ [electrons/cm^2]	μ [cm^2/Vs]
298 K	$4x10^{12} - 3x10^{13}$	280-1000
77 K	$1.6x10^{12} - 2.7x10^{13}$	9000-16000

A 400 nm thick polycrystalline PZT film was deposited by the CSD technique onto this GaN/AlGaN/GaN heterostructure with a 2DEG located 20 nm below the ferroelectric layer. The annealing process done to crystallise the PZT layer was with an RTA at 700 °C for 30 s in air. This annealing process was optimised in order to obtain the best crystalline quality of PZT, without severely degrading the transport properties of the 2DEG. See section 4.1.2 and 5.2 for the details regarding this technique and the optimisation of this ferroelectric layer on the AlGaN heterostructure.

Mesas, of Hall bar structure, with a depth of 500 nm, figure 7.3, were defined by ECR-RIE. Electrodes of Ti/Al/Ti/Au, 30 nm/100 nm/30 nm/30 nm respectively, were deposited by electron beam evaporation as bottom electrodes to the 2DEG.

The PZT film was poled using the SFM domain writing technique, described in section 3.3.4, with a DC voltage of ±40 V applied to the SFM conductive cantilever tip, figure 7.2. No top electrode was used for this experiment and the created polarisation pattern was controlled by piezoresponse force microscopy, figure 3.10.

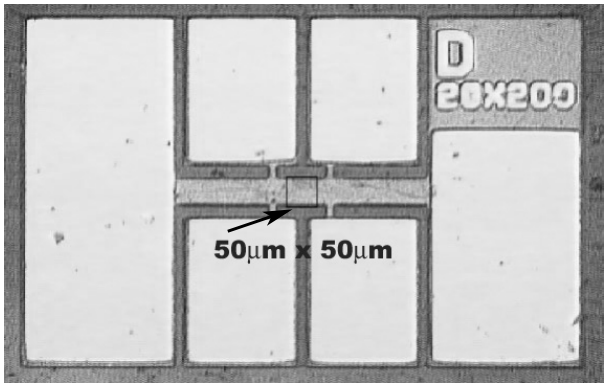


Figure 7.3: The PZT/AlGaN/GaN Hall bar structure without top electrode. Showing the 50x50 μm^2 active area that was poled with $\pm$40 V to the conductive cantilever tip using a SFM technique.

7.2.1 Transport Measurements

In order to evaluate the effect of the polarised ferroelectric film on the 2DEG the preferential polarisation was induced in the area of 50x50 μm^2 and then the 2DEG was characterised by the Hall effect. Firstly, measurements were done without poling in order to define the initial electron concentration. The concentration was found to be 5x10^{12} $^{\text{electrons}}/_{\text{cm}^2}$ and remained virtually unchanged within the temperature range from 77 K to 298 K. Then the studied area was poled with $-$40 V, corresponding to the depletion effect of electrons in the 2DEG and the measurements were repeated. As the last step, the polarity on the same area was inverted being poled by +40 V and the third series of transport measurements were performed. Figure 7.4 shows that the electron concentration changes approximately by a factor of two as the sign of polarisation in PZT switches. These values are summarised in table 7.2. At 298 K and 77 K it was possible to modulate the electron sheet concentration by a factor of two when poling with $\pm$40 V.

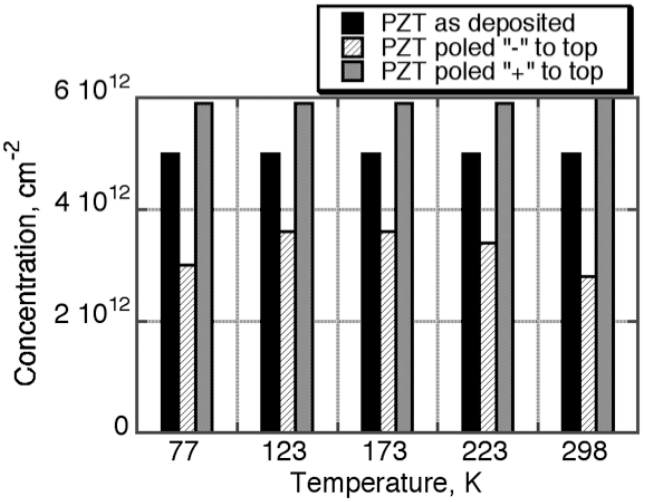


Figure 7.4: Effect of spontaneous polarisation in the PZT film on the electron concentration in the 2DEG, when poling with $\pm$40 V applied to the SFM conductive cantilever tip.

The fact that the sheet concentration measured in the "as deposited" PZT state did not

Table 7.2: Electron sheet concentration of the 2DEG in the CSD PZT/GaN/AlGaN/GaN structure when being modulated with a DC bias of ±40 V.

	$\mathbf{n_s}$ [electrons/cm^2]		
	As deposited	After −40 V	After +40 V
298 K	5x10^{12}	2.8x10^{12}	6x10^{12}
223 K	5x10^{12}	3.3x10^{12}	5.8x10^{12}
173 K	5x10^{12}	3.7x10^{12}	5.8x10^{12}
123 K	5x10^{12}	3.7x10^{12}	5.8x10^{12}
77 K	5x10^{12}	3.0x10^{12}	5.8x10^{12}

change with temperature, at 5x10^{12} $^{\text{electrons}}/_{\text{cm}^2}$ was as expected. This is due to the fact that the electron sheet concentration in a AlGaN heterostructure is controlled by the total polarisation in each layer which is fairly stable with temperature, to $\Delta n_s \approx 5\%$. Larger modulations of the sheet concentration are normally due to parallel conduction at the substrate interface. Therefore, if a stronger depletion effect can be observed at lower temperatures it is more informative to study the electron mobility or sheet resistance. The measurements of the electron mobility was temperature dependent, however it was virtually independent of the poled polarisation, measured as 1200 $^{\text{cm}^2}/_{\text{Vs}}$ at 298 K and 4200 $^{\text{cm}^2}/_{\text{Vs}}$ at 77 K. The fact that the electron mobility varies with temperature confirms the fact that if a stronger modulation/depletion effect is expected at low temperatures then it is of interest to study the mobility instead of the sheet concentration. The reason why μ was not impacted when poling the ferroelectric gate is of concern and needs to be further investigated.

Although the results presented here are not strong, they are a positive indication to further optimise device fabrication in order to observe a stronger effect of depolarisation due to the change of the spontaneous polarisation in the ferroelectric layer. More extensive measurements need to be done, especially in determining the dependence of polarisation in the PZT layer and the mobility in the 2DEG with temperature. It could be that many of the problems occurring here are due to the poor quality of PZT deposited. This poor quality is due to the sensitivity of both the crystalline quality of PZT and preservation of transport properties of the 2DEG with the high temperature annealing process. It is thus of interest to investigate other PZT deposition processes that are done at lower temperatures, without annealing steps, and different ferroelectric layers. Also of interest is to use an AlGaN heterostructure with a higher concentration of aluminium in an attempt to limit inter-diffusion occurring at the PZT/AlGaN interface and obtain a higher quality PZT layer.

7.2.2 PZT/MgO/AlGaN

Before switching to a different deposition process of the ferroelectric layer an MgO buffer layer was deposited by pulsed laser deposition onto the standard Cree AlGaN/GaN heterostructure used throughout this thesis. The most important reason for implementing this buffer layer was to inhibit the diffusion occurring at the PZT/AlGaN interface during the rapid thermal annealing process, preserving the 2DEGs transport properties. Also this layer could help preserve the original ferroelectric properites of the PZT layer de-

posited by CSD, thus allowing for the observation of a stronger depletion effect in the 2DEG than that presented above, in section 5.2.

The MgO layer deposited was 10 nm ± 5 nm by PLD, pulse laser deposition, from a MgO target onto the AlGaN/GaN heterostructure. Onto which a PZT(40:60) layer of 300 nm was deposited by the CSD technique and annealed at 700 °C for 30 s. There was no degradation of the transport properties of the 2DEG after the deposition of MgO and the high temperature annealing process for the CSD PZT. No seeding layer was used since the direction of orientation of MgO is (111), so it was assumed that this will help grow the PZT in the preferential direction of (111). However, this was not the case and the PZT layer had random orientation without any signs of pyrochlore phases. Circular gold electrodes were deposited onto a non etched structure for simple ferroelectric and depletion measurements.

C-V measurements

C-V measurement were done at 100 kHz with an AC modulation voltage of 0.01 V_{AC} and a DC poling volatage of ±5 V_{DC}, applied for 2 s. Both C-V measurements and PFM measurements concluded that there was no ferroelectric switching of the PZT film in the MFS structure, see figure 7.5. This could possibly be due to large screening effects produced by the MgO buffer layer, that might be too thick 15 nm, impinging the 2DEG of being affected by the charge associated with the ferroelectric polarisation, or the poor quality of the CSD PZT. With the PLD system used it is not possible to control the thickness of the layer grown to a better accuracy than 10 nm ± 5 nm. Therefore, it is not possible to further optimise the deposition conditions in order to grow a thinner MgO layer. For the use of a buffer layer it is important to have an "ultra-thin" buffer layer in order to not completely screen the polarisation, if the MgO layer is 15 nm there is a risk that it is too thick.

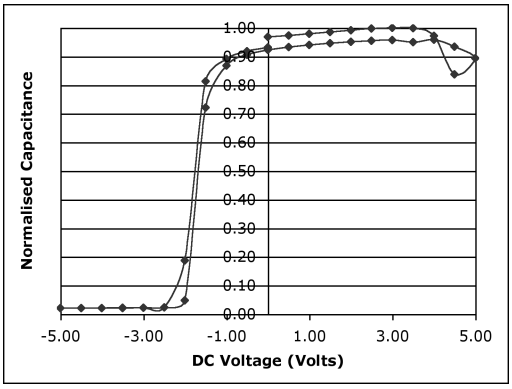


Figure 7.5: Normalised C-V curve of 300 nm CSD PZT/10 nm MgO/AlGaN heterostructure.

Unfortunately, there was only one trial done for the deposition of CSD PZT on a MgO buffer layer. Possible optimisation of the multitude of processing steps and conditions could lead to a better insight of the mechanisms behind the non-switching of the ferroelectric layer deposited onto MgO/AlGaN.

7.3 Sputtered PZT Gate

After the results with CSD PZT, attempts were made to optimise the PZT deposition process on AlGaN using multiple target magnetron sputtering. After many unsuccessful trials of obtaining pyrochlore PZT the right combination of parameters were obtained and 100% perovskite PZT(111) was deposited without any trace of pyrochlore phases, see section 5.4. The main advantage of working with the magnetron sputtered PZT is that the correct phase could be deposited at a temperature of 570 °C or lower. This is a clear advantage of minimising the diffusion of the elements occurring at the PZT/AlGaN interface, while preserving the great transport properties of the 2DEG at the AlGaN/GaN interface.

7.3.1 Transport Measurements

A $Pb(Zr_{0.40}, Ti_{0.60})O_3$ ferroelectric film, with thickness 130 nm, was deposited by magnetron sputtering. During the deposition the temperature of the substrate was kept as low as 570 °C. The sheet resistance, R_s, of the 2DEG was measured on the Hall bars with a Keithley 230 current source and Keithley 6517A electrometer. The electron concentration, n_s, in the 2DEG was determined by Hall measurements in a magnetic field of 0.385 T and 12 T. Conduction measurements were performed in the temperature range from 12 K to 300 K using a closed-cycle helium cryostat, Helix Technology Corporation. Additionally, measurements at low temperatures down to 12 K were performed in a normal 3He cryostat.

The experiment was performed as follows, Stolichnov et al. [2006], Stolichnov et al. [2007]. First, the Hall bar with PZT as-deposited was measured in the entire temperature range in order to determine R_s, n_s and μ. Then the four squares of 50x50 μm^2 were poled with −50 V applied to the CP-Research scanning probe microscopes conductive cantilever and the same measurements were repeated. This area can be visualised in figure 7.3, where instead of poling an area of 50x50 μm^2 between the branches, as was done for the case when using CSD PZT, a larger area of 200x50 μm^2 was poled, that extended over the four branches to the four electrodes. This was done in an attempt to observe a stronger modulation of the transport properties due to the spontaneous polarisation with a larger change in the Hall voltage measured vertically across two of the electrodes in the middle of the Hall bar. Then, this area was poled with +50 V and the transport properties were measured again. Finally, PZT was removed by chemical wet etching and the same measurement was repeated. Additionally, for comparison purposes R_s and n_s were measured on the AlGaN/GaN sample without having had any PZT deposited on it.

It was seen by PFM measurements that the device initially had a random polarisation domain pattern, see figure 7.6a, whereas when poled negative a preferential bottom-to-top orientation was observed in the spontaneous polarisation, see figure 7.6b. It is expected that when the spontaneous polarisation in the PZT is orientated from bottom-to-top that a full or partial depletion can be observed in the 2DEG.

The sheet resistance of the AlGaN/GaN sample without PZT deposited on it showed a behavior typical for this kind of 2DEG structures where R_s decreases with temperature, see figure 7.7. In order to examine the possible impact of the PZT deposition on 2DEG properties, these results were compared to the sample where PZT was deposited and

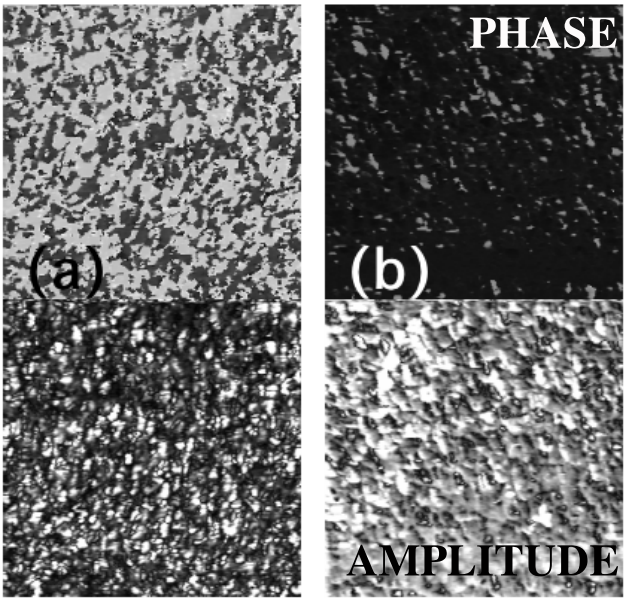


Figure 7.6: PFM images of the active 2x2 μm^2 area poled for the depletion measurements a) in the as deposited state and b) after the active area has been poled with -50 V applied to the SFM conducting cantilever. The piezoresponse is divided into phase images, the two top images, and amplitude images, the two bottom images.

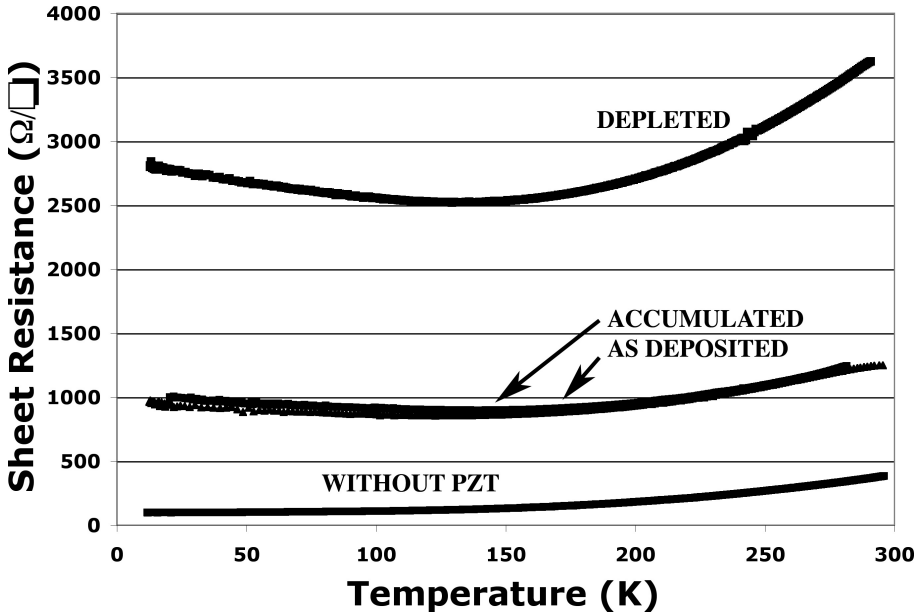


Figure 7.7: Sheet resistance of the 2DEG vs temperature in the PZT/AlGaN/GaN structure, for different poling treatments of the PZT gate. The curve for a sample without PZT is shown as a reference, also shown is the accumulated state, poled $+50$ V, and the depleted state, poled -50 V.

subsequently removed by chemical etching. The same sample with removed PZT, has a R_s that is larger by a factor 3 compared to the un-touched AlGaN/GaN sample. This degradation of the 2DEG is presumably provoked by the inter-diffusion that causes defect formations in the upper AlGaN layer. However, the 2DEG is not destroyed completely and remains suitable for the study of the ferroelectric gate operation.

Table 7.3: Sheet resistance, mobility and concentration of electrons in the 2DEG of the PZT/AlGaN/GaN structure, for as-deposited PZT, PZT poled with −50 V to the SFM cantilever and PZT depoled with +50 V.

		300 K	**77 K**
As deposited	$R_s\ \Omega/\square$	1270	1000
	$\mu\ \mathrm{cm^2/Vs}$	820	1330
	$n_s\ \mathrm{cm^{-2}}$	6x10^{12}	4.7x10^{12}
Poled −50 V	$R_s\ \Omega/\square$	3620	2810
	$\mu\ \mathrm{cm^2/Vs}$	440	620
	$n_s\ \mathrm{cm^{-2}}$	3.9x10^{12}	3.6x10^{12}
Poled +50 V	$R_s\ \Omega/\square$	1250	970
	$\mu\ \mathrm{cm^2/Vs}$	820	1240
	$n_s\ \mathrm{cm^{-2}}$	6.1x10^{12}	5.2x10^{12}

The essential result of this work is the reversible change of conduction in the 2DEG by switching the polarisation in the PZT gate. Poling the gate with the negative voltage results in decreasing R_s by approximately a factor 3, figure 7.7. After erasing this poled state by applying the positive voltage, +50 V, the initial conduction in the 2DEG was restored. Transport measurements show that both n_s and μ decrease as a result of poling the gate, table 7.3. This can be explained by the strongly non-uniform domain pattern in the poled gate as seen in the PFM images after poling in figure 7.6. The non-uniformity of the spontaneous polarisation in the ferroelectric layer can result in a non-uniform depletion profile, which reduces the electron mobility. After erasing the poled state R_s, n_s and μ are nearly completely restored.

The results presented here were highly stable with time. Already a sufficient time elapsed between the poling of the PZT with the PFM and bringing the sample over to the separate cryostat for Hall measurements. It is expected that if it is possible to measure the transport properties immediately after poling that a stronger depletion effect can be observed, that is not stable with time and decays to the depletion effect observed above.

In principal, one can expect the PZT gate to produce a much stronger depletion effect than observed in the gate depletion effect demonstrated above. The charge carrier density of $10^{13}\,\mathrm{cm^{-2}}$ in the 2DEG corresponds to a charge density of approximately $1.6\,\mu\mathrm{C/cm^2}$, whereas the remanent polarisation in PZT is about $20\,\mu\mathrm{C/cm^2}$. The situation where the remanent polarisation is completely screened by the charge of opposite sign located at a distance of 20 nm from the interface is unrealistic because in that case the depolarisation field is prohibitively high so that it would depole the polarisation of the PZT layer completely. In reality, the more realistic scenario is that more than 90 % of the polarisation is compensated in a much thinner layer close to the PZT/AlGaN interface and the remaining charge is distributed within a relatively wide region including the AlGaN/GaN junction with 2DEG. It may be possible to reach a stronger depletion effect through the

optimisation of the PZT deposition conditions in a way to reduce the inter-diffusion that enhances formation of charged defects. Additionally, a ferroelectric layer of higher quality may provide a more uniform polarisation pattern with better retention, which could also contribute to the stronger depletion effect.

Attempts to pole the gate in the opposite direction by applying +50 V were not successful in provoking charge accumulation and the resulting polarisation distribution was random, similar to the as-deposited PZT. The conduction of 2DEG remained virtually the same as for the PZT before poling, figure 7.7. Removal of PZT by chemical etching provoked only a small change in the conduction properties of 2DEG, figure 7.7, suggesting the permanent degradation of the upper AlGaN layer and 2DEG.

The experimental results suggest that the artificial domain pattern written on the ferroelectric gate can be projected directly onto the 2DEG. Hence, the arbitrary-shaped low-dimensional semiconductor structures can be defined with nano-scale resolution by domain engineering. The essential advantage of such ferroelectric lithography compared to alternative techniques is that the created patterns are re-writable. The domain pattern can be modified or completely erased and re-written without causing any damage to the sample, which opens new opportunities for experiments with semiconductor nanostructures as well as for device optimisation.

7.3.2 Strong Depletion Effect

The following results are separated from the previous presented since they were only achieved once and were not reproduced due to technical difficulties. However, these results are interesting to present as they show a strong modulation of the electrons in the 2DEG giving vital information on the PZT/AlGaN structure.

This device has a 2 nm TiO_2 seeding layer onto which was sputtered 195 nm of PZT(40:60). Top electrodes of Cr/Au, 10/100 nm, were deposited by electron beam evaporation and bottom electrodes of Ti/Al/Ti/Au, 30/100/30/30 nm, were deposited by lift off technique. After which the Hall bar mesa structure, shown in figure 7.8, was etched with the ECR-RIE for 12 min with an etching rate of 19.2 $^{nm}/_{min}$. The final step in the processing of this device was the ohmic contact of the bottom electrode to the 2DEG which was improved with an annealing process in nitrogen for 30 s at 700 °C.

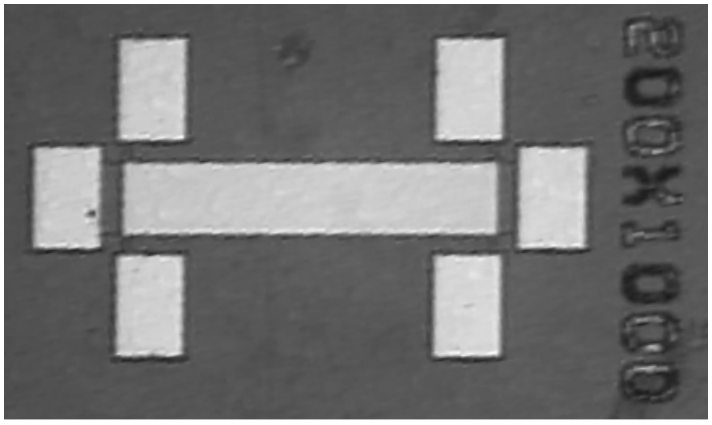


Figure 7.8: Hall bar of the electroded ferroelectric gate of 200x1000 μm^2.

After the processing of this device Hall measurements were done with a source to drain current, I_{ds}, of 0.1 μA and a magnetic field of 0.6 T. These measurements were performed at room temperature and allowed for controlling the sheet resistance, electron sheet concentration and mobility of electrons in the 2DEG.

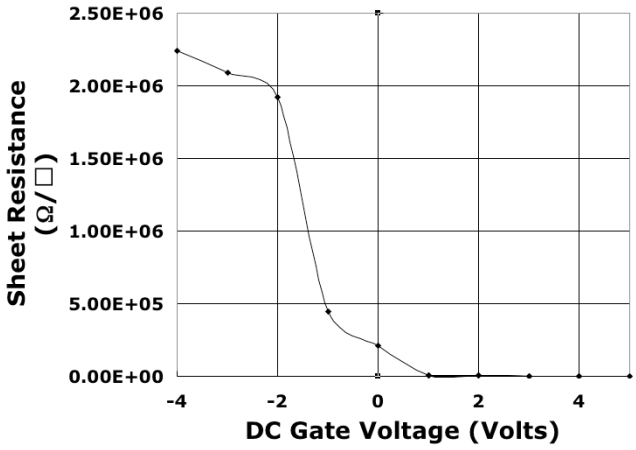
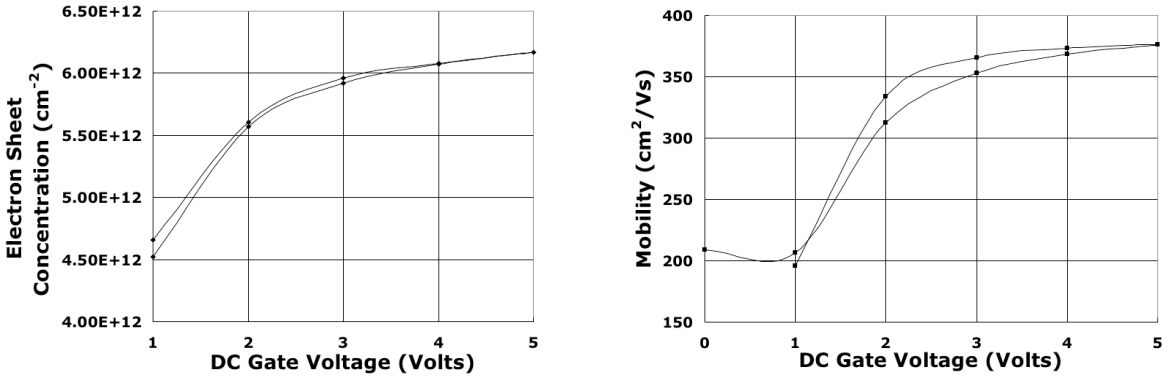


Figure 7.9: Change in the sheet resistance 5 s after applying a gate voltage to a Au/Cr/PZT(40:60) 195 nm/AlGaN heterostructure.

Within measurements the cabling arrangement was changed to apply a DC bias for approximately 5 s and return the cabling to the original setup that allows for Hall effect measurements. Hall measurements were done approximately 30 s after the application of the DC bias and demonstrate the short term retention of the polarisation in the PZT layer. The results of applying the DC bias to the sheet resistance are in figure 7.9, the sheet concentration in figure 7.10a and the mobility in figure 7.10b. The DC bias was applied from +5 V to −5 V. When applying a DC bias less than 0 V to the gate electrode, invoking the depleted state, it was no longer possible to measure n_s and μ with Hall effect measurements.



(a) (b)

Figure 7.10: Change of a) the electron sheet concentration and b) the electron mobility in the 2DEG 5 s after applying a gate voltage to a Au/Cr/PZT(40:60) 195 nm/AlGaN heterostructure.

It was observed that the sheet resistance increased by a factor of 800 when −5 V was applied to the gate electrode. This sample was only able to perform this depletion twice possibly due to depolarisation fields or other effects such as the slow arrival of equilibrium

due to charge compensation. An effect of accumulation of charge was also observed in R_s, n_s and μ when increasing the poling voltage from 0 V to 5 V. This increase in transport properties could be the result of one of the following two possibilities. The least probable is that an effect on accumulation of charge occurs when the polarisation is poled upwards. Alternatively, is that the PZT is deposited with random orientation giving already some effect of depletion of the electrons in the 2DEG, when the PZT is poled positively the transport properties of the 2DEG are returned to values closer to their original values.

Retention of DC Poling

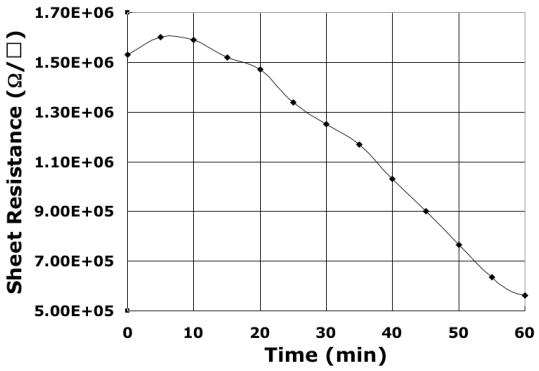


Figure 7.11: Retention of the sheet resistance after having applied −5 V to the gate voltage to a Au/Cr/PZT(40:60) 195 nm/AlGaN heterostructure.

The long term retention of the depletion of the −5 V written state was done by observing the change in sheet resistance with time. It was observed that the polarisation state was not stable and the sheet resistance of the 2DEG gradually decreased, figure 7.11. This indicates either the relaxation of the written ferroelectric state to its previous state due to the depolarisation field or a time delayed effect of charge compensation. After three days the sheet resistance returned to that measured in the as-deposited state.

Unfortunately, these results were only obtained once which could be due to the degradation of the PZT layer in the final nitrogen annealing causing the PZT layer to fatigue much faster than when it is not annealed in nitrogen and in its optimal MFM configuration.

7.4 P(VDF/TrFE) Gate

The spin casted 250 nm P(VDF/TrFE)(70:30) layer was first tested in the MFM configuration to have the correct XRD spectrum. After which ferroelectric P-V curves allowed for measuring the remanent polarisation P_r=6.9 $\mu C/cm^2$, the positive coercive field, $+E_c$=850 kV/cm and the negative coercive field, $-E_c$=1200 kV/cm. Since the XRD spectrum and polarisation vs voltage curves were representative of the co-polymer ferroelectric layer it was possible to proceed to the MFS structure with the AlGaN/GaN heterostructures as is shown in figure 7.12. When 250 nm P(VDF/TrFE)(70:30) was spin casted onto AlGaN it had a XRD spectrum similar to that in the MFM configuration. Poling measurements were then done with PFM to observe that it was possible to pole the ferroelectric layer with both polarities and have long term retention of its polarisation, greater than 116 hrs.

It was thus possible to continue investigating this structure with C-V, sheet resistance and Hall measurements to observe the modulation of the electrons in the 2DEG due to poling of the co-polymer P(VDF/TrFE) ferroelectric layer.

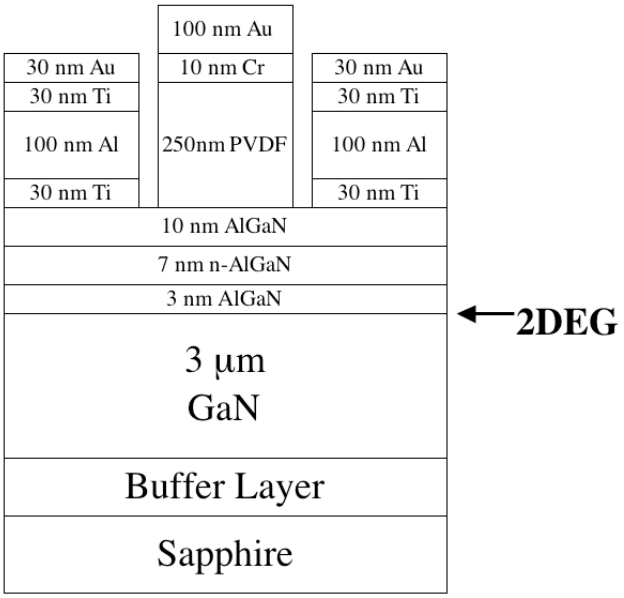


Figure 7.12: P(VDF/TrFE)/AlGaN/GaN cross section.

In total three different devices were fabricated with this P(VDF/TrFE)/AlGaN/GaN structure, figure 7.12. The easiest structure to make was a simple capacitor structure where electrodes were deposited using a shadow mask onto the P(VDF/TrFE) and no etching was performed. Afterwards, van der Pauw structures of 1x1 cm^2 were made with shadow masks to facilitate the processing steps while still being capable of making Hall measurements. Lastly, with more knowledge of the processing of P(VDF/TrFE), etched Hall bar structures of 200x1000 μm^2 were processed.

7.4.1 P(VDF/TrFE) Capacitor

The first structure to study was the simplest to make, a simple capacitor structure. Circular electrodes of diameter 200 μm were deposited using a shadow mask onto the P(VDF/TrFE) and no etching was performed. With this structure it was only possible to estimate the change of the electron sheet concentration in the 2DEG with C-V measurements.

C-V curves

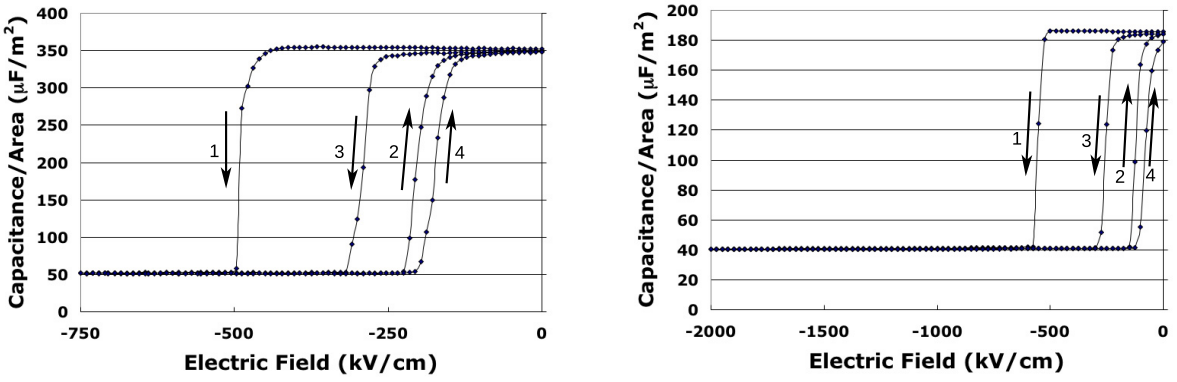
C-V curves were performed to ensure that there was retention of the DC gate voltage applied, indicating ferroelectric characteristics and depletion of electrons in the 2DEG. When ferroelectric switching is observed the C-V curve is in the counterclockwise direction, however if the mechanism behind the switching is due to charge injection, clockwise C-V curves should be observed. Henceforth this is a very simple technique used in order to determine the role of the ferroelectric layer on the 2DEG located in the AlGaN.

The total capacitance of the structure can be estimated by using the following equation 7.1 and calculating the total capacitance for two capacitors in series. Where one layer is AlGaN and the other is P(VDF/TrFE), table 7.6 has been used to better visualise this. The final value of the capacitance per area is independent on the area of the capacitor studied, C/A=4.17x10^{-4} F/m^2.

$$C = \frac{\epsilon_o \epsilon A}{d} \tag{7.1}$$

Table 7.4: Summary of parameters to calculate the capacitance/area of the 250 nm P(VDF/TrFE)/20 nm AlGaN structure

ϵ_o	8.85x10^{-12} C^2/Nm^2
$\epsilon_{Al_{0.3}Ga_{0.7}N}$	10.2
$\epsilon_{P(VDF/TrFE)(70:30)}$	13
$d_{Al_{0.3}Ga_{0.7}N}$	20 nm
$d_{P(VDF/TrFE)(70:30)}$	250 nm
$Area_{Capacitor}$	2x10^{-8} m^2
$C_{Al_{0.3}Ga_{0.7}N}$	8.85x10^{-11} F
$C_{P(VDF/TrFE)(70:30)}$	9.20x10^{-12} F
$C_{TotalCapacitor}$	8.34x10^{-12} F
C/A	417 μF/m^2



(a) (b)

Figure 7.13: C-V curve of a spin casted 250 nmP(VDF/TrFE) with a 100 nm Cr top electrode. Performed with 0.05 V$_{AC}$ and 0.5 s application of the DC voltage a) at 10 kHz for a DC bias from 0 V to −15 V, and b) at 1 MHz for a DC voltage from 0 V to −40 V.

Top electrodes of 100 nm Cr, with circular shape, diameter 200 μm, were deposited by sputtering and a bottom electrode of indium was used. No structure was etched into the P(VDF/TrFE) or the AlGaN. These experiments were preliminary in helping us understand that the P(VDF/TrFE) did exhibit ferroelectric properties and it was possible to measure this ferroelectricity when it was deposited onto AlGaN.

C-V measurements were done at a frequency range of 1 kHz to 1 MHz, all of which had curves that showed hysteretic behavior. Shown in figure 7.13 are two extremes, in figure

Table 7.5: Summary of the ferroelectric memory window, ΔV_1 and ΔV_2, observed in the capacitance/area vs voltage curves of the 250 nm P(VDF/TrFE)/20 nm AlGaN structure

$\mathbf{\Delta V_1}$ [Volts]	$\mathbf{\Delta V_2}$ [Volts]	**Frequency** [kHz]	$\mathbf{V_{DC}}$ [Volts]	$\mathbf{T_{DC}}$ [s]	$\mathbf{V_{AC}}$ [Volts]
4.57	2.68	100	10	1	0.1
5.82	2.34	10	15	0.5	0.05
5.63	2.44	10	15	0.5	0.01
8.46	1.87	10	30	0.5	0.01
9.05	1.5	10	40	0.5	0.01
7.91	2.44	1000	30	0.5	0.05
8.50	3.50	1000	40	0.5	0.05

7.13a is the measurement done at 1 kHz to −15 V and in figure 7.13b is the measurement done at 1 MHz to −40 V. Table 7.5, summarises a larger series of C-V measurements performed on the same sample and allows to observe the change of the memory window, ΔV_1 and ΔV_2, with the measurement parameters. ΔV_1 is the measured as the FWHM of the first CV curve done, that is for the first cycle from 0 V to $-V_{DC}$ and ΔV_2 is measured as the FWHM for the second curve done after the first cycling without any delay. It is expected that for the first cycle it should take a larger negative DC bias for depleting the 2DEG than for the second curve. Ideally, the 2DEG should stay depleted until a positive DC bias is applied, but a reduction in its memory window is also a sign of retention of the depletion state. From here it can be noted that the memory window is biggest when using a large DC bias, a DC bias applied for a long time, small AC frequency and small AC modulation voltage.

The retention of this structure is not expected to be long term due to the fact that the second consecutive hysteresis loop has a finite memory window of ΔV_2 where the capacitance after the first loop returns to the original value. Since no positive bias was applied, it should be expected that the 2DEG should remain in the depleted state but this is not the case. The C-V curve that exhibited the best retention was performed at 10 kHz with −40 V and had memory windows of ΔV_1=9.05 V and ΔV_2=1.5 V.

Sheet Concentration from C-V curves

Using the estimation for the electron sheet concentration introduced in section 2.1.2, equation 7.2, it was possible to estimate the change of the sheet concentration due to the poling voltage for the C-V curves presented above in section 7.4.1. This method is for the approximation that the AlGaN layer is an ideal dielectric with a huge Schottky barrier between it and the ferroelectric layer. Mechanisms such as charge injection, and charge trapping are ignored in this approximation

$$n_s = \frac{C_g V_{gt}}{Aq} \tag{7.2}$$

To determine the most accurate sheet concentration one can only consider the measurements at low AC frequency. The variation of sheet concentration with AC frequency is

Table 7.6: Summary of parameters to calculate the depleted electron sheet concentration of the 2DEG in the P(VDF/TrFE)/AlGaN structure from C-V curves.

Frequency [kHz]	**DC field** [kV/cm]	**DC bias** [V]	$\mathbf{n_s}$ [electrons/cm^2]
10	-441	-8.81	3.08x10^{12}
	-263	-5.25	1.78x10^{12}
100	-400	-8	2.46x10^{12}
	-275	-5.5	1.74x10^{12}
1000	-500	-10	1.16x10^{12}
	-225	-4.5	4.9x10^{11}

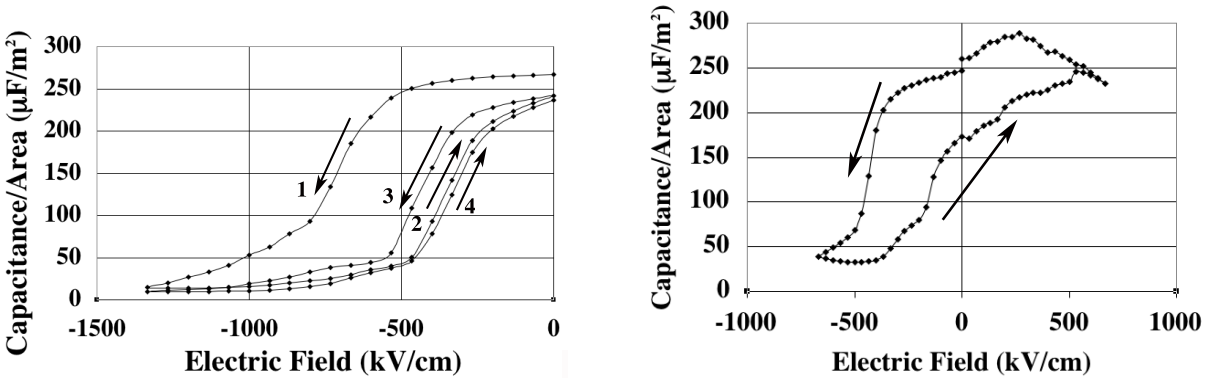
visible in table 7.6 where the sheet concentration decreases with increasing AC frequency. It is therefore decided to be most reliable to only determine the sheet concentration for C-V curves done with an AC frequency of 10 kHz. This is due to the fact that the capacitance or dielectric constant of a material is frequency dependent. Also these calculations were compared with transport measurements done when poling the ferroelectric and depleting the 2DEG. It was determined from those transport measurements that it was not possible to deplete the sheet concentration to as low as 2x10^{12} $^{\text{electrons}}/_{\text{cm}^2}$, especially keeping in mind that the electron sheet concentration should not variate more than 5% in an AlGaN heterostructure. The calculation for the electron sheet concentration using the C-V curve should rather be used to demonstrate the effect of depletion and not for precise electron sheet concentration calculations.

7.4.2 Van der Pauw Structure

After which van der Pauw structures of 1x1 cm^2 were made with shadow masks to facilitate the processing steps while still being capable of making fairly accurate Hall measurements. With this it was possible to deposit the bottom electrodes in the four corners, anneal the bottom electrodes in nitrogen for 30 s at 700 °C. After which the P(VDF/TrFE) was deposited by the CSD technique and Au/Cr, 100/10 nm, electrodes were deposited by electron beam evaporation. The main benefit of using this scheme was that no etching process had to be done and no steps involved the use of acetone. The disadvantage of course being in the fact that the van der Pauw structure is not as ideal as the Hall bar structure for controlling the properties of the 2DEG.

C-V curves

The C-V curves shown in figure 7.14 show better retention characteristics than those measured on the capacitor structures in figure 7.13. In figure 7.14a is the C-V curve of the van der Pauw structure at 1 MHz, 40 V_{DC} for 0.5 s, and 0.1 V_{AC}. The memory window of this ferroelectric film is ΔV_1=9.25 V and ΔV_2=2.5 V. It is interesting here to see that in the return cycle of the hysteresis loop the capacitance does not return to its initial value indicating that there is some retention of the depleted state. Also it is possible to better deplete the 2DEG in the AlGaN heterostructure as the capacitance/area value decreases to 9.6 $^{\mu\text{F}}/_{\text{m}^2}$. In figure 7.14b the C-V curve on the same van der Pauw structure



(a) (b)

Figure 7.14: C-V curves of a 1x1 cm^2 van der Pauw structure of Au/Cr/P(VDF/TrFE)/AlGaN. Performed a) at 1 MHz, 40 V_{DC} for 0.5 s and 0.1 V_{AC} and b) at 1 MHz, 20 V_{DC} for 0.5 s and 0.01 V_{AC}.

is measured at 1 MHz with 20 V_{DC} applied for 0.5 s and 0.01 V_{AC}. The memory window of this ferroelectric film is ΔV=2.5 V, what is interesting here is that it was possible to apply positive DC biases without injecting charge due the high frequency and low AC modulation voltage.

Transport Measurements

Hall measurements were done with this same large, 1x1 cm^2, van der Pauw structure applying a current of 1 mA. Measurements were done only at room temperature due to issues regarding the electrical contact to the five electrodes and the fixation of the sample to the support. The Hall measurements were done immediately after applying a DC voltage from −30 V to +30 V for a duration of approximately 5 s.

A summary of the most important results is in table 7.7, where the values of the R_s, n_s and μ are given for the extreme poling voltages. F, the form factor is also included as it gives an indication of the symmetry and accuracy of the measurement. In the case of a perfect measurement, or symmetric measurement the form factor should equal one, if the form factor is close to zero the measurement is unreliable. The main change in transport properties occurs when going from 0 V to −30 V. The result of applying this −30 V DC voltage occurs with an increase of R_s by a factor 3.04, a decrease of n_s by a factor 1.91 and a decrease of μ by a factor 1.85.

More details can be found in the graphs of the R_s in figure 7.15, n_s in figure 7.16a, and μ in figure 7.16b. What is very interesting to remark is how all of these curves exhibit retention-like behavior. This is similar to the ferroelectric hysteresis loop that possess both a positive and negative remanent polarisation occurring on the up and down cycling of the DC bias field. This concept can be visualised in figure 7.15 where the R_s is changing from 339 Ω/□ to 661 Ω/□. In figure 7.16a the n_s is changing from 6.5x10^{12} electrons/cm^2 to 1.02x10^{13} electrons/cm^2. In figure 7.16b the μ is changing from 1570 cm^2/Vs to 1750 cm^2/Vs.

From these curves it is possible to observe that there is retention occurring in this ferroelectric/semiconductor structure, however it is not the long term retention, necessary for

Table 7.7: Sheet resistance, mobility and concentration of electrons in the 2DEG of the P(VDF/TrFE)/AlGaN/GaN structure, for as-deposited P(VDF/TrFE), poled with −30 V to the top electrode, poled back with 0 V, poled again with +30 V and finally with 0 V.

V_{DC} [Volts]	F	R_s [Ω/□]	n_s [electrons/cm^2]	μ [cm^2/Vs]
0	0.999	339	1.02x10^{13}	1810
-30	0.944	852	6.40x10^{12}	1140
0	0.985	611	6.50x10^{12}	1570
30	1	351	1.02x10^{13}	1740
0	0.998	312	1.15x10^{13}	1750

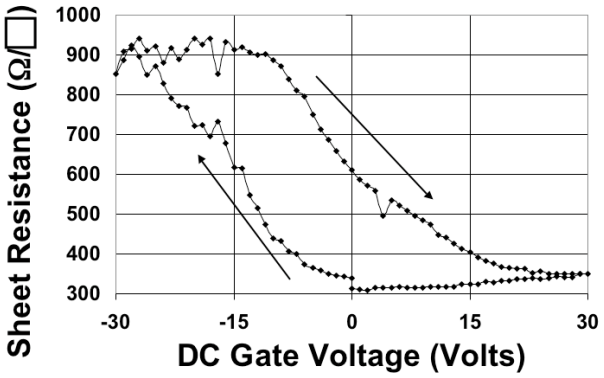
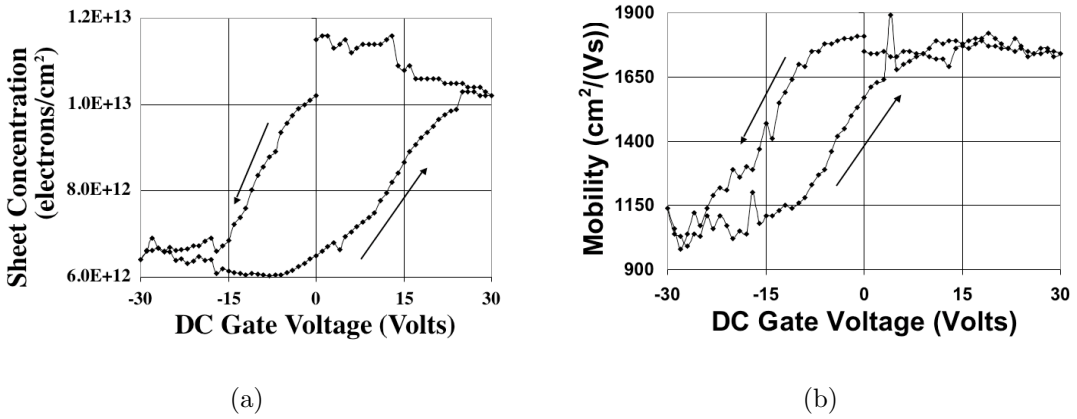


Figure 7.15: Sheet resistance from the Hall measurements after having applied a gate voltage varying from ±30 V.

FeFET devices. This is confirmed in one measurement in the figures 7.15, 7.16a and b which was done after a larger delay from the application of the DC voltage. After applying +4 V, more time than usual was taken to measure the transport properties, which is visible by the sharp peaks in all three curves.

This same sample underwent, at a later time, simple sheet resistance measurements as a function of DC voltage and retention time using the van der Pauw structure by using the equations and constraints listed from equation 3.5 to 3.10, listed in chapter 3 of this thesis. The first measurement of the sheet resistance was measured as 332 Ω/□, which is an accurate measurement of the 2DEG, the same as when using Hall measurements. When measuring a Hall bar structure without any ferroelectric layer and with the Ti/Al/Ti/Au annealed bottom electrodes the sheet resistance of the 2DEG in the AlGaN heterostructure was measured to be 430 Ω/□. Therefore, first and foremost the sheet resistance values measured here are found to be reliable.

The DC bias voltage was thus applied to the Cr/Au gate electrode but only in the negative direction, since measurements were unstable when applying positive DC biases possible due to charge injection. 5 min after the DC voltage was applied the sheet resistance was measured, the results of which are shown in figure 7.17. The sheet resistance increases from 332 Ω/□ in the as deposited state to over 600 Ω/□ after applying −120 V. The retention of this sheet resistance after applying a gate voltage of −180 V was measured and is shown in table 7.8. After 75 min the sheet resistance decreased down to 375 Ω/□, and after a



(a) (b)

Figure 7.16: a) Electron sheet concentration and b) mobility from the Hall measurements after having applied a gate voltage varying from ±30 V.

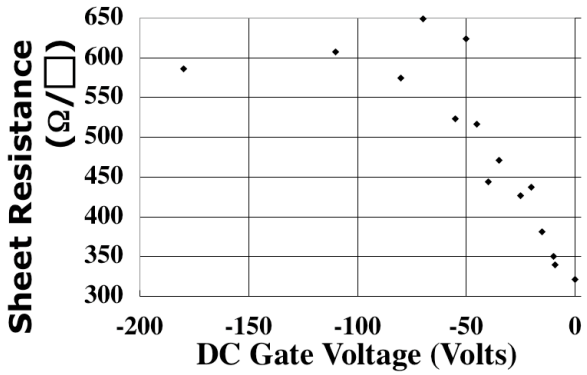


Figure 7.17: Van der Pauw measurements of the sheet resistance taken 5 min after the DC voltage was applied.

couple of hours the sheet resistance had relaxed to its initial value.

Although this sample shows a decrease of the sheet resistance by a factor three when negatively poling the P(VDF/TrFE) layer there is no long term retention of this modulation. It is interesting still to process a Hall bar structure to observe if the effect is similar or not. Hall measurements are usually preferred to simple sheet resistance measurements, since more information is obtained about the electrons in the 2DEG.

7.4.3 Hall Bar Structures

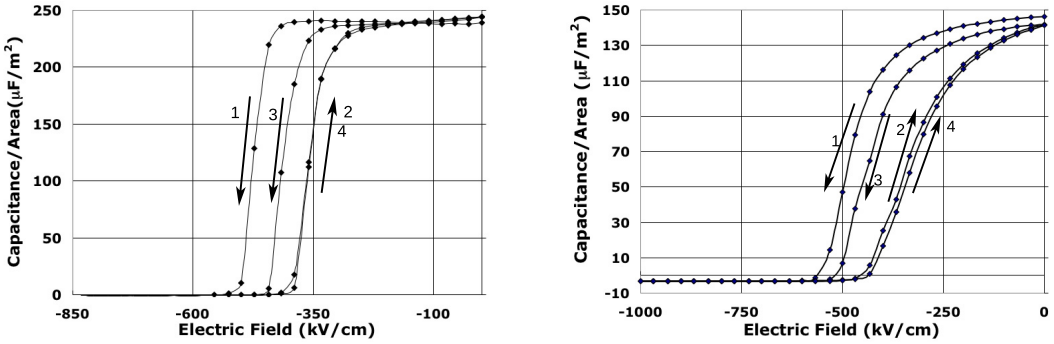
To investigate if a stronger depletion effect can be observed, Hall bar structures were fabricated, with geometry of 200x1000 μm^2. Bottom electrodes were first deposited and annealed for 30 s at 700 °C, after which the mesa structure was dry etched for 10 min or approximately 330 nm. The P(VDF/TrFE)(5%) was then spun on for a thickness of approximately 250 nm. After which gold top electrodes of 100 nm were evaporated on the P(VDF/TrFE) by joule effect and wet etched. The following measurements, using a top electrode on the P(VDF/TrFE), allowed for the direct observation to the changes to the transport properties of the 2DEG while being poled as well as after being poled.

Table 7.8: Time dependent Van der Pauw measurements of the sheet resistance after a gate voltage of −180 V was applied.

Retention Time [min]	**R_s [Ω/□]**
5	586.0
80	374.2
1035	332.3

C-V Curves

All of the C-V curves measured showed ferroelectric behaviour within the measured frequencies of 1 kHz to 1 MHz, see figures 7.18a and 7.18b. Better ferroelectric retention was observed for C-V curves at high frequency 1 MHz such as in figure 7.18b where the capacitance does not return to its original value after the 2DEG was depleted and the DC bias of 0 V was applied.



(a) (b)

Figure 7.18: C-V measurement of a 300x300 μm^2 van der Pauw structure of Au/P(VDF/TrFE)/AlGaN a) at 1 kHz and b) at 1 MHz.

Transport Measurements

With the knowledge from the large van der Pauw structures it was most interesting to see if it was possible to get better retention of the depletion effect. It was observed with the smaller 300x300 μm^2 van der Pauw structures and Hall bar structures that it was possible to get sufficient C-V curves. Before doing more extensive Hall measurements simple van der Pauw sheet resistance measurements were done on the small structures. Retention experiments were done after applying a DC bias voltage of −80 V to the top electrode, the results of which is shown in figure 7.19. The retention thus of the written polarisation in the ferroelectric P(VDF/TrFE) co-polymer layer does not induce a stable effect of depletion in the 2DEG. These results are similar to the retention of the depletion effect in the large van der Pauw structure, table 7.8. Hall measurements were done afterwards on a Hall bar structure of 200x1000 μm^2 and gave similar results to what was measured on both the small and large van der Pauw structures.

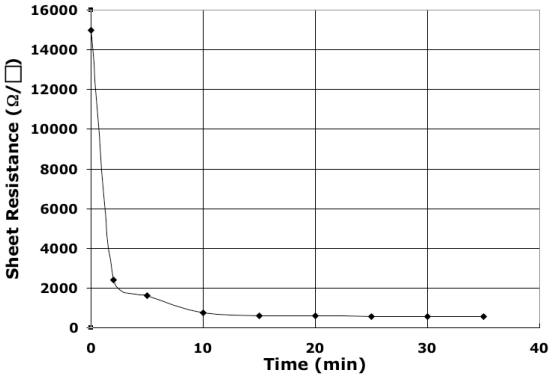


Figure 7.19: Van der Pauw measurements with current 1 μA of the sheet resistance taken after applying the DC voltage of −80 V.

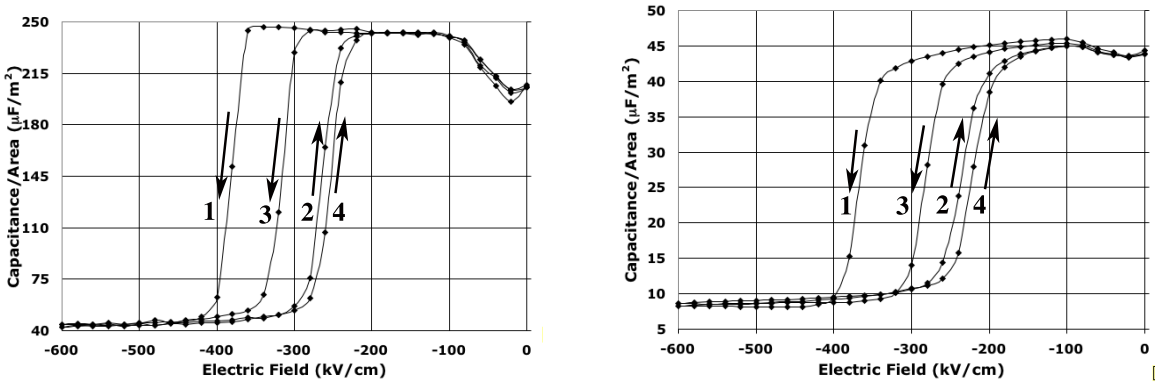
In section 6.2.3 it was shown that it was possible with the PFMs conductive cantilever to write stable domain patterns with no decay in the piezoresponse for 116 hrs, implying long term retention. From the sheet resistance measurements the opposite of this is observed, that is the sheet resistance can be increased due to poling, however, the sheet resistance decays exponential to its initial value. Are these two concepts contradictory or not? If the depolarisation field is the mechanism behind the short term retention then this should be visible in both sheet resistance and PFM measurements. However, due to the fact that the retention is long term with the PFM poling experiments implies that charge equilibration occurs in the 20 nm AlGaN layer after poling occurs. This could possibly be due to the large conductivity of the AlGaN layer. Also, if there is a large amount of charge injected and subsequently trapped in the AlGaN layer enough charge build up could work as a screening barrier to the 2DEG.

7.4.4 C-V Curves with HfO_2 Buffer Layer

As before a 250 nm P(VDF/TrFE)(70:30) was spin casted onto the 5 nm HfO_2 buffer layer. The sheet resistance of the 2DEG in this device increased by a factor 6 to 2266 Ω/□, with the HfO_2 deposition, which was still tolerable for observing the effect of depletion from C-V curves. Au top electrodes, of 100 nm, were sputtered onto the ferroelectric layer, with radius 310 μm or area 3.01x10^{-7} m^2.

C-V measurements were done on this sample using various parameters. At low AC frequency 10 kHz the capacitor had the C-V curve shown in figure 7.20a. Using higher frequencies the value of the total capacitance decreased but the hysteretic C-V curve showing retention remained. Figure 7.20b was done at 1 MHz. The kink existing at −50 $^{\mathrm{MV}}/_{\mathrm{cm}}$ could be due to high dielectric losses.

Table 7.9 summarises the results from various C-V curves of the same sample performed at different conditions where memory windows have been calculated for all curves and n_s for C-V curves done at 10 kHz. The memory window ΔV_1 depends mostly on the DC voltage used whereas the second cycle the memory window, ΔV_2, is more constant for different AC frequencies, voltage and DC voltage. It is important to note that the second memory window are all smaller than those from the C-V measurements made on a capacitor with P(VDF/TrFE) deposited directly onto AlGaN. The results without the HfO_2 are summarised in table 7.5 where the best C-V results give ΔV_1=9.05 and



(a) (b)

Figure 7.20: C-V curve of 250 nm P(VDF/TrFE)/5 nm HfO_2/AlGaN/GaN with 0.1 V_{AC} and a maximum DC poling voltage of −15 V_{DC} applied for 0.5 s at a) 10 kHz and b) 1 MHz.

ΔV_2=1.50. One trend is consistent in both series of C-V measurements in that ΔV_2 is always smaller than ΔV_1 indicating that there is some retention of the polarisation.

Table 7.9: Summary of the ferroelectric memory window, ΔV_1 and ΔV_2, observed in the Capacitance/Area vs Voltage curves of the 250 nm P(VDF/TrFE)/5 nm HfO_2/20 nm AlGaN structure

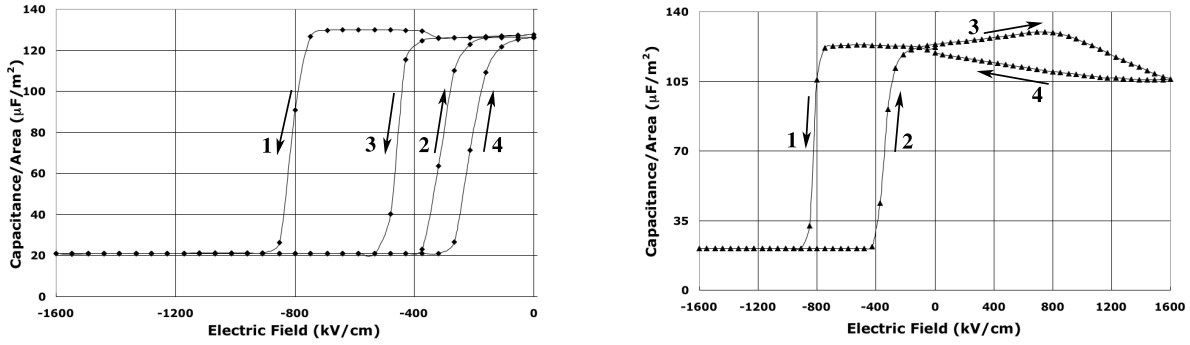
ΔV_1 [Volts]	ΔV_2 [Volts]	n_{s1} [electrons/c m^2]	n_{s2} [electrons/c m^2]	Frequency [kHz]	V_{DC} [Volts]	T_{DC} [s]	V_{AC} [Volts]
3.63	1.25	n/a	n/a	1000	15	0.5	0.1
3.00	1.25	n/a	n/a	100	15	0.5	0.1
3.00	1.25	-1.37x10^{12}	-1.07x10^{12}	10	15	0.5	0.1
1.38	1.00	-1.05x10^{12}	-1.0x10^{12}	10	10	0.5	0.1
2.50	1.13	-1.43x10^{12}	-9.78x10^{11}	10	40	0.5	0.1
2.70	1.50	n/a	n/a	100	20	0.5	0.1

Using a HfO_2 buffer layer in a P(VDF/TrFE)/$Al_{0.3}Ga_{0.7}N$ heterostructure to limit injected charge and observe better ferroelectric retention in the P(VDF/TrFE) layer and the change of conductance in the 2DEG was not proven. In fact the HfO_2 buffer layer caused the P(VDF/TrFE)/ HfO_2/AlGaN capacitor to have inferior characteristics to the P(VDF/TrFE)/AlGaN capacitors measured. One reason for this could be due to the degradation of the 2DEG due to inter-diffusion occurring during the HfO_2 deposition process.

C-V curves with HfO_2/Hf Buffer Layer

The first structure tested had a buffer layer of 9 nm HfO_2/8 nm Hf. Its C-V curve exhibited no ferroelectric hysteresis due to the thick 8 nm hafnium layer that can act as a screening layer, as discussed in section 6.3.5.

A 9 nm HfO_2/4 nm Hf buffer layer was attempted with the additional hafnium layer to preserve the transport properties of the 2DEG. After which 250 nm P(VDF/TrFE) was



(a) (b)

Figure 7.21: C-V curve of 250 nm P(VDF/TrFE)/9 nm HfO_2/4 nm Hf/AlGaN/GaN with 0.1 V_{AC} 1 MHz and a maximum DC poling voltage of 40 V_{DC} applied for 0.5 s at a) for negative bias only 1 V_{AC} and b) for positive and negative biases 0.01 V_{AC}.

spin casted on with circular gold electrodes of approximately 100 nm and diameter 640 μm. With this buffer layer it was possible to observe C-V curves when only applying negative biases with a much larger capacitance/area values than with just a HfO_2 buffer layer. Also this buffer multi-layer was capable of withstanding the application of positive DC voltages without injecting charge into the device, see figure 7.21b.

7.4.5 Leakage Current for Low Aluminium Concentrations

The success of many of the results presented in this thesis can be attributed to the high concentration of aluminium in the upper layer of the heterostructure used of 30%. This high concentration of aluminium can minimise diffusion of elements occurring at the ferroelectric/semiconductor interface. Also it could reduce the leakage current in the devices created with it. It was thus of interest here to see the difference in a C-V curve of a 100 nm Au/ 250 nm P(VDF/TrFE) capacitor structures with an AlGaN heterostructure with a lower aluminium concentration.

The C-V curves presented in section 7.4.1 demonstrated counterclockwise hysteresis curves showing memory retention for AlGaN with aluminium concentration of 30%. Capacitive structures were fabricated in the identical fashion with an AlGaN heterostructure with 11% aluminium. The exact details of this heterostructure were 20 nm $Al_{0.11}Ga_{0.89}N$/GaN having a 2DEG with transport properties of $n_s = 5x10^{12}\,cm^{-2}$ and $\mu = 1500\,^{cm^2}/_{Vs}$ at 300 K. Onto which was deposited 250 nm P(VDF/TrFE) by spin casting and circular top electrodes of 100 nm Au. Multiple C-V curves were done, all showing the same as figure 7.22, measured at an AC frequency of 10 kHz with 0.1 V_{AC}, and poled with $-20\,V_{DC}$ applied for 0.5 s. The C-V curve measured is clockwise indicating that the AlGaN is highly conductive and efficiently suppresses all retention and switching characteristics of the ferroelectrics polarisation.

It is of importance to use AlGaN heterostructures where the top layer has high aluminium concentrations. A limit to this occurs when the aluminium concentration is 50% and greater where it is no longer possible to create an ohmic contact to its 2DEG even after annealing at high temperatures in nitrogen.

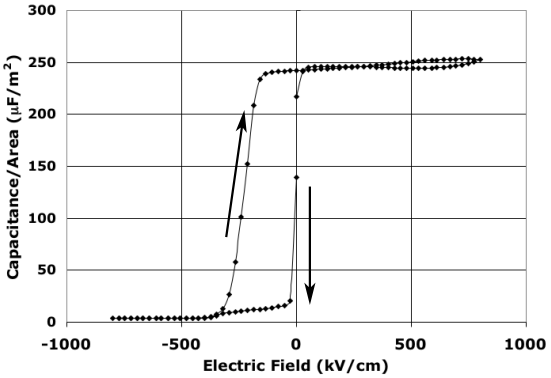


Figure 7.22: C-V curve of 250 nm PVDF/$Al_{0.11}Ga_{0.89}N$/GaN done with 0.1 V_AC at 10 kHz poling with 20 V_{DC} for 0.5 s.

7.5 Experimental Summary

7.5.1 PZT Gate

A 400 nm thick polycrystalline PZT film was deposited by the CSD deposition technique onto an GaN/AlGaN/GaN heterostructure with a 2DEG located 20 nm below the surface. The crystallisation of the PZT layer was done with an annealing process, with an RTA at 700 °C for 30 s in air, to minimise the degradation of the 2DEG while still having perovskite PZT. The PZT film was poled using the SFM domain writing technique in area of 50x50 μm^2, with a DC voltage of ± 40 V applied to the SFM conductive cantilever tip. At 298 K and 77 K it was possible to modulate the electron sheet concentration by a factor of two. However in the as deposited state there was no change of the electron sheet concentration of 5x10^{12} cm^{-2}.

The results from CSD PZT gave a positive indication of the depletion of the electrons in the 2DEG due to the poling of the PZT layer. However, of importance was to further optimise device fabrication in order to observe a stronger effect of depletion due to the change of the spontaneous polarisation in the ferroelectric layer. More extensive measurements need to be done, especially in determining the dependence of polarisation in the PZT layer to the transport properties of the 2DEG with temperature. It was therefore decided to switch to PZT deposited by multiple target magnetron sputtering in order to minimise the deposition temperature.

PZT(40:60) was deposited onto AlGaN/GaN using multiple target magnetron sputtering resulting in 100% (111) textured perovskite PZT without any trace of pyrochlore phases. Three squares of 50x50 μm^2 were poled with ± 50 V applied to the CP-Research scanning probe microscopes conductive cantilever. The essential result from this experiment was the reversible change of conduction of the 2DEG by switching the polarisation in the gate. Poling the gate with the negative voltage results in a decrease of R_s by approximately a factor of 3 within a temperature range of $4 - 298$ K, this modification was stable with time. After erasing this poled state by applying a positive voltage the initial transport properties were restored.

Another sample of 195 nm PZT(40:60) was adapted to have a Hall bar structure with top electrodes of Cr/Au, 10/100 nm, deposited by electron beam evaporation. The DC bias of

±5 V was applied directly to the top electrode after which the Hall effect was immediately measured to observe the change of transport properties after poling. It was observed that the sheet resistance increased by a factor of 800, whereas the sheet concentration and mobility were not able to be measured in the depleted state. There was no long term retention of this modulation of the sheet resistance of the 2DEG. This sample was only able to perform this depletion twice possibly due to fatigue depolarisation or other effects such as the slow arrival of equilibrium due to charge compensation.

The sputtered PZT layer was preferred to that of CSD PZT primarily due to the fact that oriented (111) PZT could be deposited while only decreasing the sheet resistance of the 2DEG in the AlGaN heterostructure by a factor of 4. Unfortunately, at this point the experiments ended involving multiple target magnetron sputtered PZT due to a series of technical difficulties with the sputtering machine. It was thus only possible to conclude that it is possible to modulate the 2DEG by the bound charge associated with the spontaneous polarisation of the ferroelectric layer. However, of interest was to understand how ferroelectric layers affect the transport properties of the 2DEG. A simple way to get a better understanding is to use ferroelectric layers of different properties, since the PZT layer has a large dielectric constant it is of interest to see how a ferroelectric layer of low dielectric constant affects the 2DEG.

7.5.2 MgO Buffer Layer

The use of a MgO buffer layer was successful in that it inhibited inter-diffusion at the interface maintaining the transport properties of the 2DEG in the AlGaN heterostructure. Specifically the transport properties were maintained after the PLD deposition of MgO and the subsequent CSD deposition of 300 nm PZT(40:60). However, it was only possible to control the thickness of the MgO layer to a minimal 10 nm ± 5 nm. Both the C-V measurements and PFM poling measurements concluded that there was no ferroelectric switching in this thin film. This could possibly be due to large screening effects produced by the MgO buffer layer, that might be too thick 15 nm, impinging the 2DEG to being affected by the bound charge associated with the ferroelectric polarisation.

7.5.3 P(VDF/TrFE) Gate

P(VDF/TrFE)(70:30) of 250 nm was able to temporarily deplete the 2DEG of electrons in the AlGaN/GaN heterostructure. This depletion was achieved by poling a gold top electrode with −40 V and performing Hall effect measurements to observe a direct increase in the sheet resistance by a factor three immediately after the voltage was turned off. This depletion effect decreased with time until reaching its pre-poled value.

It was observed to be important to use an AlGaN heterostructure with high aluminium concentration. This was determined from C-V measurements of a Au/P(VDF/TrFE)/AlGaN structure where one device had an aluminum concentration of 30% (the standard sample used in this thesis) and the other 11%. The C-V curve of the sample with 30% aluminium showed hysteretic/ retention behavior, however the C-V curve of the sample with 11% aluminium had a C-V curve representative of charge injection and not ferroelectric switching.

7.5.4 HfO_2 Buffer Layer

The use of HfO_2 to limit inter-diffusion as a buffer layer is not interesting due to an increase of a factor six of the sheet resistance in the 2DEG of the AlGaN heterostructure after its sputtering at 300 °C. It was used to attempt to limit injected charge for the P(VDF/TrFE) ferroelectric on AlGaN, however, the C-V curves generated had inferior memory retention. An attempt was done to preserve the transport properties of the 2DEG by using a bi-layered deposition process, involving the deposition of a hafnium layer before that of HfO_2. This allowed for the conservation of the 2DEG transport properties, when the hafnium layer was approximately 4 nm with 9 nm of HfO_2 with P(VDF/TrFE) the C-V measurements exhibited ferroelectric retention and limited charge injection when applying positive DC biases.

7.6 Does the Layered Structure Kill Ferroelectricity?

When a ferroelectric layer is sandwiched in a structure such as metal/ferroelectric/dielectric/metal will it have the same properties as when it is in a metal/ferroelectric/metal structure? Can the ferroelectric properties be modified according to the properties of the dielectric layer, possibly eliminating all ferroelectricity, if the correct combination of materials are not chosen? One of the main changes in the ferroelectric layer can be a decrease of its "active" spontaneous polarisation due to the large depolarisation field generated from the dielectric layer. The additional phenomenon of charge injection and thus compensation will also be taken into account in order to have a good estimate of the spontaneous polarisation of the ferroelectric layer when an additional dielectric layer is in the structure. The depolarisation field and charge compensation have been introduced in section 2.2, where a diagram representing the depolarisation field is shown in figure 2.3.

Two main problems were already addressed by Ma and Han [2002] for when a ferroelectric layer is deposited on a semiconductor. Firstly, the phenomenon of back-switching due to the large depolarisation field existing when the capacitance of the ferroelectric is greater than that of the semiconductor layer was addressed. The other being poor retention of the polarisation state due to charge trapping and injection. In this discussion the reduction of the spontaneous polarisation will be considered as an additional key challenge in implementing the FeFET.

The explanations of Ma and Han [2002] took into account the hard ferroelectric assumption, with equation 7.3, assuming that the spontaneous polarisation of the ferroelectric layer is fixed.

$$Q_f = P_s A + C_f V_f \tag{7.3}$$

Where as this can be true for a MFM structure where only a small depolarisation field exists due to a low dielectric constant layer at the ferroelectric/metal interface it does not hold true for a ferroelectric sandwiched with a dielectric layer. The reason for this is an increase in the depolarisation field that is created by the additional dielectric layer of finite thickness that has a low dielectric constant.

Using a heterostructure, with a top layer of 20 nm $Al_{0.3}Ga_{0.7}N$, causes this additional

increase to the depolarisation field. In a capacitor structure a "dead" layer of low dielectric constant creates a depolarisation field that depends on the deposition processes and materials used. If depositing a ferroelectric layer on a single layered semiconductor, where the channel that is modified is directly beneath the ferroelectric layer, such as was presented in section 2.1.2 for an LCMO semiconductor, the depolarisation field will also be minimal. But when the channel being modified is 20 nm away from the ferroelectric layer, it will have an additional increase in the depolarisation field. Current technology in growing GaN based heterostructures have optimised the technology to have a 20 nm top layer, with thinner AlGaN top layers the transport properties of the 2DEG will be decreased. Using a thicker AlGaN layer will only increase the depolarisation field and thus reduce the chances of depleting the 2DEG of its electrons, it is thus necessary to modify the ferroelectric layer.

7.6.1 Reduction of the Spontaneous Polarisation

Thermodynamics are used in order to derive the fraction of spontaneous polarisation that is remaining or active when it is deposited onto a dielectric layer. The thermodynamic theory used, or the Ginzburg Landau Theory, is described in more detail in appendix B, where the derivation begins from a Taylor expansion of the thermodynamic potential. The equation from this phenomenological theory that is necessary for estimating the fraction of spontaneous polarisation, is derived in appendix B, equation 7.4. The constant α is inversely proportional to the dielectric constant of a ferroelectric including the soft modes, ϵ_f and was derived in appendix B as equation 7.5. The constant α can also be expressed in terms of the Curie constant, C, and temperature, T_c to get a better understanding of the importance of this parameter. In order for the material to be ferroelectric α must be negative, this is only possible when T_c is greater than the temperature at which the measurement is being performed. Otherwise, when α is smaller than the measuring temperature the material goes to the paraelectric state.

$$\alpha P_s + \beta P_s^3 = E_f \tag{7.4}$$

$$\alpha = -\frac{1}{2\epsilon_o \epsilon_f} = \frac{(T - T_c)}{C} \tag{7.5}$$

The depolarisation field, which was introduced in section 2.2.1, is a main contribution to the decrease of the spontaneous polarisation. The depolarisation field can be calculated for when there is no applied electric field across the structure and equaling the voltage drop across the ferroelectric layer to that in the dielectric layer, equation 7.6.

$$d_f E_f + d_d E_d = 0 \tag{7.6}$$

This can be further simplified to equation 7.7, where the depolarisation field in the ferroelectric layer is equal to E_{dp}=E_f.

$$E_f = -\frac{d_d}{d_f} E_d \tag{7.7}$$

In a linear media, the AlGaN layer, one can use equation 7.8 to relate the electric displacement in the dielectric layer, D_d, to its electric field, E_d, and dielectric constant, ϵ_d.

$$D_d = \epsilon_o \epsilon_d E_d \tag{7.8}$$

The electric displacement in a ferroelectric layer, D_f, is given by equation 7.9. Where E_f and P_f are the electric field and polarisation of the ferroelectric layer respectively. ϵ_b is the background dielectric constant of the ferroelectric layer, representing the dielectric response of the lattice contributions not including the soft mode associated with ferroelectricity.

$$D_f = \epsilon_o \epsilon_b E_f + P_f \tag{7.9}$$

The continuity equation 7.10 states that the current flow through the interface must be continuous.

$$D_f = D_d \tag{7.10}$$

Substituting the specific equation for D_d, equation 7.8, and D_f, equation 7.9, into equation 7.10 gives equation 7.11. Since $P_f = P_s$ when there is no applied electric field across the structure.

$$E_d = \frac{\epsilon_b}{\epsilon_d} E_f + \frac{P_s}{\epsilon_o \epsilon_d} \tag{7.11}$$

Equation 7.12 is given by simplifying equation 7.11.

$$0 = E_f d_f + \frac{\epsilon_b}{\epsilon_d} d_d E_f + \frac{P_s}{\epsilon_o \epsilon_d} d_d \tag{7.12}$$

To facilitate the calculations the constant r, equation 7.13, will be used to represent the thickness of the dielectric layer, d_d, and the thickness of the ferroelectric layer, d_f.

$$r = \frac{d_d}{d_d + d_f} \tag{7.13}$$

Simplifying equation 7.12 it is possible to describe the electric field in the ferroelectric layer by a constant times the spontaneous polarisation in the ferroelectric layer, equation 7.14.

$$E_f = \frac{-r}{\epsilon_o \epsilon_b r + \epsilon_o \epsilon_d (1 - r)} P_s \tag{7.14}$$

The substitution of equation 7.14 into equation 7.4 allows for the derivation of a modified value of α that takes into account the depolarisation field created by a dielectric layer.

The constant α for a ferroelectric capacitor is then modified to α^* as shown in equation 7.15 for a ferroelectric layer on a finite dielectric layer.

$$\alpha^* = \alpha + \frac{r}{\epsilon_o \epsilon_b r + \epsilon_o \epsilon_d (1 - r)} \tag{7.15}$$

Solving equation 7.4 for P_f and calculating the ratio of the spontaneous polarisation in a ferroelectric layer in contact with a dielectric layer to that in a capacitor structure gives equation 7.16.

$$P_{s-layer} = P_s \sqrt{\frac{\alpha^*}{\alpha}} \tag{7.16}$$

Knowing that it is only possible to have α smaller than α^* it can be understood that there will always be a reduction of the spontaneous polarisation in the ferroelectric layer when it is in a structure with a finite dielectric layer. Accounting only for the change in spontaneous polarisation due to the depolarisation field it is possible using equation 7.16 to estimate the spontaneous polarisation of the ferroelectric layer when sandwiched with a dielectric layer. This will be used to demonstrate the effect for the PZT layer using the constants in table 7.10 that agree with the devices fabricated and tested for their gate operation characteristics.

Table 7.10: Constant used for calculating the fractional spontaneous polarisation for a PZT gate

ϵ_f	300
ϵ_b	10
ϵ_d	10.3
ϵ_o	$8.85\text{x}10^{-12}$ C^2/Nm^2
d	20 nm

In fact ferroelectricity will only exist if α^* is negative, when positive the depolarisation field of the dielectric layer will be too strong and negate all ferroelectricity with the ferroelectric layer being in the paraelectric phase. When the depolarisation field is overcome the spontaneous polarisation will be reduced, equation 7.16. Table 7.11 gives some calculated values of α^* and when the layer is ferroelectric the fraction of spontaneous polarisation that overcomes the depolarisation field, due to the low dielectric constant 20 nm layer of $Al_{0.3}Ga_{0.7}N$, is noted. It is observed that it is only when the thickness of the PZT layer exceeds 1150 nm that the spontaneous polarisation is not completely eliminated. However, the electron sheet concentration associated with this spontaneous polarisation is only $1.11\text{x}10^{12}$ $electrons/cm^2$, approximately one tenth of the electron sheet concentration of the 2DEG. This implies that at this thickness the maximal amount at which it is possible to deplete the 2DEG is a reduction of one tenth of its electrons.

What is interesting is that in section 7.3 a $Pb(Zr_{0.40}, Ti_{0.60})O_3$ ferroelectric film with thickness of 130 nm showed a depletion of factor 3 in the sheet resistance and a factor of 1.5 in the electron sheet concentration. The results presented in table 7.11 for a PZT film with thickness of 130 nm explains that the depolarisation field from the $Al_{0.3}Ga_{0.7}N$ layer negates completely any spontaneous polarisation existing in the ferroelectric layer. How

Table 7.11: Calculating α^* and the fractional spontaneous polarisation for PZT deposited onto a 20 nm layer of $Al_{0.3}Ga_{0.7}N$. Where the spontaneous polarisation of PZT in a MFM structure is $10\,\mu C/cm^2$.

Thickness [nm]	α^* **[Nm²/C²]**	$\frac{\mathbf{P_{s-layer}}}{\mathbf{P_s}}$	$\mathbf{n_s}$ **[electrons/cm²]**
Ferroelectricity Suppressed			
65 nm	2.41x10⁹	none	none
130 nm	1.28x10⁹	none	none
195 nm	8.35x10⁸	none	none
300 nm	4.99x10⁸	none	none
Ferroelectricity Reduced			
1146 nm	−5.96x10⁴	0.0178	1.11x10¹²
2000 nm	−7.97x10⁷	0.6504	4.07x10¹³
3000 nm	−1.16x10⁸	0.7837	4.90x10¹³

can it be that it was possible to observe the concept of depletion in the 2DEG due to the poling of the ferroelectric layer?

7.6.2 Charge Compensation

The reason why it is possible to observe the depletion of electrons in the 2DEG when poling the 130 nm PZT film is due to charge compensation. With charge compensation the spontaneous polarisation is decreased, however it can allow the PZT layer to maintain a proportion of its spontaneous polarisation in comparison to when there is no charge compensation. This spontaneous polarisation can still be sufficient to partially deplete the 2DEG when the charge compensation is optimal as will be demonstrated here.

It can be better understood why it is necessary to incorporate charge compensation into our derivation of spontaneous polarisation through the following. Using equation 7.17 derived in section 2.2.1 it is possible to estimate the depolarisation field when there is no charge compensation.

$$E_{dp} = E_f \approx -\frac{d_d}{d_f}\frac{P_s}{\epsilon_o \epsilon_d} \tag{7.17}$$

For a ferroelectric with remanent polarisation $10\,\mu C/cm^2$, a dielectric constant of the dielectric layer ϵ_d=10, thickness of the dielectric layer 10 nm and the thickness of the ferroelectric layer 130 nm the depolarisation field is calculated to be $1.74\,MV/cm$. This depolarisation field is unrealistically high, therefore as presented in section 2.2.2 it is necessary to take into account charge compensation. A main source of charge compensation comes from injected charge which decreases the depolarisation field by σ_{inj} as in equation 7.18 derived in section 2.2.2.

$$E_{dp} \approx -\frac{d_d}{d_f}\frac{P_s - \sigma_{inj}}{\epsilon_o \epsilon_d} \tag{7.18}$$

Incorporating this additional term to calculate the depolarisation field has a direct impact on decreasing it to a more realistic value. Correctly modeling the spontaneous polarisation of the ferroelectric layer, an additional term the charge compensation factor, γ, is added to the previous derived equations 7.4 to 7.16. γ can vary from 0 to 1 where 1 is when there is absolutely no charge compensation where there can be no remaining spontaneous polarisation, and 0 is when there is 100% charge compensation with zero spontaneous polarisation. The corrected spontaneous polarisation, $P_{s-active}$, is now represented by equation 7.19 when taking into account the charge compensation factor. That is due to charge compensation only a fraction of the ideal spontaneous polarisation when in a capacitor structure is "active".

$$P_{s-active} = \gamma P_s \tag{7.19}$$

Solving the continuity equation 7.10 using equations 7.8 and 7.9 as before, but including the new value for the compensated spontaneous polarisation, equation 7.19, it is possible to derive equation 7.20. α^* is the modified value for α taking into account both the depolarisation field due to a dielectric layer and for a fraction, γ, of a compensated polarisation charge.

Substituting the value for the compensated spontaneous polarisation, equation 7.19, into 7.14 and then into equation 7.4 it is possible to derive a new α^* constant. α^* has only one modification to it that is the additional γ term, see equation 7.20. It is important to note that α^* takes into account both the depolarisation field and the charge compensation factor.

$$\alpha^* = \alpha + \frac{r}{\epsilon_o \epsilon_b r + \epsilon_o \epsilon_d (1-r)} \gamma \tag{7.20}$$

Solving equation 7.4 for P_s it is possible to derive equation 7.21.

$$P_{s-layer} = P_{s-active} \sqrt{\frac{\alpha^*}{\alpha}} \tag{7.21}$$

Incorporating equation 7.19 into equation 7.21 it is possible to derive the total spontaneous polarisation of the ferroelectric layer after taking into account the depolarisation field from the dielectric layer and the charge compensation factor γ. The spontaneous polarisation of the ferroelectric layer can then be expressed as a function of the ideal spontaneous polarisation in a capacitor structure, P_s and the constants α and α^*, equation 7.22.

$$P_{s-layer} = P_s \gamma \sqrt{\frac{\alpha^*}{\alpha}} \tag{7.22}$$

Using the constants for PZT listed in table 7.10 it is possible using equation 7.22 to estimate the fraction of spontaneous polarisation ($P_{s-layer}/P_s$) existing in the ferroelectric layer when it is deposited on 20 nm of $Al_{0.3}Ga_{0.7}N$. It is not possible currently to measure exactly how much charge compensation does occur at the ferroeletric/semiconductor interface. This theoretically derived expression allows for confirmation that it can be physically possible to modulate the electrons in the 2DEG when partial charge compensation occurs in a ferroelectric layer of large dielectric constant.

Table 7.12: Calculating γ and the maximal fractional spontaneous polarisation for the optimal γ, for PZT deposited onto a 20 nm layer of $Al_{0.3}Ga_{0.7}N$. Where the spontaneous polarisation of PZT in a MFM structure is $10\,\mu C/cm^2$.

Figure	**Thickness** [nm]	**γ Limit**	**Maximal $P_{s-layer}/P_s$**	**Optimal γ**	**n_s** [**electrons/cm^2**]
7.23	65	0.0725	0.0279	0.0483	$1.74x10^{12}$
7.23	130	0.1283	0.0494	0.0855	$3.09x10^{12}$
7.23	195	0.1840	0.0708	0.1227	$4.43x10^{12}$
7.23	300	0.2742	0.1056	0.1828	$6.60x10^{12}$
7.24	1146	n/a	0.3850	0.6669	$2.41x10^{13}$
7.25	2000	n/a	0.6504	1	$4.07x10^{13}$
7.25	3000	n/a	0.7837	1	$4.90x10^{13}$

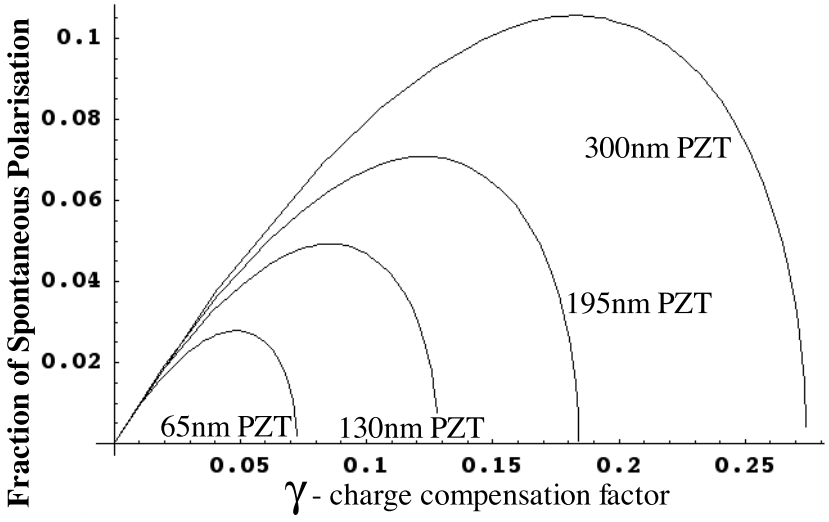


Figure 7.23: The variation of the fractional spontaneous polarisation "active" with the charge compensation factor, γ, for PZT layers of thicknesses 65 nm, 130 nm, 195 nm and 300 nm.

The results of calculations for PZT layers of thicknesses varying from 65 nm to 2 μm are summarised in table 7.12. The γ limit is the minimium factor of charge compensation necessary in order to observe ferroelectricity in the ferroelectric layer, above which no spontaneous polarisation of the ferroelectric layer is "active". The optimal γ is the theoretical value for γ when the fraction of spontaneous polarisation that is "active" in the ferroelectric layer is at its maximum (Maximum $P_{s-layer}/P_s$).

The values from table 7.12 are in fact a summarisation from the graphs ploted of equation 7.22, when varying the thickness of the PZT layer. By plotting γ vs the fraction of spontaneous polarisation is was possible to calculate the values for γ limit, the maximal $P_{s-layer}/P_s$ and the optimal γ. Figure 7.23 shows this plot for PZT layers of thicknesses varying from 65 nm to 300 nm, figure 7.24 for the PZT layer of thickness of 1146 nm and figure 7.25 for the PZT layers of thickness of 2000 nm and 3000 nm.

With a certain amount of charge compensation ferroelectricity can exist in all PZT layers deposited onto $Al_{0.3}Ga_{0.7}N$ when its thickness is greater than 65 nm due to α^* being

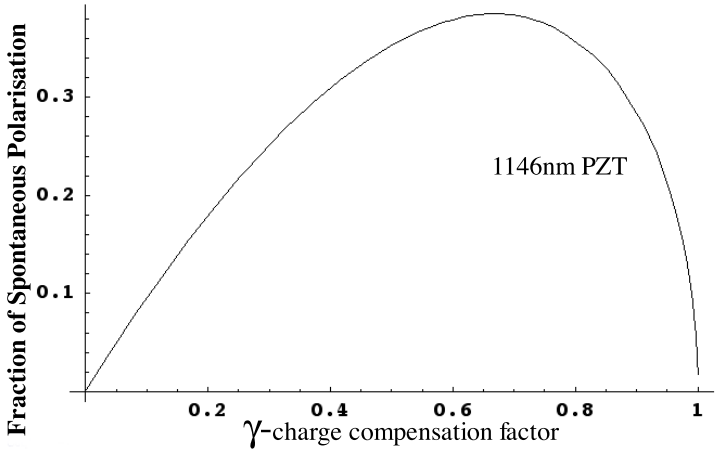


Figure 7.24: The variation of the fractional spontaneous polarisation "active" with the charge compensation factor, γ, for PZT layers of thickness 1146 nm.

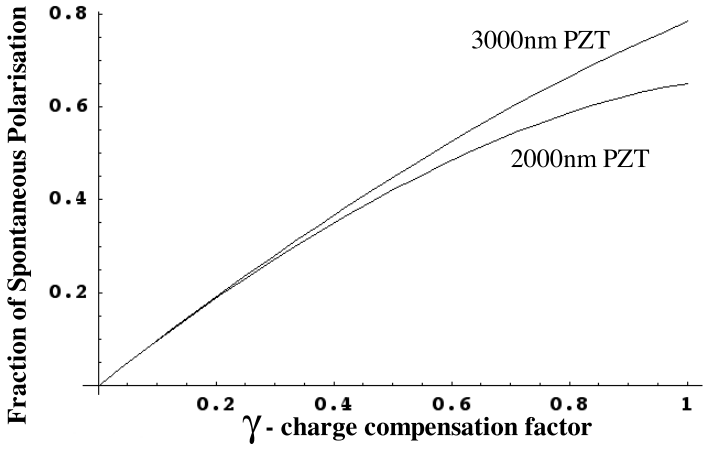


Figure 7.25: The variation of the fractional spontaneous polarisation "active" with the charge compensation factor, γ, for PZT layers of thicknesses 2000 nm and 3000 nm.

negative. It can also be noted that for PZT films of thickness greater than 2000 nm the "active" spontaneous polarisation is greatest when no charge compensation occurs.

Returning back to to the device described in section 7.3 of a $Pb(Zr_{0.40}, Ti_{0.60})O_3$ ferroelectric film with thickness of 130 nm which showed a depletion of a factor 3 in the sheet resistance and a factor of 1.5 in the electron sheet concentration. The results presented in table 7.12 for a PZT film with thickness of 130 nm explains that under the optimal charge compensation scenario the spontaneous polarisation in the ferroelectric layer is reduced by a factor of 0.0494. This spontaneous polarisation will only be able to create a bound charge density of $3.09\text{x}10^{12}$ $^{\text{electrons}}/_{\text{cm}^2}$. This bound charge will allow for an optimal modulation of the electron sheet concentration by a factor of approximately 3.2. As a modulation of the electron sheet concentration of 1.5 was observed it can be determined that this modulation was possible due to charge compensation.

7.6.3 Ferroelectric Layer with a Low Dielectric Constant

The easiest way to minimise the depolarisation field, and conserve the ferroelectrics spontaneous polarisation when working with the $Al_{0.3}Ga_{0.7}N/GaN$ heterostructure is by matching the dielectric constant of the ferroelectric layer with that of the $Al_{0.3}Ga_{0.7}N$ layer. When working with PZT one of the reasons why the depolarisation field was so high is because of its large dielectric constant $\epsilon_{PZT}= 300 >> \epsilon_{Al_{0.3}Ga_{0.7}N}=10.3$. The ferroelectric layer was thus changed to a P(VDF/TrFE)(70:30) thin film with a dielectric constant of 13, decreasing the depolarisation field by a factor of 23. The calculations as presented above were also performed for this co-polymer ferroelectric film using the constants noted in table 7.13.

Table 7.13: Constants used for calculating the fractional spontaneous polarisation for a P(VDF/TrFE) gate.

PVDF	
ϵ_f	6.5
ϵ_b	6.5
ϵ_d	10.3
ϵ_o	$8.85x10^{-12}$ C^2/Nm^2
d	20 nm

Table 7.14 summarises the values for the reduced spontaneous polarisation and the bound charge that is associated with it for P(VDF/TrFE) thickness of 5 nm to 2000 nm. Even with a large reduction in the spontaneous polarisation of a factor 0.6385 as is the case for a 30 nm layer of P(VDF/TrFE) the bound charge associated with it, $2.79x10^{13}$ electrons/cm^2, should still be sufficient to deplete the 2DEG of electrons. For this thesis only the thicker P(VDF/TrFE) films were spin casted onto the AlGaN, but this result states that it could also be possible for thinner P(VDF/TrFE) films (greater than 30 nm) deposited by the Langmuir Blodgett method to have sufficient spontaneous polarisation to deplete electrons from a 2DEG with electron concentration of $1x10^{13}$ electrons/cm^2.

Table 7.14: Calculating α^* and the fractional spontaneous polarisation for P(VDF/TrFE) deposited onto a 20 nm layer of $Al_{0.3}Ga_{0.7}N$. Where the spontaneous polarisation of P(VDF/TrFE) in a MFM structure is 7 $\mu C/cm^2$.

Thickness [nm]	α^* [$\mathbf{Nm^2/C^2}$]	$\frac{\mathbf{P_{s-layer}}}{\mathbf{P_s}}$	$\mathbf{n_s}$ [$\mathbf{electrons/cm^2}$]
Ferroelectricity Suppressed			
5 nm	$3.76x10^9$	none	none
10 nm	$1.01x10^9$	none	none
Ferroelectricity Reduced			
12.7 nm	$-2.70x10^7$	0.0557	$2.44x10^{12}$
30 nm	$-3.54x10^9$	0.6385	$2.79x10^{13}$
250 nm	$-7.86x10^9$	0.9507	$4.16x10^{13}$
2000 nm	$-8.58x10^9$	0.9937	$4.35x10^{13}$

Taking into account the charge compensation factor γ it is possible to observe that it is most probable to deplete the electrons in the 2DEG when there is no charge compensation, as it is at the spontaneous polarisation in the ferroelectric layer is at a maximum when there is no charge compensation. The results of the maximal fractional spontaneous polarisation, the optimal γ and γ limit are summarised in table 7.15 for P(VDF/TrFE) of thicknesses varying from 30 nm and 250 nm. The dependence of the fraction of spontaneous polarisation on γ for the same thicknesses is shown in figure 7.26.

Table 7.15: Calculating γ and the fractional spontaneous polarisation for P(VDF/TrFE) for the optimal γ deposited onto a 20 nm layer of $Al_{0.3}Ga_{0.7}N$. Where the spontaneous polarisation of P(VDF/TrFE) in a MFM structure is $7\,\mu C/cm^2$

Thickness [nm]	**γ Limit**	**Maximal $\mathbf{P_{s-layer}}$ / $\mathbf{P_s}$**	**Optimal γ**	**$\mathbf{n_s}$ [electrons/cm^2]**
30	n/a	0.6386	1	2.79x10^{13}
250	n/a	0.9507	1	4.16x10^{13}

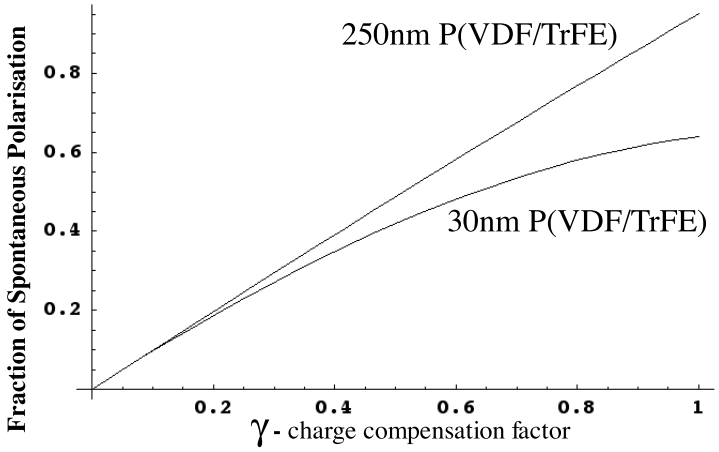


Figure 7.26: The variation of the fractional spontaneous polarisation active with the charge compensation factor, γ, for P(VDF/TrFE) layers of thicknesses 30 nm and 250 nm. Where the spontaneous polarisation of P(VDF/TrFE) in a MFM structure is $7\,\mu C/cm^2$

The spontaneous polarisation can be maintained on a finite dielectric layer when there is an optimal amount of charge compensation, if the ferroelectricity is completely suppressed when there is no charge compensation. However, if the spontaneous polarisation is only reduced when in series with a finite dielectric layer and no charge compensation exists, then the "active" spontaneous polarisation can only be decreased due to charge compensation.

In section 7.4 it was experimentally determined with 250 nm of the low dielectric constant co-polymer, P(VDF/TrFE)(70:30), that it was possible to modulate the sheet resistance of the 2DEG in the AlGaN/GaN heterostructure by at least a factor of three, when poling the ferroelectric with -30 V. However, there was no long term retention of this modulation. Using the graph in figure 7.26, of a 250 nm P(VDF/TrFE) layer in series with 20 nm of AlGaN it is shown that if there is no charge compensation, γ=1, then there should be long term retention of the modulation of the sheet resistance with the

spontaneous polarisation. That is, if the charge compensation, γ, is constant with time. However, if charge compensation increases with time the spontaneous polarisation, that is available to modulate the 2DEG, is decreased. With an increase with time to complete charge compensation there is no spontaneous polarisation left with which to modulate the electrons in the 2DEG. Currently, it is not possible to quantise the amount of charge compensation occurring at the ferroelectric/AlGaN interface.

7.6.4 Optimal Ferroelectric Material

In comparing the results of the calculations above, table 7.16, it is possible to understand that when using a ferroelectric layer with low dielectric constant there is more active spontaneous polarisation. That is there is more spontaneous polarisation available in which to modulate the electrons in the 2DEG even if the low dielectric constant has less spontaneous polarisation available in a MFM structure. For the ferroelectric films of 130 nm and 250 nm, P(VDF/TrFE) has almost all of its spontaneous polarisation active to modulate the 2DEG, however, PZT has only enough bound charge available to only partially deplete the 2DEG.

Table 7.16: Comparing the active spontaneous polarisation of the ferroelectric layer when sandwiched with a 20 nm layer of $Al_{0.3}Ga_{0.7}N$. Where the spontaneous polarisation in a MFM structure of P(VDF/TrFE) is 7 $\mu C/cm^2$ and PZT is 10 $\mu C/cm^2$.

Material	**Thickness** [nm]	**Optimal** γ	**Maximal** $\mathbf{P_{s-active}}$ [$\mu\mathbf{C/cm^2}$]	$\mathbf{n_s}$ [$\mathbf{electrons/cm^2}$]
P(VDF/TrFE)	130	1	6.350	3.97×10^{13}
PZT	130	0.0855	0.494	3.09×10^{12}
P(VDF/TrFE)	250	1	6.655	4.16×10^{13}
PZT	250	0.1542	0.890	5.56×10^{12}

In section 2.5.1 the results from the papers of Aizawa et al. [2004] and Takahashi et al. [2005] were introduced. They integrated two different ferroelectric thin films, of thickness 400 nm, onto silicon with a HfO_2 buffer layer. The ferroelectric $SrBi_2Ta_2O_9$(SBT) showed the strongest effect of depletion with the longest retention in the silicon drain source channel than the results from the $(BiLa)_4Ti_3O_{12}$(BLT) film. This collaborates the results above in that SBT has a lower dielectric constant of approximately 200-300, whereas that of BLT has a dielectric constant of 300-500. If the above approximation for the spontaneous polarisation holds true then it is the SBT film that has more active spontaneous polarisation in which to modulate the 2DEG. The HfO_2 buffer layer can act as a tunneling barrier that does not allow for an increase of charge compensation with time and a strong bi-stable modulation of electrons in the channel.

The use of a low dielectric constant ferroelectric layer gives the possibility for a stronger bi-stable modulation of the semiconductors channel. This holds true not only for the work done in this thesis but is also supported by the results presented by Aizawa et al. [2004] and Takahashi et al. [2005].

7.6.5 Integrating Ferroelectrics and Semiconductors

The integration of ferroelectrics on semiconductors can be facilitated by using ferroelectrics with low crystallisation temperatures or by using buffer layers. When using ferroelectrics with low crystallisation temperatures the solution is efficient as there should be no degrading of the semiconductors transport properties. Initially, it was thought that the high temperature and chemical stability of the GaN-based semiconductors would minimise inter-diffusion and allow them to have the high temperature perovskites deposited onto them. However, it was determined that this was not the case and that careful controlling of the semiconductors transport properties need to be done in order to monitor any change in them.

7.7 Summary: Ferroelectricity in a Layered Structure

It has been theoretically derived that when depositing a ferroelectric layer on a semiconductor heterostructure, which has a dielectric layer of finite thickness, the spontaneous polarisation in the ferroelectric layer can be decreased in comparison to when it is in a capacitor, MFM, structure. This decrease in spontaneous polarisation is due to both the depolarisation field and incomplete charge compensation at the ferroelectric/dielectric interface. If a ferroelectric layer is deposited onto a semiconductor, whose channel to be modified is directly under the ferroelectric layer this decrease in polarisation is less prominent. But in the cases for semiconductor heterostructures where the channel that is modified is located a distance greater than 20 nm from the ferroelectric/dielectric interface these physical phenomenons have a greater impact on the decrease of the spontaneous polarisation.

When trying to use PZT as the ferroelectric gate with $Al_{0.3}Ga_{0.7}N$ the depolarisation field is constrictively high. This is in large part due to the large dielectric constant of the PZT layer in comparison to that of $Al_{0.3}Ga_{0.7}N$. This depolarisation field alone can completely negate all of the spontaneous polarisation in the PZT layer until the PZT has a thickness greater than 1 μm. Due to the fact that depletion observations were made experimentally with a PZT layer of thickness 130 nm helped us understand that all phenomenon were not taken into account. It was necessary to include charge compensation in the derivation of the modified spontaneous polarisation. With this modification it was termed feasible to decrease the sheet resistance of the 2DEG by a factor three. This theoretically verified our experimental observation of a decrease in the electron sheet concentration by a factor of 1.5.

Since the developers of semiconductor heterostructures have already minimised the thickness of the dielectric layer, 20 nm, with a dielectric constant of approximately 10 it is more interesting to vary the ferroelectrics properties in order to minimise any changes in the spontaneous polarisation. The two ways to do this is by using a ferroelectric layer with a small dielectric constant or by using a thick ferroelectric layer.

Working with a ferroelectric layer of low dielectric constant is one approach to minimise the depolarisation field and conserve the spontaneous polarisation of the ferroelectric. This was done by experimenting with the co-polymer P(VDF/TrFE)(70:30). With the theory

derived here it should be feasible to deplete the 2DEG with this layer as the reduction in spontaneous polarisation is less significant. However, the experimental results showed that it is possible to deplete the electrons in the 2DEG by poling the P(VDF/TrFE) layer without having long term retention of this depletion. This can be due to the fact that compensating charge is built up, with time, at the ferroelectric/semiconductor interface causing the elimination of all spontaneous polarisation in the ferroelectric layer.

Chapter 8

Conclusion

The present work directly demonstrates the ferroelectric gate operation and capabilities in the PZT/AlGaN/GaN and P(VDF/TrFE)/AlGaN/GaN systems, which constitutes a new step towards a GaN-based ferroelectric FET device.

8.1 Gate Operation

It was proven that once PZT had been deposited on AlGaN/GaN it was possible to pole the PZT and have it retain this polarisation. Hall measurements showed that the polarisation of the PZT layer impacts the conductivity in the 2DEG, inducing local depletion of charge carriers in the 2DEG when it is poled negatively. More specifically, a (111) oriented sputtered PZT(40:60) ferroelectric gate, of 130 nm, on the $Al_{0.3}Ga_{0.7}N$ heterostructure depleted the two dimensional electron gas with an increase of the sheet resistance by a factor of three, when poling the PZT layer with -40 V directly to the conductive cantilever used in a piezoresponse force microscope. This increase in sheet resistance was stable for more than three days and was the first successful observation of a PZT gate on a semiconductor heterostructure. More measurements can be done in varying the thickness and composition of the PZT layer to get a better fundamental understanding of the PZT/AlGaN/GaN system before it becomes suitable for FeFETs. With improved quality of the PZT film and an optimised poling procedure one may expect a stronger depletion effect than that reported.

The ferroelectric co-polymer P(VDF/TrFE) (70:30) was investigated as a gate on the $Al_{0.3}Ga_{0.7}N$ heterostructure, due to its low dielectric constant, ϵ=13. It was also of interest to investigate this ferroelectric because it has a low crystallisation temperature of 130 °C which most semiconductors will be able to sustain, without any degradation to its properties. When the P(VDF/TrFE) was poled, with -30 V to a top gold electrode, the sheet resistance was modulated by a factor three. There was only short term retention of this modulation, possibly due to the increase of charge compensation with time until a full suppression of the spontaneous polarisation ocurred. Currently, this structure does not meet the demanding 10 year retention requirements necessary for FeFETs. One application, for this structure, is dynamic random access memory, DRAM, where the refresh rate necessary would be minimised, allowing for lower power consumption.

The Landau theory was combined with the concept of ferroelectric depolarisation field

to predict the changes in the spontaneous polarisation of a ferroelectric layer, when it is deposited onto a semiconductor heterostructure. In some scenarios, the depolarisation field created by the AlGaN top layer can not only partially suppress but completely negate all of the spontaneous polarisation in the ferroelectric layer. The effect of suppressing the spontaneous polarisation can be reduced if charge compensation of the spontaneous polarisation is taken into account. An optimal design of a FeFET would have a small depolarisation field, which can be done by using a ferroelectric layer with a small dielectric constant or a thick ferroelectric layer.

8.2 Processing

The two ferroelectric layers lead zirconium titanate, PZT, and the organic polymer poly(vinylidene fluoride/trifluoroethylene), P(VDF/TrFE) were successfully deposited onto the 20 nm AlGaN/GaN heterostructures. High quality ferroelectric crystalline layers were deposited while preserving the transport properties of the 2DEG in the AlGaN/GaN heterostructure. PZT was best deposited by multiple target magnetron sputtering since it was possible to obtain highly textured (111) perovskite PZT without any traces of pyrochlore phases, while only increasing the sheet resistance of the 2DEG at the AlGaN/GaN interface by a factor three. The low crystallisation temperature of P(VDF/TrFE)(70:30), 130 °C, allowed for the spin casting of a high quality ferroelectric co-polymer without any change in the transport properties of the AlGaNs 2DEG.

The deposition of the additional buffer layers, MgO and HfO_2, were also obtained on the 20 nm AlGaN/GaN heterostructures. The MgO layer was deposited by PLD onto AlGaN, and successfully preserved the transport properties of the 2DEG in the AlGaN/GaN heterostructure, after the deposition of MgO and a 300 nm CSD PZT layer. Unfortunately, it was only possible to control the thickness of the MgO layer deposited to a minimal 10±5 nm, which gave too thick of a buffer layer, and acted as a charge screening layer. The RF sputtering process for HfO_2 on AlGaN was developed and optimised. When depositing HfO_2 on AlGaN diffusion occurs causing an increase of the 2DEGs sheet resistance by a factor six, and did not reduce charge injection in a P(VDF/TrFE)/HfO_2/AlGaN structure. A two step deposition, of hafnium and HfO_2, was developed and preserved the 2DEG transport properties. Preliminary experiments with this bi-layered buffer shows that it reduces charge injection, however, further optimisation needs to be done.

The ECR-RIE etching process that was developed for etching PZT with a plasma chemistry of Ar, CCl_4 and CF_4 was extended and modified to simultaneously etch a PZT/AlGaN/GaN structure with an etching rate of 30 $^{nm}/_{min}$, without destroying the aspect ratio of the side walls.

8.3 Outlook

The goal achieved in this thesis is a step forward in the understanding of the coupling between two different systems: a ferroelectric film and a AlGaN/GaN heterostructure with a 2DEG located close to the interface. An insight into the properties of the ferroelectric/semiconductor interface, which is important for further development of ferroelectric devices was obtained with this research. However, the successful operation of

the devices presented here have still to be optimised before being suitable for commercial devices.

The multiple target RF sputtered PZT gate on AlGaN was shown to modulate the sheet resistance of the 2DEG by a factor of three with long term retention. The variation of deposition conditions were not fully exhausted in this thesis and the annealing in nitrogen of the bottom electrodes should be done as a first step in order not to degrade the switching characteristics of PZT. Of interest would be to fabricate devices with a wide range of PZT thicknesses to see its impact on the modulation of the electrons in the 2DEG. The use of a HfO_2/Hf buffer layer in a PZT/AlGaN structure could sufficiently reduce inter-diffusion at the interfaces while allowing the 2DEG to be modified by its poling. The investigation of PZT depositions at lower temperature can also be investigated, including single target sputtering of PZT which can usually grow perovskite PZT at a lower temperature than multiple target sputtering.

An advantage of using PZT is that when combined with AlGaN it allows for high temperature devices. The disadvantage is that due to the large dielectric constant of PZT, when it is in contact with the AlGaN layer a large depolarisation field inhibits the modulation and retention of the depletion of electrons in the 2DEG. The effects of depolarisation field can be minimised by using a ferroelectric with low dielectric constant such as P(VDF/TrFE) which has a dielectric constant of 13. However, it has a low melting temperature of 160 °C and Curie temperature of 110 °C, which only allows for its use in devices operated at 60 °C and below. A change in the P(VDF/TrFE) composition could increase the Curie temperature of the ferroelectric layer allowing for the design of devices at higher temperatures.

The deposition of P(VDF/TrFE) on AlGaN was developed precisely in hope of observing a stronger depletion effect, because it has a smaller dielectric constant and the depolarisation field created is less significant. The same modulation of the sheet resistance by a factor of three was observed when poling the P(VDF/TrFE) film, however, this modulation had no long term retention. This short term retention could be due to the fact of charge leakage in the AlGaN and it is thus of interest to also optimise the AlGaN/GaN heterostructure. It was only possible in this research to make initial experiments with this co-polymer ferroelectric layer. Of interest is to deposit thin films by the Langmuir-Blodgett method, to see if these modified structures can cause a stronger depletion effect in the AlGaN/GaN heterostructures.

Low-dimensional nano-structures such as quantum dots, wires, and rings have potential to be implemented in this ferroelectric/semiconductor heterostructure allowing for the studying of phenomena associated with quantum confinement and ballistic electron transport. Their applications would include single-electron transistors and spintronic devices for a future generation of electronics. This thesis is an instrumental step forward in the demonstration of a possibility of fabrication of such nano-structures by direct ferroelectric domain writing using a ferroelectric/semiconductor heterostructure device.

The proposed approach provides unique features that are attractive for fundamental studies as well as for engineering of nano-devices. The project suggests a technique of semiconductor device fabrication in a reversible way, with the possibility of subsequent patterning, erasing and re-writing of different nano-features on the same device structure. This delivers new opportunities for a wide range of physical experiments involving electron transport in low-dimensional systems as well as for device optimisation. The study of domain writing

and switching kinetics in ferroelectric films deposited on semiconductor heterostructures, with a 2DEG, is of interest for high-density information storage solutions alternative to existing devices.

Appendix A

PZT Sputter Conditions

Table A.1: PZT sputter conditions when depositing on the AlGaN/GaN heterostructure

Process	Pressure [T]	Separation Distance [%]	Sample Location	Rotation Speed [rpm]	Temp. [°C]	Zr : DC Power [W]	Pb : RF Power [W]	Ti : DC Power [W]	O_2 Flow [sccm]	Partial Pressure [mT]	Time [min]
Wait for Vacuum	$6.0x10^{-5}$	100	S1T1	0	400	0	0	0	0	1	0.167
Heating	$4.0x10^{-4}$	100	S1T3	0	450	0	0	0	0	10	5
Second Heating	$4.0x10^{-4}$	100	S1T3	0	700	0	0	0	0	10	5
Gas Flow	$4.0x10^{-4}$	100	S1T3	0	700	0	0	0	20	16	180
Pre-Sputter Targets	$9.0x10^{-4}$	100	S1T3	0	700	100	200	150	20	16	10
Deposit TiO_2	$9.0x10^{-4}$	100	S1T2	0	700	0	100	0	20	10	2
Deposit PZT	$9.0x10^{-4}$	16	scan	6	700	128	300	150	20	16	22
Turn off Targets	$9.9x10^{-4}$	100	scan	6	400	0	0	0	20	16	0.167
Cooling	$9.9x10^{-4}$	100	S1T1	6	400	0	0	0	20	80	60

Appendix B

Ginzburg Landau Theory

The Legendre transform can be used to describe the Helmholtz free energy, H, in terms of the internal energy, U, temperature, T, and entropy, S for a mechanically free sample, Strukov and Levanyuk [1998], with:

$$H = U - TS \tag{B.1}$$

The differential of the thermodynamic potential for a ferroelectric material with total polarisation, P_{total} is given by:

$$dG = -SdT - P_{total}dE \tag{B.2}$$

At constant temperature the differential of the thermodynamic potential with respect to the electric field, E, is:

$$[\frac{\partial G}{\partial E}]_T = -P_{total} \tag{B.3}$$

Considering the total polarisation except the background contribution, P_f, as the order parameter, and only polarisation in the direction perpendicular to the sample, the Taylor expansion (using constants α and β) of the thermodynamic potential for a ferroelectric gives:

$$G = \frac{1}{2}\alpha P_{total}^2 + \frac{1}{4}\beta P_{total}^4 - EP_{total} \tag{B.4}$$

Higher order terms, P_{total}^6 and above, of the Taylor expansion were ignored due to the fact that P_{total} is already small so that these terms will not significantly contribute to the thermodynamic potential. Polarisation gradients and their surface boundary conditions were also not included due to the assumption that the polarisation is distributed evenly in the ferroelectric film.

The system, or structure, prefers to minimise the free energy, which is determined by calculating $\partial G/\partial P_f = 0$ from the above equation B.4.

$$\frac{\partial G}{\partial P_f} = 0 = \alpha_1 P_f + \beta P_f^3 - E \tag{B.5}$$

Where:

$$P_{total} = P_f + P_b \tag{B.6}$$

When there is no electric field applied to the ferroelectric film there is only the depolarisation field in the ferroelectric layer, E=E_f and the total polarisation of the ferroelectric layer is spontaneous, P_f=P_s.

$$E_f = \alpha P_s + \beta P_s^3 \tag{B.7}$$

Derivation of α for T < T_c

The derivation of α can be done for no electric field or depolarisation field giving the following equation:

$$0 = \alpha P_s + \beta P_s^3 \tag{B.8}$$

Solving for P_s gives:

$$P_s^2 = -\frac{\alpha}{\beta} \tag{B.9}$$

$$\frac{1}{\epsilon_o \epsilon_f} = \frac{\partial^2 G}{\partial P_s^2} = \alpha + 3\beta P_s^2 \tag{B.10}$$

The substitution of equation B.9 into equation B.10 gives, α can also be expressed in terms of the materials curie constant, C, and its Curie temperature, T_c:

$$\frac{1}{\epsilon_o \epsilon_f} = -2\alpha = -2\frac{(T - T_c)}{C} \tag{B.11}$$

Electric Displacement for Ferroelectric Materials

The classical equation used for the electric displacement, D, in terms of the total polarisation of a material, P_{total}, is:

$$D = \epsilon_o E + P_{total} \tag{B.12}$$

Where it is possible to modify equation B.12 to obtain equation B.14 using the fact that the total polarisation can be separated into two polarisations, that of ferroelectricity and the other of some backgroud polarisation, P_b, equation B.6.

This background polarisation is in fact related to the hard lattice contribution of the film and does not describe a ferroelectric layer. It can be expressed in terms of the background dielectric constant, ϵ_{b},:

$$P_b = \epsilon_o(\epsilon_b - 1)E \tag{B.13}$$

Equation B.12 can then be expressed as such:

$$D = \epsilon_o\epsilon_b E + P_f \tag{B.14}$$

In the hard ferroelectric assumption, $\mathrm{P_s}$ is considered constant and the electric displacement can be expressed as equation B.15:

$$D = \epsilon_o\epsilon_f E + P_s \tag{B.15}$$

Appendix C

XRD Reference Spectra

JCPDS File No.	86-147
Chemical Compound	TiO_2
Crystal Structure	tetagonal - rutile
	P42/mmm (136)
a lattice	4.594 Å
c lattice	2.9586 Å

JCPDS File No.		2-1078
Chemical Compound		GaN
Crystal Structure		Hexagonal
		P63mc(186)
a lattice		3.186 Å
c lattice		5.178 Å
2θ	Texture Index	Orientation
34.605 °	50	002
73 °	20	004

JCPDS File No		50-346
Chemical Compound		$Pb(Zr_{0.44}Ti_{0.56})O_3$
Crystal Structure		Tetragonal
		P4mm
a lattice		4.0172 Å
c lattice		4.1391 Å
2θ	Texture Index	Orientation
21.443 °	16	001
22.097 °	18	100
30.995 °	100	101
31.448 °	37	110
38.398 °	24	111

JCPDS File No.	3-721
Chemical Compound	$PbTiO_3$
Crystal Structure	Tetragonal
a lattice	3.9044 Å
c lattice	4.1522 Å

JCPDS File No.		42-1650
Chemical Compound		PVDF
Crystal Structure		Monoclinic
		P21/c
a lattice		4.96 Å
b lattice		9.64 Å
c lattice		4.62 Å
2θ	Texture Index	Orientation
17.869 °	34	100
18.392 °	41	020
20.119 °	100	110
33.194 °	23	130
37.281 °	23	040
37.413 °	23	210
38.626 °	27	131

JCPDS File No		34-104
Chemical Compound		HfO_2
Crystal Structure		Monoclinic
		P21/a
a lattice		5.2851 Å
b lattice		5.1819 Å
c lattice		5.1157 Å
2θ	Texture Index	Orientation
28.336 °	100	-111
58.635 °	5	-222
61.759 °	6	311

JCPDS File No.		2-0885
Chemical Compound		Hf
Crystal Structure		Hexagonal
		P63/mmc
a lattice		3.32 Å
c lattice		5.46 Å
2θ	Texture Index	Orientation
31.475 °	80	100
32.778 °	100	002
35.308 °	40	101

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Acknowledgments

I have worked on this thesis from January 2003 to March 2007 in the Ceramics Laboratory at EPFL. First of all I would like to thank Professor Nava Setter and Dr. Igor Stolichnov for taking me into their group. I thank you for your advice and the trust you have shown in my work.

Thanks to Prof. Hans Jorg Mathieu for presiding the jury and thanks to Prof. Nicolas Grandjean, Dr. Stéphane Hiboux and Prof. Jeffrey S. Cross for having taken the time to assist in my exam.

Thanks to those who have assisted me with the experiments, the members of the Ceramics Laboratory, with special thanks to the senior scientists, Dr. Tagantsev, Prof. Muralt, Dr. Damjanovic and Dr. Colla. Thanks to Roman Gysel, Andreas Nöth and Florian Calame for proofreading this thesis. Thanks to the staff at the Center of MicroNanoTechnology, CMI, especially Guy Clerc and Philippe Langlet, for their great help. Thanks to Giancarlo Corradini from the Laboratory of Microengineering for Manufacturing 2 for help with the bonding of working devices. Thanks to Nicolas Leiser for the help in the clean room at the Institute of Quantum Electronics and Photonics. Thanks to Marcel Py from the Laboratory of Quantum Optoelectronics at the Institute of Quantum Electronics and Photonics, IPEQ, for help with the Hall measurements. Thanks to Lazlo Forro, from the Laboratory of Nanostructures and Novel Electronic Materials, for help with 4K cryostats. Thanks to Dr. Su Dong, Dr. Silviu Cosmin Sandu, Dr. Marco Cantoni, Mathieu Charrière and Julien Maret all from the Ceramics Laboratory for help with TEM imaging. Thanks to Nicolas Xanthopoulos in the Metallurgical Chemistry Laboratory at the Institute of Materials for surface analysis and depth profiling by XPS.

Thanks to Lino Olivetta, Jaques Castano, Mme Eva Maria Favre, Mme Emanuela Mancianti Groebli, and Mme Yuko Kagata Spitteler.

Special thanks to all my friends: Erika, Jochen, Aga, Michal, Blanca, Michal, Elina, Michal, Kris, Martin, Pam, Andy, Pascal, Natascha, Sergey.....

Great many thanks to my friends and family who gave me enormous amounts of support when I broke my back in the summer of 2005. Special thanks to Pam and Martin for coming by so often and making "Knödel" and "Kaiserschmarren". To my mother thanks for coming all the way over to Switzerland to be my nurse and right arm for six weeks. Many thanks to my second "backbone", husband, for being so helpful and patient.

Many thanks to my family in-law for their support and for coming to visit us. Thanks Birgit, Hans, Sandra, Søren and Clara for the wonderful moments.

To the people I owe the most: Mom and Dad, thanks for always believing in me. To Wendy my wonderful sister and my great husband Kim.

Publications

Papers

1. I. Stolichnov, L. Malin, P. Muralt and N. Setter. Nonvolatile gate effect in the PZT/Al-GaN/GaN heterostructure. Journal of the European Ceramic Society, to be published, 2007.

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Curriculum Vitae

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EDUCATION

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B.A.Sc. Engineering Physics program
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2001 Technical University of Denmark
Guest student (physics and semiconductor processing)

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French studies

1995 - 1997 Capilano College
Engineering transfer program

WORK EXPERIENCE

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Carbon nanotubes for field emission displays

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Superconducting tunneling junctions

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CDMA network setup and analysis