Growth mechanisms of III-V semiconductor nanostructures on silicon

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PAR

Eleonora RUSSO

acceptée sur proposition du jury:

Prof. K. Scrivener, présidente du jury
Prof. A. Fontcuberta i Morral, directrice de thèse
Prof. J. Arbiol, rapporteur
Prof. J.-C. Harmand, rapporteur
Dr M. A. Lingenfelder, rapporteuse

EPFL

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Alla mia stella, Beatrice,
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Abstract

The aim of this thesis is to understand the dynamics of the growth of catalyst-free III-V semiconductor nanostructures on silicon substrates, focusing the attention mainly on the early stages of growths. A detailed understanding of this first phase of the process is a key step to obtain a completely successful integration of highly functional materials, like the III-Vs, on the CMOS platform, and to synthesize nanostructures with tailored properties. Indeed, the first mandatory step in nanotechnology is the possibility to fabricate nanostructures and nanomaterials, i.e. structures and materials with at least one dimension falling in the nanometer scale. Among different nanostructures, semiconductor nanowires (NWs) have proven to be versatile building blocks for a manifold of applications.

In this work two types of nanostructures have been investigated: NWs and V-shaped nanomembranes. Their growth has been performed by molecular beam epitaxy (MBE), a technique that allows to produce ultrapure nanostructures, with very high crystalline quality and atomically sharp interfaces. The growth has been obtained with a self-catalyzed approach, meaning that no external material, apart the constituents of the semiconductor to be grown, has been used. This allows to avoid any possible contamination of the substrate, a fundamental requirement to ensure a full compatibility with the silicon technology.

We performed a systematic study on the growth directions of self-catalyzed GaAs NWs grown on silicon substrates. Indeed, when growing III-V NWs on silicon non vertical wires always appear. In order to make NW-based structures on silicon effective for applications like energy harvesting (one of the most promising so far) it is mandatory to control the growth direction and in particular to maximize the yield of NWs perpendicular to the surface. By analyzing the first stages of growth we shed light on the mechanism responsible for the different NWs orientations: we optimized the growth conditions to obtain up to a 100% yield of vertical NWs.

Having attained growth of nanostructures in an ordered manner along regular arrays is a subsequent step for the fabrication of devices. In this work our capability to control growth of InAs and GaAs NWs in arrays is presented and the existing challenges for the reproducible growth are highlighted.

Lastly, we turned to the growth of nanostructures on exactly oriented (001) substrates, which would make the III-V/group IV integration compatible with the current technological processes. This led us to the discovery of a new class of III-V semiconductor nanostructures, called V-shaped nanomembranes, characterized by a unique morphology and growth mechanism and possessing interesting optical properties. An accurate characterization of their morphology and a complete understanding of their nucleation and growth mechanism is

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reported. These results give a clear pathway of how to obtain fully controlled structures which as such could be useful for the realization of complex branched interconnected nanoelectronic devices.

Key words: III-V nanostructures, nanowires, nanomembranes, molecular beam epitaxy, growth mechanisms

Résumé

Le but de cette thèse est de comprendre les dynamiques de croissance de nanostructures de matériaux semi-conducteurs III-V sur des substrats de silice, synthétisées sans l'aide de catalyseurs et en accordant une attention particulière aux premiers stades de croissance. Une compréhension exhaustive de la phase initiale du processus est fondamentale afin de pouvoir intégrer des matériaux hautement fonctionnels, tels que les matériaux composés par les colonnes III et V, sur la plateforme CMOS et afin de pouvoir synthétiser des nanostructures avec des propriétés ad hoc. En nanotechnologie, la capacité de fabriquer des nanostructures et des nanomatériaux, c'est-à-dire des structures et des matériaux ayant au moins une dimension de l'ordre du nanomètre, constitue un prérequis décisif. Parmi les différentes nanostructures, les nano fils de matériel semi-conducteur ont révélé leur potentiel d'utilisation comme éléments constitutifs polyvalents dans différentes applications.

Dans ce travail de thèse, nous avons investiguè deux types de nanostructures : les nanofils et les nanomembranes a V. Leur croissance a ètè obtenue par èpitaxie à faisceau molèculaire. Cette technique permet de produire des nanostructures ultra pures de haute qualitè cristalline et avec des interfaces d'une prècision au niveau atomique. La croissance a ètè obtenue sans introduire d'autres matèriaux que les constituants du semi-conducteur à rèaliser. Ceci a permis d'èviter toute contamination du substrat, exigence d'importance fondamentale pour une compatibilitè complète avec la technologie du silice.

Nous avons effectuè une è tude systè matique des directions de croissance de nanofils en GaAs sur des substrats de silice. Les nanofils III-V croissent non seulement verticalement par rapport au substrat mais aussi en suivant diffè rentes orientations inclinè es. Toutefois, pour utiliser les nanofils dans des applications telles que la rè colte d'è nergie (une des plus prometteuses jusqu'ici), le contro̅le de la direction de croissance et la maximisation du nombre de nanofils orthogonaux à la surface de croissance acquiè rent une importance fondamentale. En analysant les premiers instants de croissance, nous avons compris le mè canisme responsable des diffè rentes orientations, ce qui nous a permis d'optimiser les conditions de croissance pour obtenir 100% de nanofils verticaux.

La croissance de nanostructures de façon ordonnèe et dans des positions prèdèfinies est une ètape ultérieure de la rèalisation d'un dispositif. Dans ce travail de thèse, nous dèmontrons notre capacitè à faire croître des nanofils de GaAs et de InAs alignès et nous mettons en èvidence les difficultès rencontrèes dans la reproductibilitè des croissances.

Enfin, nous nous sommes occupès de la croissance de nanostructures sur des substrats avec orientation cristallographique (001) dans le but de rendre l'intègration des matèriaux III-V et

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groupe IV compatible avec les processus technologiques de l'industrie des semi-conducteurs actuelle. Ceci nous a fait dècouvrir une nouvelle classe de nanostructure III-V, les nanomembranes a V, caractèrisèes par une morphologie et un mècanisme de croissance uniques et dotèes de propriètès optiques intèressantes. Nous rapportons une description soignèe des caractèristiques de leur morphologie, de leur nuclèation et de leur mècanisme de croissance. Ces rèsultats montrent clairement la voie pour obtenir des nanostructures parfaitement contrôlèes utilisables pour la rèalisation de nanodispositifs èlectroniques interconnectès.

Mots clefs : nanostructure III-V, nanofils, nanomembranes, èpitaxie à faisceau molèculaire, mècanisme de croissance

Riassunto

Lo scopo di questa tesi è la comprensione delle dinamiche di crescita di nanostrutture di materiali semiconduttori III-V su substrati di silicio, sintetizzate senza l'ausilio di catalizzatori, con particolare attenzione ai primi stadi di crescita. Un' esaustiva comprensione della fase iniziale del processo è fondamentale per poter integrare materiali altamente funzionali, come i materiali composti delle colonne III e V, sulla piattaforma CMOS, e per poter sintetizzare nanostrutture con proprietà ad hoc. Un prerequisito chiave nelle nanotecnologie è infatti la capacità di fabbricare nanostrutture e nanomateriali, cioè strutture e materiali con almeno una dimensione nell'ordine del nanometro. Tra le varie nanostrutture, i nanofili di materiale semiconduttore hanno dimostrato di poter essere utilizzati come versatili elementi costitutivi in diverse applicazioni.

In questo lavoro di tesi sono state investigati due tipi di nanostrutture: i nanofili e le nanomembrane a V. La loro crescita è stata ottenuta per epitassia a fascio molecolare. Questa tecnica permette di produrre nanostrutture ultra pure, di grande qualità cristallina e con interfacce precise a livello atomico. La crescita è stata ottenuta senza introdurre materiali diversi dai costituenti del semiconduttore da realizzare. Questo ha permesso di evitare ogni possibile contaminazione del substrato, requisito di fondamentale importanza per una completa compatibilità con la tecnologia del silicio.

Abbiamo eseguito uno studio sistematico delle direzioni di crescita di nanofili in GaAs su substrati di silicio. I nanofili III-V non crescono soltanto verticalmente rispetto al substrato ma anche seguendo diverse orientazioni inclinate. Tuttavia, per utilizzare i nanofili in applicazioni come quelle di raccolta dell'energia (le più promettenti finora), diventa di fondamentale importanza controllare la direzione di crescita e la massimizzazione del numero di nanofili ortogonali alla superficie di crescita. Analizzando i primi istanti di crescita abbiamo compreso il meccanismo responsabile delle diverse orientazioni. Questo ci ha permesso di ottimizzare le condizioni di crescita per ottenere il 100% di nanofili verticali.

Un passo successivo per la realizzazione di un dispositivo è crescere le nanostrutture in maniera ordinata in posizioni predefinite. In questo lavoro di tesi dimostriamo la nostra capacità di crescere nanofili di GaAs e InAs allineati ed evidenziamo le difficoltà esistenti nella riproducibilità delle crescite.

Infine, ci siamo occupati della crescita di nanostrutture su substrati con orientazione cristallografica (001), al fine di rendere l'integrazione dei materiali III-V e gruppo IV compatibile con i processi tecnologici dell'attuale industria di semiconduttori. Questo ha portato alla scoperta di una nuova classe di nanostrutture III-V, le nanomembrane a V, caratterizzate da una morfo-

logia e un meccanismo di crescita unici e con interessanti proprietà ottiche. Riportiamo una caratterizzazione accurata della loro morfologia e la descrizione della loro nucleazione e del loro meccanismo di crescita. Questi risultati indicano una strada chiara per poter ottenere nanostrutture perfettamente controllate utili per la realizzazione di nanodispositivi elettronici interconnessi.

Parole chiave: nanostrutture III-V, nanofili, nanomembrane, epitassia a fascio molecolare, meccanismi di crescita

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List of Acronyms

$APBs$ Anthiphase boundaries

CBE Chemical Beam Epitaxy

CVD Chemical Vapor Deposition

EDX Energy-Dispersive X-ray

fcc Face centered cubic crystal

FM Frank-van der Merwe

$HAADF$ High Angle Annular Dark Field

LA Laser Ablation

MBE Molecular Beam Epitaxy

$MOVPE$ Metal Organic Vapor-Phase Epitaxy

NWs Nanowires

QDs Quantum Dots

$RHEED$ Reflection High Energy Electron Diffraction

SAE Selective Area Epitaxy

SK Stranski Krastanov

$STEM$ Scanning Transmission Electron Microscopy

UHV Ultra High Vacuum

VLS Vapor Liquid Solid

VSS Vapor Solid Solid

VW Volmer Weber

WZ Wurtzite

ZB Zinc-blende

1 Introduction

The aim of this thesis work is to study the growth of III-V compound semiconductor nanostructures on silicon substrates. Two types of nanostructures have been investigated: nanowires and V-shaped nanomembranes. Both have been synthesized by molecular beam epitaxy without the use of external catalysts. Several aspects of the growth have been analyzed ranging from the nucleation to the organization in ordered arrays.

The first chapter presents a concise description of the III-V semiconductor nanostructures, showing their peculiar properties and their potentiality as building blocks for future electronics and optoelectronics.

The second chapter describes the growth mechanisms and techniques of the nanostructures examined in this thesis. It also provides a literature review highlighting some open issues in our research field and explaining the choices made during the thesis.

In the third chapter our growth experiments and the original contribution of this thesis are presented. A detailed study on the initial stages of growth of self-catalyzed nanowires on silicon substrate is reported, with the aim of understanding the appearance of non vertical wires. The mechanism responsible for the occurrence of non vertical growth directions is unraveled and the possibility to control and tune it through the growth conditions is experimentally proven. In the same chapter our capability to control the growth of nanowires along regular patterns is also presented. Lastly, a recently discovered class of III-V semiconductor nanostructures, called V-shaped nanomembranes, is described in detail. The unique morphology and crystalline structure is characterized accurately and a complete understanding of the nucleation and growth mechanism is reported.

The fourth chapter presents the possibilities for future development of our work and concludes the thesis.

1.1 The down scaling: from micro to nano fabrication

In 1947 at the Bell Lab, John Bardeen, Walter Brattain and William Shockley invented the bipolar transistor after a relatively brief period of collaboration [1]. They probably did not imagine that their device would have resulted in one of the most important inventions of the century, effectively giving birth to the electronics industry. The three American physicists eventually won the Nobel Prize in 1956 for their research on semiconductors and the discovery of the transistor effect . In the late 1950s another invention by a Texas Instrument engineer, Jack Kilby, revolutionized the electronics industry once again: the integrated circuit [2]. Kilby devised a way to produce all the components of a circuit (resistors, transistors, capacitors, etc) on the same die. This idea, which earned him the Nobel Prize, helped the improvement of performance, reduced the cost of making the systems and ultimately opened the age of microelectronics.

For 40 years the microelectronics industry experienced a phase of explosive growth: integrated circuits or "chips" become more and more powerful and at the same time cheaper. As a reference, in 1971 the cost of a transistor was 1$, which today is the cost of 10 millions transistors! Nowadays integrated circuits are ubiquitous in our daily life: mobile phones, digital camera, computers, MP3 players, games consoles, cars, credit cards, medical devices...and the list could continue.

The down-scaling of integrated circuits has been the driving force in the development of increasingly more advanced microelectronic devices. Indeed, the power consumption and the production cost per transistor decrease significantly with the down-scaling while the speed of the circuit increases. In the 70s the transistor feature size was 10 μm; at the turn of the XXI century the microelectronics industry moved towards the limit envisaged by the Nobel laureate Richard Feynman, who proposed to shrink devices toward their physical limits, "where wires should be 10 or 100 atoms in diameter" in his landmark 1959 talk "there is plenty of room at the bottom" [3]. In recent years the microelectronics industry has reached the nanoscale and has scaled the transistor feature size down to 22 nm. With such small feature size in mass production, the micro-electronics industry has become nano-electronics.

In the last few years however the pace of miniaturization has considerably slowed down as the conventional fabrication methods - called "top-down" since small features are realized from bulk materials by a combination of lithography, etching, and deposition - are reaching the limit of their capability and facing technological and fundamental challenges. Transistors have not reached yet the minimum size at which they would theoretically cease to operate properly[1], however the tremendous cost increase of lithographic tools and in general of semiconductor production facilities is hindering the development of even smaller electronic components.

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[1] For example, breakdown could happen for a too short gate insulator thickness oxide, or the subtreshold current could be unacceptable for a too short channel length, or even drain-source punch-through could occur

1.2   The bottom up approach

An alternative methodology, called "bottom-up", is showing promising results in overcoming the limitations outlined above. Bottom-up is the common building technique in the biological world: it is the mechanism that underlies the assembly of DNA, proteins, lipids, etc. In this technique, structures with nanometric dimensions are built from their smallest possible components, atoms and molecules; in man-made processes this technique is already used in areas such as molecular synthesis, colloid chemistry, polymer science [4]. The bottom-up approach has the potential to control the dimension of structures with near atomic scale precision, going far beyond the limits of top-down technology based on lithography. This bears the promise of bringing new strategies and opportunities that could benefit the semiconductor industry and the research in nanotechnology in general [5].

In the last decades fundamental and applied sciences have shown increased interest in the growth and fabrication of nanostructures with "bottom-up" techniques. Examples of these nanostructures are nanowires (NWs) [6, 7] and other peculiar and complex structures such as nanomembranes [8–10], nanowalls [11], nanoplates [12], nanosheets [13, 14], nanotrees [15], tripods and tetrapods [16–18].

In addition to their promising role as building blocks for integrated circuits of the next generation, nanostructures give scientists the possibility of: (1) investigating new physical properties and phenomena, e.g. those associated with the preponderance of surfaces and interfaces, (2) studying the physics associated with small dimensions, (3) increasing the functionality of materials by reducing them to the nanoscale (the properties of nanoscale objects sometimes differ than those of the same materials at the bulk scale), (4) reaching architectures more complex than those achievable with the planar technology, thanks to the third dimension component [5, 19].

1.3   III-V compound semiconductor materials

Reduction in size is linked to better performance of microelectronic devices, but this is not the only venue pursued in recent years by the micro and nano electronic industries to improve integrated circuits: devices can be faster if are realized with materials with high carrier velocities. For this reasons modern electronics has also turned its attention to III-V compound semiconductors.

III-V compound semiconductors are obtained by combining group III elements (like Al, Ga, In) with group V elements (N, P, As, Sb) of the periodic table. Some examples are GaAs, AlAs, InAs, InP.

Many of the III-V materials have a direct band gap and high mobilities due to carriers effective masses smaller than those in silicon. They also have the ability to adsorb light in a wide range of the solar spectrum. These peculiar optical and electronic properties make them widely

used in optoelectronics and in radio frequency applications such as lasers, light-emitting diodes, fibre-optic systems, wireless local-area networks, satellite communications, radar, radioastronomy and defence systems. In photovoltaics the highest efficiency for a third generation solar cell has been achieved with a III-V multi-junction structure [20].

The monolithic integration of III-V compound semiconductor materials on silicon represents a way to combine these properties with the mechanical strength and the maturity of silicon on the same platform. Unfortunately this exciting and interesting challenge presents several issues such as lattice mismatch, difference in crystal structure and a large difference in thermal expansion coefficients.

To give few details on these issues let us consider the case of the growth of GaAs on silicon.

Antiphase boundaries

Silicon and GaAs have similar crystalline structures made by two interpenetrating face centered cubic (fcc) primitive lattices (diamond structure). Silicon is a non-polar semiconductor i.e. both sub lattices are occupied by the same atom; GaAs is a polar semiconductor i.e. the two fcc lattices are not the same: one is occupied by Ga atoms, the other one by As atoms. When GaAs is grown on silicon it can happen that the first monolayer is part gallium and part arsenic since silicon has the same probability to bond with As and Ga atoms. The coexistence of areas with Ga atoms and areas with As atoms on the initial layer leads to the formation of As-As bonds and Ga-Ga bonds at the interface between domains. These defects are called anti phase boundaries (APBs). They should be avoided since they can degrade significantly the performance of the device [21].

Thermal mismatch

GaAs and Si have 60% mismatch in thermal expansion coefficient at room temperature. This difference narrows only slightly at the elevated temperatures. The mismatch in thermal expansion causes thermal stress in the GaAs layer that can lead to the distortion of the GaAs lattice and at the subsequent degradation of the optical properties and to silicon bowing, bending and cracking [21].

Lattice mismatch

The lattice constant of GaAs is $a_{GaAs} = 5.65$Å while the one of Silicon is $a_{Si} = 5.43$Å. Lattices constants for other semiconductors with the correspondent band gap energy are reported in figure 1.1. This lattice mismatch causes strain in the GaAs lattice during the growth. The energy associated with the strain scales linearly with the thickness of the GaAs epilayer h [22]. The lattice mismatch needs to be accommodated and this can be done in two ways. If the GaAs epilayer is thinner than a critical value h_d the mismatch is accommodated by elastic defor-
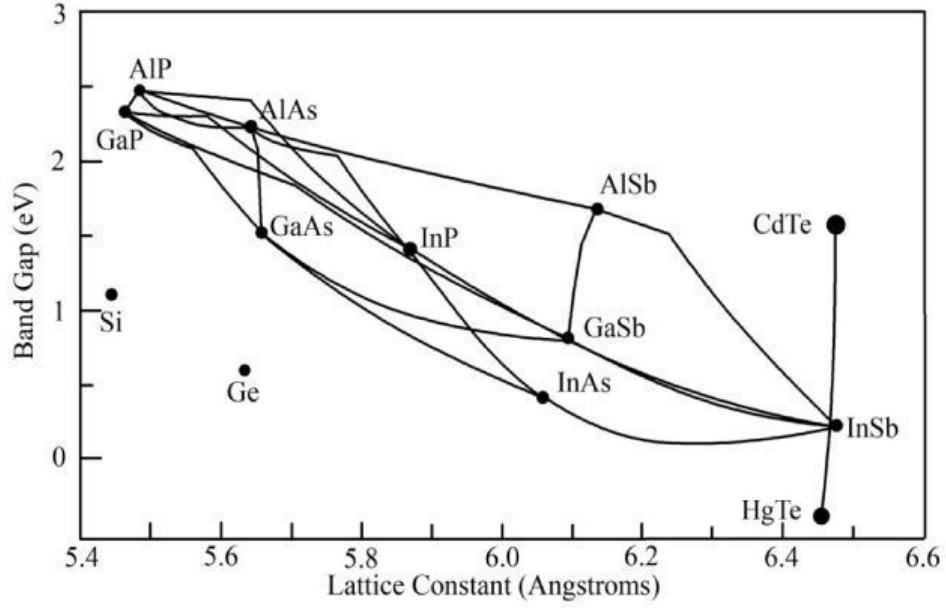
Figure 1.1: Band gaps for group IV and selected III-V binary semiconductors as a function of the cubic lattice parameter. In open access from [24].

mation of the lattice. When, with the proceeding of the growth, the GaAs epilayer overcomes the critical value h_d, the strain energies become larger and the mismatch is accommodated plastically through the formation of misfit dislocations at the interface. The critical thickness at which dislocations occur decreases rapidly with the lattice mismatch. Typical values are $h_d \sim$ 10 nm for lattice mismatches of 1% and $h_d \sim$ 1 nm for lattice mismatches of 4% [23].

1.4   The role of nanostructures in III-Vs integration on Silicon

The lattice and thermal mismatch can be overcome if III-V compound semiconductors are grown in form of nanostructures. Thanks to reduced contact area with the silicon substrate and the presence of sidewalls and facet edges, the strain due to the lattice mismatch is minimized and elastically relaxed at the interfaces. As a consequence of moderate strain the formation of dislocations can be minimized or even be eliminated. Moreover the small footprint and the single nucleation event per crystallite will guarantee a strongly reduced probability for APBs formation. As such, III-V compound semiconductor nanostructures hold the promise to be the fundamental building blocks for the future silicon-based microelectronics. For this to become a reality, the nanostructures have to be synthesized with a tunable and reproducible morphology, structure and chemical composition: size is crucial since at the nanoscale small variations can affect the performance of the device. Structure of the crystal directly affect the band structure and the electronic properties. Defects like twins and stacking faults impact the optoelectronic performances. Finally, control over the chemical composition means for example controlling the doping of the nanostructure and then making them functional from

an electronic point of view.

In the last years the growth of III-V semiconductor nanostructures on silicon substrates, especially in the form of nanowires, has been intensively studied [25–31] and several examples of bottom-up assembled optoelectronic [32–34], energy harvesting [35–37], field effect transistor nanodevices [38, 39] and sensors [40] have been already realized.

Much progress has been made in these years but despite the efforts spent in combining III-V materials with group IV substrates, several issues are still unsolved such as the appearance of parasitic non vertical wires or the lack of reproducibility in the growth of ordered arrays of nanostructures. Since most of the properties and characteristics of the nanostructures are determined at the early stages of growth, a completely successful integration will be achieved only with a fundamental understanding of the elementary processes occurring at these moments. Thus the growth process must be well controlled and predictable and the growth mechanism of the nanostructures has to be understood in depth: this constitutes the main topic of this thesis work.

2 III-V Nanostructures on Silicon

This thesis work is concerned with two particular types of III-V compound semiconductor nanostructures epitaxially grown on silicon substrates: Nanowires (NWs) and V-shaped nanomembranes. NWs are among the most widely investigated research topics in the nanosciences nowadays, while V-shaped nanomembranes are a new form of nanostructure recently discovered by our group.

NWs are single-crystalline, filamentary and highly anisotropic nanostructures with diameters between 20 and 200 nm that result from rapid growth along one direction (figure 2.1a). The research on NWs (previously dubbed whiskers) started more than 60 years ago when Conyers, Herring and John K. Galt at Bell Laboratories demonstrated for the first time that tin whiskers have an elastic and plastic behavior similar to a perfect crystal [41]. A series of subsequent studies in the field led to a new concept of crystal growth from vapor, called the Vapor Liquid Solid (VLS) mechanism, first described by Wagner and Ellis in 1964 [42] and to the synthesis of different materials in the form of whiskers like GaAs, GaP, Si and Ge [43–45].

30 years later Hiruma *et al.* renewed the interest in these structures [46, 47] and pioneering works at the beginning of the 2000s by the Lieber group at Harvard University [48], the Yang group at University of California Berkeley [49], and by the Samuelson group at Lund University [50] finally demonstrated the feasibility of growing whiskers at the nanoscale, or NWs, with the VLS mechanism. At a later stage the interest in NWs definitively expanded at an exponential rate as can be seen in figure 2.2, and other groups started conducting research in the field [6, 30, 31, 51–57], including ours [58, 59].

To date a large variety of bulk materials ranging from metals to semiconductors has already been synthesized in the form of NWs through several different growth mechanisms and fabrication techniques. Apart from the VLS growth mechanism, other important examples are the *Vapor Solid Solid* (VSS) and the *Selective Area Epitaxy* (SAE) growth mechanisms. Examples of techniques are *Molecular Beam Epitaxy* (MBE), *Metal Organic Vapor-Phase Epitaxy* (MOVPE), *Chemical Beam Epitaxy* (CBE), *Chemical Vapor Deposition* (CVD) and *Laser Ablation* (LA).

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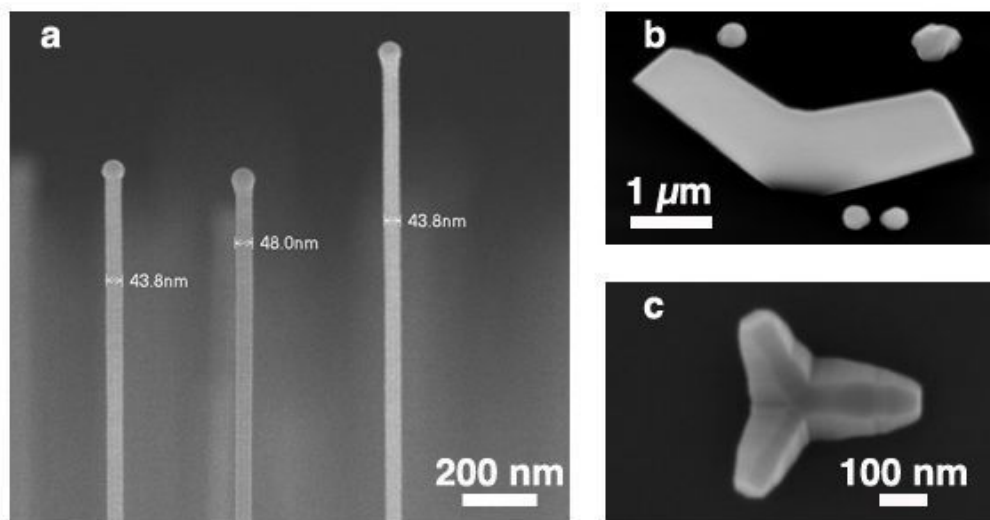
Figure 2.1: Examples of III-V nanostuctures grown on silicon substrates by molecular beam epitaxy: a) nanowires; b) V-shaped nanomembrane; c) tripod
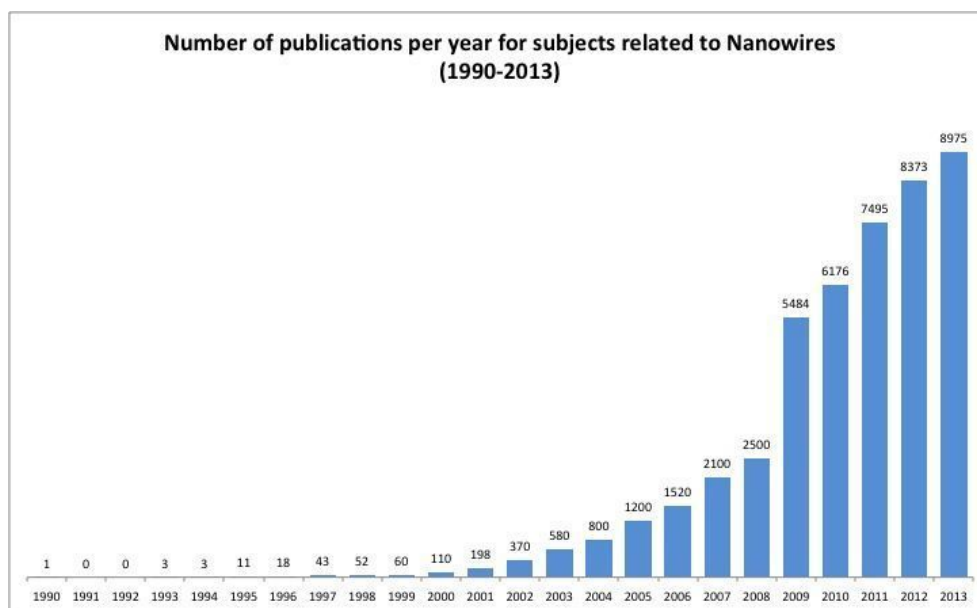
Figure 2.2: The number of publications on topics related to NWs has greatly increased from 1990 to date. Data from ISI WEB of Knowledge.

In addition to NWs, many peculiar shapes have recently been created in trying to reduce the scale of semiconductor structures: examples are nanomembranes (figure 2.1b) or nanowalls, nanosheets, nanoflowers and also branched structures, like tripods (figure 2.1c) and tetrapods. The growth and development of these nanostructures with high morphological complex-

ity adds significant versatility in realizing architectures that would be impossible with the traditional thin film technology. Thanks to their third dimension, these nanostructures are potential building blocks for advanced electronics such as interconnected devices [15].

The growth of nanostructures on silicon substrates must fulfill four key criteria in order to be deemed viable for applications: first, the growth should be gold-free. Gold is commonly used as seed for growths but it is known to easily diffuse and to create unwanted deep levels, especially in silicon and as such it must be avoided in research which targets integration on the Si platform. For this reason, I have used the Vapor Liquid Solid mechanism with a self-catalyzed approach for the growth of GaAs NWs and the Selective Area Epitaxy for the synthesis of InAs NWs, as these two growth mechanisms do not make use of gold. The VLS mechanism with its general principles will be described in section 2.2. Then the self-catalyzed and SAE growths will be discussed respectively in 2.3.1 and in 2.3.2. I will briefly review the Au-assisted growth of III-V NWs, then I will focalize on the state-of-the-art of self-catalyzed GaAs NWs and of SAE grown InAs, which are the material systems object of this thesis.

As a second criterion, the growth has to be obtained in an ordered manner on previously designed arrays, which allows for precise positioning of masks and contacts, thus greatly facilitating the processing of the device. Moreover, the orientation of the nanostructures on the substrate must be tunable, e.g. to attain growth of vertical structures.

Lastly, the use of exactly oriented (001) substrates is required for true industry compatibility. This would make the integration compatible with the current technological processes, while at the same time it would result in the reduction of structural defects.

For both NWs and V-shaped nanomembranes, our growth technique of choice has been Molecular Beam Epitaxy. Since MBE is an extremely clean fabrication technique, as we will describe in the following section, it allows to produce ultrapure structures with very high crystalline quality and atomically sharp interfaces.

2.1 Molecular Beam Epitaxy

Molecular beam epitaxy is a technique for epitaxial growth, favored among other techniques for obtaining very high purity samples thanks to its ultra-high vacuum (UHV) conditions, to the absence of chemical precursors and to the extreme purity of the source materials. It is also a tool for growing high quality structures with sharp and abrupt interfaces thanks to the low and well controlled growth rates.

All my growth results have been obtained with a DCA P600 MBE machine (figure 2.3), whose installation at EPFL started in 2009. A relevant part of my activities during the first two years of my Ph.D. thesis have been related to its completion and to maintenance and testing of the machine.

Our system is an ensemble of chambers connected to each other. It consists of a load lock
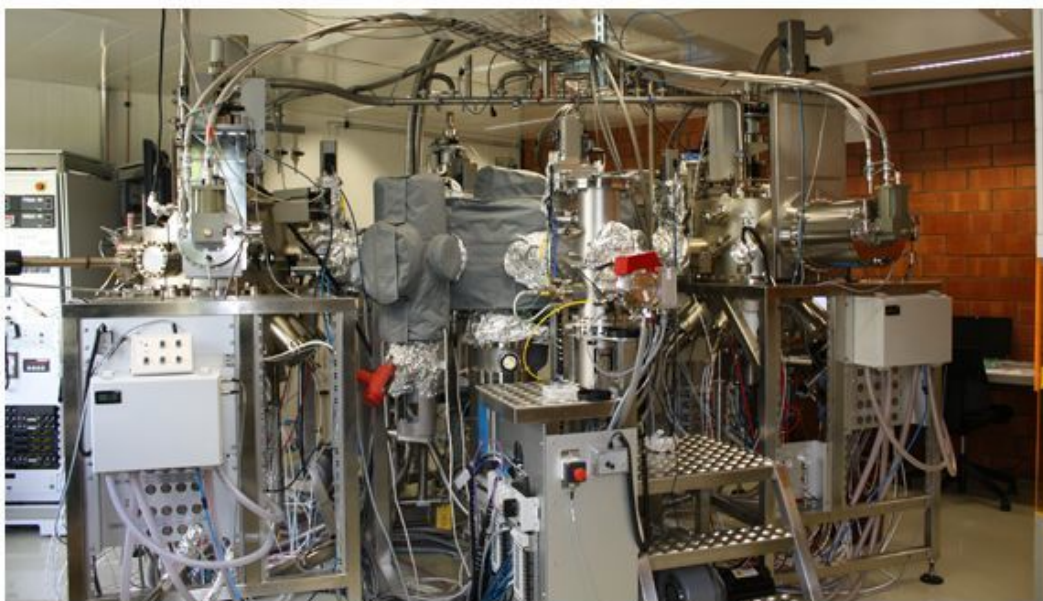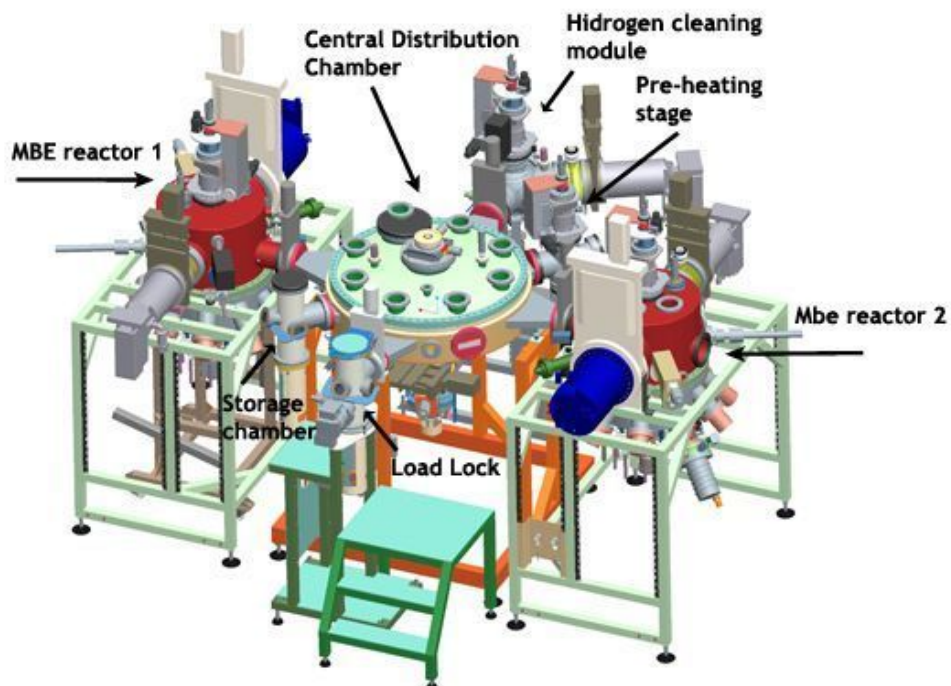
Figure 2.3: Side views of the Molecular Beam Epitaxy machine installed at EPFL. It is a P600 Dual chamber from DCA Instruments. Reprinted with permission from DCA Instruments Oy (http://www.dca.fi).Top: technical drawing showing the different components of the system. Bottom: picture of the machine after the installation at EPFL. The stairs bring the operator to the load lock module; the storage and central distribution chambers are under baking; two reactors are present, respectively on the right and on the left of the system.

chamber module, a central distribution chamber with a robot handler, a storage chamber, a pre-heating treatment module, a Hydrogen cleaning stage and two deposition chambers. Each chamber has its own pumping system and can be isolated from the others by UHV bakeable gate valves. UHV indeed is essential to reduce the impurity to a minimum level and it is guaranteed by CTI Cryogenics On-Board cryopumps.

The samples are introduced in a load lock chamber where they are out-gassed using a quartz lamp heater system. Then they are transferred into the central distribution chamber through a robot arm that allows the movement of the samples from chamber to chamber. Two stepper motors control the rotational and translational moves of the samples. The motion sequences are initiated via a digital I/O interface.

A storage module is connected directly to the central distribution chamber for additional substrate housing. A high temperature heating stage is available for prior to growth substrate treatment. Here silicon wafers are degassed at 600°C for 2 hours. Our system is also equipped with a Hydrogen cleaning chamber for passivation treatment of the substrate surface. This module features substrate manipulator, quadrupole mass analyzer, a pyrometer for substrate temperature measurement, a Reflection High Energy Electron Diffraction (RHEED) system and an atomic Hydrogen source, not functional during the period of my thesis.

The two deposition chambers are designed for high mobility III-V molecular beam epitaxy. A front view picture of the reactor I used during my Ph.D. thesis and its schematic drawing are reported in figure 2.4.

This deposition chamber has two separate liquid N_2 cooled cryopanels. One separates the materials sources both thermally and chemically from each other; the other one surrounds the upper part of the growth chamber. They help in minimize the re-evaporation of material from the walls and provide additional pumping.

A substrate manipulator is provided to smoothly rotate the wafers for a better growth uniformity across the samples. The manipulator heater can bring the substrate up to 1000°C to remove any possible contaminants. Usually our samples are grown under a rotation of 7 rpm and after a degassing at 770°C for 30 minutes.

An Ircon pyrometer is included for substrate temperature control and measurements . The device is calibrated by observing the phase transition of the surface reconstruction of Si(111) from (7x7) to (1x1) that occurs at 830°C [60].

The reactor has ten ports for effusion cells and valved cracker cells. The setup configuration during my Ph.D. thesis comprises effusion cells for Ga, In and Al, motorized As and Sb valve crackers, silicon and carbon sublimation sources for doping. All source ports are symmetrically mounted on a radial array with respect to the chamber axis. The beams then converge towards the substrate which is held face-down during all manipulations and process steps. The reactor features individual beam shutters positioned with the purpose of interrupting the beams
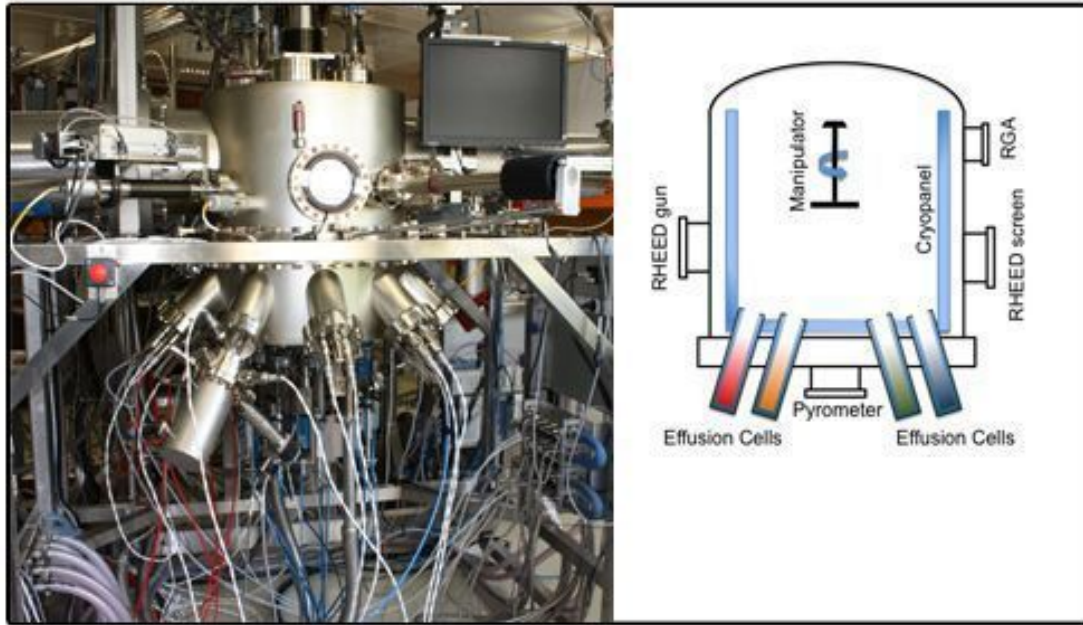
Figure 2.4: Left: front view of the MBE reactor I have used to grow the samples analyzed in this work. Right: Schematic drawing of the chamber.

between the sources and the substrate and a main shutter to interrupt all beams at once.

Day-by-day calibrations of the molecular beams are done with a beam flux monitor and growth monitoring through a RHEED system. Details on this technique can be found in references [61] and [62].

Each deposition chamber also contains a residual gas analyzer for contamination monitoring and a bevel for cleave edge overgrowth.

After having described our equipment and technique, we turn our attention on the growth methods of interest.

2.2   The Vapor Liquid Solid growth mechanism

The metal-catalyst-assisted Vapor Liquid Solid (VLS) growth mechanism was suggested for the first time by Wagner and Ellis in 1964 [42]. The name is due to the fact that three phases are involved: vapor, liquid and solid. To date it is the most widely used approach to synthesize one dimensional structures like whiskers or nanowires (NWs).

In this new concept of crystal growth, metal particles (droplets) are dispersed on the substrate and are used as catalysts, i.e. as preferential sites for the decomposition of the precursors. The mechanism proposed by Wagner and Ellis assumes that the catalyst droplet forms a liquid
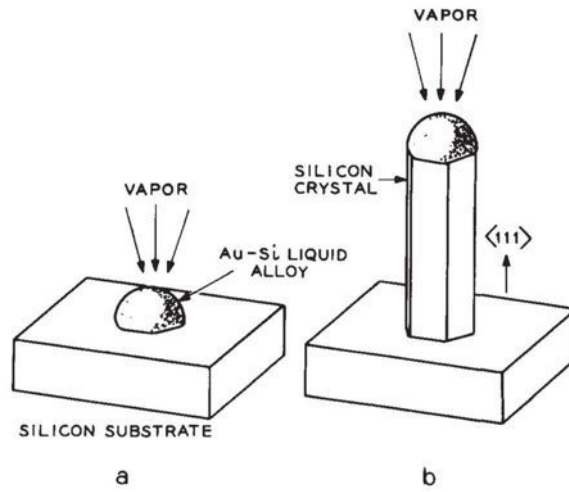
Figure 2.5: The Wagner-Ellis illustration showing the growth of a silicon whisker by VLS: a) liquid droplet on the substrate at the initial stages of growth; b) growth of the crystal under the droplet. Reprinted with permission from [42]. Copyright Applied Physics Letters 1964, AIP Publishing LLC.

alloy (figure 2.5 a). The role of the catalyst is to gather molecules of the precursor material coming from a gas phase and to decompose them at a much higher rate than the rest of the surface. By continuing this process the droplet becomes supersaturated, i.e. the concentration of the components in the alloy is higher than the equilibrium concentration. This leads to the precipitation of crystalline material in the form of whiskers underneath the droplets (figure 2.5 b) and to a reduction of the free energy of the alloy system.

Wagner and Ellis used this method to demonstrate the growth of Si whisker on a Si(111) substrate at a temperature of around 1000°C. They used gold as metal catalyst and vapor sources like $SiCl_4$ and H_2.

The Au-Si phase diagram in figure 2.6 can help us to understand the role of the metal droplet while growth occurs. It is worth to note that this phase diagram is constructed from a bulk system. Since the thermodynamic properties of a nanosystem are different from those of a bulk, the phase diagram related to our system would be slightly different and would show a deviation of the Si-rich liquids line at lower temperatures [63, 64]. Even if the corrected phase diagram would provide a deeper knowledge of the drop composition as key step for controlling the VLS growth, however the bulk Au-Si phase diagram contains the main physics governing the general mechanism.

The bulk Au-Si phase diagram shows an eutectic point at an Au:Si ratio of 4:1 at about 363°C. This temperature is remarkably lower than the melting temperature of pure Au (1064°C) and pure Si (1414°C). At a temperature above 363°C Au particles can form Au-Si eutectic droplets on the silicon surface (gold does not wet silicon surfaces). For regions in the phase diagram
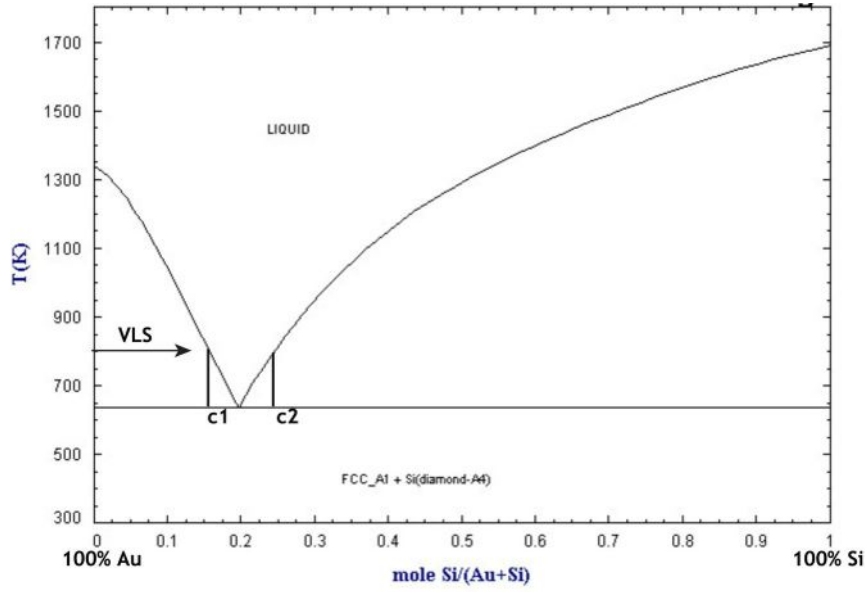
Figure 2.6: Si-Au phase diagram (adapted from [65]).

between the liquidus and the eutectic temperature, there is a coexistence of a liquid phase with the liquidus composition and a solid phase precipitate. The nature of precipitates depends on whether the mixture is rich in gold or in silicon. When Si is supplied to the system in vapor phase, the preferential decomposition of precursors followed by their incorporation into the droplets leads to an increase in Si concentration beyond the equilibrium composition (super-saturation), as described by the arrow in the phase diagram. For silicon concentration *c1* and *c2* the alloy Au-Si is liquid. In order to re-establish the equilibrium, a Si-rich solid precipitates underneath the droplets forming a monolayer. The precipitation occurs at concentration below *c2* [1]. The concentration of Si in this monolayer is given by the nearest phase boundary on the Si-rich side, i.e. 100% Si .

After the nucleation of the first monolayer the supersaturation drops. Then the droplet can be refilled again by supplying Si from the vapor phase. By continuing this process the growth of the whiskers (or nanowires) proceeds and the liquid droplets rise from the substrate surface. Since the time for the formation of a monolayer is shorter than the refilling time, the supersaturation exhibits a sawtooth behavior [66, 67].

The whiskers grow only in the area seeded by the metal catalysts along the <111> direction; their diameter is mainly determined by the size of the catalysts while their length is proportional to the growth time.

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[1] For concentration equal or higher than *c2* silicon will precipitate within the droplet and not necessarily only on the substrate.

Au-assisted III-V semiconductor NWs

To the best of our knowledge, the first growth of Au-assisted III-V semiconductor whiskers has been reported by Hiruma *et al.* [47]. Here GaAs and InAs whiskers have been grown by MOVPE on GaAs substrates with different crystal orientations. The wires show a preferred growth direction, the <111>B, as this minimizes the total free energy. They then grow vertically on GaAs(111)B and form an angle of 35° with the substrate on GaAs(100).

Several years later, in 2004, the growth of III-V semiconductor NWs has been demonstrated on silicon substrates by Mårtenson *et al.* [7]. In their work GaP NWs, chosen for their small lattice mismatch with silicon (0.4%), have been synthesized on Si(111) and Si(001) by MOVPE with size selected aerosol gold nanoparticles as catalysts. Again the preferred NWs growth direction is found to be the <111>B. On Si(001) substrates, NWs grow in the different <111> directions at 35° with the substrate, two more respect what has been previously observed on GaAs(100). Indeed, as mentioned in section 1.3, compound semiconductors are polar while elemental semiconductors, like silicon, are not. The four out-of-plane <111> directions respect to Si(001) are then equivalent so NWs grow in any of them. We will discuss the NW growth directions more in-depth in section 2.3.1. Preliminary results with other larger mismatched material systems (like GaAs) already envisaged the possibility to combine otherwise incompatible materials through strain relaxation. Soon afterwards GaP, GaAs, InP and InAs NWs have indeed been grown on silicon (lattice mismatch ranging between 0.4% and 11.6%) by Roest *et al.* [68].

In the same year the first growth of GaAs NWs on silicon substrates by Molecular Beam Epitaxy has been presented [69]. It is worth to note that in the MBE the gold nanoparticles do not act as catalysts since the materials are delivered as atomic beams. They rather act as a material collector that directs the adatom fluxes towards the tip of the NW. In this work two peculiar traits of NWs have been identified: 1) NWs have a very uniform diameter along the entire wire length. 2) NWs show a quite high density of stacking faults in the <111>B growth direction. This latter point leads to the coexistence of two crystalline phases, hexagonal wurtzite (WZ) and the cubic zinc-blende (ZB), in the NW structure[2]. Since such a mixed, or in general imperfect, crystal structure affects the electronic and optical properties of the NWs, many studies (not all on silicon substrates and precisely reviewed in [70]) have been devoted to understand the reasons behind the occurrence of wurtzite and zinc-blende, and the growth conditions or parameters leading to the appearance of one phase or the other [57, 71–74].

Other studies have examined ways to improve the crystalline quality of NWs, for example reducing the occurrence of twin defects by decreasing the growth temperature [75, 76]. Other

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[2]While III-V semiconductors crystallize in bulk form as cubic zinc-blende, surprisingly III-V NWs often adopt the hexagonal wurtzite structure. These crystal structures differ by the stacking sequence of their atomic planes. Zinc-blende structure has a $ABCABCABC$ stacking sequence along the <111> direction, while wurtzite structure has $ABABAB$ stacking sequence. Each letter represents a bilayer with a different transverse position. Misplacements of a single bilayer create segments of a phase into the other. In wurtzite phase ($ABABAB$), a misplacement of a single bilayer (stacking fault) leads to the sequence $ABABCBCB$ and then to a segment of zinc-blende. In the zinc-blende structure ($ABCABC$), two misplacements create two twin planes. The stacking sequence becomes $ABCACBA$ and then $ABCACA$, with wurtzite segments.

works have been dedicated to the study of the nucleation of NWs with the aim of acquiring further control on the growth. For example some works have been devoted to understand the role of the substrate [56, 77], while other works have focused on understanding the broadening of the NWs length distribution despite a narrow catalyst size distribution [78]. In order to gain a deep understanding and control capabilities on the growth other crucial studies are those related to the thermodynamic of the growth [79], the strain relaxation [25, 28], and those which have formulated models for the growth mechanism [67, 80].

Although GaAs is by far the most widely investigated among the different III-V compounds, studies have been reported analyzing the growth of other III-V compound NWs, such as InAs, on silicon substrate by MBE [81].

2.3   Gold-free growth

Gold has been the catalyst most commonly used since the experiments done by Wagner and Ellis. As we detailed in section 2.2, III-V semiconductor NWs have been successfully grown by the VLS mechanism using gold as catalyst. Au nanoparticles can be produced easily (for example by evaporation and annealing of a thin film) and work well as seed particle for many material systems i.e in forming liquid alloys with the growth species. Gold is also chemically inert meaning that it does not oxidize, which may hinder the catalytic properties [82].

Even if gold has important advantages for controlling the growth, it is known to introduce unwanted deep levels in silicon, which makes it not compatible with the current CMOS technology [83]. As a consequence there has been an intensive search of alternative processes and different approaches have been demonstrated where other metals have been used to replace gold as the catalyst of the growth. Examples are Al for GaN NWs [84], Ni for GaAs NWs [85] or Pd for InAs NWs [86], but many other materials have been reported [87].

Relatively recently, the possibility of a self-catalyzed process has also been reported [27, 31, 58, 59, 88]. In this method, similar to a VLS process, foreign catalysts (i.e. materials different from the constituents of the semiconductors to be grown) are not needed and as a consequence, any contamination is avoided. Conversely, gallium droplets are used to grow GaAs NWs, indium droplets to grow InAs and so on. Indeed this method is known more precisely as group-III-assisted growth of III-V NWs. I used this growth principle to grow the GaAs NWs reported in Paper I, II, III and IV listed in chapter 3.

Another technique to circumvent the use of gold is Selective Area Epitaxy (SAE) in which nanostructures are not catalyst assisted, a technique that I used to grow the InAs reported in Paper III.

In the following sections I will give more details on these two main growth procedures I have used in my work.

2.3.1 The Ga-assisted growth of GaAs NWs
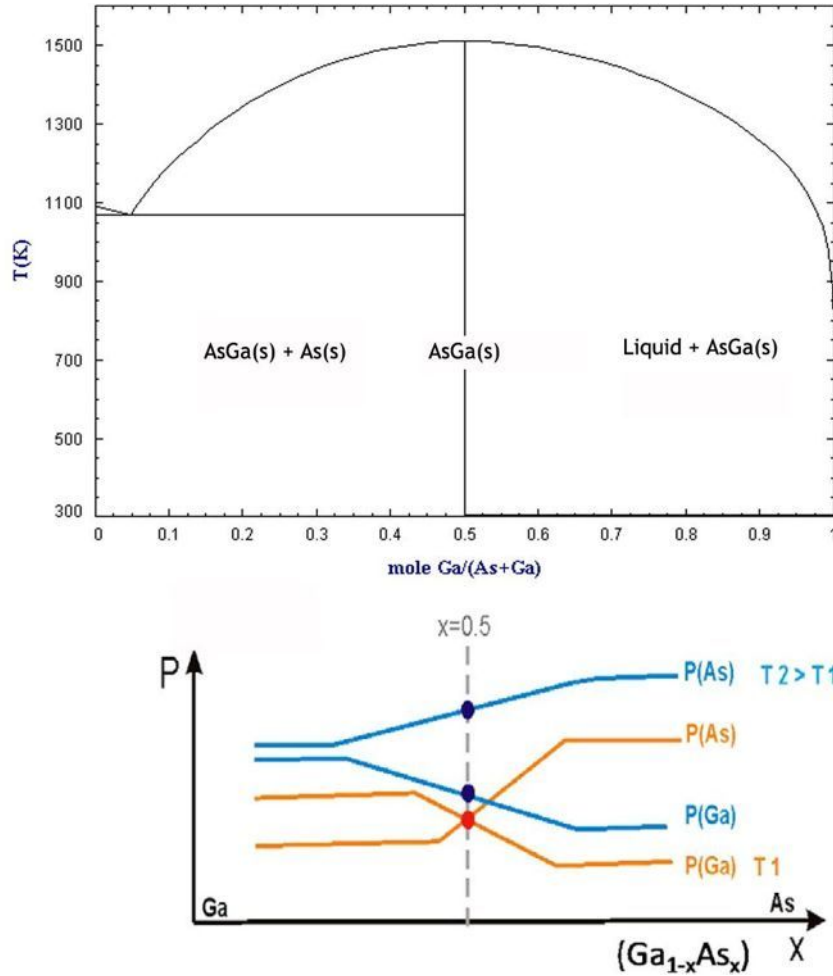
Figure 2.7: Top. As-Ga phase diagram (adapted from [89]). Bottom. Partial pressures of Ga and As at the GaAs surface as a function of temperature. For temperatures higher than 630°C Ga-rich liquid (droplets) accumulates at the GaAs surface. T_1 and T_2 denote temperatures respectively lower and higher than the congruent temperature. Reprinted with permission from [90]. Copyright 2009, Springer-Verlag Berlin Heidelberg.

Ga-assisted growth is a self-catalyzed process in which gallium droplets are used to seed the growth of GaAs NWs. In 2008 Fontcuberta *et al.* demonstrated the Ga-assisted synthesis of GaAs NWs by MBE on GaAs substrates [59]. Shortly later the growth has been reported for Si(111) [91] and Si(100) [31, 92] too.

To start a Ga-assisted growth it is needed to form gallium droplets on the substrate. In order to do this there are two conditions to fulfill. First of all we need to use gallium rich conditions to promote accumulation of gallium on the substrate. Figure 2.7 shows the partial pressures of Ga and As at the GaAs surface as a function of temperature. For temperatures T_1 below a critical value, the vapor pressures of Ga and As equilibrate the stoichiometry of GaAs to 50% of each

17

element. At temperatures T_2 higher than the critical value, the higher vapor pressure of As leads to the selective evaporation of As at the surface, that results in turns in the formation of Ga droplets. This critical value is called congruent temperature and it is around 630°C [93, 94]. This also means that a Ga pre-deposition is not really necessary to promote the formation of droplets and that Ga and As can be supplied simultaneously.

As second important condition we need to avoid the spreading and increase of the gallium droplets, i.e. gallium should not wet the substrate surface [59, 95]. A non wetting substrate is obtained by covering silicon or GaAs wafers with an oxide. Indeed, oxide turned out to be a key parameter for obtaining successful growths, which outcomes are strictly dependent on the nature of the oxide [96].

The growth of GaAs NWs on silicon wafers is schematically depicted in figure 2.8 and proceeds as follows. When Ga and As sources are opened, adatoms and molecules reach the silicon substrate (2.8 a) where they can be adsorbed. For what explained above, if the silicon wafer is heated around the congruent temperature and if the native oxide is not removed, As molecules will easily desorb (2.8 b) while Ga adatoms will diffuse and form droplets (2.8 c). As for Au-assisted growth, after the Ga droplets reach the supersaturation the GaAs NW growth starts at the droplet/silicon interface.

In order to understand the growth mechanism of these nanostructures several works have focused on investigating the fundamental parameters governing the Ga-assisted growth of GaAs NWs [58, 91, 97–101]. The growth rate has been found to be proportional to the arsenic beam equivalent pressure (BEP), in contrast to what happens in the case of MBE thin film growth, and to be several time larger than the deposition thickness [58, 91, 98–100]. This means that the arsenic diffusing through the gallium droplet and precipitating underneath is driving the growth and that the direct impingement of As and Ga (2.8 d-e) is not sufficient to explain the NW elongation rate. A diffusion-induced contribution has to be considered as the dominant mechanism: the Ga adatoms arrive at the liquid droplet also from a diffusive process on the substrate and along the NW sidewalls (2.8 f) [58].

The As_4 molecules are not involved in a surface diffusion process but in a re-emission mechanism. The As_4 species do not reach the catalyst by diffusion since they are volatile and desorb at the growth temperature. A second source of As_4 is instead a re-evaporation of As_2 and As_4 species from the substrate and NW sidewalls that can then reach the droplets (2.8 g) [27].

In the NWs growth, gallium is a liquid reservoir for the GaAs deposition and determines the NW diameter. For high Ga rate (low V/III BEP ratio) the NW diameter tends to increase over time because Ga accumulates in the droplets and enlarges them. By increasing the V/III ratio it is possible to reach a dynamical steady state that leads to a constant droplet and in turn to a constant diameter along the wire. If the ratio becomes too high, the Ga droplets shrink over time leading to a tapered geometry [58, 91, 101]. The complete consumption of the Ga droplets will stop the VLS mechanism.
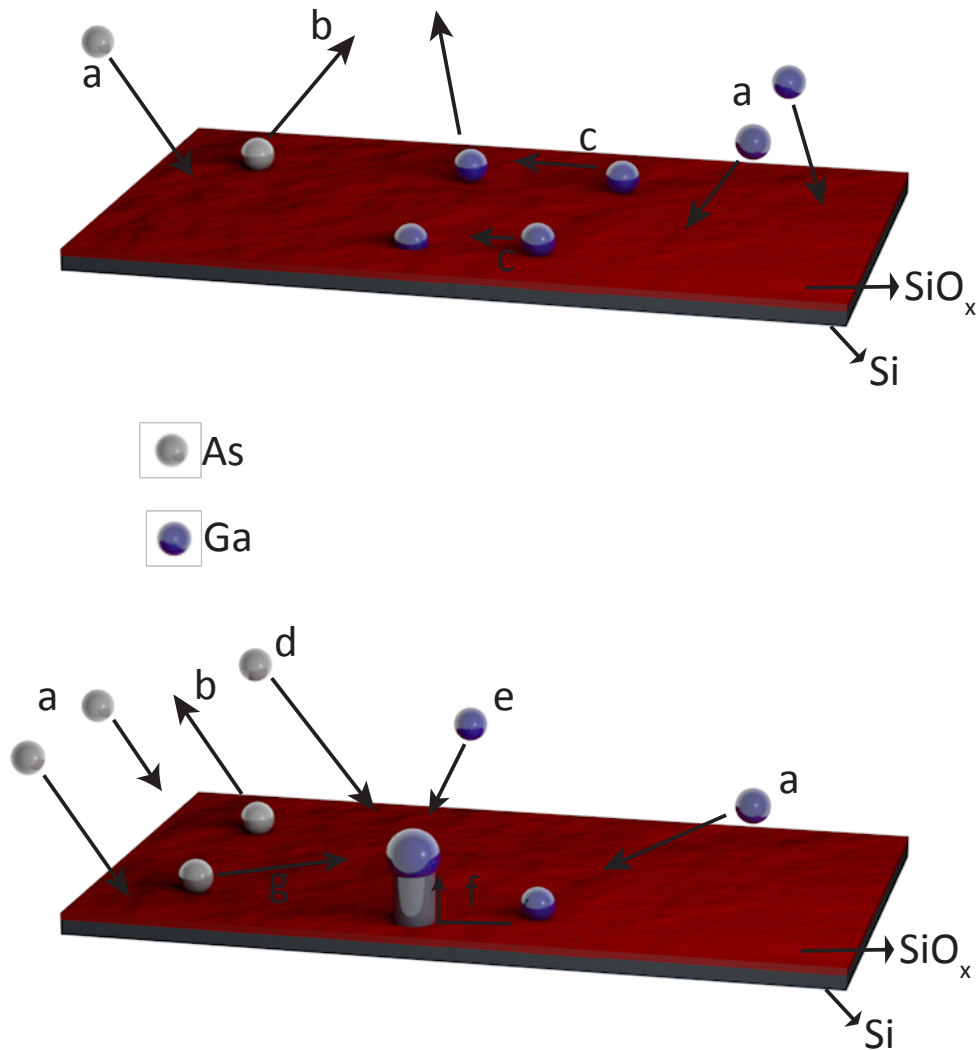
Figure 2.8: Kinetics processes during the Ga-assisted GaAs NWs growth. a) As and Ga impinge-ment on the substrate. b) As desorption from the substrate. c) Ga diffusion on the substrate. d) Direct impingement of As onto the droplet surface. e) Direct impingement of Ga onto the droplet surface. f) Ga diffusion from the substrate along the sidewalls to the drop. g) Second source of As after re-evaporation.

Unlike Au-assisted GaAs NWs, Ga-assisted GaAs NWs show a prevalent zinc-blende crystal structure. Due to the small difference in the energy of two phases, Ga-assisted GaAs NWs show often the occurrence of both cubic and hexagonal phases. Several works have been devoted to understand under which conditions the NWs adopt a ZB or a WZ crystalline structure and how it is possible to favor one or the other [31, 97, 98, 101–104]. In many cases it was found that the key factor is the V/III ratio. Indeed the droplet size affects the difference in formation free energies between the WZ and ZB structures [98, 101–104].

The ability to selectively control the crystal structure is only one of the requirements necessary to make GaAs NWs interesting for future applications. To be functional from an electronic point of view the NWs need to be doped. The doping, i.e. the controlled incorporation of impurities with different atomic number in the crystal structure, can modulate the electrical conductivity of a semiconductor and it is as such an essential element in the realization of any kind of electronic device. The doping of Ga-assisted GaAs NWs is a challenging task: the small size of the NWs makes it difficult to determine doping levels, carrier concentrations and mobilities. Moreover the growth mechanism itself, the VLS, which means out of equilibrium growth conditions and the presence of a catalyst, is at the origin of a complicated doping incorporation mechanism, based on three competing incorporation paths: incorporation from the side facets, from the gallium droplet and by diffusion from the shell to the core [105]. We refer to references [106–109] for in-depth analysis that are beyond the scope of this thesis.

Many applications, especially in the energy harvesting area, require heterostructures, i.e. a change in doping and/or composition within the same NW structure. Heterostructures can be axial or radial: in the axial heterostructures the heterointerface is perpendicular to the wire axis; in the radial or coaxial heterostructures the heterointerface is parallel to the wire axis [110–113]

A final, crucial requirement in the growth of NWs is that to meet industrial requirements they have to be grown with ordered and controlled position on full wafers and, in most cases, vertically respect to the substrates.

Growth directions of GaAs NWs on silicon substrates

The NWs grow in the growth direction that minimizes the total free energy. The largest contribution to the total free energy is given by the surface free energy of the interface between the NW and the metal catalyst. For diamond and zinc-blende crystals the surface free energy is generally smaller along the <111> orientation than, for example, that of <100>, and thus NWs tend to grow in the <111> direction.

To fully characterize the growth of III-V semiconductor NWs on silicon there is another element to be considered: the polarity (see for definition section 1.3). While some surfaces in the zinc-blende crystal are polar, such as the {111} planes, others, such as {110} and {100} planes that contain equal amounts of the III and V elements, are not. As a consequence, the <111> direction can be distinguished into <111>A and <111>B depending on the surface termination (the <111>A is group III terminated while <111>B is group V terminated, see figure 2.9 top). The <111>B has the lower surface energy [114] and, as a consequence, III-V compound semiconductor NWs show the <111>B as preferred growth direction.

The choice of (111)B substrates leads naturally to the growth of NWs which are vertically aligned respect to the substrate as the surface normal is the only available <111>B direction. When (111) elemental substrates, like silicon, are considered, the scenario becomes more
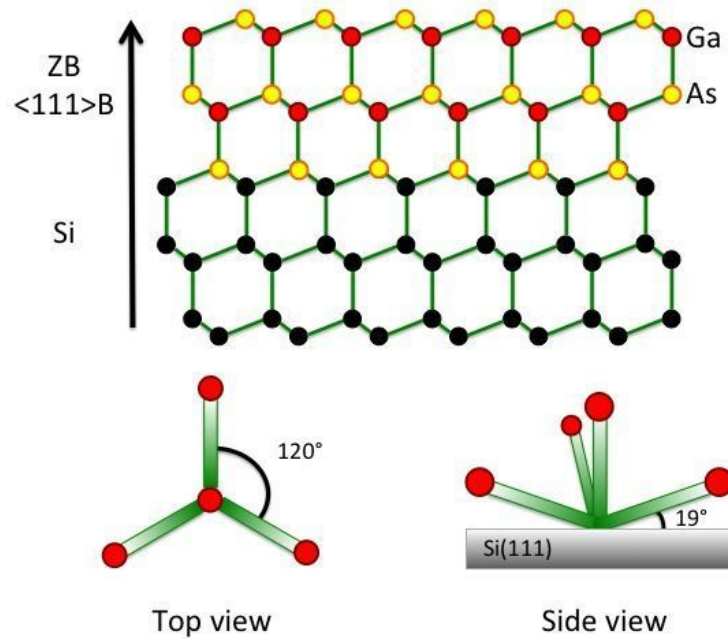
Figure 2.9: Top. Schematic drawing of the atomic arrangement in a zinc-blende crystal growing in <111>B direction on Si(111) substrate ([110] zone axis). The top surface has B polarity. Bottom. Schematic illustration of the expected NW growth direction on Si(111) substrates. The out-of-plane <111> growth directions are four: one surface normal and other three at 19.5° respect to the substrate, azimuthally separated by 120° from each other.

complicated. The four available out-of-plane <111> directions (the surface normal and other three angled 19.5° respect to the substrate) are equivalent and this allows NWs to grow tilted instead of vertically (figure 2.9 bottom).

The control on the NWs growth direction is of paramount importance for their reproducible integration on silicon substrate and for the realization of NW-based structures effective for applications. Indeed any non vertical NW is doomed to negatively affects the performance of the device as it would produce a leakage path. Despite the progress made on this topic non vertical NWs always appear and a suitable mechanism able to explain the occurrence of tilted wires is still under investigation.

Ordered arrays of GaAs Nanowires on Silicon substrates

An important issue in the growth of NWs for their application in integrated devices is the control and reproducibility in their position. Indeed if NWs want to be used in electronic devices it is necessary to create electrical contacts with these structures in a manufacturable way (on large scale and reproducible way) and this requires precise positioning control of the
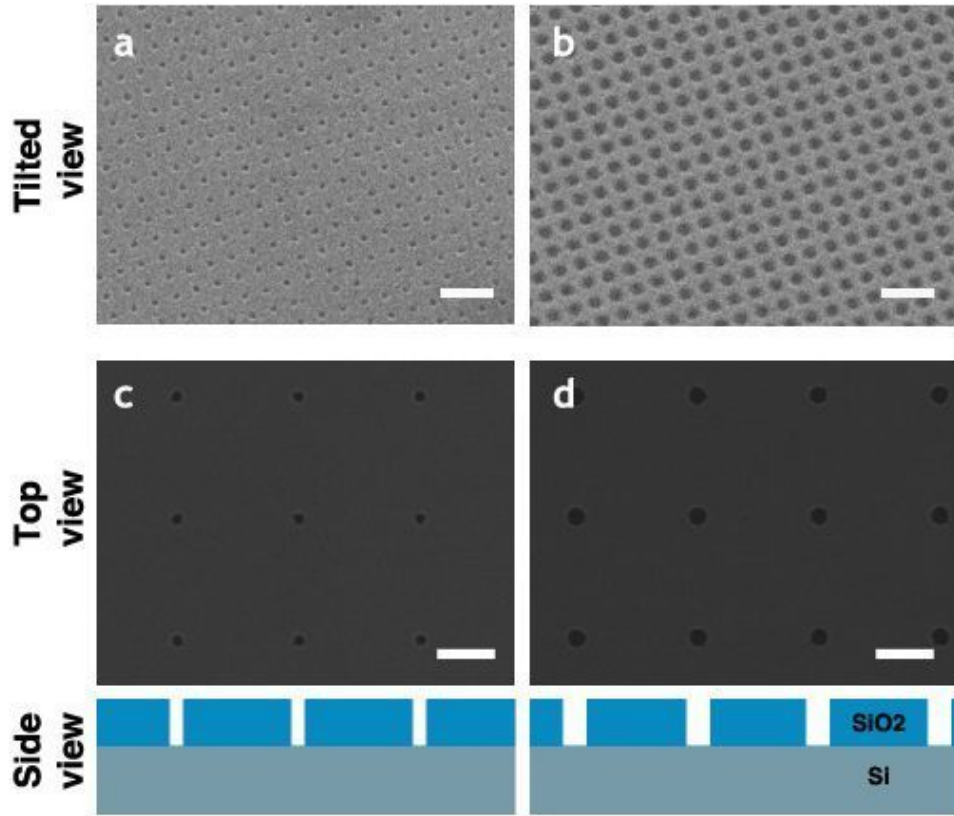
Figure 2.10: Examples of nanoscale arrays of holes defined by beam lithography in a SiO_2 layer. Top. 20° tilted views of 30 nm (a) and 90 nm (b) holes at a inter hole distance (pitch) of 200 nm. Middle. Top view of 50 nm (c) and 100 nm holes at a larger pitch (1μm). The scale bar is 500 nm. Bottom. Schematic of the side view of a typical array. Holes are defined in a SiO_2 layer grown on a silicon substrate.

structures to be contacted. Alternatively, precise positioning of masks is needed to facilitate the device processing.

The most common way of organizing growth of NWs on a substrate is to pattern it with metal nano-droplets (gold is the most frequently used material but other metals have been also tested) or with nanoscale openings on a silicon dioxide mask, which is more appropriate in case of catalyst-free growth of NWs. Several patterning methods have been already used for achieving nanoscale features on the substrate such as e-beam, nano sphere, phase shift or nano-imprint lithography. E-beam lithography is the more frequently used technique for nano patterning; examples of nanoscale holes defined in a SiO_2 layer with this method are illustrated in figure 2.10. Nano-imprint lithography started to recently attract attention thanks to the relative low costs and the capability of patterning substrates on large scale [115].

The growth of Ga-assisted GaAs NWs in arrays on silicon substrates is a challenging task. The first two works on this topic have been recently published by Plissard *et al.* [101, 116].

Morphology and growth yield of vertical NWs have been studied as a function of the growth parameters and array geometry. Here and in the rest of the thesis, the yield is defined as number of openings nucleating vertical NWs divided by the total number of openings in the array. In these papers the size of the droplet and consequently the diameter of the NWs have been found to be primarily determined by the V/III ratio and growth temperature and not directly related to the dimensions of the holes of the array. The yield of vertical NWs reported in [101] was 60% and has been incremented up to 95% in [116] by optimizing the mask oxide thickness and the Ga pre-deposition time. However some growth results seem to be not entirely consistent and hinting to a lack of reproducibility.

Gibson *et al.* also recently reported on the growth of self-catalyzed GaAs NWs on patterned silicon substrates [117, 118]. Length and diameters of NWs have been found to increase by increasing the inter-hole distance (pitch) of the array. This behavior has been explained in terms of evaporation and secondary adsorption of both gallium and arsenic. The importance of properly removing the SiO_2 from the bottom of the holes has been underlined. NWs grown in oxide free holes present low dispersion in length and radius. Conversely, NWs grown in holes with residual oxide present non uniform morphology. The residual, and likely non uniform, oxide layer could be indeed the cause of a spread in incubation time. If the oxide is too thick no growth is observed. The highest yield reported in the papers is 60%, a result which can be regarded as good given the difficulties in obtaining successful growths.

It is also worth mentioning the growth of GaAs NWs on silicon using nanoimprint lithography by Munshi *et al.* [119]. A yield of vertical NWs of about 80% has been achieved by tuning properly the growth conditions even if some results seem to be not consistent. As seen in [116], the Ga pre deposition time seems to be a key parameter for achieving a high yield of vertical GaAs NWs on array as it drastically spoils the growth if times are set too short.

All the papers above hint at focusing the attention on the shape of the gallium droplet and to its interaction with the silicon substrate. It has been shown that the parameters most affecting the yield are the Ga pre deposition time and the thickness of the mask oxide. The time of Ga predeposition changes the size of the droplet. This in turn could change the shape of the droplet and the contact angle with the substrate and eventually lead to to conditions favorable or unfavorable for the growth of vertical NWs. The modulation of the oxide thickness as done in [116] implies a change in the morphology (both aspect ratio and roughness) of the holes. A change in the aspect ratio could also have an impact on the shape of the droplet if the dimensions of droplets and holes are comparable. Lastly, different oxide thicknesses imply different etching time, i.e. likely different roughness of the silicon surface at the bottom of the holes. This could in turn affect the shape of the droplet. This needs further investigation.

2.3.2 InAs NWs growth by Selective Area Epitaxy

Another way to prevent the use of gold for the synthesis of NWs is Selective Area Epitaxy (SAE). Here the growth is not catalyst assisted at all i.e. no catalyst is needed and the growth
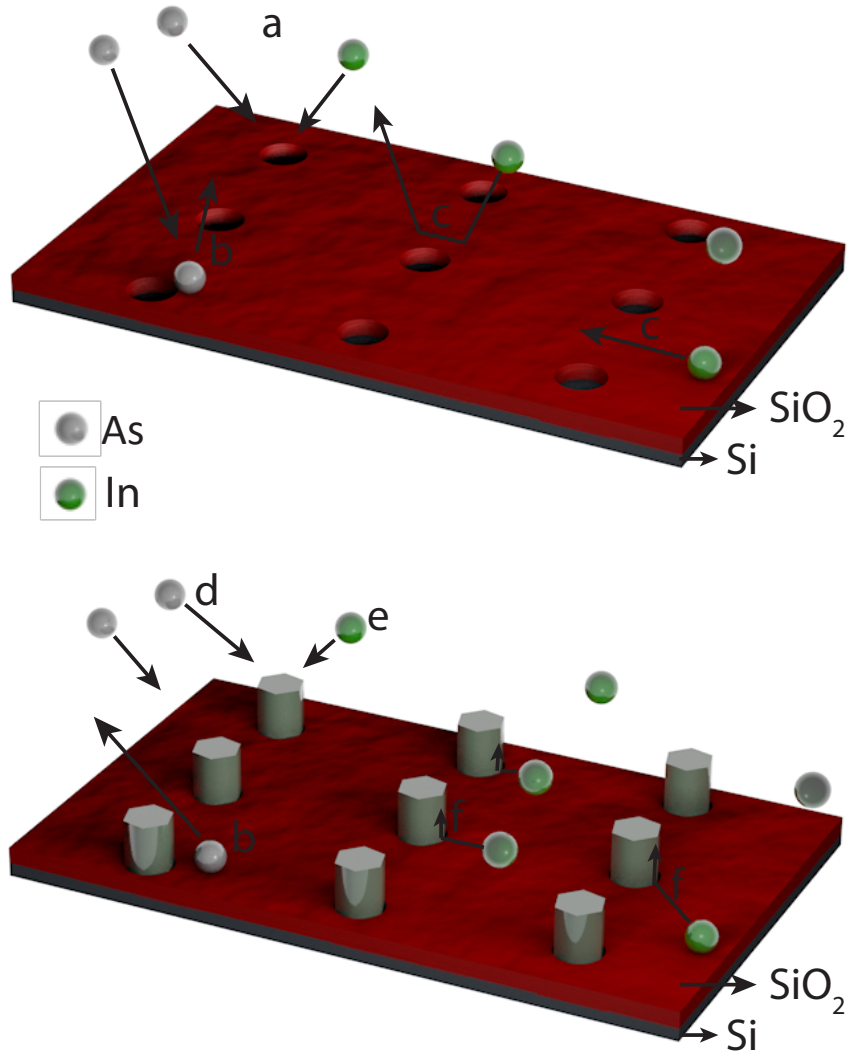
Figure 2.11: Kinetics processes during the InAs NWs growth by SAE. a) As and In impingement on the substrate. b) As desorption from the substrate. c) In diffusion on the substrate and evaporation. d) Direct impingement of As onto the NW surface. e) Direct impingement of In onto the NW surface. f) In diffusion from the substrate along the sidewalls.

mechanism relies on the preferential formation of facets. Since the crystal facets with the lower formation energy in III-V semiconductor are {110} and {111}, monodimensional enhanced growth in form of vertical NWs is possible only on (111)B III-V or on (111) silicon substrates.

The purpose of SAE is to restrict the incorporation of adatoms to only certain areas of a sub-

strate, which makes the technique particularly suitable for growth on patterns. The first step of the process is hence to create the pattern on the substrate. A common way to accomplish this is with nanoscale openings on a silicon dioxide mask (figure 2.11 top). The wafer is covered with an amorphous layer, typically SiO_2, that is patterned with nanoscale apertures, for example through lithography and etching. The epitaxy should occur only in these opened area and not on the oxide. The preferential growth of the nanostructures in the openings rather than on the SiO_2 of the growth mask, the so-called selectivity, can be reliably achieved with techniques like chemical vapor deposition (CVD) or metalorganic vapor phase epitaxy (MOVPE) since it relies on the preferential decomposition of the precursors on some materials. The first successful growths of periodic arrays of high aspect ratio III-V semiconductor NWs by SAE have been obtained with these techniques. We report as a reference the works conducted by the group of Takashi Fukui on the growth of semiconductor pillar arrays [120, 121] and the ones on the growth of high uniform arrays of hexagonal III-V semiconductor NWs on different substrates like GaAs ad InGaAs NWs on GaAs(111)B [122–124], InP NWs on InP(111)A [125, 126], InAs NWs on InAs(111)B [127] and finally on Si(111) [128].

InAs is an attractive material thanks to its peculiar properties: it possesses one of the highest mobilities in the group of III-V semiconductor (33000 $cm^2/(Vs)$) and has small electron effective mass and low band gap energy (0.36 eV). It is as such a good candidate for low power and high speed electronics and its integration on silicon it has been object of in-depth investigation [129].

To the best of our knowledge, the first SAE growth of InAs NWs on silicon substrate by MBE has been reported by Hertenberger *et al.* [130]. Here the InAs NWs, vertically aligned with respect to the substrate and with an hexagonal cross section, show a growth rate proportional to the arsenic beam equivalent pressure, the same that was found for self-catalyzed GaAs NWs (see section 2.3.1).

Interestingly, the growth rate has been found to be dependent on the distance between the openings of the pattern (pitch). This means that growth occurs in two different regimes depending on the value of the pitch. These two regimes correspond to: (i) competitive growth regime characterized by shorter Nws for small pitches and (ii) diffusion limited or independent growth regime for longer pitches. The switch between the two regimes is determined by the indium surface diffusion length on SiO_2 (λ_{SiO_2}). λ_{SiO_2} limits the sample area from which each NW can collect the In species which are diffusing on the sample. For a small spacing (pitch $< 2\lambda_{SiO_2}$), the indium adatoms are shared between the NWs. By increasing the spacing, the surface collection area available exclusively to each single NW increases, resulting in a linear increase of the growth rate. In the opposite limit of a large spacing (pitch $> 2\lambda_{SiO_2}$) the NWs can be treated as independent isolated islands. In this regime the surface collection area saturates and the growth rate is no longer dependent on the pitch. Similar observations have been made by other groups examining the growth of NWs on patterns [131, 132] and by us (Paper III, Paper VI).

It is worth to note that, in the case of MBE, the selectivity is obtained by setting the growth conditions so that the sticking coefficient of the adatoms is zero on the oxide and non zero in the apertures. This will result in diffusion of the adatoms from the oxide to the windows and in a preferential desorption of adatoms on the oxide compared to the exposed surface [133].

The growth of NWs on precise locations and with controlled positioning is the ideal setting for studying their growth mechanisms but also for investigating fundamental matters of great relevance for their use in applications. As an example, NWs are expected to play an important role in the development of solar cells since they can overcome the geometrical limitations of a conventional solar cell [134] by decoupling the direction of carrier absorption from the direction of carrier separation. The challenges associated with the growth of GaAs NWs in arrays on silicon substrate have prevented so far the achievement of a solar cell based on these materials and geometry. Conversely, InAs arrays are relatively straightforward to grow. For this reason, and despite the small InAs band gap that hinders the achievement of high efficiency [135], InAs NWs grown in arrays have been chosen as model system to study the potentiality of NWs as future solar cells [136].

2.4 Growth on Si(100) substrates

A further step towards industrial applications for nanostructures grown on silicon would be the use of Si(100) as a substrate. This is the platform in use in all the microelectronic industry, as CMOS fabrication on (110) and (111) has been traditionally hampered by their inferior gate oxide reliability. Moreover the electron channel mobility of a MOSFET on Si(100) is higher than that on Si(111) [137].

Due to its technological importance, the Si(100) surface has been intensively studied and characterized. In the ideal bulk-terminated Si(100) surface each atom of the topmost layer has two dangling bonds. This makes the surface unstable so the atoms rearrange to lower the surface energy. The observed reconstruction is a dimerization: surface atoms move close to each other to form one bond called dimer [138, 139]. The formation of dimers halvens the number of dangling bonds and thus reduces the surface energy.

Silicon surfaces are not flat but contain steps at a macroscopic scale. Stepped (or vicinal) surfaces are usually produced on purpose through a miscutting at a small angle. Indeed steps are useful in epitaxy since they can act as nucleation centers or can induce step-flow growth. The vicinal Si(100) surface, i.e with its surface normal a few degrees away from (100) towards the <011> direction, can be described as stairs-like surface with microscopically wide flat terraces separated by monoatomic steps (figure 2.12). Each terrace is characterized by dimer rows along the <110> directions. The dimer row directions of terraces separated by an odd number of single steps are perpendicular to each other, or equivalently two neighboring terraces have two surface atomic configurations rotated by 90° with respect to each other.

In the realm of NWs (100) substrates are not commonly used. Instead (111) substrates are
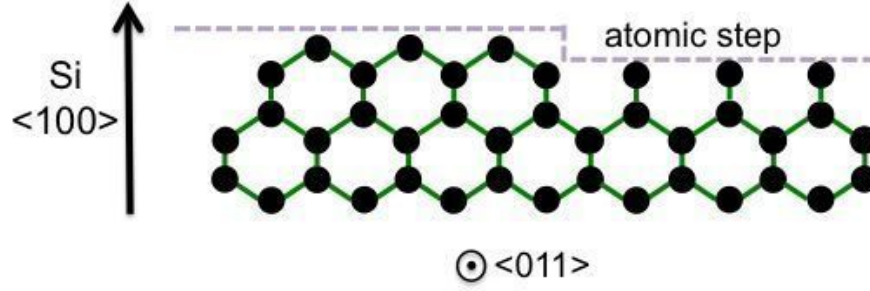
Figure 2.12: Atomic model of step structures for a vicinal Si(100) surface. (100) terraces are arranged in a staircase fashion. The step height is one atomic layer high and the two neighbor terraces have their dimer row directions rotated by 90°.

chosen to obtain NWs vertically oriented respect to the surfaces since NWs grow preferentially in the <111> direction. However <111>-oriented NWs show a high density of planar defects or even polytypisms that can significantly affect the optical and electronic properties of the NWs. Conversely the growth in the <100> direction would result in the reduction of the density of dislocations and stacking faults since slip occurs on {111} planes along the <110> directions for a fcc crystal.

Vertically standing and defect free pure ZB InP NWs have been obtained on InP(001) substrates by Au-assisted metal organic vapor phase (MOVPE) epitaxy [140] and, as a step further, in arrays with a yield of vertical wires of 50% [141]. Growth by MBE has also been reported: for group III-phosphide NWs [142] and group III-nitride NWs that seem to show less preference towards a particular growth direction [143–145].

However, if we consider silicon substrates, no prior literature exists on gold-free vertical group III-arsenide nanostructures epitaxially grown on Si(100), with the closest result we have found regarding the use of SiO_2 nanotubes template [146].

Indeed, many research works have shown that the growth on Si(100) is dominated by the Stranski Krastanov growth mode which leads to the formation of quantum dots (QDs) . The growth of V-shaped InAs nanomembranes, whose discovery is one of the main results of this thesis as we will discuss below, depends on this mechanism; for this reason we will review some key concepts and works related to Stranski Krastanov growth of QDs.

2.4.1 Stranski Krastanov growth of QDs

QDs are zero-dimensional semiconductor structures (~10 nm in the three dimensions) where charge carriers are confined in the three spatial directions [147]. As a result the energy levels are discrete and the density of states consists of a series of delta-function-like peaks. The quantization of electron energies leads to unique photonic and electronic properties thus making the physics of QDs very intriguing research topic [148].

27

QDs are of particular interest not only as systems to study a wide range of physical phenomena but in many applications too. They can be building blocks for fast electronic devices [149], they can emit light if excited, the smaller the dot, the higher the energy of the emitted light and thus be used as biosensors [150]. QDs can be applied into various optoelectronic devices like solar cells [151], light emitting diodes [152], photodetectors [153] and field effect transistors [154].

There are two families of QDs: colloidal [155] and epitaxial [147]. In this second group QDs at a semiconductor surface can be obtained by conventional lithographic techniques or by "self-assembly". In the first case the dimensions of the QDs are limited by the resolution of lithography, in the second case QDs are produced spontaneously, in the *Nature's way* [156], and, under optimized conditions, with high density and homogenous size. The condition to fulfill here is a large lattice mismatch between the one of material deposited and the one of the semiconductor surface. In this Nature's way three dimensional islands or QDs will form in the Stranski Krastanov (SK) or in the Volmer Weber (VW) growth modes.

As discussed in the introduction, the planar growth of a epilayer on a large mismatched substrate, like GaAs or InAs on Si, will suffer of the formation of dislocations at the interface if the thickness of the epilayer is larger than a critical thickness h_d. Dislocations form to release the strain. However the lattice mismatch can be accomodated not only with the formation of dislocations but also through the formation of three-dimensional islands in the VW or SK growth mode. Here the strain is efficiently released thanks to the availability of free lateral surfaces.

SK is a "layer+island" growth mode that consists of two process steps. The growth of a layer A on the substrate B starts with the formation of a film (wetting layer) in a "layer by layer" mode. Then above a critical thickness h_c the growth continues with the nucleation of 3D islands. Indeed if

$$\Delta \gamma_n = \gamma_A - \gamma_B + \gamma_i < 0 \tag{2.1}$$

where γ_A and γ_B are the surface free energies of A, B and γ_i is the interfacial free energy, the growth will occur layer by layer (Frank-van der Merwe growth -FM-) and we will have the formation of the wetting layer. However, the strain energy, which is considered in γ_i, increases with the thickness of the epilayer. At some thickness h_c, $\gamma_A + \gamma_i$ exceeds γ_B and the growth mode changes to SK, resulting in 3D islands on the 2D wetting layer [157].

This means that in the SK mechanism the surface energy competes with the driving force for island formation, i.e. the energetically unfavorable formation of lateral facets in presence of a wetting force competes with the energetically favorable process of elastic stress relaxation. The competition between surface energy and strain determines the minimum energy shape of the islands. Furthermore the island shape is not fixed, but changes continuously with the

volume [158].

In analogy with the critical thickness for dislocation h_d, h_c depends on the lattice mismatch and decreases with it. However their dependence from the lattice mismatch is different since they are determined by two different ways of stress relaxation. Qualitatively, for lattice mismatches < 2%, $h_d < h_c$ and the elastic stress is released with the introduction of misfit dislocations. Conversely, for lattice mismatches > 2%, $h_d > h_c$ and the stress is released through the formation of 3D islands [22]. For very large lattice mismatches, the formation of three dimensional islands can occur at critical thicknesses $h_c < 1\,ML$. In this case the 2D wetting layer is not formed and we talk about Volmer Weber (VW) growth mode.

Over the past years the self organization of QDs have been studied for several material systems, such as III-V on III-V [159], II-VI on II-VI [160] and IV on IV [161]. As seen before for III-V materials in general and in analogy with them, the incorporation of III-V QDs on group IV represents a highly sought goal as it would bring to conventional substrates the excellent optical properties and capabilities of QDs. Among the different possibilities of material system, InAs/Si QDs is one of the most commonly studied. Several groups reported on the growth of such structures by MBE through the SK growth mechanism [162–167]. Furthermore an optimal tuning of the growth conditions (mainly the temperature and In flux) led to the synthesis by the VW growth mechanism [168–170].

Concerning the morphology of SK InAs on silicon, these clusters are usually found to be pyramids with bases slightly elongated (rectangular) and oriented along [011] and [0-11] directions [163, 164]. Interestingly, InAs/Si islands seem to develop {111} facets on the pyramidal core [167].

One limitation of the SK growth mechanism is that the QDs cover the surface randomly without any control on the nucleation site. The capability to grow QDs on precise positions is highly desirable for realizing optical and electronic devices. This is obtained by growing QDs on a surface patterned with nanoscale holes [171]. However one should note that the mechanism of self-assembly on a patterned area is fundamentally different from the one on a unconfined area. Indeed the window size can affect the minimum energy configuration i.e. the preferred shape of the island and can suppress the island formation if it is below a critical size. As seen before, the competition between strain and surface energy (in absence of constraints on the surface) determines the aspect ratio of the island. If constraints are present like confined area, there is an energy penalty to be introduced in the energy balance. The island forms with an aspect ratio higher than the one it would prefer on a free surface. This causes an increases in surface energy and a decrease in stress energy, then overall a increase in the total free energy. If the aspect ratio is sufficiently larger than its preferred value, the penalty is so high that the free energy of the island configuration exceeds the one of a flat film and the island formation is suppressed [172].

2.5   Beyond Nanowires

NWs are only one among many shapes that have been achieved in trying to reduce the scale of semiconductor structures. In fact, many other shapes are possible. Here we review some of the literature on the subject. Other peculiar morphologies are nanowalls [11] (figure 2.13 a-b), nanosheets [13, 14] (figure 2.13 c), nanoflowers [173] (figure 2.13 d), nanotrees [15] (figure 2.13 e), nanomembranes [8–10] (figure 2.13 f), nanoplates [12] (figure 2.13 g), and branched structures like tripods and tetrapods [16–18] (figure 2.13 h-k) and so on. These nanostructures with different sizes and shapes have recently attracted great attention for two main reasons: 1) they can be used to realize architectures otherwise impossible with the traditional thin film technology. 2) they can show unusual physical or chemical properties: their shape can dramatically enhance the intrinsic properties [174]. In particular, branched structures can increase even more the functionality of nanostructures, by providing a path to interconnect different elements on the substrate.

One peculiar branched shape that has been observed in many semiconductor nanocrystals is the tetrapod. This shape consists in a central nucleus from which facets four arms extend at tetrahedral angles. Examples are ZnO [175], CdTe [176], CdS [177], and CdSe [178] tetrapods. Interestingly for these kind of material systems TEM analysis gave the evidence that the central core region has cubic ZB phase and that it is bounded by {111} facets; the growth of the arms occurs instead in WZ phase (figure 2.13 j). Any strain is generated at the arm/nucleus interface since along the <111> directions the two phases differ only in the stacking sequence while there is a perfect match in lattice parameters.

Also other branched shapes like dipods and tripods have been observed. Tripods are crystals with three arms usually with three-fold symmetry with respect to the center of the structure; dipods have two arms that have been found to form a L-, I- or V-shape [179].

All these branched structures reported above are colloidal (i.e. dispersed within a continuous medium) or freestanding (i.e. detached from any substrate) products. To the best of our knowledge, only one group reported on the growth of such structures on a substrate [16, 180]. Growth on a preexisting substrate is indeed a crucial step for the practical use of these structures. Utama *et al.* reported for the first time the synthesis of epitaxial II-VI semiconductor tripods and tetrapods on mica substrates. These structure also show a ZB nucleus and arms in WZ phase. The work demonstrated that the polarity plays an important role in determining the morphology of the structures and their arrangement on the substrates. Arms grow only on the seed facets that have the same polarity as the fast growth plane; structures can show only few orientations and the directions at which the arms point are related by rotation of predictable angles (this also implies an epitaxy with the substrate).

Interestingly, this work also suggests the possibility to switch from branched structures to NWs by changing the surface preparation. Even if the mechanism responsible for the occurrence of this phenomenon has not been fully understood, the results of Utama *et al.* envisages a way of tuning rationally the morphology of epitaxial nanostructures to achieve higher complexity on

the same substrate.

It is worth to note that here the epitaxy is achieved via the van der Waals attraction between the dipole across the nanostructure and substrate surfaces[3]. Typically the epitaxy of a conventional bulk system on a substrate or of a semiconductor NW on silicon, that we described above, is achieved via the covalent chemical bonding between the atoms of the surfaces in contact. To the best of our knowledge, the growth of branched InAs structures with conventional epitaxy by MBE and the possibility to modulate their morphology has not been reported so far.

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[3]In the Van der Waals epitaxy the epilayers are grown onto substrates whose surface does not have a high density of dangling bonds. Unlike that in conventional heteroepitaxy, the heterointerface of substrate-epilayer is connected via van der Waals bonds. Due to the weak interaction, heteroepitaxial growth is not restricted to few combinations of mismatched materials. Indeed the lattice matching condition is drastically relaxed and an epilayer grows from the beginning with its own lattice constant forming an interface with only a small amount of defects. It is expected that good heterostructures can be grown even between materials having large lattice mismatch [181].
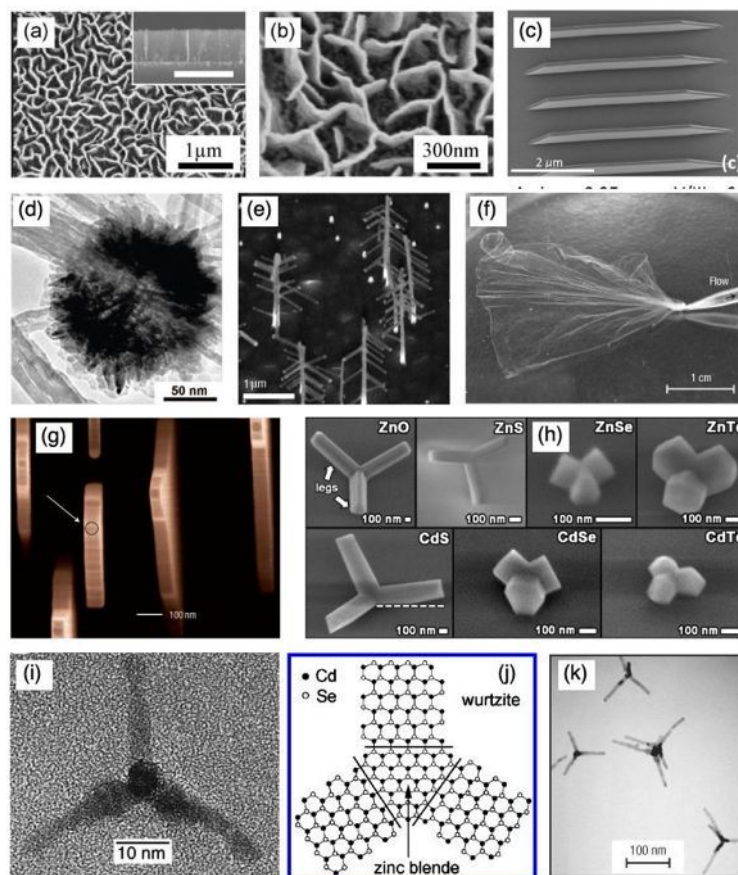
Figure 2.13: Variety of nanoscale shapes achieved with different growth mechanisms and techniques. (a-b) SEM images of the carbon nanowalls grown on Si substrate. Reprinted with permission from [11]. Copyright Applied Physics Letters 2004, AIP Publishing LLC. (c) SEM images of GaAs nanosheets grown on GaAs(111)B substrates. Reprinted with permission from [14]. Copyright 2013 American Chemical Society. (d) TEM image of a manganese oxide nanoflower. Reprinted with permission from [173]. Copyright 2008 American Chemical Society. (e) SEM images of GaP nanotrees. Reprinted by permission from Macmillan Publishers Ltd: Nature Materials [15], copyright 2004. (f) Optical micrograph showing the aspiration process of a 16 cm^2 nanomembrane. Reprinted by permission from Macmillan Publishers Ltd: Nature Materials [9], copyright 2006. (g) SEM images of InAs nanoplates grown perpendicular from the surface of a (100) GaAs substrate. Reprinted by permission from Macmillan Publishers Ltd: Nature Nanotechnology [12], copyright 2007. (h) SEM images of individual II-VI tripods on muscovite mica substrate. Reprinted with permission from [16]. Copyright 2012 American Chemical Society. (i) HRTEM image of a typical tetrapod-shaped CdSe nanocrystal. (j) Two-dimensional representation showing the structure of a tetrapod. The nucleus has a zinc-blende structure, with wurtzite arms growing out of each of the four {111} equivalent facets. (i) and (j) are reprinted and adapted with permission from [178]. Copyright 2000 American Chemical Society. (k) TEM image of CdTe tetrapods. Reprinted by permission from Macmillan Publishers Ltd: Nature Materials [176], copyright 2003.

3 Results

III-V compound semiconductor nanostructures have been intensively investigated for the perspectives they offer in fundamental and applied research. The integration on the mature, cost effective and high performance silicon platform would lead to a combination of the best properties of both the semiconductor classes and it is the key for their industrial applications. However the process of integration is a technological feat. Although many progresses and developments have been made in the recent years, important issues are still unsolved.

The goal of this thesis was to understand the dynamics of the growth of gold-free III-V semiconductor nanowires (NWs) and nanomembranes on silicon substrates by molecular beam epitaxy (MBE), focusing the attention mainly on the nucleation stages. My work led to the publication of the articles listed in section 3.1. Other works I have been involved in, submitted at the time of presenting the thesis and not discussed in this work, are listed in section 3.4.

Figure 3.1 is a visual summary of the results obtained during these four years at Laboratory of Semiconductor Materials, EPFL. The first challenge that we faced was to understand the occurrence of non vertical wires in Ga-assisted GaAs NWs grown on Si(111). We demonstrated that orientations different from vertical can be explained with the formation of secondary grains due a three-dimensional twinning phenomenon. This mechanism can be tuned as a function of the growth conditions by changing the relative size between the GaAs grain and the Ga droplet. We also demonstrated how a further optimization of the growth conditions results in a 100% yield of vertical NWs (figure 3.1 a).

Another part of my research has been devoted to the realization of regular arrays of NWs. While InAs NWs tends to grow in a relatively straightforward manner on patterned Si(111) substrates, GaAs NWs remain more challenging, as a successful growth depends critically on the cleaning steps, annealing procedure, pattern design and on the morphology of the silicon substrate and of the mask oxide. An overview of the obtained results are presented in figure 3.1 d-e and figure 3.1 n-p.

Lastly, we made a further step and we turned to the growth of NWs on oriented (001) substrates.
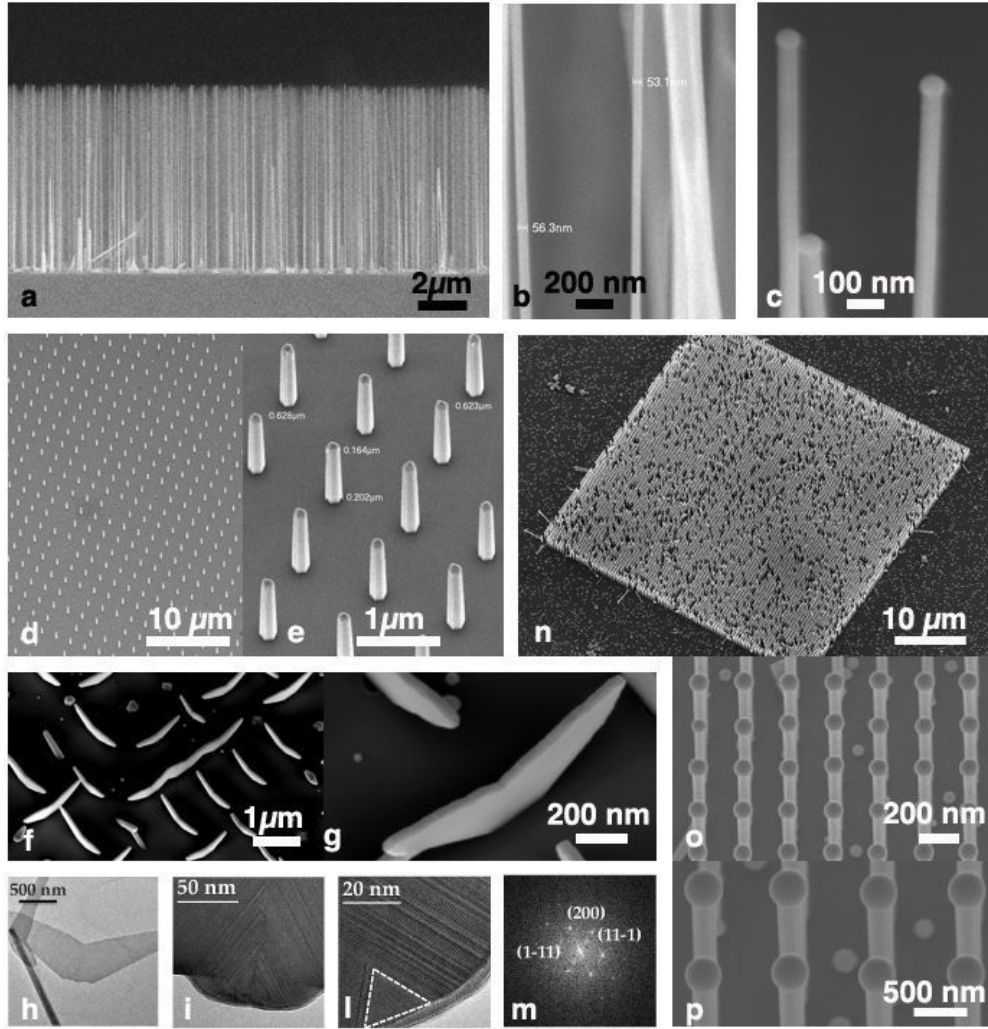
Figure 3.1: (a-c). Cross-section scanning electron microscopy (SEM) micrographs of self-catalyzed GaAs nanowires (NWs) on Si substrate grown by molecular beam epitaxy (MBE). (a) 100% yield of vertical wires is achieved by optimization of the growth conditions. High magnification on the thin diameters in (b) and on the NWs tips in (c). (d-e). 20° tilted SEM images of InAs NWs on a patterned Si(111) substrate grown by Selective Area Epitaxy at different magnifications. (f-g). Tilted SEM images of typical V-shaped InAs nanomembranes grown on Si(001) substrates at different magnification. The images reveal the peculiar V-shaped of the membranes with arms branching towards two <111>B directions. (h) Transmission electron microscopy (TEM) micrograph of an InAs nanomembrane. All the V-shaped InAs nanostructures analyzed exhibit distinguishing features: a nucleus region in the base and the two arms coming out of this nucleus. (i-l) High resolution TEM images of the nucleus. (n) Diffraction pattern of the nucleus. The InAs nucleus has a perfect zinc-blende crystalline structure. (n-p). 20° tilted SEM images of GaAs NWs on a patterned Si(111) substrate grown by the vapor-liquid-solid mechanism with a self-catalyzed approach.

This led us to the discovery of a new class of III-V semiconductor nanostructures, called V-shaped nanomembranes, characterized by a unique morphology and growth mechanism and possessing interesting optical properties (figure 3.1f-m).

3.1 Papers included in my thesis work

This thesis is based on the following papers:

I **Three-dimensional twinning of self-catalyzed GaAs nanowires on Si substrates**
E. Uccelli, J. Arbiol, C. Magen, P. Krogstrup, E. Russo-Averchi, M. Heiss, G. Mugny, F. Morier-Genoud, J. Nygard, J.R. Morante and A. Fontcuberta i Morral
Nano Lett. 11 (2011) 3827
I took part in the growth of the wires, I performed the SEM characterization, I observed and analyzed the multiple growth directions of the wires discussed in the paper. I contributed to the illustrations and I took part in writing and discussing the paper.

II **Suppression of three dimensional twinning for a 100 % yield of vertical GaAs nanowires on silicon**
E. Russo-Averchi, M. Heiss, L. Michelet, P. Krogstrup, J. Nygard, C. Magen, J.R. Morante, E. Uccelli, J. Arbiol, A. Fontcuberta i Morral
Nanoscale 4 (2012) 1486
I planned and executed the growth of GaAs wires, took part to the SEM characterization, I extracted and analyzed the data and I took part in writing the manuscript.

III **III-V nanowire arrays: growth and light interaction**
M. Heiss[a], E. Russo-Averchi[a], A. Dalmau-Mallorqui[a], G. Tütüncüoglu[a], F. Matteini, D. Rüffer, S. Conesa-Boj, O. Demichel, E. Alarcon-Llado and A. Fontcuberta i Morral
[a] equal contribution
Nanotechnology 25 (2014) 014015
I planned the growth experiments and I obtained the NWs arrays, I performed the morphological characterization of the structures. I contributed to the illustrations and to the writing of the paper.

IV **Amorphous silicon mediates a high yield in GaAs nanowire arrays on Si obtained by the Ga-assisted method**
E. Russo-Averchi, J. Vukajlovic Plestina, G. Tütüncüoglu, A. Dalmau-Mallorqui, M. de la Mata, D. Rüffer, H.A. Potts, F. Matteini, J. Arbiol, S. Conesa-Boj and A. Fontcuberta i Morral
submitted
I planned and executed the growth of high yield GaAs NWs in arrays. I took part to the sample preparation and to the SEM characterization of the structures. I did the figures and I contributed to write the manuscript.

V **Vertical "III-V" V-shaped nanomembranes epitaxially grown on a patterned Si(001) substrate and their enhanced light scattering**
S. Conesa-Boj[a], E. Russo-Averchi[a], A. Dalmau-Mallorqui, J. Trevino, E. F. Pecora, C. Forestiere, A. Handin, M. Ek, L. Zweifel, L. R. Wallenberg, D. Rüffer, M. Heiss, D. Troadec, L. Dal Negro, P. Caroff and A Fontcuberta i Morral
[a] equal contribution
ACS Nano 6 (2012) 10982
I planned the growth experiments and I discovered the V-shaped nanomembranes, I did the SEM characterization. I contributed to the illustrations. I wrote the paper with the coauthors.

VI **Growth mechanisms and process window for InAs V-shaped nanoscale membranes on Si(001)**
E. Russo-Averchi, A. Dalmau-Mallorqui, I. Canales-Mundet, G. Tütüncüoglu, E. Alarcon-Llado, M. Heiss, D. Rüffer, S. Conesa-Boj, P. Caroff and A. Fontcuberta i Morral
Nanotechnology 24 (2013) 435603
I planned the growths, conducted part of the experiments, I extracted, analyzed and interpreted the data. I did the figures and took part in writing the manuscript.

VII **Bottom-up engineering of InAs at the nanoscale: from V-shaped nanomembranes to Nanowires**
E. Russo-Averchi, G. Tütüncüoglu, A. Dalmau-Mallorqui, I. Canales-Mundet, M. de la Mata, D. Rüffer, J. Arbiol, S. Conesa-Boj and A. Fontcuberta i Morral
in review
I planned the growth experiments, I analyzed the data. I contributed to the illustrations and to the writing of the paper.

The results published in these papers will be summarized in the following sections. Each argument is discussed separately and it is followed by a reproduction of the related papers.

3.2 Control of the NW growth direction

Publications:

I **Three-dimensional twinning of self-catalyzed GaAs nanowires on Si substrates**
E. Uccelli, J. Arbiol, C. Magen, P. Krogstrup, E. Russo-Averchi, M. Heiss, G. Mugny, F. Morier-Genoud, J. Nygard, J.R. Morante and A. Fontcuberta i Morral
Nano Lett. 11 (2011) 3827

II **Suppression of three dimensional twinning for a 100% yield of vertical GaAs nanowires on silicon**
E. Russo-Averchi, M. Heiss, L. Michelet, P. Krogstrup, J. Nygard, C. Magen, J.R. Morante,

E. Uccelli, J. Arbiol, A. Fontcuberta i Morral
Nanoscale 4 (2012) 1486

Following the VLS theory, the NW growth is 2D nucleation limited at the liquid-solid interface. This means that the liquid has to reach a critical level of supersaturation to overcome a nucleation barrier at the top facet in order to allow the formation of a small nucleus. The nucleation takes place preferentially at the triple phase line, then a monolayer forms via step flow. Other facets, not nucleation limited, can reshape. This leads to the formation of one monocrystalline grain during the early stages of growth. The shape of this grain is the polyhedron closed by the lowest energy facets, which are the {111} and {110} surfaces for zinc-blende and diamond crystals. The grain can assume a prismatic shape with {110} lateral facets; if all the facets are {111} surfaces, the grain is a octahedron. In case of a III-V crystal the eight facets of the octahedron are not equivalent but have alternate termination: four are <111>A and four <111>B, as depicted in figure 3.2 a [182].

When growing III-V NWs on elemental (111) substrates, like silicon, only two growth directions are expected: for a single grain with B polarity, i.e. with the top surface parallel to the substrate As terminated (see figure 3.2 b-d), the NWs should grow perpendicularly to the substrate. If the top surface of the grain has A polarity, the NWs grow with a tilt forming an angle of $19.5°$ with the substrate as the three lowest free energy {111}B facets point out of the substrate at this angle (figure 3.2 e).

Surprisingly, we observed experimentally that GaAs NWs can grow following different directions: we found wires growing at $34°$ or $51°$ or even horizontally, crawling on the surface. We also observed that only some orientations are allowed (the measured angles form a discrete set) and that their occurrence is a function of the V/III beam equivalent ratio. Indeed the lower is the V/III ratio the higher is the occurrence of non-vertical orientations and the more the angles allowed. Conversely, the density of vertical wires increases by increasing the V/III ratio while the number of different tilted orientations decreases, but it is never zero. It seems that we converge towards what is predicted by the standard theory, i.e. the tilted wires are mainly at $19.5°$.

These findings are inconsistent with the crystallography of a single grain and indicate that the existing theory is not adequate enough.

A detailed analysis of the crystalline phase of the grain of tilted NWs has been key to unravel the reasons behind the occurrence of different growth directions. The analysis consisted in a STEM-HAADF (Scanning Transmission Electron Microscopy - High Angle Annular Dark Field) imaging performed on a probe aberration corrected microscope. This analysis gave us the experimental evidence of multiple grains: tilted wires are found to originate not from a single crystalline grain but from polycrystalline grains, composed by different grains separated by twins at {111} planes. This work has been executed at the Institut de Ciencia de Materials de Barcelona, Spain, in collaboration with Prof. Jordi Arbiol.
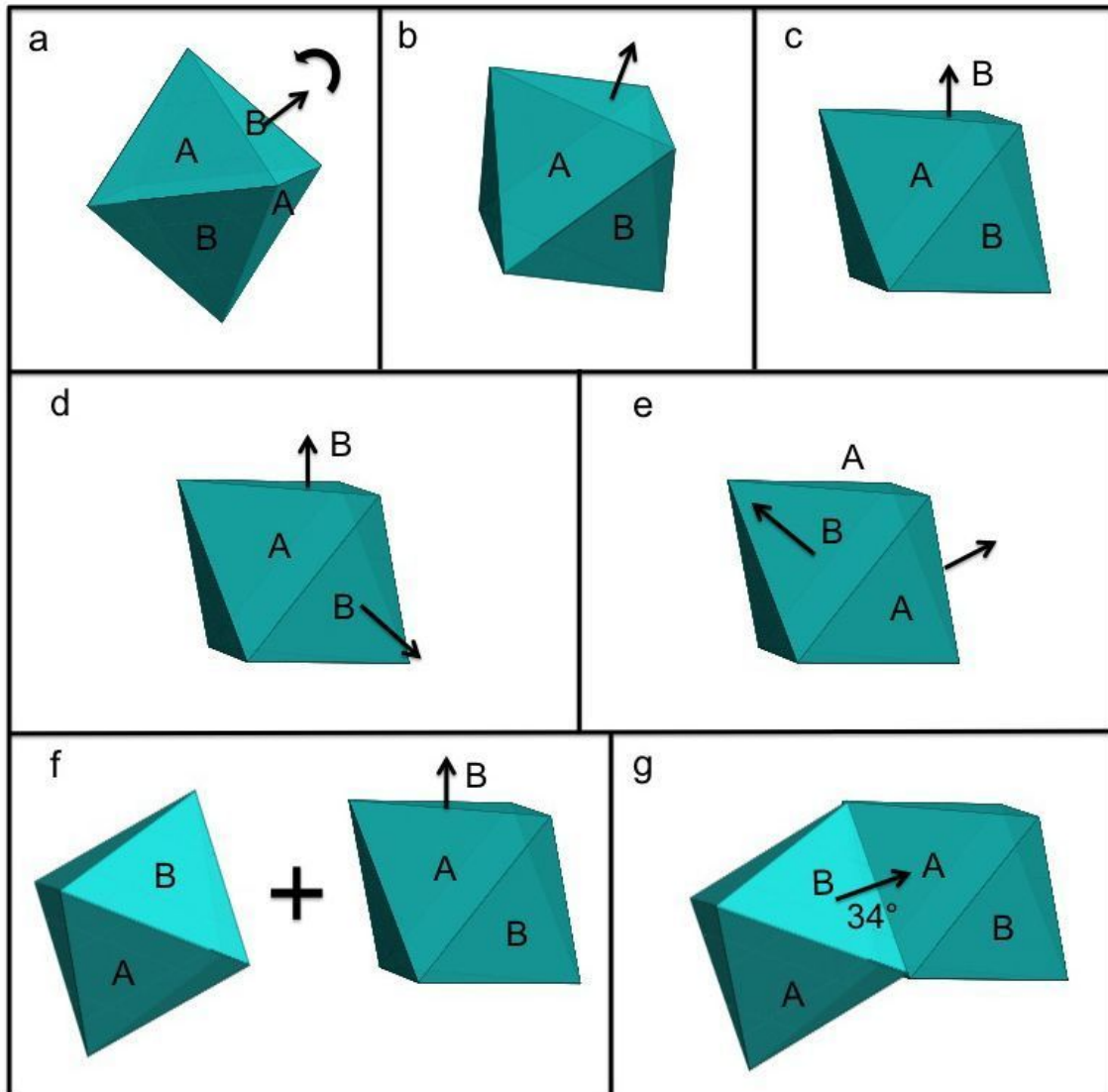
Figure 3.2: (a-c) 3D scheme of a octahedral grain formed by {111} surfaces in the case of a III-V crystal: four facets have A polarity and four B polarity. d) octahedral with (111)B surface in epitaxy with the substrate: the top surface is (111)B, the other three {111}B facets will face downwards the substrate. e) octahedral with (111)A surface in epitaxy with the substrate: the top surface is (111)A, three {111}B facets points out of the substrate. (f-g) polycrystalline grain formed by a primary grain with B polarity and a secondary grain. In this configuration growth at an angle of 34° with the substrate is allowed.

To explain this observation we developed a new theoretical model, called *Three dimensional multiple order twinning,* according to which twinning and further growth on the lateral facets of the (first) single grain result in the formation of secondary grains, and overall in a polycrystalline grain (figure 3.2 f-g).

The occurrence of different discrete orientations is the consequence of how the polycrystalline grains are geometrically built from primary and secondary grains. The formation of new grains implies the formation of new {111}B facets. According on how they combine, the NWs can grow along directions different than 19° and 90° because the (111)B facets of the new grains will be in a different position respect to those of the primary grain. For example, one secondary grain attached to a primary grain with B polarity (first order twinning) explains the formation of the growth directions 34° (figure 3.2 g). Different arrangement and combinations of more grains (multiple order twinning) can explain many other orientations just with geometrical rules. The higher is the number of grains attached (the higher the order of twinning), the more the combinations and then the more the growth directions allowed. These growth directions are determined by geometrical construction and can be obtained through mathematical calculations, assuming that the growth proceeds on facets with B polarity and that the polarity is conserved along the direction perpendicular to the twin.

Now the question is why the secondary grains form and why the occurrence of different orientations depends on the V/III ratio. The *Three dimensional multiple order twinning* model takes into account that the observed nucleation time of the NWs grown at a low V/III ratio is much larger than the one of NWs grown at a high V/III ratio (20 s for V/III=60 versus 2 min for V/III=15). This increase in the nucleation time must result in a larger Ga droplet, i.e. the Ga droplets increases with time.

At low V/III ratio, a Ga droplet increased quickly in size can wet the sides of the grain. In this configuration the favored shape of the grain is an octahedron. The wetting of the side facets favors also the formation of secondary grains and thus of non vertical growth directions, as explained above. By increasing the V/III ratio, the nucleation time decreases and so does the relative size of the droplet respect to the grain. When the droplet covers only the top surface of the grain its favored shape is a prism with a top (111)B surface and lateral {110} facets. In this case the NWs can grow only perpendicular to the substrate. By increasing the V/III ratio then the formation of octahedral grains and eventually secondary grains becomes less and less probable and the number of allowed tilted growth directions decreases as a consequence.

This means that the *Three dimensional multiple order twinning* mechanism can be in principle controlled and tuned as a function of the growth conditions. Indeed, by adjusting the growth temperature which can affect the size ratio between the GaAs grain and the Ga droplet in the same way as the V/III ratio, a 100% yield of vertical wires has been achieved and the three dimensional twinning completely suppressed. A more detailed theory still needs to be formulated to fully describe the dynamics of the process.

It is worth noting that these results are general across the III-V semiconductor family and as such are of paramount importance for the reproducible integration of self-catalyzed III-V NWs on group IV substrates.

NANO L E T T E R S

Three-Dimensional Multiple-Order Twinning of Self-Catalyzed GaAs Nanowires on Si Substrates

Emanuele Uccelli,[†,¶] Jordi Arbiol,[‡,¶] Cesar Magen,[§] Peter Krogstrup,[‖] Eleonora Russo-Averchi,[†] Martin Heiss,[†] Gabriel Mugny,[†] François Morier-Genoud,[⊥] Jesper Nygård,[‖] Joan Ramon Morante,[#,∇] and Anna Fontcuberta i Morral[*,†]

[†]Laboratoire des Matériaux Semiconducteurs, Ecole Polytechnique Fédérale de Lausanne, 1015 Lausanne, Switzerland

[‡]Institució Catalana de Recerca i Estudis Avançats (ICREA) and Institut de Ciència de Materials de Barcelona, ICMAB-CSIC, E-08193 Bellaterra, Catalonia, Spain

[§]Instituto de Nanociencia de Aragon-ARAID and Departamento de Física de la Materia Condensada, Universidad de Zaragoza, 50018 Zaragoza, Spain

[‖]Nano-Science Center, Niels Bohr Institute, University of Copenhagen, 2100 Copenhagen, Denmark

[⊥]Laboratoire d'Optoelectronique Quantique, Ecole Polytechnique Federale de Lausanne, 1015 Lausanne, Switzerland

[#]Catalonia Institute for Energy Research, IREC, 08930 Sant Adrià del Besòs, Spain

[∇]Department d'Electrònica, Universitat de Barcelona, 08028 Barcelona, Spain

S *Supporting Information*

ABSTRACT: In this paper we introduce a new paradigm for nanowire growth that explains the unwanted appearance of parasitic nonvertical nanowires. With a crystal structure polarization analysis of the initial stages of GaAs nanowire growth on Si substrates, we demonstrate that secondary seeds form due to a three-dimensional twinning phenomenon. We derive the geometrical rules that underlie the multiple growth directions observed experimentally. These rules help optimizing nanowire array devices such as solar or water splitting cells or of more complex hierarchical branched nanowire devices.
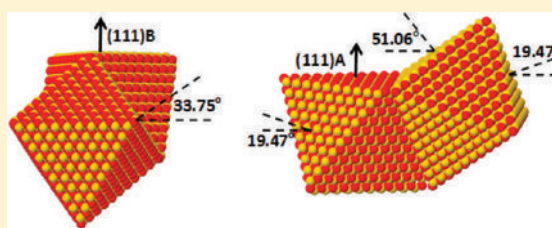
The integration of III−V nanowires (NWs) on silicon and germanium has excited a whole area of research and technology as it enables the integration of highly functional materials on the CMOS platform.[1−7] Although the self-organized growth of III−V NWs on silicon has been intensively studied in the last years,[8−12] important issues that concern the polarity mismatch between III−V NWs and the group IV substrate remain unsolved. The pioneering works of Atwater and Lewis show that nanowire arrays are at the forefront of solving the renewable energy challenge of the 21st century.[13,14] Unfortunately, defects such as nonvertical NWs occur often and result in the deterioration of the performance of nanowire array devices such as solar cells since the nonvertical nanowires provide undesired leakage paths.[15] Only with a fundamental understanding of the elementary processes occurring at the initial stage of nanowire growth it will become possible to obtain a completely successful integration of III−V nanowires on group IV substrates. It has been predicted[16] and recently demonstrated[17,18] that NW growth is 2D nucleation limited at the liquid−solid interface[6] and that the nucleation takes place preferentially at the triple phase line. Consequently, the growth dynamics are highly dependent on changes in the morphology of the liquid phase,[19] which determines

not only whether the structure becomes wurtzite or zinc blende[20] but also why kinking and crawling phenomena occur.[21−23] Twinning has also been revealed as an important issue, as it can lead to crystalline phase change and kinking.[24−26] The consequences for the electronic transport of the existence of twinning and a mixture in crystal phase have been demonstrated.[27] The existence of crystallographically equivalent twin boundaries with opposite polar bonding across the interface would lead to even stronger perturbations of electronic structure of the material.[28] However, the issue of polarity conservation across the twin has only been raised occasionally, mainly due to the difficulties in its determination.[29]

Orthodox theories assume that the initial stage of vapor−liquid−solid (VLS) growth of nanowires takes place at the liquid−solid interface forming a monocrystalline seed.[17] This phenomenon is consistent with the growth of nanowires in epitaxial relation with the substrate. However, nanowires grown in other directions always appear, especially when III−V materials
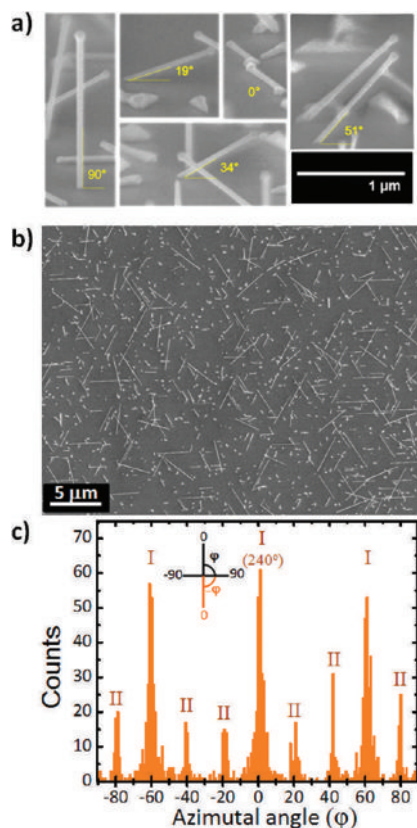
Figure 1. (a) Cross-section scanning electron micrographs of GaAs nanowires growing in different angles with respect to the substrate surface. Nanowires formed with 90° angle, results from the growth from a single crystalline seed with B polarity (As terminated), while the 19° growth direction results from the growth from a single crystalline seed with A polarity (Ga terminated). The rest of growth directions can be explained with multiple order twinning: the 0° angle is a result of multiple 3D twinning on a seed with B polarity, while 34 and 51° originate from a second order twinning with seeds exhibiting B and A polarity, respectively. (b) Planar view of a field of nanowires grown under V/III ratio of 30. The multiple orientations of the nonvertical wires are clear. (c) Histogram of the nonvertical nanowire orientations found from the analysis of 500 nanowires grown under the same conditions as in (a) and (b). The occurrence of different directions is quantized, in agreement with our 3D twinning theory.

are grown on group IV materials such as silicon or germanium.[30,31] Following the orthodox theory, for self-catalyzed nanowires growing always in the [111]B direction, only two types of growth orientations should be observed when grown on group IV (111) substrates. For a single seed with B polarity, i.e., an As terminated (111) surface, the nanowires should always grow vertically at 90° with respect to the substrate surface. For a single seed with A polarity, i.e., a Ga terminated (111) surface, nanowires should turn into a growth direction of 19.47° from the substrate (see S1 in Supporting Information). Our results shown here question the single crystalline nature of the seed assumed so far and impose a paradigm shift of nanowire growth. Here we present an explanation and experimental evidence of a manifold of growth directions, which are typically found to occur and which
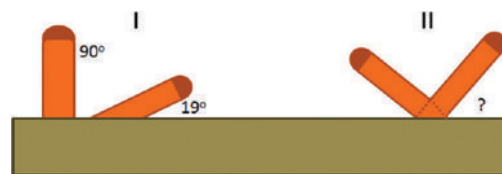
Figure 2. Schematics of the two types of growth obtained. Type I refers to the cases where a direct crystallographic relation between the nanowire growth direction and the substrate is found and type II when three-dimensional twinning is found. We draw the case in which two nanowires grow from the same point (like in Figure.3), but this does not have to be the case for type II.

are not in direct epitaxial relation with the substrate (cf. Figure 1). Using aberration corrected high angle annular dark field (HAADF) scanning transmission electron microscopy, we observe the polarity of the nanowire structures and the occurrence of 3D twinning at the initial stage of GaAs nanowire growth provoking nonepitaxial growth relations with the Si substrate. The results are general to the III−V semiconductor family and could potentially be extended to other substrates than silicon.

GaAs nanowires were grown on a 2 in. Si(111) undoped substrate by the gallium-assisted method[32,33] using a DCA P600 MBE machine. The wafers were transferred directly from the wafer box to the MBE machine without any removal of the native oxide. Prior to growth, the substrates were degassed at 770 °C for 30 min. The nanowires were obtained under rotation of 7 rpm at a temperature of 620 °C under a flux of Ga equivalent to a planar growth rate of 0.3 Å/s. The V/III ratio was varied between 15 and 60. The Ga and As fluxes were opened at the same time. We used reflection high-energy electron diffraction (RHEED) in situ for the detection of the nanowire nucleation, which corresponds to the onset after which electron diffraction signal from the nanowires is obtained. This corresponds to a size of the nucleation seeds of 10−20 nm. The morphology of the samples was characterized by scanning electron microscopy (SEM). After cross sections were prepared with a focused ion beam, the structure was investigated by aberration corrected high angle annular dark field (HAADF) scanning transmission electron microscopy (STEM) imaging. 3D atomic models have been obtained by using the Rhodius software package.[34]

Figure 1a contains representative cross-section scanning electron microscopy (SEM) images of nanowires grown on Si(111) under a V/III ratio of 30. Under these conditions we find that 53% of the nanowires grow vertically and about 6% with a 19° angle growing away from the substrate and 6% with a 19° angle growing toward the substrate (the growth then often stops leading to the formation of a triangular object or it continues further following the substrate surface). Interestingly, we find that 41% of the nanowires grow in other directions that are quantized. The growth angles, which are different from 90, 19, or −19° (e.g., 34° or 51°), are inconsistent with the crystallography of a single seed. The occurrence of quantized families of angles can be observed in a more precise way in a planar view SEM image of a nanowire field, such as the one shown in Figure 1b. Typically, one would expect the nonvertical wires would form families of angles separated by 120°. Clearly, in Figure 1b one observes many more of them. In Figure 1c, we show the histogram of the NW orientations computed from −90 to 90° (Figure 1c). We find nine quantized orientations separated by
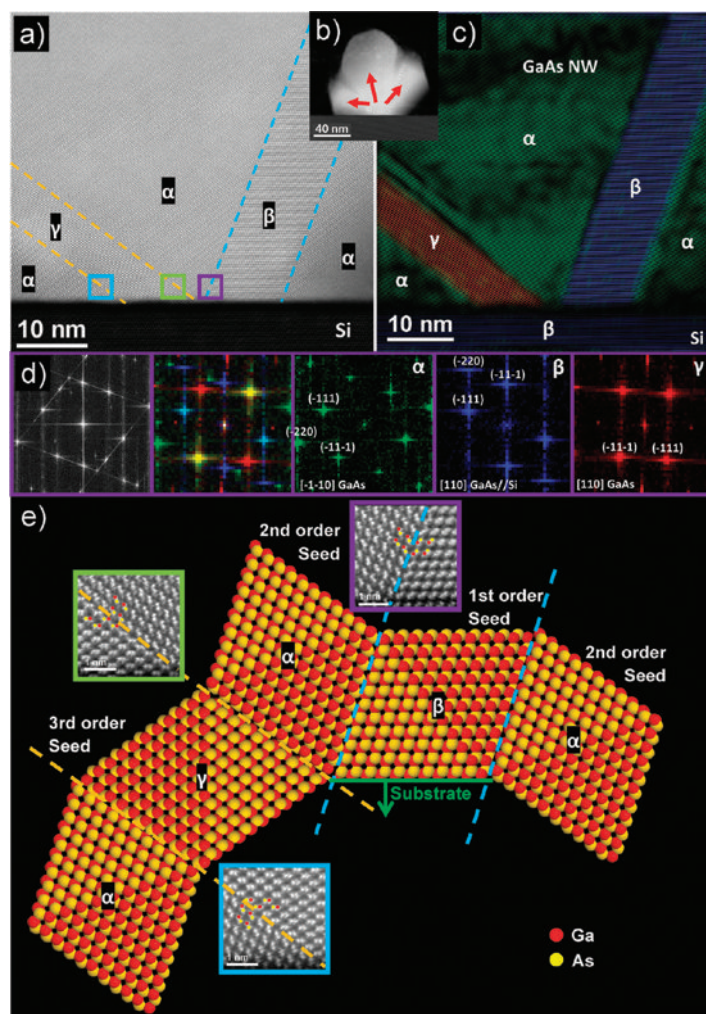
Figure 3. (a) Atomic HAADF STEM micrograph of the initial stages of GaAs nanowires exhibiting a multiple crystalline seed structure. (b) Low magnification TEM image of the sample, showing the three nanowire growth directions. (c) Visualization of the different crystal orientations by coloring them according to their characteristic frequency spots in the power spectra. For clarity, we show the filtered images. (d) Power spectra obtained in each of the crystalline regions of α, β, γ. (e) Simulation of the atomic positions of the crystalline regions of α, β, γ, showing the direction of the twinning and formation of secondary octahedral. The red and yellow spheres correspond to Ga and As atoms, respectively. The polarity analyses have been performed in detail in each of the twin boundaries (for more details see S2, Supporting Information). We find twins always perpendicular to the nanowire growth axis, and we never observe a change of the polarity (orthotwins).

about $\pm 19°$ from the three main peaks, instead of the three expected originally. As will be shown in the following, these angles can only be explained with the formation of multiple seeds at the initial stages of the nanowire growth, a consequence of a 3D twinning phenomenon. Experimental evidence and theoretical details of this model are presented here below.

Before we proceed with the understanding of this phenomenon and for the sake of clarity, we draw schematically the occurrence of these two types of growth in Figure 2. The nanowires labeled as type I correspond to the ones for which there is a clear crystallographic relation between the growth direction and substrate. These are nanowires that grow perpendicularly with the substrate (seed nucleating with B polarity) and with a 19° angle (seed nucleating with A polarity). For nanowires type II,

such relation is not clear. As it will be shown in the following, for a clear understanding of the occurrence of these other angles, one needs to analyze in great detail the crystallography at the initial phases of growth.

To discover the underlying mechanism for the different growth angles, it has been key to analyze the crystalline phase of a group of nanowires growing from the same stem and branching toward distinctly different directions (Figure 2). STEM-HAADF imaging was performed on a probe aberration corrected microscope (FEI Titan 60−300 kV), which allows us to analyze the elemental composition at the atomic level. A polarity analysis of the different branches of the NW seed,[35] has to our knowledge not been reported before. In Figure panels a and b of 3, we show the existence of different grains in the seed, separated by twins at
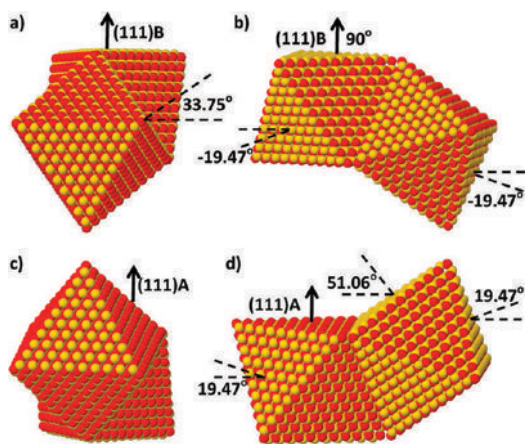
Figure 4. 3D atomistic models of the structures obtained when secondary crystalline seed forms from 3D twinning in one of the (111)B facets of an individual crystalline seed exhibiting either B (a, b) or A (c, d) polarity. The formation of secondary seeds opens up the possibility of other growth angles than the ones expected from a single crystalline seed (90 and 19.47°), such as 33.75 and 51.06°.

{111} planes. The corresponding interface exhibits 34 or 71° with respect to the surface, giving rise to other grains, which we denote α, β, or γ, depending on the orientation with respect to the substrate. The power spectra of these zones obtained by calculating the fast Fourier transform (FFT) are shown in the middle of the figure, indicating the orientations. For clarity, we have marked each of the grains with different colors by using frequency filtering in the FFT. Please note that neighboring grains share at least one common (111) plane. To indicate this, we use the color "green" when "yellow" and "blue" orientations are combined as marked in the respective FFTs. Given the three-dimensional aspect of the seeds, it is not straightforward to obtain the spatial orientation of the planes from an image projection from HAADF-STEM. Note that STEM is a technique with a low focus depth, typically 5−10 nm. As will be shown in the following, three-dimensional modeling of the structure is necessary for the interpretation of the measurements. Grain β exhibits a B polarity and it is the only to have an epitaxial relation with the Si substrate. The nanowire branches also grow following the B polarity, as expected from self-catalyzed GaAs nanowires. Surprisingly, although the [111]B growth direction is preserved, some of the NWs take other angles than what one would expect from a monocrystalline seed.

As we will see, twinning and further growth on the lateral facets results in the formation of secondary (multiple-order twinning) seeds that enable other [111]B crystal orientations. Its origin is related to the very first steps of the nanowire growth. The grains α on the left and right of Figure 3a−c exhibit a 180° rotation along the [−111] direction with respect to β. This corresponds to the formation of a twin that conserves the polarity of the structure. From this twin a new crystal grain grows from the preferred [111]B direction; see Figure 1. Now, the {111}B type facets exhibit a different position in space than the original seed. The formation of the secondary grain allows the nanowires to grow in the directions of 34° and 51° (see Figures 2 and 4). A further twin in the grain α leads to the grain γ, separated by a twin that has an angle of 34° with the substrate.

The possibilities of creating new surfaces are extremely large as they can increase by the creation of further seed crystals attached. One can predict the novel growth directions by obtaining the mirror image of the original seed along the twin plane and conserving the polarity of the crystal along the direction perpendicular to the twin. This operation is mathematically expressed by combining the Householder reflection matrices corresponding to the four (111) planes with an inversion operation with respect to the origin

$$T_{(111)} = \begin{pmatrix} -1 & 2 & 2 \\ 2 & -1 & 2 \\ 2 & 2 & -1 \end{pmatrix},$$

$$T_{(1\bar{1}\bar{1})} = \begin{pmatrix} -1 & -2 & -2 \\ -2 & -1 & 2 \\ -2 & 2 & -1 \end{pmatrix},$$

$$T_{(\bar{1}1\bar{1})} = \begin{pmatrix} -1 & -2 & 2 \\ -2 & -1 & -2 \\ 2 & -2 & -1 \end{pmatrix},$$

$$T_{(\bar{1}\bar{1}1)} = \begin{pmatrix} -1 & 2 & -2 \\ 2 & -1 & -2 \\ -2 & -2 & -1 \end{pmatrix}$$
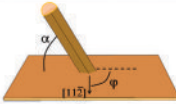
The growth orientations resulting from n-fold 3D twinning are obtained by multiplication of n times of all combinations of the matrices T_j with the [111]B directions, d_i, of the initial seed:

$$t_{i,j} = T_j d_i \tag{1}$$

Seeds nucleating with A and B polarity with respect to the silicon surface have to be considered separately, and we suppose that polarity is conserved upon twinning. The angles that define the resulting growth directions are: α, the angle with respect to the surface and φ, the angle with the in plane direction ⟨11−2⟩ when observed in planar view (from top). The calculated angles for all ⟨111⟩B growth directions that are pointing out of the substrate surface are summarized in Table 1 up to the formation of a fourth order twinning phenomenon, for seeds with both a (111)B and (111)A polarity. We start by discussing the angles resulting from a single seed. For seeds nucleating with the (111)B polarity, vertical growth is obtained by following the direction of the nucleation seed. In this case, α is 90° and there is no φ defined. If now one considers the three lateral (111)B planes of the octahedral seed, we obtain three possible growth directions with α = −19.47°. Each one of these three lateral facets will exhibit one of the planar angles with $\varphi = 60°$, 180°, and 300°. In contrast to this, considering a seed with a (111)A oriented octahedron, vertical growth is not possible. There are three lateral (111)B facets facing up at 19.47° versus the horizontal from the substrate with $\varphi = 0°$, 120°, and 240°, respectively. For higher order 3D twinning, the options for growth directions increase in a potential way.

By measuring α and/or φ, it is possible to identify the three-dimensional twinning type. The origin of the growth angles different than 90, 19.47, or −19.47° (e.g., 34° or 51°) is inconsistent with the crystallography of a single seed and can only be explained with a 3D twinning phenomenon. For example, the α = 34

Table 1. Orientation of the Nanowires Depending on the Nucleation Polarity and the Type of Facet Leading to Growth (top or lateral)[a]

	Seed type	α	φ in-plane angles to [11-2],[1-21],[-211]			
1st order	A	19.47	60.00			
	B	90.00	-			
2nd order	A	19.47	0.00			
	B	33.75	19.11	-19.11		
	A	51.06	0.00			
3rd order	A	2.12	33.00	-33.00	5.21	-5.21
	B	24.04	36.59	-36.59		
	B	33.75	40.89	-40.89		
	A	51.06	60.00			
	B	58.41	60.00			
	A	67.81	13.90	-13.90		
4th order	A	2.12	27.00	-27.00	-54.79	54.79
	B	3.54	29.00	-29.00	44.18	-44.18
	B	12.12	0.00		38.21	-38.21
	A	13.57	8.95	-8.95		
	A	22.50	40.89	-40.89		
	B	24.04	23.41	-23.41		
	A	32.06	27.64	-27.64	45.54	-45.54
	B	40.87	28.68	-28.68	53.11	-53.11
	B	53.37	54.18	-54.18		
	A	55.81	15.61	-15.61	53.82	-53.82
	B	58.41	0.00			
	A	67.81	46.10	-46.10		
	B	71.92	17.00	-17.00		

[a] α refers to the angle with the surface and φ to the angle with the equivalent ⟨11-2⟩ directions, which coincides with the projection of the [111] direction seen in a top view image. For a reference, a drawing of the angles on a substrate is shown.

and 51° angles correspond to second order seeds created by the 3D twinning. Also, we can come back to the histogram in Figure 1c. The three main peaks at 0 and ±60° correspond to nanowires growing in α = ±19.45°, from first generation seeds. The other quantized directions are mainly found at a distance Δφ of ±19° from the main peaks. According to Table 1, these angles correspond to nanowires growing from second generation seeds, with α = 33.75°. Although both the cross section and top view analysis are correct, the latter is much less subject to errors than cross-section measurements and allows for the realization of a statistical quantification in an easier way.

Finally, we discuss the occurrence of vertical, horizontal, and kinked nanowires as a function of the growth conditions. We find that the primary reason for the various nanowire orientations is related to the change in the size of the Ga droplet at the initial stage of the nanowire growth. We observe that by varying the V/III ratio from 15 to 60, with the Ga rate remaining the same, the incubation time varies from 2 min to 20 s. This increase in the nucleation time must result in a larger Ga droplet, meaning that changes in the relative size of the Ga droplet at the initial stages of growth can be controlled by varying the V/III ratio[20] and temperature. It is especially important to control the size of the Ga droplet at the initial stages of growth where the seed(s) is(are) being formed. The Ga droplet increases rapidly in size, favoring the formation of new {111} facets. In the case of a multiple-order twinned seed, the droplet can fall over to the side and be kinked. Even horizontal growth can occur. We find that lowering the V/III ratio results in a broadening of the histograms due to the occurrence of third order twinning, while on increasing the V/III ratio to 60 the second order twinning disappears (see S3, Supporting Information). To prohibit multiple-order twinning, it is therefore key to implement a high V/III ratio at least at the initial stage of growth and to keep the droplet size small enough. Very preliminary experiments indicate that 100% vertical wires are obtained when the Ga droplet is as small as ~10 nm.

In conclusion, we have found that polycrystalline seeds can occur at the initial stages of nanowire growth. The polycrystalline seed is formed by a three-dimensional twinning process. By taking into account the polarity, we deduce the geometrical rules leading to multiple-order 3D twinning, which are consistent with experimental results. These results are important for the reproducible integration of self-catalyzed III−V nanowires on group IV substrates. Moreover, this work opens the avenue for controlling the degree of complexity of nanowire networks. The understanding provided here gives a clear pathway of how to obtain fully vertical nanowire arrays, which would dramatically improve nanowire array devices such as solar or water splitting cells. Additionally, it shows how more complex branched nanowire structures could be grown, which can be useful for other

applications such as interconnected nanoelectronic devices or cell cultures.[36]

■ ASSOCIATED CONTENT

S **Supporting Information.** Polarity of single seeds and consequences for the orientation of self-catalyzed nanowires, detailed analysis of the polarity of the nanowires and at the twin interface, and statistical analysis of the nanowire orientation as a function of the V/III ratio. This material is available free of charge via the Internet at http://pubs.acs.org

■ AUTHOR INFORMATION

Corresponding Author
*E-mail: anna.fontcuberta-morral@epfl.ch.

Author Contributions
¶Equal contribution.

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PAPER

Suppression of three dimensional twinning for a 100% yield of vertical GaAs nanowires on silicon†

Eleonora Russo-Averchi,*[a] Martin Heiss,[a] Lionel Michelet,[a] Peter Krogstrup,[b] Jesper Nygård,[b] Cesar Magen,[c] Joan Ramon Morante,[de] Emanuele Uccelli,[a] Jordi Arbiol[f] and A. Fontcuberta i Morral[a]

Multiple seed formation by three-dimensional twinning at the initial stages of growth explains the manifold of orientations found when self-catalyzed GaAs nanowires grow on silicon. This mechanism can be tuned as a function of the growth conditions by changing the relative size between the GaAs seed and the Ga droplet. We demonstrate how growing under high V/III ratio results in a 100% yield of vertical nanowires on silicon(111). These results open up the avenue towards the efficient integration of III–V nanowire arrays on the silicon platform.

A Introduction

The defect-free growth of III–V materials on silicon substrates would allow the integration of optoelectronic devices with CMOS technology, as well as the possibility of increasing the efficiency-to-cost ratio in solar cells.[1,2] The challenge of combining these two platforms is a consequence of: (a) the lattice-mismatch between III–Vs and silicon, and (b) the formation of anti-phase boundaries due to the mismatch in polarity between III–Vs and silicon. This area has gained a renewed interest, thanks to the possibility of obtaining defect-free III–V nanowires (NWs) on silicon or even germanium.[3–9] Although the self-organized growth of III–V NWs on silicon has been intensively studied in the last few years,[10–14] important issues such as those concerning the polarity mismatch between III–V NWs and the group IV substrate remain unsolved.

Recently, we have shown that multiple seed formation by three-dimensional twinning is responsible for the existence of a manifold of quantized orientations in self-catalyzed GaAs nanowires grown on silicon.[15] In this manuscript, we provide a detailed study about the occurrence of three-dimensional twinning with respect to the growth conditions. These results bring the necessary understanding for controlling the degree of complexity in nanowire arrays. In particular, we demonstrate the procedure by which a full yield of vertical GaAs nanowires can be obtained. This development is of great importance, as 100% yield vertical nanowires would for example avoid shortcuts in nanowire based solar cells or water splitting devices.[16,17]

B Experimental

Self-catalyzed GaAs nanowires were obtained on an undoped 2″ Si(111) substrate by the gallium-assisted method, in which a surface oxide is used to nucleate Ga droplets for the nanowire growth[18,19] using a DCA P600 MBE machine. The substrate temperature was previously calibrated by measuring the phase transition of the surface reconstruction of Si(111) from (7 × 7) to (1 × 1) at 830 °C.[20] The experiment is performed under an As partial pressure in the chamber below 10^{-13} Torr since an As exposure of the surface leads to a more stable Si(111):As (1 × 1) surface. The wafers were introduced directly in the MBE machine without any surface treatment or removal of the native oxide. Prior to growth, the substrates were degassed at 770 °C for 30 min. The nanowires were obtained under a rotation of 7 rpm at a temperature between 620 and 645 °C under a flux of Ga equivalent to a planar growth rate of 0.3 Å s⁻¹. The V/III beam equivalent pressure (BEP) ratio was varied between 15 and 60. The grown samples were then analysed by scanning electron microscopy (SEM) and aberration corrected high angle annular dark field (HAADF) scanning transmission electron microscopy (STEM).[21] 3D atomic models have been obtained by using the Rhodius software package.[22]

[a]*Laboratoire des Materiaux Semiconducteurs, Ecole Polytechnique Federale de Lausanne, 1015 Lausanne, Switzerland. E-mail: anna. fontcuberta-morral@epfl.ch; Fax: +41 21 693; Tel: +41 21 693 73 94*

[b]*Nano-Science Center, Niels Bohr Institute, University of Copenhagen, 2100 Copenhagen, Denmark*

[c]*Instituto de Nanociencia de Aragon-ARAID and Departamento de Física de la Materia Condensada, Universidad de Zaragoza, 50018 Zaragoza, Spain*

[d]*Catalonia Institute for Energy Research, IREC, 08930 Sant Adrià del Besòs, Spain*

[e]*Department d'Électrònica, Universitat de Barcelona, 08028 Barcelona, Spain*

[f]*Institució Catalana de Recerca i Estudis Avançats (ICREA) and Institut de Ciència de Materials de Barcelona, ICMAB-CSIC, E-08193 Bellaterra, CAT, Spain*

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C Results

We start by presenting the occurrence of different growth orientations with respect to the substrate as a function of the growth conditions. Fig. 1 shows the SEM images of nanowires obtained under a V/III BEP ratio of 15, 30 and 60. The images have been taken at an angle of 30°. Nanowires grow directly on the substrate, with very little parasitic growth between them.[23] At the end of each nanowire, there is a gallium droplet leading the growth. We observe nanowires perpendicular to the substrate in all conditions. We also find many other orientations, especially for low V/III ratios. Particularly at the lowest ratio (V/III BEP = 15), we find many nanowires growing parallel to the substrate. As we increase the V/III ratio, the proportion of horizontal (crawling) nanowires decreases and is nearly null at a V/III BEP ratio of 60. A similar behaviour is observed for the other non-perpendicular orientations; they tend to be reduced for the higher V/III ratio but are still not zero at a V/III ratio of 60.

We have realized a quantitative statistical analysis of occurrence of the observed orientations. For this, we have combined cross-sectional and top view SEM measurements. As we have shown in our previous work, the analysis of the planar view allows us to realize a fast and reliable statistics on the occurrence of various angles. However, one of the disadvantages is that certain orientations cannot be distinguished unambiguously.
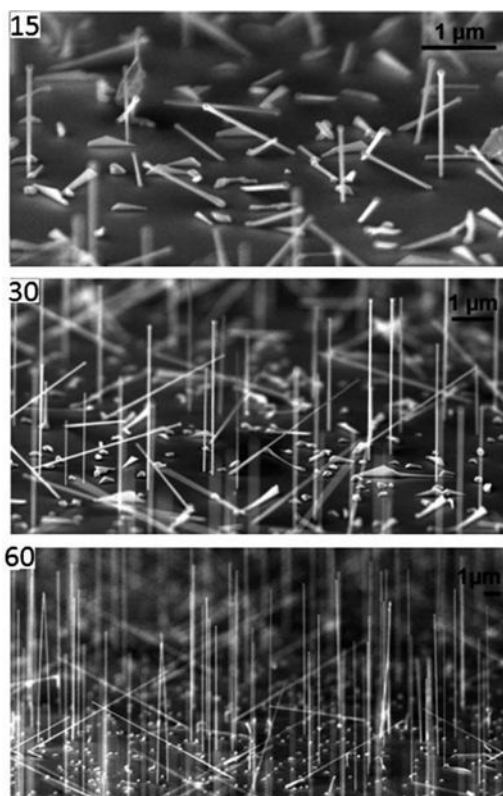
This is the case for nanowires growing with a ±19° and 51° angle with the substrate. The histogram of orientations with respect to the surface for the three different growth conditions is shown in Fig. 2. We find six discretized orientations at angles: 0, ±19, 34, 51 and 90°. The occurrence of the particular angles different from 19 and 90° is a consequence of the formation of multiple seeds at the initial stages of growth combined with a 3D twinning phenomenon.[15] Several 3D animated atomic simulations of the growth mechanisms implying first and second order twinning can be found elsewhere.[24]

In order to understand the relative occurrence of the different orientations as a function of the growth conditions, start by recalling the structural relationship of the 111B orientations with respect to the underlying substrate. If nucleation takes place with a B polarity at the liquid–solid interface the NW will grow vertical to the substrate if no 3D twinning takes place. However if the droplet increases in size and expands beyond the top facet, 3D twinning will naturally take place in order to minimize the free energy and new 111B growth directions will start forming. Nanowire growth parallel to the substrate (0°) can be thought of as those which started from a GaAs B-polarized seed in the −19° 111B orientation and did not stop at the substrate surface but instead managed to continue growing crawling *via* a high order multiple twinning mechanism. For this reason we have put the −19° and 0° together in the histogram. A seed nucleating with A polarity results in a nanowire growing at 19° if it is free of 3D twinning. The angles 34° and 51° correspond to nanowires whose seeds have experienced a single 3D twinning phenomenon (marked II in the graph). The difference between them is the polarity in the nucleation, which is respectively B and A. We also observe one orientation typical of second order twinning after nucleation with A polarity, corresponding to nanowires marked with III_A. Finally, all wires growing perpendicular to the substrate (90°) exhibit B polarity with respect to the substrate

Fig. 1 Representative SEM micrographs of a field of nanowires grown at 620 °C under a V/III BEP ratio of 15, 30 and 60. The percentage of vertical nanowires increases.
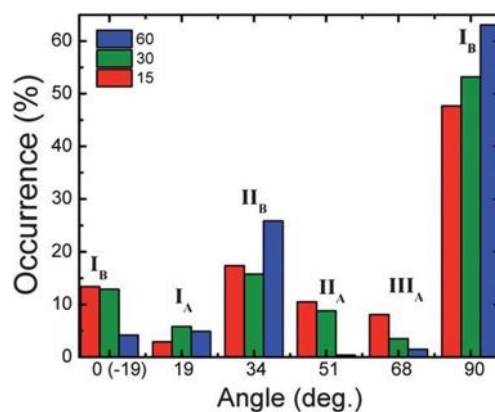
Fig. 2 Statistical analysis of the orientations of the nanowires with respect to the silicon surface as a function of the V/III BEP ratio. The labels I, II and III correspond respectively to first order nanowire growth and growth from second or third order seeds resulting from 3D twinning. The labels A and B refer to the polarity of the initial seed in contact with the substrate. The nucleation of seeds with A polarity decreases as the V/III BEP ratio is increased. Angles 0 and −19° are grouped together because crawling NWs start by growing towards the surface at −19°.

and have not suffered any 3D twinning phenomenon. From the results presented in the histogram, we deduce the general trend that the increase of the V/III BEP ratio results in the decrease of multiple twinning phenomena. Interestingly, we also find an important reduction in the initial seeds with A polarity. We speculate that the polarity of the initial seed might be linked to the time necessary for the formation of the seed. It seems that B polarity is favoured when this incubation time is reduced. This interesting phenomenon would require further theoretical investigations. Overall, we find an increase in the percentage of vertical wires, from 48 to 63%. Still, at the highest ratio the proportion of vertical nanowires is not 100%.

D Discussion

The characteristics of the seed formed in the initial stages of growth are intimately linked to the occurrence of orientations with respect to the substrate.[15] In the following, we try to elucidate the processes occurring in the initial stages of growth. We start by presenting a cross-section aberration corrected HAADF STEM micrograph of a nanowire and the substrate (Fig. 3). The interface of the nanowire and the substrate is not flat and abrupt. In fact, the GaAs penetrates about 5 nm inside the Si substrate. The interface at the bottom of this nanoscale hole is flat (parallel to the (111) orientation of the substrate). By analyzing the composition of the GaAs dumbbells at the GaAs/Si interface, we find that the polarity at the nucleation is B type (Fig. 3c and d). This is in agreement with the fact that this particular nanowire

grows perpendicularly to the substrate and has not suffered any 3D twinning phenomenon.[15] We find the strain coming from the mismatch between GaAs and Si is released in the interface at the pinhole, allowing GaAs to grow perfectly relaxed (Fig. 3e).

The formation of these nanoscale holes is not particular of the nanowire orientation, we have also observed it in nanowires growing in other directions (Fig. 3f and h). The size and morphology are in all cases quite similar. We believe that the formation of this nanoscale hole is related to the initial stages of growth in the following way: first, gallium gathers on the native silicon oxide forming droplets. Then, gallium pins at some defect of the native silicon oxide and reacts forming a highly volatile gallium oxide and silicon:[25]

$$SiO_x + Ga \rightarrow Ga_xO_y (\uparrow) + Si$$
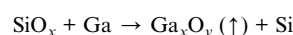
As silicon is soluble in Ga at the growth temperature (1%),[26,27] gallium starts to dissolve the silicon thereby forming a nanoscale hole. By taking into account the solubility of Si in Ga, one can calculate that a 3 nm deep and 10 nm wide hole in the silicon can be obtained by the dissolution of a Ga droplet with a radius of 36 nm. This small calculation already hints at the possibility of having the Ga droplet larger than the initial GaAs seed. Finally upon supersaturation of the gallium droplet with As, growth starts at the interface with the substrate. For illustration, we have represented these steps in Fig. 4.

Given the picture of the initial stages presented here, one can try to depict in a qualitative way the role of the V/III ratio in the occurrence of 3D twinning. The first element to consider is the relative size between the Ga droplet and the GaAs seed. Indeed, as the V/III ratio is increased we might pass from a situation in which the Ga droplet covers completely the seed to the situation where it is just covering the top surface. Let us examine these two opposite cases, schematically drawn in Fig. 5a and b. Fig. 5c shows a model for the formation of horizontal (crawling) NWs ($-19°$, $0°$) by following the growth mechanism proposed in (a) (initial octahedral seed). In Fig. 5d we show the growth mechanism for the formation of 34° NWs after a 3D twinning mechanism at the 2nd order.[28]

Let us consider what would be the shape of the seed with the minimal energy in each of the cases. Following Wulff's theory,[29] the equilibrium shape of the seed is given by the intersection of the lowest energy surfaces in the so-called 'gamma-plot'. It is not straightforward to apply Wulff's theory to solid–liquid systems out of equilibrium, but we can say that the thermodynamic driving force (the free energy change upon solidification per atom) is the greatest towards the corresponding 'Wulff shape' of the liquid–solid system. The system tends to form {111}B liquid–solid interfaces because this is the lowest free energy
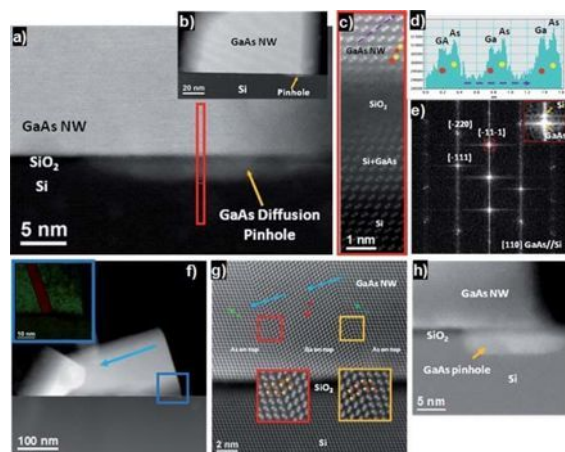
Fig. 3 (a and b) Cross-sectional aberration corrected HAADF STEM micrographs of a vertical nanowire, showing the formation of a nanoscale hole inside the silicon substrate; (c) magnified atomic resolution view of the red selected area in (a); (d) intensity profile obtained along the purple dashed arrow in (c); (e) power spectrum at the basis of the nanowire shows that the GaAs is completely relaxed; (f) cross-section aberration corrected HAADF STEM micrographs of a horizontal nanowire (-19 deg); the inset shows the formation of a twin boundary perpendicular to the growth direction; (g) magnified detail of the twinned area, polarity is kept along the twin boundaries; and (h) magnified detail of the pinhole region. Note that the final diameter of the nanowire is larger than the original pinhole because of the non-zero radial growth rate.
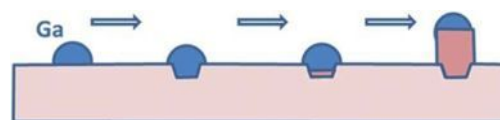
Fig. 4 Schematics of the initial stages of the Ga-assisted growth on a silicon substrate. The Ga droplet first pins on the substrate and, after dissolution of the native oxide, it dissolves the silicon forming a nanoscale hole. Upon saturation of the Ga droplet, the GaAs nanowire growth starts.

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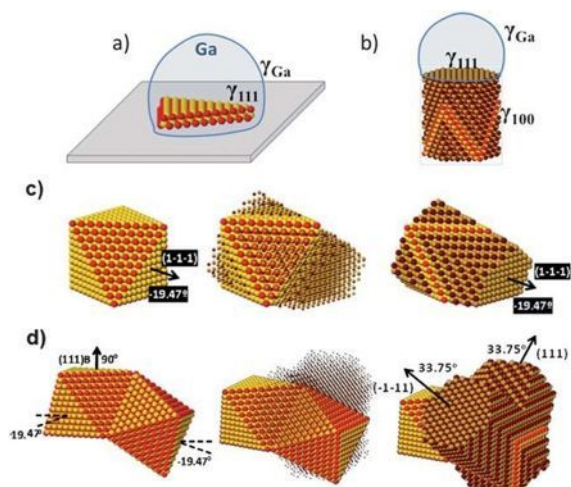
Fig. 5 Two different hypothetical case scenarios for the initial stages of nanowire growth. (a) For a low V/III ratio the Ga droplet covers the whole GaAs seed, thereby enabling the formation of octahedral seeds exhibiting (111) type of facets. (b) When the V/III ratio increases, the Ga droplet does not cover the totality of the GaAs seed, only the top (111) surface. In this case a hexagonal prism is energetically favorable. (c) Example of horizontal NW growth following the growth mechanism proposed in (a). (d) Growth mechanism following a second order twinning. See also the following link for 3D atomic animated simulations of the different twinning growth mechanisms: http://www.icmab.cat/gaen/research/160.

configuration of the system, however the choice of the 111B facet will depend on the relative size of the liquid phase. When the droplet is covering the seed and side facets, this is an octahedron. In the case where the Ga droplet is only covering the top surface of the seed, the most advantageous structure is composed of a top (111)B surface. The side facets which are not in direct contact with the Ga droplet pertain to the family {110}, as usually found experimentally.[30,31]

Now we turn to the important point of controlling the nanowire orientation with respect to the substrate. If we believe that the size ratio between the GaAs seed and the Ga droplet plays a role in the existence of multiple seeds, the substrate temperature could also be used for the further increase in the density of vertical nanowires. We have realized growths under a V/III BEP ratio of 60 at temperatures ranging between 620 and 645 °C. For our beam flux conditions the optimal substrate temperature is 645 °C. A typical SEM image of nanowires grown under a V/III BEP ratio of 60 and a temperature of 645 °C is shown in Fig. 6. Just with this small change in the growth conditions, we have obtained a 100% yield of vertical nanowires.

E Conclusions

We have presented a systematic study on the growth directions and occurrence of 3D twinning of MBE based Ga assisted growth of GaAs nanowires on silicon(111). We have shown how a small V/III ratio results in the existence of 3D twinning and a large percentage of discrete growth directions. We also
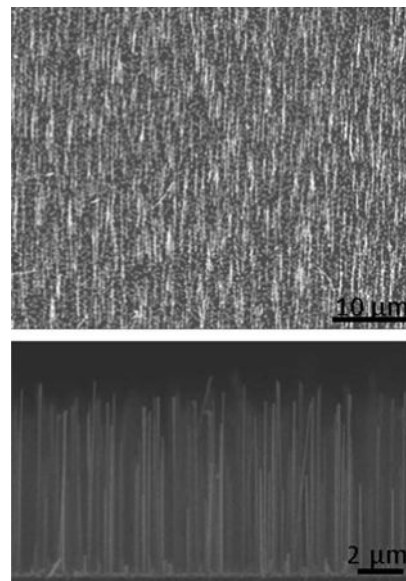
Fig. 6 Representative SEM micrograph of a field of nanowires grown at 645 °C under a V/III BEP ratio of 60 (top) and in cross-section (bottom).

demonstrate how a further optimization of the growth temperature results in a 100% yield of vertical nanowires.

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50

3.3 Ordered arrays of NWs

Publications:

III **III-V nanowire arrays: growth and light interaction**
M. Heiss[a], <u>E. Russo-Averchi</u>[a], A. Dalmau-Mallorqui[a], G. Tütüncüoglu[a], F. Matteini, D. Rüffer, S. Conesa-Boj, O. Demichel, E. Alarcon-Llado and A. Fontcuberta i Morral
[a] equal contribution
Nanotechnology 25 (2014) 014015

IV **Amorphous silicon mediates a high yield in GaAs nanowire arrays on Si obtained by the Ga-assisted method**
<u>E. Russo-Averchi</u>, J. Vukajlovic Plestina, G. Tütüncüoglu, A. Dalmau-Mallorqui, M. de la Mata, D. Rüffer, H.A. Potts, F. Matteini, J. Arbiol, S. Conesa-Boj and A. Fontcuberta i Morral
submitted

After the control of the NWs growth direction, a further step towards the fabrication of devices is the control of the arrangement of NWs on the silicon substrate. We achieved ordered growth on precise locations of Ga-assisted GaAs NWs and of InAs NWs grown by selective area epitaxy (SAE), as presented in paper III and IV.

A high yield of vertical InAs NWs on patterned silicon substrates has been obtained by carefully tuning the growth conditions. An overview of SEM images of samples grown on patterns with different geometries is shown in figure 3.3: we could achieve a good selectivity by optimizing the growth temperature. Indeed, the coverage of the mask oxide by InAs clusters is close to zero. The yield of vertical wires nucleating in the holes of the patterns is very high, ranging form 91 to 96%.

All the samples are characterized by a significant length variation of the NWs as a function of the inter-wire distance. In particular, we identify two regimes: (i) a competitive growth regime with shorter NWs for narrow inter-wires distances and (ii) a diffusion limited or independent growth regime for wider distances, as also found in literature [130–132]. The switch between the two regimes is determined by the indium surface diffusion length on SiO_2. This work represents a first step along a promising line of research where more activity is envisaged in the future for the team. As an example of further possible activity, InAs arrays are an optimal setting to study structural and functional properties of the NWs by Raman spectroscopy.

While InAs NWs in array are relatively straightforward to grow, GaAs NWs present many more challenges: many parameters, related both to the sample preparation and to the growth conditions, seem to be involved for the realization of a successful array with a high yield of vertical wires and as such they need to be carefully tuned. In particular, the cleaning steps, the thickness of the mask oxide and the Ga pre deposition seem to be key. InAs and GaAs NWs grow following two different growth mechanism: while InAs grows in the mask openings
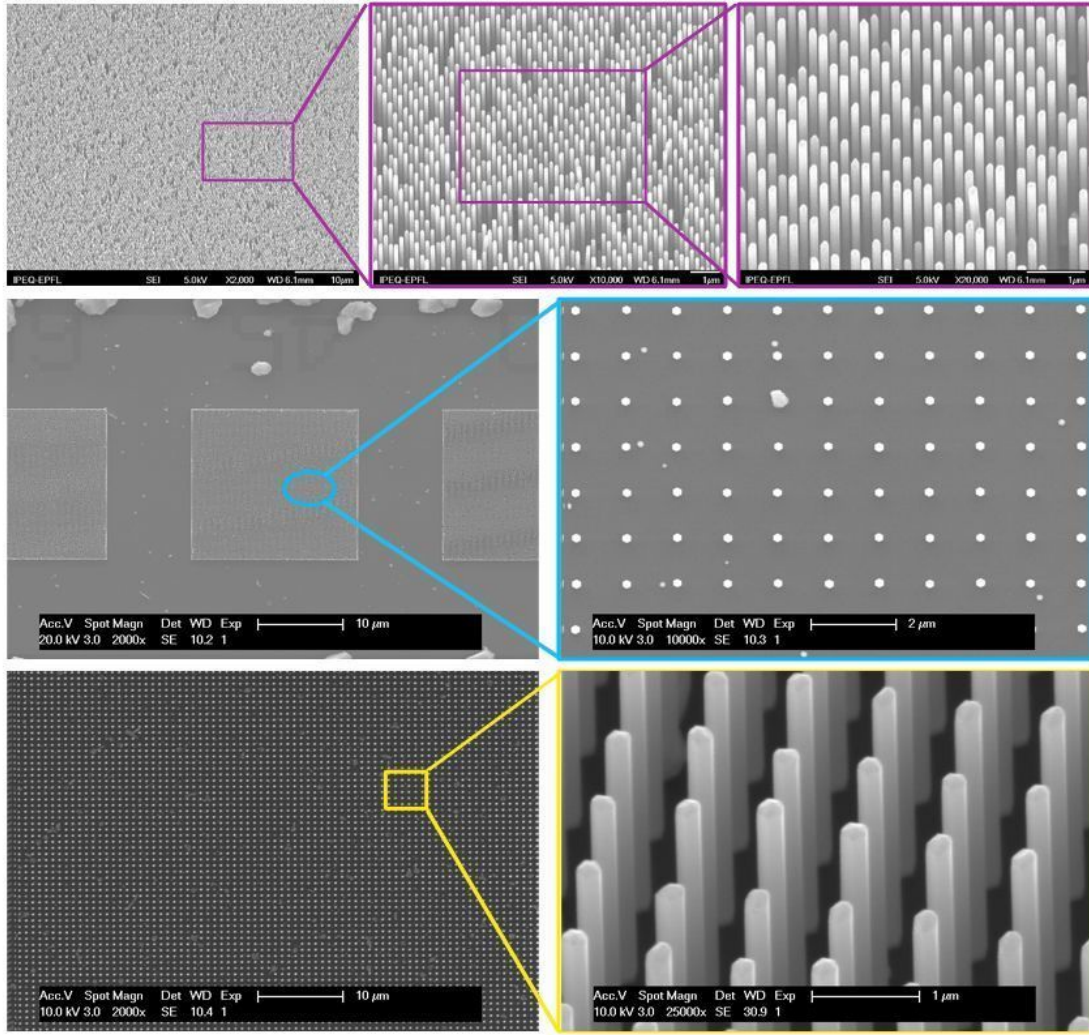
Figure 3.3: SEM micrographs of InAs NWs obtained on patterned silicon substrates. The images reveal the good selectivity and the high yield achieved by optimizing the growth conditions.

similarly to a 2D layer and only confined in the nanoscale holes, GaAs NWs require the initial formation of a Ga droplet. The lack of reproducibility in the growth of ordered arrays of GaAs NWs reported by several works, which we also encountered, gave us the hint to focus our attention on the shape of the Ga droplet and to its interaction with the silicon substrate.

Very recent results indicate that key parameters to achieve a high yield array are the size and contact angle of Ga droplet and their interaction with the exposed areas of the patterned substrate. Figure 3.4 (a) shows a successful array with 80% of GaAs NWs growing perpendicularly respect to the substrate. The NWs are uniform in length and diameter. The same growth conditions have been been used for the sample shown in Figure 3.4 (b). Here the yield of
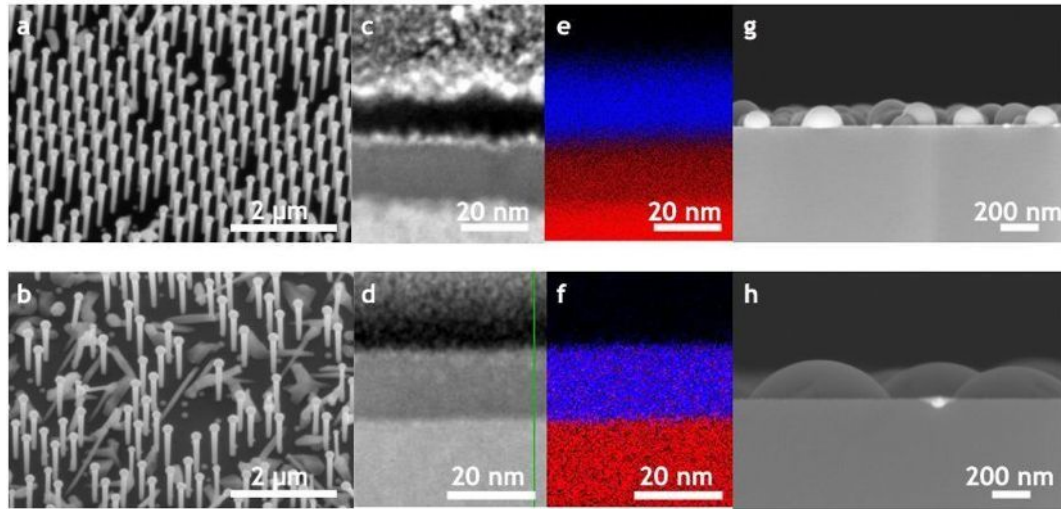
Figure 3.4: (a-b) SEM micrographs of GaAs NWs obtained on patterned silicon substrates. In (a) an amorphous silicon intermediate layer is present between the crystalline substrate and the oxide mask. The yield of vertical NWs is 80%. In (b) the thermal oxide layer is directly on top of the monocrystalline silicon. The yield of vertical wires is very low. HAADF images of the substrates (c-d) and corresponding EDX analysis (e-f), with the Si map in red and the O map in blue. The analysis is performed at the interface between the silicon substrate and the mask oxide. The presence of amorphous silicon in (a) and (c) is confirmed by the lack of oxygen in the EDX analysis. Cross sectional SEM images of Ga droplets deposited on amorphous silicon (g) and on crystalline silicon (h). The droplets have different sizes and contact angles depending on the surface.

vertical wires is very low. In both cases the substrate is Si(111) and the mask oxide is a thermal oxide layer obtained by dry oxidation. The key difference is a thin layer of amorphous silicon between the mask oxide and the crystalline substrate that is present only for the sample in (a). HAADF and energy-dispersive X-ray (EDX) analysis highlight the difference between the two sample, as reported in Figure 3.4 (c-f). This analysis has been performed in collaboration with Prof. Jordi Arbiol and Maria de la Mata at ICMAB, UAB Campus, Barcelona. The amorphous layer is also observed at the bottom of the nanoscale holes of the array, as it is not etched in the buffered hydrofluoric acid that we used to define the holes in thermal oxide mask. It is important to note that the amorphous silicon is completely crystallized after the degassing and growth steps, since its crystallization starts at temperatures higher than 500°C [183, 184].

Amorphous and crystalline silicon have different values of surface energies; as a consequence, wetting of Ga presents a different nature in the two cases. Ga droplets deposited on amorphous silicon before it crystallizes and on crystalline silicon are shown in Figure 3.4 (g-h): the Ga droplets obtained on what initially was amorphous silicon have a contact angle of 84±4°; the ones deposited on crystalline silicon have a contact angle of 52±3°. The Ga droplets deposited directly on crystalline silicon are also significantly larger than the ones observed on

amorphous silicon. While the droplet size and contact angle in the case of amorphous silicon substrate favor vertical nanowire growth, contact angles smaller than 90° make nucleation at the triple-phase line especially difficult [73].

These results suggest that the wetting properties at the open surface of the holes should be improved to achieve an optimal contact angle. The creation of an appropriate native oxide may also lead to the ideal conditions obtained with amorphous silicon. In general new perspectives for the rational and reproducible growth of GaAs nanowire arrays on silicon are opened.

III–V nanowire arrays: growth and light interaction

M Heiss[1], E Russo-Averchi[1], A Dalmau-Mallorquí[1], G Tütüncüoğlu[1], F Matteini, D Rüffer, S Conesa-Boj, O Demichel, E Alarcon-Lladó and A Fontcuberta i Morral

Laboratory of Semiconductor Materials, Ecole Polytechnique Fédérale de Lausanne, 1015 Lausanne, Switzerland

E-mail: anna.fontcuberta-morral@epfl.ch

Abstract

Semiconductor nanowire arrays are reproducible and rational platforms for the realization of high performing designs of light emitting diodes and photovoltaic devices. In this paper we present an overview of the growth challenges of III–V nanowire arrays obtained by molecular beam epitaxy and the design of III–V nanowire arrays on silicon for solar cells. While InAs tends to grow in a relatively straightforward manner on patterned (111)Si substrates, GaAs nanowires remain more challenging; success depends on the cleaning steps, annealing procedure, pattern design and mask thickness. Nanowire arrays might also be used for next generation solar cells. We discuss the photonic effects derived from the vertical configuration of nanowires standing on a substrate and how these are beneficial for photovoltaics. Finally, due to the special interaction of light with standing nanowires we also show that the Raman scattering properties of standing nanowires are modified. This result is important for fundamental studies on the structural and functional properties of nanowires.

(Some figures may appear in colour only in the online journal)

1. Introduction

Semiconductor nanowires have been the object of intensive study in the last few years. Their longitudinal geometry and small footprint provide numerous advantages for optoelectronic and energy harvesting and storage devices [1–5]. Additionally, they can be the base for more complex nanostructures such as axial/radial heterostructures, nanotrees, nanocrosses, nanomembranes and nanocubes/diamonds [6–11]. Recently, it has been shown that the relatively small cross-section of the nanowires provides a path for the integration of mismatched materials within a nanowire [12, 13] and also to grow nanowires of a certain material on mismatched substrates [14]. Novel materials combinations have been achieved such as the growth of Si segments in a III–V nanowire [15–17] and III–V nanowires on silicon for high performance electronics [18, 19].

The integration of III–V nanowires on silicon is particularly attractive in the area of photonics and photovoltaics [20]. For example, a GaAs nanowire-based solar cell could be grown on a silicon pn junction forming a dual-junction solar cell [21]. Here, nanowires would not only provide the active material for the top cell; they could intrinsically provide an antireflective layer. Several works have shown that the arrangement of nanowires in a nanowire-based solar cell is extremely important for both the collection of light in the wires and for an isotropic reduction of the reflectivity [22, 23]. Recently, studies on single and multiple nanowire-based solar cells have shown photonic effects which lead to a several-fold broadband increased absorption in each nanowire. In particular, the Lund group has obtained a conversion efficiency of 13.8% under 1.5 AM illumination conditions by optimizing the nanowire array configuration [23]. Along the same lines, we have recently shown that light absorption in a single nanowire solar cell can be enhanced more than one order of magnitude due to a self-concentrating effect [24]. To the best of our knowledge, the effect on the nanowire dimensions and density on a substrate have not been investigated in detail yet.

In this work, we present some recent results on the gold-free growth of III–V nanowire arrays and on the interaction of light with the nanowires of the arrays. We highlight some of the existing challenges for the understanding and for the reproducible growth of nanowires in the array form. Next, we turn to the application of nanowire

arrays. We start presenting finite-difference-time-domain simulations on the light absorption of III–V nanowire arrays as a function of the inter-wire distance and show some results on Raman spectroscopy of nanowires as a function of the nanowire spacing. It is particularly interesting that the self-concentration effect in nanowire results in a variation of the Raman selection rules and opens up possibilities in the area of light scattering with nanowire-based nanostructures.

2. Growth of III–V arrays on silicon

Organized growth of nanostructures on a substrate is the first step towards the rational and parallel fabrication of devices. In addition, by growing nanowires on precise locations and with controlled positioning should be the ideal setting for studying their growth mechanisms. The most common way of organizing growth of nanowires on a substrate is to pattern a substrate either with gold nano-droplets or with nanoscale holes on a silicon dioxide mask. Nanoscale openings in a silicon dioxide mask provide a preferential site for nanowire for catalyst-free growth methods. However, given the same growth conditions, growth dynamics of nanowires depends in a high degree on their dimensions and center-to-center distance [25–29]. The nanoscale features for nanowire growth can be defined on a substrate by electron beam, nanosphere, phase-shift or nano-imprint lithography [30–34].

III–V nanowires grow mostly along the (111)B direction [35, 36]. This represents a challenge for growing on (111) silicon, as the polarity at the interface needs to be type B for the nanowires to grow perpendicularly to the substrate [37–42]. It is interesting to compare the catalyst-free growth of InAs and GaAs on silicon: while GaAs nanowires grow assisted by a Ga droplet at their tips, InAs nanowires seem to grow without the assistance of an In droplet by selective area epitaxy [43–45]. At the same time, InAs nanowire arrays are relatively straightforward to grow, while GaAs encounter many more challenges [46–49].

Nanowire arrays were grown by molecular beam epitaxy (MBE) in a DCA P600 system without the use of a predefined metal particle. In order to localize the growth on the substrate, thermally oxidized silicon wafers were patterned with nanoscale holes. The holes were defined by electron beam lithography and wet-chemical etching based on 7:1 buffered hydrofluoric acid solution. In order to ensure an oxide-free surface in the holes, the wafers were shortly dipped in the same HF solution prior to growth. They were subsequently kept in isopropanol until the loading in the MBE to preserve the cleanliness of the substrate. The patterns consisted in a square arrangement of holes of nominal sizes ranging between 90 and 150 nm. The inter-hole distance or pitch was varied between 200 and 2000 nm on the same substrate. The oxide thickness was 20 nm for the InAs growth and was varied between 5 and 30 nm for the GaAs.

2.1. InAs

InAs nanowires on patterned silicon substrates were grown at a nominal In growth rate of 0.2 Å s^{-1}, As$_4$ partial pressure

of 6.0×10^{-6} Torr (BEP: beam equivalent pressure) and substrate temperature of $500\,^\circ$C for 1 h. Scanning electron micrographs (SEM) of InAs nanowire arrays grown on a Si(111) substrate are shown in figures 1(a)–(g). In the context of InAs nanowire growth, it is well known that a tradeoff exists between the growth selectivity and the final length of the nanostructures [46]: this has recently also been observed in the case of InAs V-shaped membranes [50]. The selectivity of growth in the openings of the substrates improves with the temperature until parasitic growth on SiO$_2$ completely disappears. Indeed, the sticking probability of indium ad-atoms on oxide decreases by increasing the temperature leading to the nucleation of nanowires only in the predefined holes. However, the higher is the temperature the higher is desorption of the deposited material and thus the shorter the structures grown. This means that the ideal growth conditions represent a compromise between optimal selectivity and maximum length, and these are the ones we adopted in this study. Within these growth conditions we could achieve high selectivity and aspect ratio, which were needed for the optical measurements. The nanowire growth yield, here defined as number of openings nucleating nanowires divided by the total number of openings in the pattern, was 92%.

The sample reported in figure 1 shows a significant size variation of the nanowires as a function of the inter-hole distance (pitch). In particular the diameter and length saturates around a value of 155 and 1480 nm for pitch 800 nm. A similar behavior has been observed by other groups in the case of ordered growth of InAs nanowires [44, 46, 51] and nanomembranes [50]. The dependence of the nanowire length as a function of the pitch can be explained by the existence of two separate growth regimes: (i) a competitive growth regime with shorter nanowires for narrow inter-holes distances and (ii) a diffusion-limited or independent growth regime for wider pitches. The indium surface diffusion length on SiO$_2$ (λ_{SiO_2}) determines the switch between the two regimes. Indeed, λ_{SiO_2} limits the surface collection area i.e. the sample area from which each wire can collect the In species diffusing on the oxide. For a small nanowire spacing (pitch $< 2\lambda_{SiO_2}$), the indium ad-atoms are shared between the wires. By increasing the spacing, the surface collection area available exclusively to each nanowire increases, resulting in a linear increase of the growth rate. In the opposite limit of a large spacing (pitch $> 2\lambda_{SiO_2}$) the wires can be treated as independent isolated islands. In this regime the surface collection area cannot increase anymore and the growth rate is no longer dependent on the pitch. The calculated volume of the nanowires depends on the pitch and it can be seen that it saturates when the growth reaches the diffusion-limited regime (see figure 1(e)). For completeness, in figure 1(f) we show the equivalent layer thickness, defined as the thickness of the equivalent layer obtained with the same InAs volume. This will be useful for the analysis of the Raman scattering data in the arrays, as discussed later in this work.

2.2. GaAs

We turn now to the study of Ga-assisted growth of GaAs nanowires on SiO$_2$/Si patterned substrates. In this

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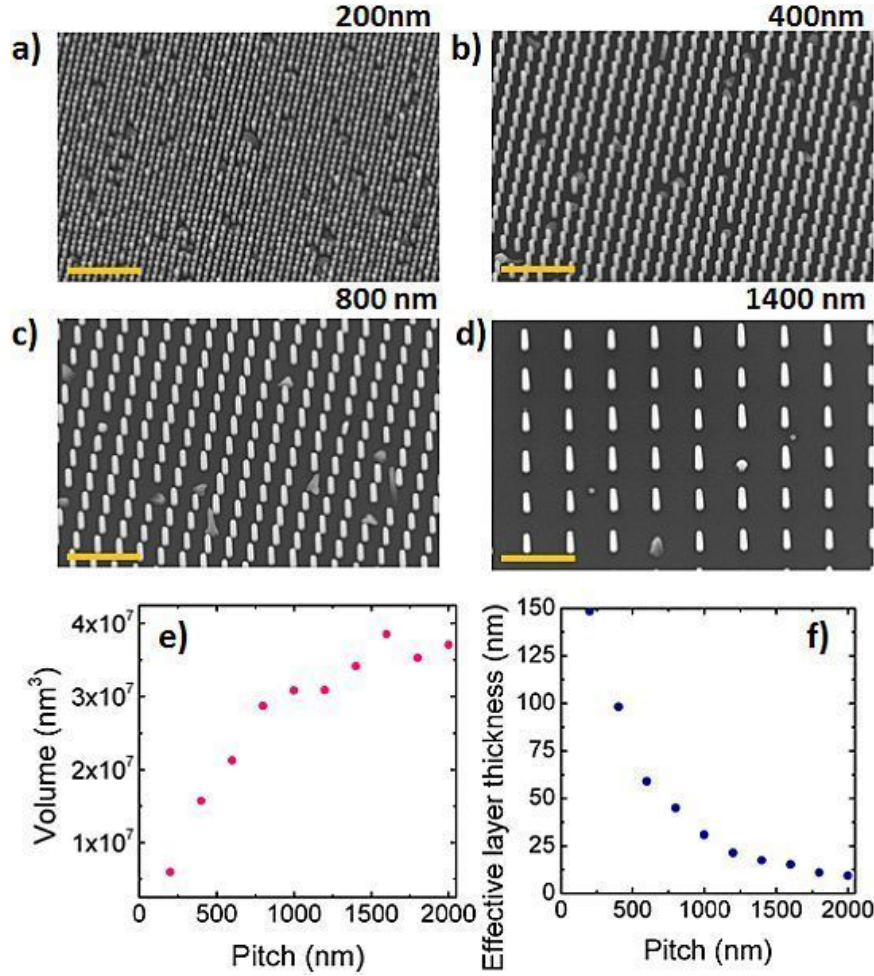
Figure 1. (a)–(d) Scanning electron micrographs of InAs nanowires obtained on a patterned Si substrate for different pitch (scale is 2 μm), (e) nanowire volume (V_{NW}) and (f) effective layer thickness as a function of the pitch.

case, a nanoscale Ga droplet gathers preferentially As_4 molecules to drive the GaAs growth. The Ga droplet is continuously replenished by the diffusion of Ga-adatoms from the facets and surface for ensuring the continuous nanowire growth [52]. Recently, it has been shown that the substrate preparation and the pre-growth conditioning are key to achieve high-yield growth of GaAs nanowire arrays by the Ga-assisted method [49]. We have investigated two of these main factors, namely the degassing of the sample prior to growth and the thickness of the growth mask layer. Figure 2 shows a sequence of 20° tilted SEM images of the nanowire arrays obtained in this study. The GaAs nanowires grown on patterned Si(111) substrates, with a nominal Ga growth rate of 1 Å s^{-1}, As_4 partial pressure of 2×10^{-6} Torr, substrate temperature of 615 °C, and with 7 rpm substrate rotation. In all cases the samples have been degassed at 600 °C for 2 h and they have been all grown with the same growth recipe. Figure 2(a) shows the results of the first growth: the yield of vertical wires is low and parasitic bulk growth occurs. The sample reported in figure 2(b) has been grown after a further

heating at 770 °C for 30 min in order to remove any possible contaminants of the surface: the density of vertical wires is significantly improved, thus demonstrating that the sample preparation and the cleaning of the surface are decisive steps in obtaining high quality nanowire arrays.

Subsequently, we evaluated the influence of thickness of the oxide layer on nanowire growth yield. The thickness of the oxide layer was determined with spectroscopic ellipsometry prior to growth. Growths of GaAs nanowires on arrays with SiO_2 layers of 13, 18 and 21 nm thickness are reported in figures 2(c)–(i). As also found by Plissard *et al* [49], by decreasing the oxide thickness the yield improves to dramatically drop again at thinner thicknesses. We found an optimal oxide thickness of 18 nm, which is not affected by the pitch of the array. The geometry of the pattern is found to affect in itself the yield of vertical wires, an observation which needs further investigation. The maximum yield (65%) is reached for pitch = 400 nm and opening size = 100 nm (figure 2(c)).
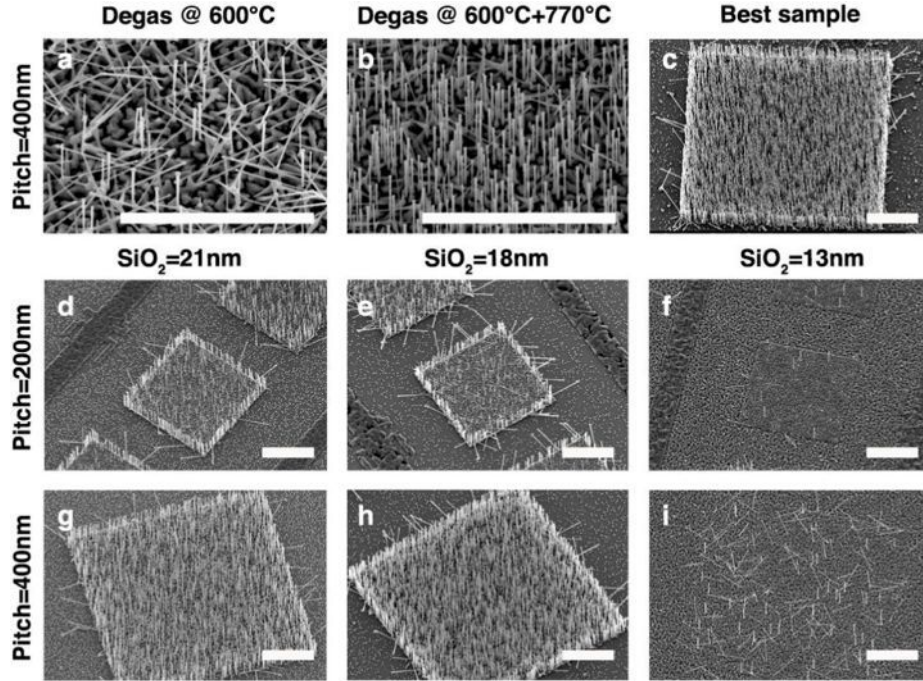
Figure 2. Scanning electron micrographs of GaAs nanowires obtained on patterned (111)Si substrates as a function of the oxide thickness, pitch and substrate preparation conditions (see text).

Further optimization can be achieved by studying several other parameters like the substrate temperature, the V/III ratio and the catalyst pre-deposition. However we have encountered several issues in the long-term reproducibility of the samples. In particular, we have recently observed that small changes in the surface roughness of the substrates results in extremely different nanowire density and orientation on a silicon substrate [53]. We believe this kind of variation from batch to batch might be one of the sources for lack of reproducibility for the Ga-assisted growth of GaAs nanowire arrays.

3. Light interaction with III–V nanowire arrays

We turn now our attention towards understanding of how a planar light wave incident perpendicularly to the substrate interacts with standing nanowires. As mentioned above, we have recently shown a self-concentration effect occurring in single nanowires standing on a substrate [24]. Here below we present calculations on light absorption in standing nanowires, and we show how this changes in an array as a function of the inter-wire distance. Finally, we show how this concentration effect affects the Raman spectra of nanowires.

3.1. Light absorption in standing nanowires

Light absorption in standing GaAs nanowires of different diameters surrounded by vacuum was calculated by solving the wave equation for an incident radiation propagating along

the nanowire axis. For this, we use finite-difference-time-domain simulations [54], similar to what the Witzigmann group has been realized recently [55]. We start by presenting the propagation of a planar wave impinging vertically on a 2 μm long GaAs nanowire. We have calculated the spectral and diameter dependence of the absorption rate. The enhancement in absorption for a single standing nanowire is defined as the ratio between the absorbed power and the power of the incident electromagnetic radiation on the nanowire surface ($S = \pi r^2$, where r is the nanowire radius):

$$\text{Absorption enhancement} = \frac{P_{\text{absorbed}}}{P_{\text{inc}}S} \tag{1}$$

where P_{absorbed} is the power absorbed by the nanowire and P_{inc} is the incident power surface density. Clearly, this efficiency will be larger than 100% in the cases where the absorption cross-section is larger than the *apparent* one defined by the physical limits of the nanowire. The spectral dependence of the absorption enhancement as a function of the nanowire diameter is plotted in figure 3(a). The color scale denotes the value of the enhancement. The graph is composed of two main branches of enhanced absorption. The first one, defined by an enhancement of the spectral absorption close to 70 fold, corresponds to nanowires between 50 and 150 nm. It is important to note that the absorption enhancement is always higher than 10 in the 300–900 nm range, where GaAs absorbs at room temperature. The second branch corresponds to an enhancement of 10 fold in the absorption for diameters above 150 nm. These both branches correspond to resonances for which the light is better trapped in the nanowire structure.
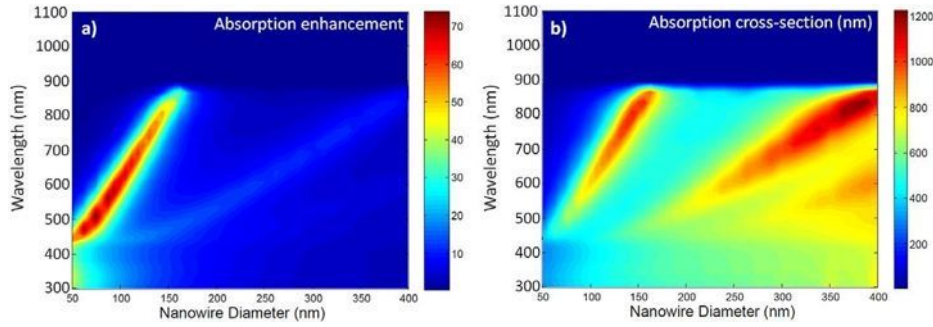
Figure 3. (a) Absorption enhancement and (b) diameter of the absorption cross-section of single vertical GaAs nanowires standing on a Si substrate as a function of the diameter.

Along these branches, the resonant wavelength increases with the nanowire diameter. It is interesting to note that there is at least a four-fold increase of the absorption in the whole spectrum even for larger nanowires (diameter above 100 nm). This represents a significant broadband absorption increase, difficult to observe in lying nanowires [56–59].

A way of capturing the origin of the dramatic increase in light absorption, we proceed by calculating the absorption cross-section, defined by the disk of radius r^* corresponding to the equivalent area under which the absorbed power density $P_{abs}/\pi r^{*2}$ is equal to the incident surface power density, P_{inc}:

$$r^* = \sqrt{\frac{P_{abs}}{\pi P_{inc}}}. \qquad (2)$$

In figure 3(b) we plot the spectral dependence of the capture cross-section diameter ($2r^*$) as a function of the nanowire diameter. In a thin film the absorption cross-section has identical dimensions to its size, while in the case of nanoscale objects the cross-section can be quite larger [60, 61]. We find cross-sections as large as 1200 nm for the longest wavelengths (830 nm) and largest nanowires. Interestingly, the plot of the cross-sections diameter amplifies the branches found in the absorption efficiency mapping. One of the consequences of the large absorption cross-section in standing nanowires is that in a solar cell they should be disposed at an optimized distance. At the same time, the self-concentrating effect should result in an increase of the device efficiency and provides a path for surpassing the efficiency limits posed by Shockley and Queisser in 1961 as explained in the [24, 62].

We direct now our discussion towards the interaction of light in nanowire arrays as a function of the inter-wire distance or pitch. We have extended our calculations to nanowire forming square arrays on silicon and exhibiting a diameter of 150 nm. For simplicity in the calculations we have assumed a square array. In a real nanowire-based solar cell device, the arrangement should be optimized so that the nanowires are separated by the optimum pitch and avoid any possible diffraction effects [63, 64]. Figure 4(a) depicts the square of the electric field of light propagating in the nanowire (which is proportional to the light intensity), weighted by the solar spectrum 1.5 AM as a function of the pitch. The smallest pitch is 150 nm, which corresponds to the thin film case.
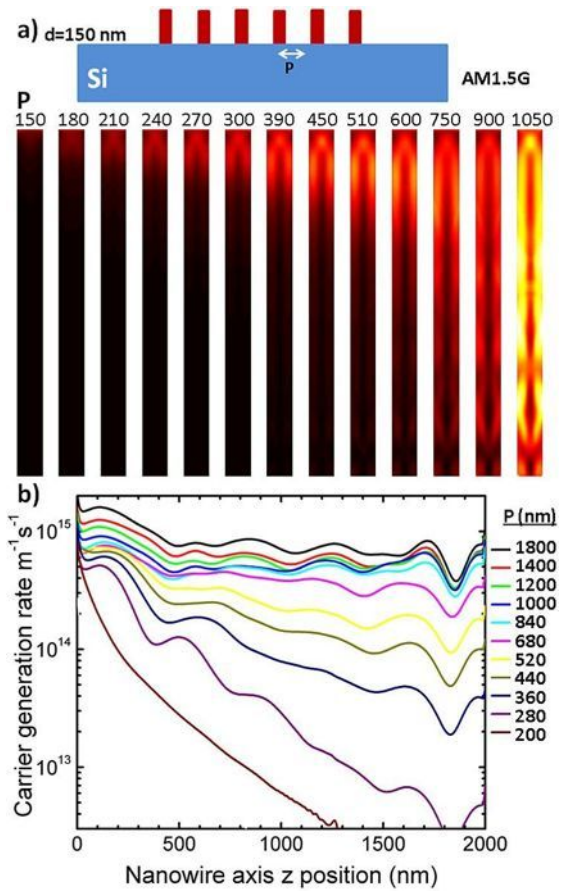
Figure 4. Calculations of light absorption in GaAs nanowires in an array in AM 1.5 conditions. (a) Average of the square of the electric field in the nanowire for different pitch, (b) profile of the carrier generation along the nanowire axis as a function of the pitch.

In this case, the light intensity decays exponentially at the top of the nanowire/thin film. By separating the nanowires the light starts to be present to a deeper length within the nanowire. For a pitch of 750 nm a significant amount of light is able to propagate till the bottom of the nanowire.

The intensity of light along the nanowire axis increases by further separating the nanowires. One should note that the distribution of the intensity along the nanowire seems to exhibit some nodes, showing that the absorption enhancement corresponds to a resonance and that the nanowire acts as a sort of cavity. From the distribution of the square of the electric field along the nanowire we calculate the overall carrier generation rate along the nanowire axis. The results are shown in figure 4(b). In agreement with the distribution of the light intensity, the generation of carriers increases and homogenizes along the nanowire axis when the pitch of the nanowire array increases. Interestingly, the carrier generation does not follow the exponential decay from Lambert–Beer law but a relatively homogeneous absorption along the nanowire axis. This distribution of light absorption is at the same time more beneficial for carrier extraction in the radial pn junction design. Along with the self-concentration effect, the generation of carriers all along the nanowire axis could lead to devices with a higher V_{OC} and a smaller series resistance. Overall this would result in a higher photo-conversion efficiency.

3.2. Raman scattering in standing InAs nanowire arrays

Backscattering Raman measurements were conducted using the 488 nm line of an Ar/Kr$^+$ gas laser focused on the InAs arrays, described in section 2.1, through a 0.75 N.A. microscope objective. The total laser power for the experiments was kept at 300 μW. The Raman scattered light was projected on the entrance slit of a triple grating spectrometer and collected by means of a charge coupled device. Experiments were conducted on a series of as-grown nanowires obtained during a single MBE growth run on a sample with patterned fields of varying inter-wire spacing. Figure 5(a) shows a typical Raman spectrum of the InAs nanowires obtained under such conditions. One can observe two modes at 211 and 236 cm^{-1}, reported respectively as TO and LO for InAs. Still, the exact position of these modes depends on the existence of zinc-blende, wurtzite and/or twining defects [65–68]. We also observe a mode at 520 cm^{-1} resulting from the silicon substrate. Figure 5(b) shows the absolute intensities of these modes in dependence of nanowire array spacing. One can see that while the absolute intensities of InAs related modes decrease with nanowire spacing the relative intensity of the silicon mode is increasing.

Figure 5(c) depicts the top InAs surface coverage and equivalent thin film volume normalized to the values extrapolated for 0 nm pitch (thin film case). As seen in figure 5(b), for small pitch distances, both TO and LO decrease in intensity, which is explained by the loss of InAs scattering cross-section because of the lower nanowire density in the probing area. Interestingly, for pitches larger than the laser spot diameter (around 800 nm), the LO intensity reaches a plateau and even increases slightly with pitch distance, thus indicating that an effect beyond the purely geometric material decrease plays a role. Actually, the signal seems to correlate with the volume of a single nanowire from figure 5(c), fact that suggests a light coupling effect that allows the light to probe
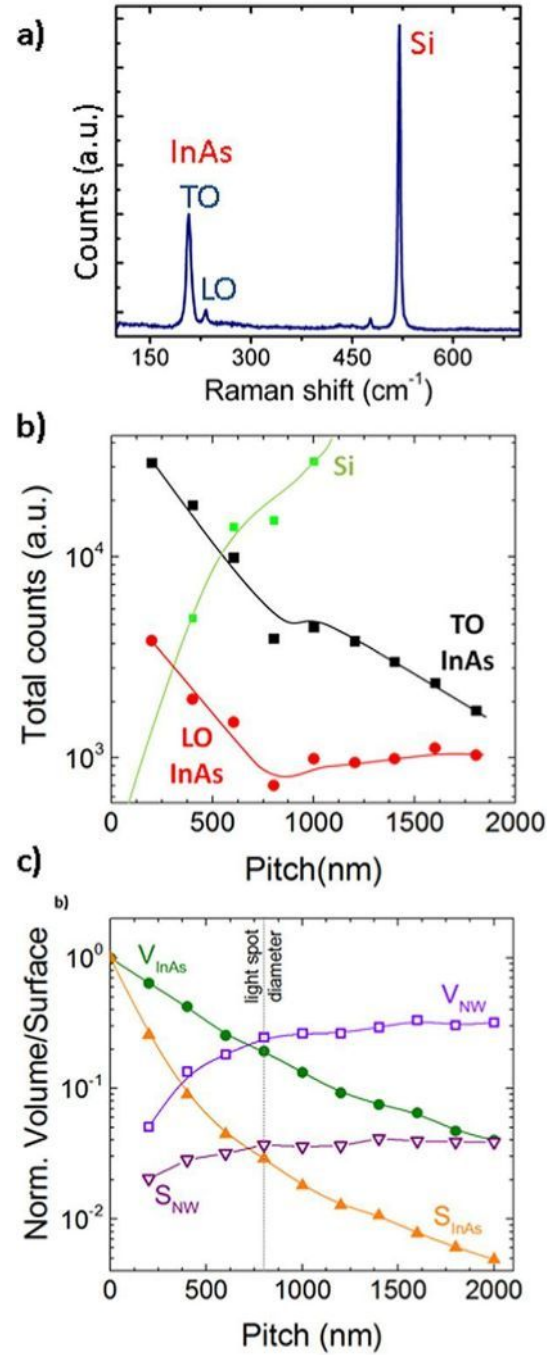
Figure 5. Raman spectroscopy in InAs nanowire arrays. (a) Typical spectrum of the InAs nanowires on Si, (b) evolution of the intensities of the peaks corresponding to InAs and Si and (c) normalized values of the volume of a single nanowire (V_{NW}), equivalent thin film thickness of the array (V_{InAs}) as well as the surface covering of the nanowire array (S_{InAs}) and single nanowire (S_{NW}).

the whole nanowire volume even though the strong absorption of InAs at 488 nm (absorption length is about 8 nm). In Raman spectroscopy, not only enhancement for incident light

is important, but also how the scattered light interacts with the nanowire and should be taken into account [69–71]. It has been shown in previous works that light extraction efficiency in an array can be explained by the Maxwell–Garnett effective medium approximation [72]. Under such framework, arrays with smaller nanowire density present an effective refractive index closer to that of air, thus enabling a better light extraction. However, the light resonances at the nanoscale should be also taken into account to have a full understanding of the Raman signal.

Similarly, the TO intensity also shows a change in the intensity decay as a function of the pitch for pitch distances around 800 nm. However, contrary to the LO mode, the TO intensity decreases back again for large pitch distances (larger than 1200 nm). In wurtzite material, it has been observed by Raman scattering that light coupling enables light entering the nanowires to a considerable extent through their side facets even for normal incidence and small bandgap material [73, 74]. Because the Raman signal is directly related to the electric field direction through the symmetry of the vibrational mode in question, the change in the field direction at the nanoscale can completely modify the Raman selection rules for different modes from the macroscopic point of view. Our results thus seem to indicate a similar effect, where the electromagnetic resonances in the nanowire favor symmetry conditions for extraction efficiency of the LO scattered light. This opens the way for fundamental studies in the area of LO phonon–electron/hole scattering in doped nanowires [75, 76].

4. Conclusions

In conclusion we have demonstrated growth of self-catalyzed InAs and GaAs nanowire arrays on a (111)Si substrate and explained some of the challenges associated with obtaining high yield. We have also explored the concept of ideal nanowire array configuration for optimal light absorption. In particular, we have shown how planar light waves incident perpendicularly to the substrate can exhibit resonances for certain nanowire diameters. This results in a self-concentration effect and a several-fold enhancement in the absorption rate. This phenomenon can be very useful in photovoltaic and light emitting devices. Finally, we show how the occurrence of absorption resonances in nanowires can lead to an enhancement of the LO phonon scattering, which can be of fundamental importance for the study of structural and functional properties of nanowires by Raman spectroscopy.

Acknowledgments

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Amorphous silicon mediates a high yield in GaAs nanowire arrays on Si obtained by the Ga-assisted method.

Eleonora Russo-Averchi[1], Jelena Vukajlovic Plestina[1], Gözde Tütüncüoglu[1], Anna Dalmau-Mallorquí[1], Maria de la Mata[2], Daniel Rüffer[1], Heidi A. Potts[1], Federico Matteini[1], Jordi Arbiol[2,3], Sonia Conesa-Boj[1] and Anna Fontcuberta i Morral[1]*

[1] Laboratoire des Matériaux Semiconducteurs, Ecole Polytechnique Fédérale de Lausanne, 1015 Lausanne, Switzerland

[2] Institut de Ciència de Materials de Barcelona (ICMAB-CSIC), Campus de la UAB, 08193 Bellaterra, CAT, Spain

[3] Institució Catalana de Recerca i Estudis Avançats (ICREA), 08010 Barcelona, CAT, Spain

ABSTRACT. GaAs nanowire arrays on silicon offer great perspectives in the optoelectronics and solar cell industry. To fulfil this potential, gold-free growth in predetermined positions should be achieved. Ga-assisted growth of GaAs nanowires in the form of array has been shown to be challenging and difficult to reproduce. In this work we provide some of the key elements for obtaining a high yield of GaAs nanowires on patterned Si in a reproducible way. By modifying the surface properties of the nanoscale areas exposed to growth with the addition of an amorphous silicon intermediate layer between the crystalline substrate and the oxide mask, the size and the contact angle of the Ga droplet are suitably modified, leading to a high yield of vertical nanowire. This work opens new perspectives for the rational and reproducible growth of GaAs nanowire arrays on silicon.

Semiconductor nanowires (NWs) have been the subject of extensive investigations in recent years, motivated in part by the unique physical properties provided by their essentially one-dimensional geometry. These novel properties, as well as new material combinations that can only be achieved with NWs[1,2,3], offer a large number of potentially useful applications in a broad range of electronic, optoelectronic and energy harvesting devices[4,5,6,7,8,9,10]. A particularly useful property is that their small diameter allows their growth on lattice-mismatched substrates[11,12,13]. A natural consequence is that NWs enable the integration of highly functional III-V compounds with silicon-based technologies[14,15,16,17]. This represents a unique opportunity to combine the advantages of III-V materials such as direct band gap and high mobility with Si, which is extensively used in microelectronics industry[18,19].

In the past, regular arrays of NWs have been achieved by patterning a substrate with gold nanoparticles[20,21,22]; such a configuration demonstrated the rational use of NWs, showing their potential integration in mass-production applications. These pioneering works rely on the use of the gold droplets for the nucleation and growth of the NWs through the Vapour-Liquid-Solid process (VLS), however gold is a non-desired impurity in silicon technology, so other methods have been investigated for the growth of NWs on silicon substrates[23,24,25]. Ga-assisted growth is a successful example showing how this precious metal can be avoided for the growth of III-V NWs on III-V and on Si substrates[26]. Following this method, nanoscale gallium droplets collect arsenic from the gas phase. Subsequent supersaturation leads to the precipitation of GaAs underneath. The Ga droplet should be refilled continuously to ensure a sustainable growth. Applying this method, arrays of GaAs NWs have been obtained on patterned GaAs substrates[27], while fabrication of GaAs NWs on a patterned Si surface has shown to be by far more challenging. One of the main challenges has been the reproducibility in obtaining high yield of vertical GaAs NWs. Key elements such as gallium pre-deposition, thickness and composition of the growth mask have shown to be important parameters for a successful growth[28,29]. Still, successful growths of GaAs NW arrays by the Ga-assisted method are rare in literature[30,31,32].

In this work we bring new elements of analysis for understanding how a high yield can be obtained for the growth of Ga-assisted GaAs arrays on silicon. We have found that the microstructure of the Si wafer, in particular the interface between the Si and the SiO_2 growth mask, is decisive for achieving highly controlled vertical GaAs NWs. Progress in the deterministic GaAs NW growth at selected positions on a Si substrate is the first step towards the rational fabrication of advanced devices on the silicon platform.

We synthesized GaAs NWs by the Ga assisted method using a DCA P600 molecular beam epitaxy (MBE) machine. 4 in. Si(111) wafers have been patterned with arrays of nanoscale holes following a typical nanofabrication method[28,32,33]. First, a 20 nm thick SiO_2 layer has been grown by thermal oxidation on the silicon wafers as growth mask. The holes were defined by electron-beam lithography and wet chemical etching based on 7:1 buffered hydrofluoric acid (BHF) solution (see Supporting Information for further details). The wafers were subsequently diced into 35×35 mm^2 square chips sized for the MBE sample holder. Prior to growth, the substrates were heated to 770 °C for 30 min to remove any possible surface contaminants. In the following we will refer to this process step as *degassing*. The growth was carried out at a nominal Ga growth rate of 1 Å/s, As$_4$ partial pressure of 2 x 10^{-6} Torr, at a substrate temperature of 630 °C, and with 7 rpm rotation. In some of the growths, Ga was pre-deposited to facilitate the formation of Ga droplets. This has been accomplished by keeping the Ga shutter open since the ramp up of the substrate temperature for the degassing step. In the following we specify whether or not such pre-deposition has been performed. The morphology of the samples was characterized by scanning electron microscopy (SEM) and by transmission electron microscopy (TEM). TEM cross-sections were prepared by using a Focus Ion Beam (FIB).
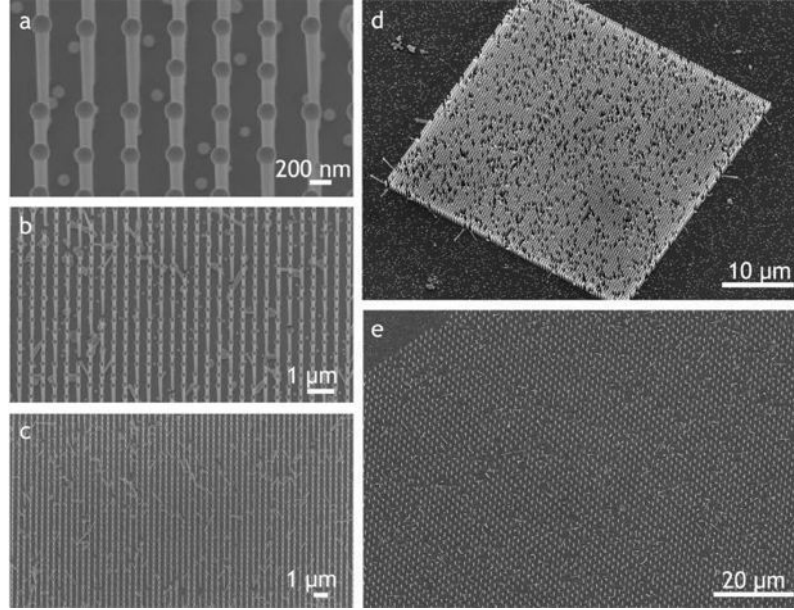
Figure 1. Scanning electron microscopy (SEM) images of GaAs nanowires grown on patterned Si(111) substrates at 630 °C, at a nominal Ga growth rate of 1 Å/s and under an As_4 partial pressure of 2 x 10^{-6} Torr. (a-c) are 20° tilted images and (d-e) are tilted views with additional in-plane rotation. The yield of vertical nanowires is 80%. The hole diameter size is 90 nm for all the images. The interhole distance is 400 nm in (a-d) and 1600 nm in (e).

SEM micrographs of successful GaAs NWs arrays grown on a Si(111) substrate are shown in Figure 1. Figure 1a-d show tilted views of the NWs grown in patterns with a nominal hole diameter of 90 nm and an inter-hole distance of 400 nm at different magnification and with additional in plane rotation (d). Figure 1e shows the results for a larger inter-hole distance (1600 nm). The NWs are uniform in length and diameter. They present a slightly inverse tapering and a Ga droplet at their tip. The yield of vertical NWs - defined as number of openings nucleating vertical NWs divided by the total number of openings in the array - is 80%. The yield is independent from the inter-hole distance of the array. The majority of holes not leading to the

formation of vertical NWs correspond to a failure in nanowire nucleation, while only few consist of tilted NWs. This could be due to an incomplete definition of the holes by the e-beam lithography. An optimization of the pattern definition could in principle lead to an improved yield of vertical wires.

As found by other groups[29,34], the gallium pre-deposition step has a strong influence on the yield of vertical NWs. Figure 2 (top) shows representative SEM images of the growth results obtained with and without the Ga pre-deposition, keeping all the other growth parameters unvaried. The two substrates originated from the same wafer, which we refer as *Wafer 1*. As we can see in the picture, omitting the Ga pre-deposition step leads to an extremely low yield of vertical wires and a high density of non-vertical wires and parasitic growth. An identical set of growths, with and without the Ga pre-deposition, has been performed on a similar Si wafer of a different batch. We refer to these two samples as *Wafer 2*. Fig. 2 (bottom) shows the results of the growths. In this case, irrespective of the Ga pre-deposition, the yield of vertical wires is very low. Instead, many tilted wires and parasitic growth are found on the substrates.
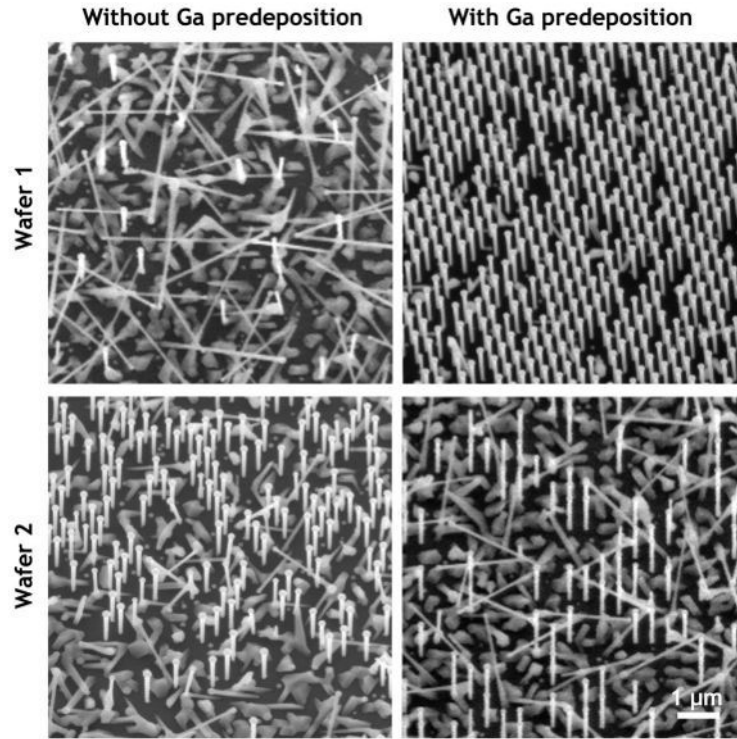
Figure 2. Tilted SEM micrographs of GaAs NWs grown in arrays defined on two different 4 in. wafers (Wafer 1 and Wafer 2) with and without the pre-deposition of Ga droplets. (Top) For the growth on Wafer 1, the yield of vertical wires strongly depends on the Ga pre-deposition. (Bottom) For the growth on Wafer 2, the yield of vertical nanowires is very low in both cases. For all the images the interhole distance is 400 nm and the hole diameter size is 90 nm.

The discrepancy between the results obtained on the two wafers was unexpected, since *Wafer 1* and *2* had been subject to identical sample preparation and growth protocols. This prompted us to investigate the characteristics of what were supposed to be identical substrates in detail. To this purpose, lamellas containing cross-sections of the substrates were prepared by focus ion beam (FIB).

We start by analysing the structure of the Si chip in a region outside the pattern. Figure 3 displays cross sectional high angle annular dark field (HAADF) images of representative samples of *Wafer 1* and *Wafer 2*, taken at the interfaces between Si and the thermal SiO_2, and the corresponding energy-dispersive X-ray spectroscopy (EDX) maps. The same analyses have been performed on four chips, two of *Wafer 1* and two of *Wafer 2*. Two samples correspond to remaining wafer pieces which had not been loaded in the MBE reactor, i.e. they have been analysed just after the sample preparation; the other two have been analysed at the end of the growth process and correspond to the samples depicted in Figure 2.

We start by considering the pieces not loaded in the MBE (Figure 3a-b). Surprisingly, the sample from *Wafer 1* shows an unexpected amorphous layer between the crystalline silicon and the SiO_2. This 13 nm thick layer consists of amorphous silicon, as confirmed by the lack of oxygen in the EDX analysis. The interface between amorphous silicon and crystalline silicon is considerably rough. Conversely, the piece from *Wafer 2* shows the thermal oxide layer directly on top of the monocrystalline silicon, as one would expect from the sample preparation. The SiO_2 layer of the chip from *Wafer 1* has been found to be rather non uniform, with thickness ranging from 10 to 20 nm, unlike for *Wafer 2* sample, although an identical dry oxidation has been performed on the wafers. The analysis of the chips after growth is shown in Figure 3c-d. In this case, for both samples only thermal oxide is found on the crystalline silicon. Since the crystallization of amorphous silicon starts at temperatures higher than 500°C, we think that it has crystallized during the heating of the substrate in the growth chamber[35,36]. Our Si provider suggested that the amorphous layer was generated by the mechanical treatments such as slicing and lapping and by an insufficiently long chemical mechanical polishing (CMP) step at the end

of the substrate preparation. We believe indeed that the large thickness of the layer of amorphous silicon layer prevented its full crystallization during the thermal oxidation.
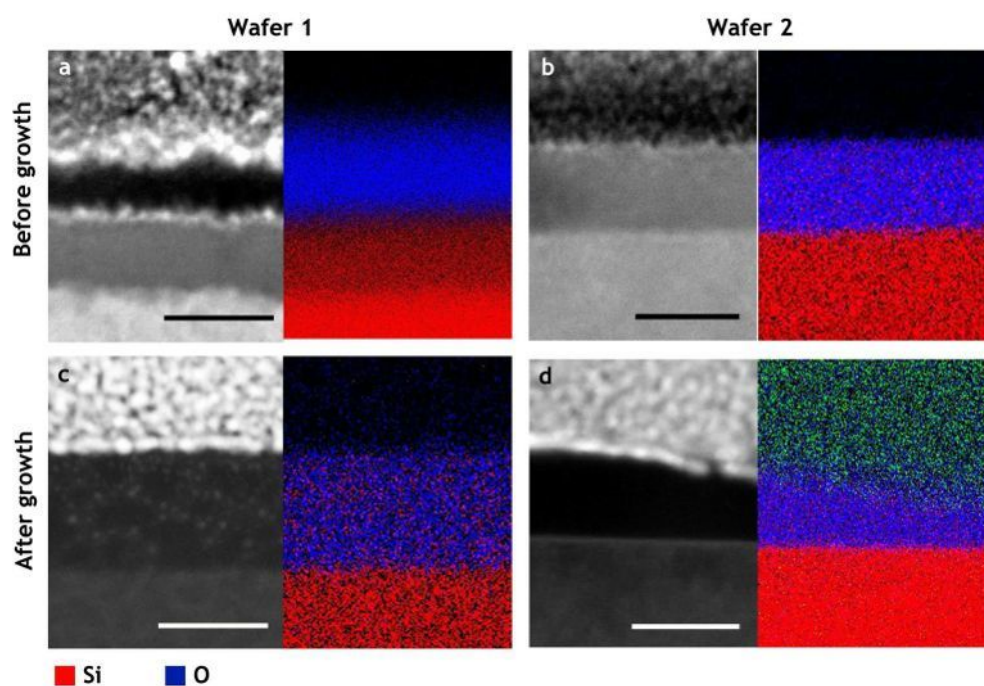
Figure 3. HAADF images of representative samples of Wafer 1 and Wafer 2, studied before and after growth, and corresponding EDX results, with the Si map in red and the O map in blue. The analysis is performed at the interface between the silicon substrate and the mask oxide. The sample from Wafer 1 shows an unexpected layer of a-Si that crystallizes after growth. The sample from Wafer 2 shows uniquely a thermal oxide layer grown directly on the crystalline silicon substrate. The scale bar is 20 nm.
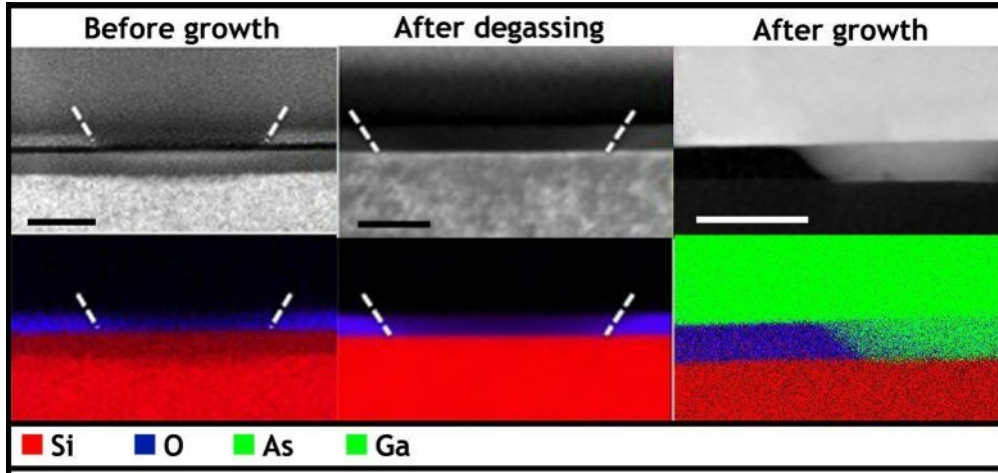
Figure 4. (Left) HAADF image of a nanoscale hole where the SiO$_2$, the amorphous Si and the crystalline Si can be distinguished and the corresponding EDX map. (Center) HAADF and EDX analysis of the hole degassed in the MBE reactor. The amorphous silicon layer is crystallized. (Right) HAADF and EDX analysis performed after the growth. A GaAs NW nucleates in the hole, grows vertically and also radially once higher than the hole. The scale bar is 50 nm.

We turn now the attention to a patterned region of the silicon chip: cross-sectional HAADF images of nanoscale holes from *Wafer 1* with the corresponding EDX maps are shown in Figure 4. The analysis has been performed prior to growth (Figure 4 Left), after the degassing step in the MBE chamber (Figure 4 center) and after the growth (Figure 4 Right). Here we also observe the presence of an amorphous silicon layer below the SiO$_2$ prior to degassing or growth. The amorphous layer, which is also observed at the position of the holes, is completely crystallized after the degassing and growth steps. After crystallization, the silicon surface at the bottom of the hole appears completely flat, as shown in Figure 4 (Right).

We thus conclude that the presence of a layer of amorphous silicon seems to be a necessary but not sufficient condition to guarantee a high yield of vertical wires, and that the addition of the Ga pre-deposition is also required. We remind here that in our case the Ga shutter is opened at the very beginning of the growth process and thus during the degassing step. During this time, the temperature of the Ga cell is ramping up to a achieve a nominal Ga growth rate of 1 Å/s, and the substrate temperature is ramped up from 200°C up to 770°C at a rate of 50°C/s for the degassing step. Therefore, the amorphous layer is expected to crystallize in a relatively short time once the substrate approaches the degassing temperature[36]. The Ga pre-deposition, however, already starts at lower substrate temperatures, when the amorphous layer has not yet crystallized. We believe that the Ga droplets are formed on the amorphous silicon at the bottom of the holes before it crystallizes. When the Ga pre-deposition is not performed during the heating of the substrate, or when the amorphous layer is not present, the Ga droplets form directly on the crystalline silicon of the substrate.

Crystalline and amorphous silicon possess different surface energies. As a consequence, wetting of Ga should also present a different nature. Knowing that the characteristics of the Ga droplets affect the yield of vertical NWs[37,38], we looked at their shape and contact angle on amorphous and crystalline silicon. A thin amorphous silicon layer was deposited by means of Plasma-Enhanced Chemical Vapour Deposition (PECVD) on a Si(111) wafer. The substrates were exposed to BHF wet etching to ensure their surfaces were free of oxide; both samples have been heated to 770°C for the degassing step with the increasing Ga deposition during the ramp up, simulating the initial step of our growth process.

SEM micrographs of the Ga droplets obtained on the two kinds of surfaces are shown in Figure 5. The Ga droplets deposited on what initially was amorphous silicon have a contact angle of

84±4°; the ones deposited on crystalline silicon have a contact angle of 52±3°. The Ga droplets deposited directly on crystalline silicon are also significantly larger than the ones observed on amorphous silicon. Both, the droplet size and contact angle, could favour vertical nanowire growth in the case of the originally amorphous silicon substrate. Contact angles smaller than 90° render nucleation at the triple-phase line especially difficult[39],[40]. Additionally, we envisage in patterned substrates that when the sizes of the holes and the droplet are similar, the lateral walls affect the extension and position of the droplet. It also suppresses the existence of the triple-phase line at the interface with the silicon substrate. If the triple-phase line occurs on the SiO_2, the loss of epitaxial relation with the substrate results in random orientation of the nanowires. Although this study has been performed on unpatterned substrates, we believe that it highlights important aspects of the initial stages of growth and how to obtain high yields of vertical wires.

We conclude that the size and the contact angle of the Ga droplets as well as their interaction with the substrate play a fundamental role in the successful growth of vertical GaAs NW arrays. Our results suggest some possible modifications to the nanofabrication methods usually employed for nanoscale holes. In particular is should be advantageous to change the wetting properties at the open surface of the holes. Recent unpublished results show that there is an optimal contact angle for obtaining high yield of vertical wires, which can be obtained by a careful control of the native oxide[40]. Finally, if amorphous silicon should be used at the interface between the substrate and the SiO_2 mask, it is necessary to investigate the required layer thickness, as the amorphous silicon layer will party crystallize during the thermal oxidation process. Alternatively, if the process should be compatible with thin amorphous silicon layers, the growth mask material should be reconsidered.
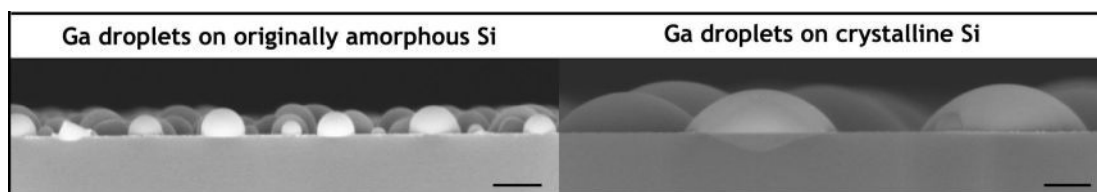
Figure 5. Cross sectional SEM images of Ga droplets deposited on originally amorphous silicon (left) and on crystalline silicon (right). The droplets have different sizes and contact angles depending on the surface. The scale bar is 200 nm.

In conclusion, we have provided new elements for the achievement of a high yield of vertical GaAs NWs on a patterned Si substrate. A Ga pre-deposition step prepares the Ga droplets for nanowire growth. The nature of the surface during this pre-deposition is key for the obtaining the contact angle and position of the triple-phase line. We have obtained ideal conditions by using an oxidized Si substrate containing an amorphous layer at the interface with the crystalline substrate. Other treatments such as the creation of an appropriate native oxide layer may lead to a similar effect.

AUTHOR INFORMATION

Corresponding Author

* E-mail: anna.fontcuberta-morral@epfl.ch

Author Contributions

ERA, GT, DR, HAP and FM contributed to the growth. ERA, JVP, GT and ADM fabricated the samples. JA, MdlM and SCB performed HAADF STEM and EDX analysis. ERA made the figures and the artwork. ERA and A.F.iM. wrote the manuscript in collaboration with all the authors. A.F.iM. supervised the project. All authors have given approval to the final version of the manuscript.

Synopsis TOC:

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3.4 InAs V-shaped nanomembranes

Publications:

V **Vertical "III-V" V-shaped nanomembranes epitaxially grown on a patterned Si[001] substrate and their enhanced light scattering**
S. Conesa-Boj[a], E. Russo-Averchi[a], A. Dalmau-Mallorqui, J. Trevino, E. F. Pecora, C. Forestiere, A. Handin, M. Ek, L. Zweifel, L. R. Wallenberg, D. Rüffer, M. Heiss, D. Troadec, L. Dal Negro, P. Caroff and A Fontcuberta i Morral
[a] equal contribution
ACS Nano 6 (2012) 10982

VI **Growth mechanisms and process window for InAs V-shaped nanoscale membranes on Si[001]**
E. Russo-Averchi, A. Dalmau-Mallorqui, I. Canales-Mundet, G. Tütüncüoglu, E. Alarcon-Llado, M. Heiss, D. Rüffer, S. Conesa-Boj, P. Caroff and A. Fontcuberta i Morral
Nanotechnology 24 (2013) 435603

VII **Bottom-up engineering of InAs at the nanoscale: from V-shaped nanomembranes to Nanowires**
E. Russo-Averchi, G. Tütüncüoglu, A. Dalmau-Mallorqui, I. Canales-Mundet, M. de la Mata, D. Rüffer, J. Arbiol, S. Conesa-Boj and A. Fontcuberta i Morral
in review

For a straightforward integration with the silicon platform the growth of ordered nanostructures should be accomplished on (001) substrates, the platforms in use in the production of semiconductors. We took the challenge of growing III-V compound semiconductor nanostructures on Si(001) to make a step further on their epitaxial integration on a such important surface. Surprisingly, in trying to grow InAs by solid source MBE, we discovered a new class of nanostructures which we called V-shape nanomembranes.

Our InAs V-shaped nanomembranes grow vertically aligned respect to the substrate and possess a peculiar V-shape, with two arms tilted ~34° respect to the substrate. This growth direction is consistent with the <111> direction of the substrate. The arms show two preferred directions of elongation, perpendicular between them in a top down projection: <110> and <1-10>. A schematic drawing of the InAs nanomembranes, represented with an oxide mask and substrate, is shown in figure 3.5.

Since these structure had never been examined before, the V-shaped nanomembranes required an in depth scanning electron microscopy (SEM) and transmission electron microscopy (TEM) analysis in order shed light on their morphology, crystal structure, epitaxial relationship with the substrate and on the polarity of the arms. These studies, done in collaboration with Dr. Philippe Caroff, are reported and detailed in Paper V.
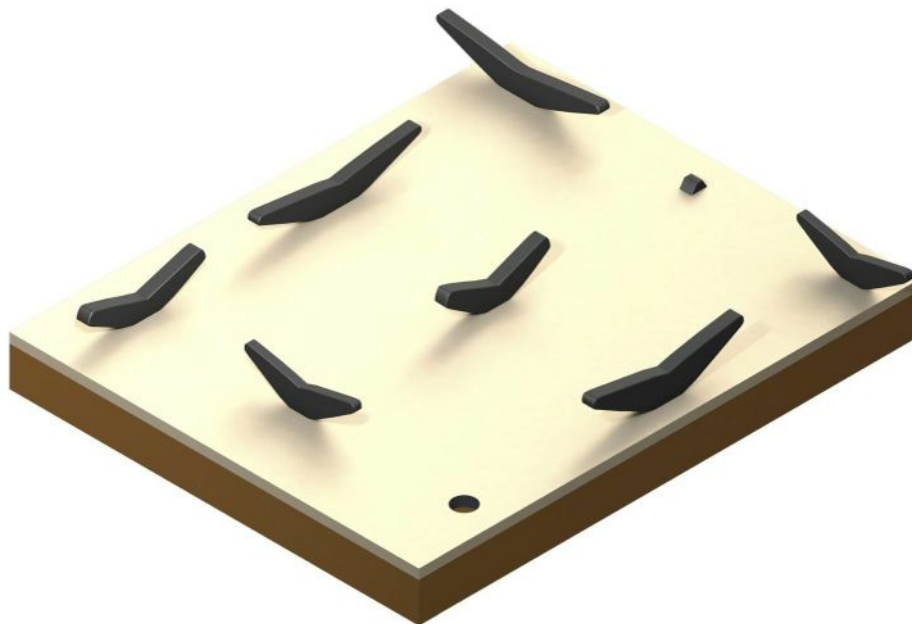
Figure 3.5: Schematic illustration of an array of InAs V-shaped nanomembranes. The V-shaped nanomembranes are positioned by means of nanoscale arrays of holes created in a thin SiO_2 mask. They grow perpendicularly to the Si(001) substrate, while their two constituent arms are tilted. These arms elongate in two perpendicular directions.

As a first step, we focused the attention on the InAs/Si (membrane/substrate) interface. The membranes and the silicon substrate are found to be in epitaxial relationship and their lattice mismatch of 11.7% completely relaxed. Interestingly, a triangular island (nucleus) from which the nanomembranes originate (figure 3.6 a-c) is present at the interface. This nucleus is responsible for the epitaxial relation with the substrate. It is delimited by a (100) bottom facet and two (11-1) and (1-11) inclined facets and its crystalline structure is pure zinc-blende (figure 3.6 c-d). The two arms grow from two opposite sides of the pyramid, with flat lateral facets corresponding to the low energy, non-polar (0-11) and (01-1) surfaces.

Unlike the central nucleus, the arms show a wurtzite phase. To fully determine their crystalline structure, an analysis of the polarity has been performed through Convergent Beam Electron Diffraction (CBED) at Lund University, in collaboration with Prof. Reine Wallenberg and Dr. Martin Ek. In this technique, converging the electron microscope beam to the sample causes the spots in the diffraction pattern to expand to discs. In this CBED pattern the effects of slightly different beam tilts on the diffraction can be observed simultaneously, with each beam tilt corresponding to a point within the discs. The polarity is determined by observing the differences in two opposite reflections and by comparison with a a simulated pattern. The growth direction of the arms was found to be <000-1>, indicating that both arms grow with a B
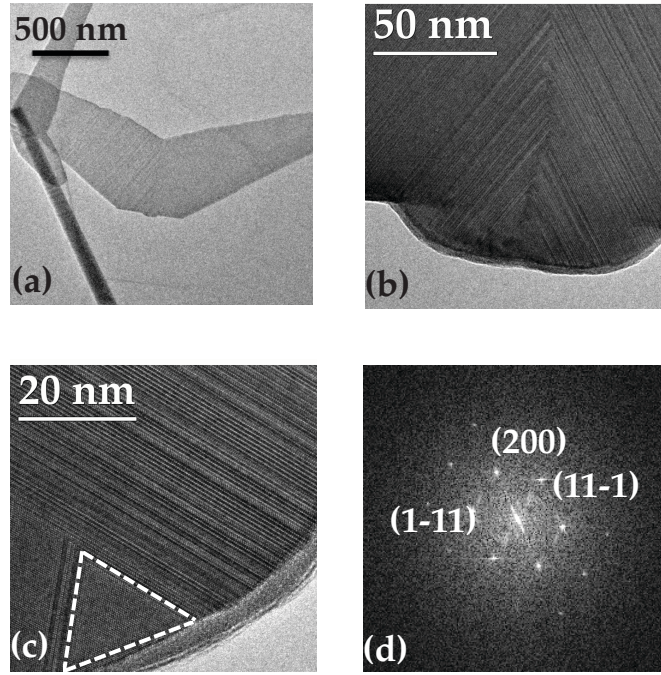
Figure 3.6: (a)TEM micrograph of a typical V-shaped membrane. (b-c) High resolution TEM image of central part of the structure and of the nucleus region. (d) Power spectrum of the nucleus indicating the zinc-blende structure.

polarity.

Under opportune conditions, such as small distances between the holes of the arrays or long growth times, the arms of the nanomembranes can be enough long to merge. We studied the merging of two membrane in high resolution TEM. Interestingly we found that the branches grow onto each other and form a triangular island with a defect-free zinc-blende phase. This island is similar to the one observed in the nucleation stage of the structure but 30 times larger. A similar sharp change of the crystal structure from wurtzite to perfect zinc-blende has been recently observed by Kang *et al.* in merging gold-assisted InAs NWs MBE grown on InAs(001) substrates [185]. In this work the transition between wurtzite and zinc-blend was not found to affect the conductance in merging wires thus envisaging that complex branched structures, like our nanomembranes, can become the basic building blocks for interconnected nanoelectronic devices.

The direction of elongation of the arms with respect to the substrate has been studied from an atomistic point of view by modeling the epitaxy between the InAs nucleus and the Si(001) surface. The occurrence of two preferred direction of elongation is linked to the presence of steps on the (001) silicon surface. As seen in section 2.4, we have two possible configurations of terraces, that are related by a 90° rotation (figure 3.7 a). In a cross-section along the (011) planes of the diamond and zinc-blende structure, the atoms typically arrange in hexagons forming a honeycomb network (figure 3.7). Let us start by considering that the As atoms are
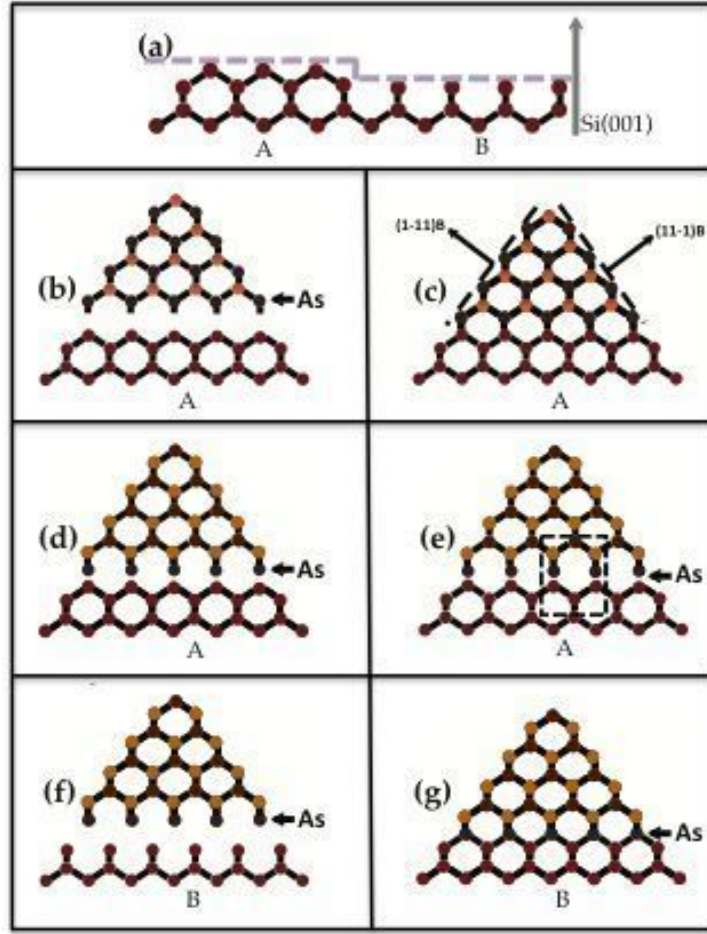
Figure 3.7: Atomistic model of the coupling between the (001) silicon substrate and the InAs nucleus. The red spheres represent the Si atoms, the brown and orange ones represent respectively As and In. (a) The Si(001) surface in cross-section along the (011) plane: the atoms arrange in hexagons forming a honeycomb network. The Si(001) surface is composed of terraces. Depending on where the surface is cut we have two types of configurations, A and B, related by a 90° rotation. (b) The atomic arrangement the InAs nucleus in cross-section along the (011) plane: the zinc blende structure arranges as diamond. (c) On terrace A it is allowed the completion of the honeycomb structure. This explain one direction of eleongation. (d) The same InAs nucleus rotated by 90° to explain the other direction of eleongation. (e) This configuration is not energetically allowed. (f)-(g) The honeycomb structure is completed on terrace B. The (111)B facets of the islands are oriented in one <011> direction or rotated by 90° depending on the type of terrace they start growing on.

the ones bonding directly with the silicon substrate. The atomic arrangement of the base of the InAs pyramid is illustrated in figure 3.7 b-g. In b) and c) the InAs nucleus is oriented so that the (111)B facets, on which the growth of the arms is allowed, are the ones at the left and right (configuration 1). In d)-g) the pyramid is rotated by 90°: here the (111)B facets are the one in the front and back and the membranes would grow perpendicularly compared to the case
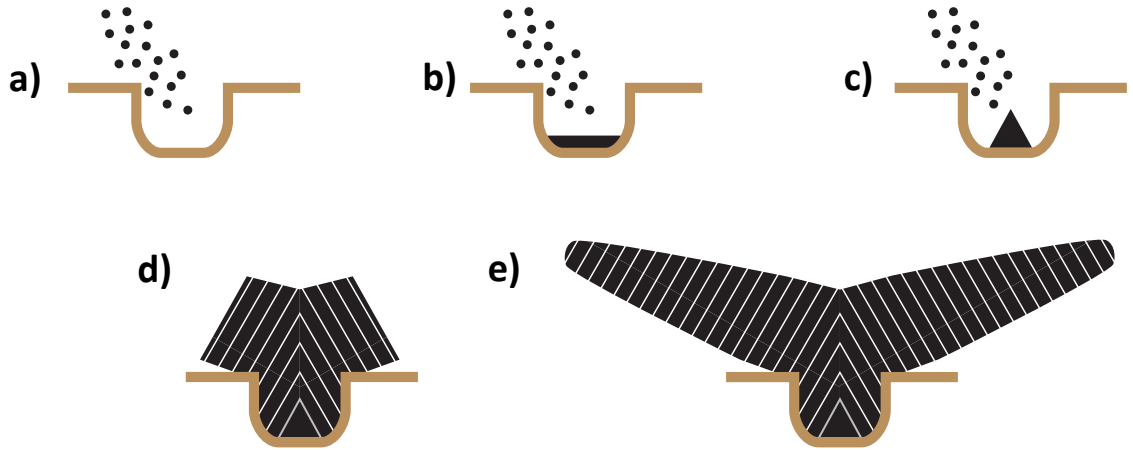
Figure 3.8: Growth mechanism of InAs nanomembranes.(a) After the opening of the sources, In adatoms reach the substrate and accumulate in the areas without oxide. (b) An InAs wetting layer starts to grow epitaxially. (c) A defect-free pyramidal shaped island form after the deposition of 1ML of InAs. This pyramid is bound by low index surfaces ({111} in our case) to minimize its total surface free energy. (d) The growth proceeds selectively on the (111)B facets of the pyramid. (e) The arms grow flat with facets corresponding to the low energy, non-polar (0-11) and (01-1) surfaces. On these planes the growth is slow compared to <111>B and occurs via birth-and-spread mode as the homogeneous thickness confirms.

depicted in b) and c) (configuration 2). Note that the atomic arrangement of base of the InAs nucleus is different in the two cases. For each type of Si terrace only one configuration of the InAs island is possible, i.e. the one that allows the completion of the hexagon that constitutes the basic building block of the honeycomb structure; this is configuration 1 for terrace type A and configuration 2 for terrace type B. This in turn determines the relative orientation of the B-polar facets of the pyramid, which are those enabling the fast membrane growth. As a consequence, the (111)B facets of the islands (and the membranes) will be oriented in one <011> direction or rotated by 90° depending on the type of terrace they start growing on. If the In atoms are the ones bonding directly with the silicon substrate we will observe a similar effect, the direction of the B polar facets will be simply rotated by 90° with respect to the previous one, i.e. configuration 1 will bond on terrace type B and configuration 2 will bond on terrace type A.

In Paper V we also provided a microscopic model for the formation of the InAs V-shaped nanomembranes. We speculate that the nucleation and growth of the nanostructures may occur as follows: in opportune growth conditions In adatoms migrate and accumulate only in the areas of the substrate without oxide (figure 3.8 a). Here an InAs layer starts to grow epitaxially (3.8 b). Following the theory of Stranski-Krastanov quantum dot (QD) formation, one can speculate that a defect-free pyramidal shaped island should form after the deposition of 1ML of InAs (3.8 c). This pyramid would be bound by low index surfaces to minimize its total surface free energy ({111} facets in our work). Subsequently, growth would proceed selectively on the two (111)B facets of the pyramid. On the two opposite {110} planes, birth-and-spread

growth mode is favored and the growth takes the form of complete layers with homogeneous thickness (3.8 d-e).

In Paper VI we provided a complete study of the effect of the growth conditions on the morphology of the membranes. In particular we systematically examined the role of the V/III ratio, substrate temperature, mask opening size and inter-hole distances in determining the size and shape of the membranes. Statistical information such as the length and width of the membranes have been obtained by scanning planar segmented images; eventual complications, like connected membranes, have been taken into account, as discussed in the paper. The analysis has been performed on overall ~16.000 structures, imaged in top view by SEM. We found that the membranes form by combining growth mechanisms of NWs and Stranski-Krastanov type QDs. In analogy with NWs, the length of the membranes strongly depends on the growth temperature and the V/III ratio; the inter-hole distance of the sample determines two different growth regimes: a competitive growth for small distances and an independent regime for larger ones. We found that the width of the nanomembranes is mainly determined by the lateral size of the initial pyramidal island. In analogy with QDs, the width of the membranes increases with the growth temperature and does not exhibit dependence on the V/III ratio.

The beam equivalent V/III ratio was found to also play a key role in determining the yield of the nanomembranes, i.e. how many nanostructures form respect to the total number of holes in the array. This work is reported in Paper VII. At low V/III ratio, only indium droplets are found on the surface. By increasing the V/III ratio, the nanostructures start to appear but the yield is still low: the growth is dominated by the formation of irregular islands. By increasing even more the V/III ratio, the islands progressively leave room to nanomembranes and the yield increases. It is worth noting that in addition to the V-shaped nanomembranes other nanostructures are also present on the sample: in particular we have observed NWs, growing with a 34° title in a growth direction consistent with the <111> direction of the substrate, and very few tripods. By optimizing the V/III ratio a maximum yield of nanomembranes of ~88% has been achieved. In general the relative occurrence of nanomembranes against NWs is very high (~90%), however the V/III ratio does not affect the relative occurrence of nanomembranes and NW: this means that in the optimal case roughly the 8% of the holes are occupied by NWs. Even if a significant and reproducible yield of nanomembranes has been achieved, the presence of NWs suggests that a step further in controlling the growth is still needed. We will discuss this point in following sections.

Through a fruitful collaboration with Prof. Luca Dal Negro at Boston University, the optical properties and the potentiality of the InAs V-shaped nanomembranes in applications have been investigated. These nanostructures show the ability to significantly localize and enhance electromagnetic radiation. Indeed, the nanomembranes have been excited with a plane wave propagating the (001) direction (i.e. perpendicularly respect to the substrate), with electric field polarization either parallel (i.e. parallel to the direction of elongation of the arms in (001) projection) or perpendicular. For transverse polarization, the field is uniformly distributed on

the lateral facets. Conversely, when the incident field is longitudinally polarized, the total field on the surface of the membrane is strongly localized at the tips of the arms and along the edges of the facets. The experiments also show the presence of distinctive optical resonances. Indeed, for both longitudinal and transverse excitation, a resonant scattering behavior controlled by the geometrical parameters of the nanomembranes exists.

Lastly, second harmonic experiments demonstrated that the V-shape morphology of the nanomembranes plays an important role in enhancing the second harmonic emission. The second harmonic intensity strongly depends on the width of the nanostructures and it increases by decreasing the width. An enhancement of the second harmonic generation of approximately a factor 500 compared to the signal measured in the case of a InAs bulk material has been observed for nanomembranes as thin as 70 nm. As such, the V-shaped nanomembranes possess an interesting potential as tip-enhanced nano sensors, light emitters and non linear optical elements (Paper V, [174]).

For applications in research areas where the shape of the nanostructures plays a major role, such as non linear optics as explained above, or energy storage and energy generation, a new degree of freedom in the engineering of bottom-up nanostructures is represented by the ability to control the shape of the structures. Very intriguing is the possibility to switch between different shapes within the same material system for example by inducing new branches or by directly crystallize the material in different configurations. In Paper VII we experimentally demonstrated a simple method for controlling the shape of the nanostructures: we showed the ability to move from the growth of V-shaped nanomembranes to the growth of NWs without changing the growth conditions but by modulating the surface roughness of the substrate.

As mentioned before, when growing InAs V-shaped nanomembranes on Si(001) substrates, tilted NWs are always found on the sample, although in small occurrence. A high resolution TEM analysis of several InAs NWs gave the evidence that nanomembranes and NWs rely on two different growth mechanisms. While the V-shaped nanomembranes originate from two opposite facets of a rectangular pyramidal nucleus, at the bottom part of the NWs any nucleus has been found. This suggested that the formation of QDs through the SK growth mode is suppressed in the holes of the array where NWs appear.

In Paper VII we then examined the possibility to promote or quench the appearance of nanomembranes or nanowires respectively by favoring or suppressing the SK growth mechanism. As seen in section 2.4.1, the formation of SK type of QDs on patterns can be suppressed if the opening areas are smaller than a critical value. Indeed, if QDs are grown in confined area like holes, they show an aspect ratio higher than on a free surface. This causes an increase in surface energy that scales up with reducing the hole size. If the holes are too small, the energy penalty is so high that islands formation is not longer energetically favored and the SK growth mechanism is suppressed. This led us to fabricate arrays with smaller holes and to investigate growth in such structures.

To realize a pattern with smaller holes we modified the etching step: we replaced the wet etching (isotropic, inevitably it changes the diameter of the holes) with a dry etching (anisotropic). We found that small holes actually favor the growth of NWs over nanomembranes offering a first way to modulate their relative occurrence. However, unexpected results, like a higher occurrence of NWs in lager holes, prompted us to perform further TEM analysis.

A cross sectional high resolution TEM analysis performed on holes obtained by dry and wet etching showed that the nanoscale features have two completely different morphologies: unlike the case of wet etching, the holes defined with dry etching show a deep dig in the crystalline silicon. This penetration in silicon together with the fact that the dry etching involves a ion bombardment, made us speculate that the surface at the bottom of the hole is rougher that the one obtained with a wet etching. This means that the real driver in controlling if nanomembranes or NWs are favored is not as much the hole size *per se* but the roughness of the substrate. A small hole size simply increases the probability of having a too small confined areas, favoring in turn the growth of NWs.

We confirmed our finding by preparing samples with a rougher or smoother surface at the bottom of the holes. In line with our theoretical framework, the relative occurrence of wires increased on the rougher surface and decreased on the smoother one, independently from the hole size. The ability to manipulate the shape of the nanostructures, like moving form nanomembranes to NWs, represents a further step in the fabrication of advances interconnected nano devices and nanosystems.

ARTICLE

Vertical "III−V" V-Shaped Nanomembranes Epitaxially Grown on a Patterned Si[001] Substrate and Their Enhanced Light Scattering

Sònia Conesa-Boj,[†,¶] Eleonora Russo-Averchi,[†,¶] Anna Dalmau-Mallorqui,[†] Jacob Trevino,[‡] Emanuele F. Pecora,[‡] Carlo Forestiere,[‡,§] Alex Handin,[‡] Martin Ek,[⊥] Ludovit Zweifel,[†] L. Reine Wallenberg,[⊥] Daniel Rüffer,[†] Martin Heiss,[†] David Troadec,[⊥] Luca Dal Negro,[‡] Philippe Caroff,[∥] and Anna Fontcuberta i Morral[†,*]

[†]Laboratoire des Matériaux Semiconducteurs, Ecole Polytechnique Fédérale de Lausanne, 1015 Lausanne, Switzerland, [‡]Department of Electrical and Computer Engineering & Photonics Center, Boston University, 8 Saint Mary Street, Boston, Massachusetts 02215, United States, [§]Department of Electrical Engineering, Università degli Studi di Napoli Federico II, via Claudio 21, Napoli 80125, Italy, [⊥]nCHREM/Polymer & Materials Chemistry, Lund University, Box 124, S-22100 Lund, Sweden, and [∥]Institut d'Electronique, de Microélectronique et de Nanotechnologie, UMR CNRS 8520, Avenue Poincaré, B.P. 60069, 59652 Villeneuve d'Ascq, France. [¶]These authors contributed equally to this work.

ABSTRACT We report on a new form of III−V compound semiconductor nanostructures growing epitaxially as vertical V-shaped nanomembranes on Si(001) and study their light-scattering properties. Precise position control of the InAs nanostructures in regular arrays is demonstrated by bottom-up synthesis using molecular beam epitaxy in nanoscale apertures on a SiO$_2$ mask. The InAs V-shaped nanomembranes are found to originate from the two opposite facets of a rectangular pyramidal island nucleus and extend along two opposite ⟨111⟩ B directions, forming flat {110} walls. Dark-field scattering experiments, in combination with light-scattering theory, show the presence of distinctive shape-dependent optical resonances significantly enhancing the local intensity of incident electromagnetic fields over tunable spectral regions. These new nanostructures could have interesting potential in nanosensors, infrared light emitters, and nonlinear optical elements.
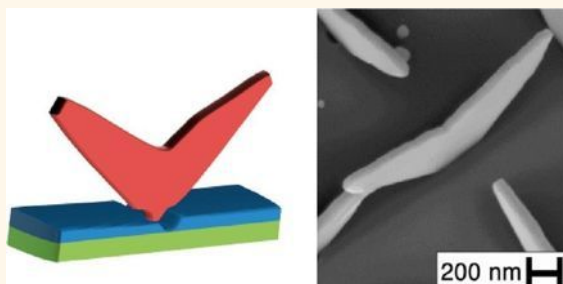
KEYWORDS: III−V nanostructures · nanomembranes · V-shape · nucleation · light scattering

In the last few decades, there has been both in fundamental and applied science a constant effort in reducing the size of semiconductor structures with composition, crystal structure, and morphology controlled down to the nanoscale.[1−3] One of the advantages of nanostructures over traditional thin film technology is the third dimension component resulting in the possibility of reaching complex architectures, impossible by other means. A large variety of shapes have been controllably achieved, spanning from nanomembranes or nanowalls,[4−10] nanotrees,[11] nanoflowers,[12,13] to nanowires.[14−16] Concurrently, nanowires have also enabled three-dimensional hierarchical structures by the formation of tripods,[17] tetrapods,[18] and more generally branched nanostructures.[19−24] This adds a significant versatility from the point of view of material design because these nanostructures can intrinsically integrate p−n junctions and heterostructures such as quantum dots, barriers, and quantum wells.[25,26]

Silicon is the most widely used semiconductor in integrated circuits, while III−V semiconductors are used in optoelectronics and in radio frequency applications, such as digital wireless communications. Most of today's electronics relies on silicon, due to optimal electronic properties and ease of micro-to-nano fabrication. Heterogeneous integration of silicon of III−V compound semiconductors, which have a direct band gap and high carrier mobilities, is thus an exciting challenge as it would lead to a

combination of the best properties of both semiconductor classes. However, traditional III−V thin film integration on silicon has shown to be extremely challenging due to the lattice, thermal, and polarity mismatches.[27] Free-standing nanoscale structures offer the possibility of epitaxial integration on mismatched group IV substrates. Their small footprint and single nucleation event per nanostructure guarantee an extremely reduced probability for antiphase domain boundary formation and an efficient elastic strain relaxation at the interface—even though the defect density is not zero even for small diameter nanostructures.[28−30]

Several approaches have been investigated for the integration of III−V semiconductors and silicon: heteroepitaxial growth using metalorganic chemical vapor deposition,[31] direct epitaxy (which suffers from lattice and polarity mismatch),[32] growth of a graded SiGe buffer layer for GaAs,[33] and Sb-based metamorphic layers,[34,35,36] wafer bonding,[37,38] and localized epitaxy[39] in nanoscale areas forming nanowires.[40] Recently, gold-free III−V nanowires have been used in high-performance vertically integrated transistors, opening a real perspective for high-performing materials integrated on Si.[41] Additionally, growth achieved on [001]-oriented substrates would bring the integration with current technological processes closer, while at the same time it would result in the reduction of structural defects in nanowires.[42,43] To the best of our knowledge, no example of gold-free vertical III−V nanostructures epitaxially grown on Si(001) has yet been reported. Finally, growth of III−V semiconductors on Si should be obtained in an ordered manner, as this allows for precise positioning of masks and contacts, thus greatly facilitating rational device processing.

In this work, we explore a new form of III−V nanostructures, grown epitaxially on (001) silicon substrates by solid source molecular beam epitaxy (MBE). The nanostructures are self-catalyzed (gold-free) and positioned by means of nanoscale hole arrays created in a thin SiO_2 mask. Surprisingly, we find that instead of nanowires, which were reported for growth on Si(111),[44−48] wing-shaped single-crystalline epitaxial membranes grow perpendicularly to the Si (001) substrates. (While the nanomembranes grow vertically aligned with respect to the substrate, it will be clear from the geometry that its two constituent wings are tilted with respect to the substrate.) We show that the nucleation of these wing-shaped nanostructures originates from an initial nanoscale pyramidal island nucleus. While nucleation occurs in zinc blende phase, the growth of the wings (membranes) occurs mostly in wurtzite phase. Finally, by combining dark-field scattering measurements and light-scattering theory for arbitrarily shaped dielectrics within the accurate surface integral equation (SIE) method,[49] we demonstrate the presence of distinctive shape-dependent optical resonances that can significantly enhance the local intensity of the incident electromagnetic fields over tunable spectral regions. These findings, in combination with the large surface-to-volume ratio offered by these novel dielectric nanostructures, provide a novel approach for the manipulation of nanoscale optical fields and light−matter interactions on a Si substrate, potentially enabling a number of device applications such as enhanced nanosensors, light emitters, and nonlinear optical elements.[50]

RESULTS AND DISCUSSION

General Morphology, Growth Directions, and Epitaxial Relationships. Scanning electron microscopy (SEM) images of the V-shaped membrane structures are shown in Figure 1a−e with various tilt and rotation angles and increasing magnifications from panels c−e. Figure 1a, showing a low-magnification planar view, illustrates the two preferred elongation directions and the vertical feature of the nanostructures, with respect to the substrate. Indeed, after 1 h of growth, membranes between 0.5 and 2 μm long are found to extend along two perpendicular directions in a top-down projection: ⟨1−10⟩ and ⟨110⟩. The membrane thickness shown in the micrographs is about 170 nm, and their flat nanowalls are bound by {110} planes. Overall, depending on the growth conditions and time, the membranes exhibit thicknesses between 50 and 200 nm. The tilted images shown in Figure 1b−e reveal the V-shape of the nanostructures, with arms branching toward two ⟨111⟩ directions. The membranes nucleate in the holes of the SiO_2 mask (see schematic in Figure 1f). To investigate the epitaxial relationship between these nanostructures and the substrate, focused ion beam (FIB)-assisted lamellas were prepared along the ⟨110⟩ and ⟨1−10⟩ directions of the substrate. A low-magnification SEM image of one of these lamellas, prepared for inspection by transmission electron microscopy (TEM), is shown in Figure 1g, illustrating connected nanostructures and part of the Si substrate on which they grew. The cross-sectional lamellas were studied by high-resolution TEM focusing on the InAs/Si interface. The interface region for a single nanowing is shown in Figure 1h and in Figure 1i with lattice fringe resolution. A fast Fourier transform (FFT) was calculated from the image of Figure 1i, confirming the epitaxial relationship and the relaxed mismatch of 11.6% between the membrane and the substrate, as shown in Figure 1j.

An analysis of the merging between two membranes is shown in low- and high-resolution TEM in Figure 1k−m. The fringes from each of the branches as well as the interface can be observed. Interestingly, the branches grow onto each other, forming a triangular island with a defect-free zinc blende phase growing in the (001) direction (see diffractogram in Figure 1n). This island is similar to the one observed in the nucleation stage of the structure, with the only difference being that the size is about 30 times larger. The base is about
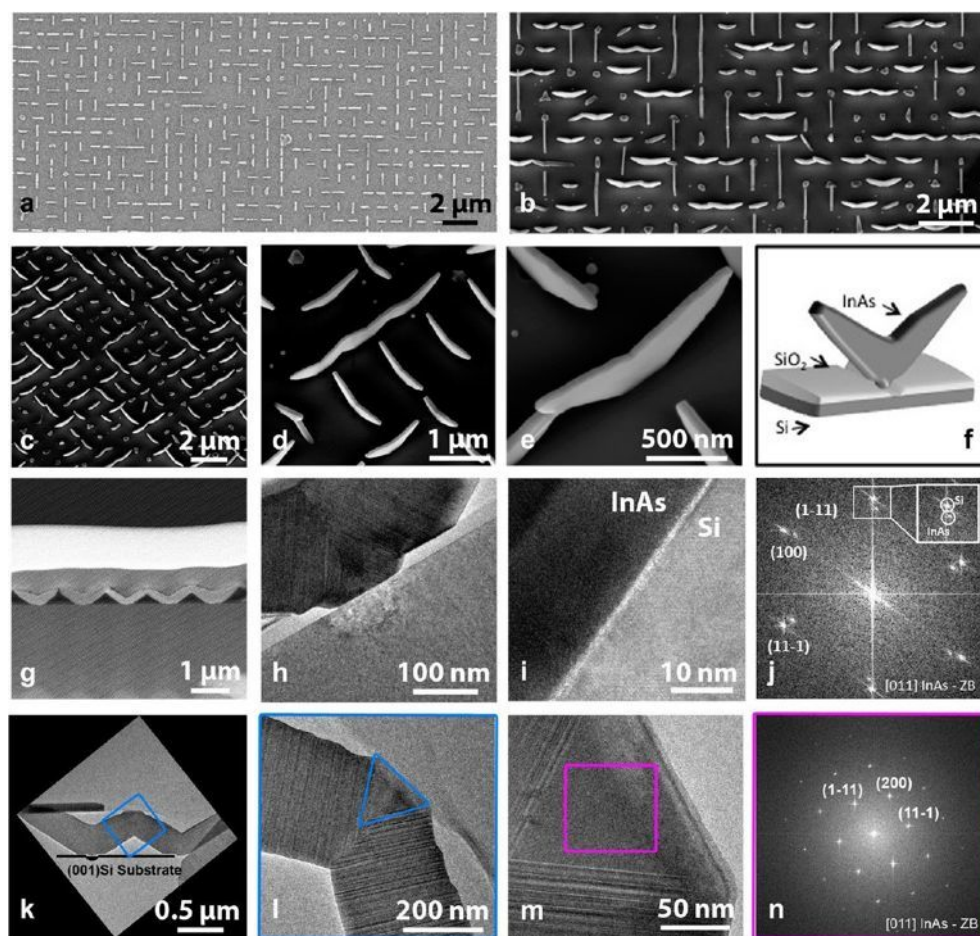
Figure 1. (a−e) Scanning electron microscopy (SEM) images of typical InAs membranes grown at 500 °C under an As_4 partial pressure of 8×10^{-6} Torr. (a) Planar view image, (b) tilted view (30°), and (c−e) tilted views with additional in-plane rotation of 45°. Different scales are presented in order to reveal the intermembrane ordering and the local structure. (f) Schematic of one V-shaped nanomembrane, represented with an oxide mask and substrate. (g) Low-magnification SEM image of a FIB-prepared, perpendicular TEM lamella showing connected wing-shaped nanomembranes. (h) High-resolution TEM image of the nanostructure/silicon interface, with clearly visible contrast probably due to ion-beam-damaged fields in the substrate part. (i) Lattice-fringe-resolved TEM image of the InAs/Si interface, and (j) associated fast Fourier transform (FFT) revealing their epitaxial relationship and differences in lattice parameters. (k,l) Low-magnification images of the region where two wings merge. (m,n) HRTEM image of the merging area exhibiting a perfect zinc blende crystalline structure, as shown by the corresponding diffraction pattern in (n).

150 nm long. This seed could eventually be used in the future to nucleate nanostructures growing in the (001) directions on a silicon substrate.

Internal Crystal Structure of the V-Shaped Nanomembrane and Its Nucleus. Interface and Polarity. Having determined the general morphology of the V-shaped nanomembranes, growth directions, and epitaxial relationship with respect to the substrate, we now turn to their detailed internal crystal structure. Figure 1h shows low-resolution TEM micrographs of the base of the InAs nanostructures grown at 520 °C, 1.15×10^{-5} As_4 Torr, and In nominal rate of 0.2 Å/s. The first distinguishing feature is the presence of the two arms extending from a central base. A small "foot" is clearly visible in the

center of the V-shape, which corresponds to the part of the membrane forming the interface with the Si substrate (Figure 3c). This foot has the same dimensions as the hole diameter in the SiO_2 mask (80 nm long and 20 nm thick). Interestingly, we find a triangular island (nucleus) at the central part of the structure. From this point, the two arms grow in a ≈19° angle consistent with the ⟨111⟩ direction of the substrate. The wings are flat with a slightly triangular shape. The flat facets correspond to the low-energy nonpolar (0−11) and (01−1) surfaces. A similar nucleation stage was observed in the case of tetrapod formation in other material systems, although only connected to the substrate *via* van der Waals interactions in those cases.[17]
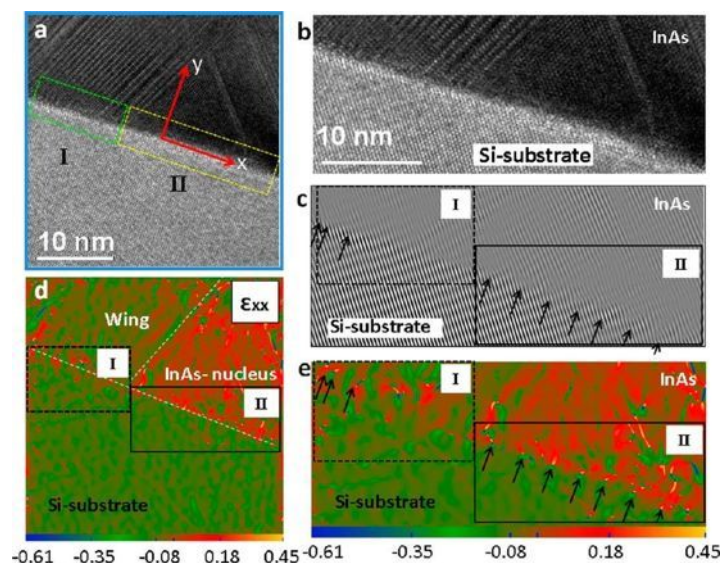
Figure 2. (a,b) Detail on the cross-sectional high-resolution TEM images taken at the interface between the InAs V-shaped nanomembrane and the Si substrate. Regions corresponding to the pyramidal nucleus and the V-shaped membrane are marked, respectively, with a yellow (II) and green (I) square. (c) Inverse Fourier transformation image obtained by masking $(11-1)$, which enables the visualization of the dislocations (marked with arrows). The distance between dislocations at the pyramidal island level is about 2.5 ± 2 nm, while they become more sporadic in the region of the V-shaped membrane. (d,e) Strain maps estimated from image in (a). The arrows in (c) indicate the position of local strain.

The nature of the interface between the InAs and the silicon is important for applications in which the membranes should be linked electronically with the substrate. A typical HRTEM image of the interface is shown in Figure 2a,b. We distinguish two regions, corresponding (I) to the V-shaped membrane and (II) to the pyramidal nucleus. The mismatch between InAs and Si is 11.6%, meaning that the accommodation should create some misfit dislocations, as observed in the case of nanowires grown on Si. We have filtered the image from Figure 2a by selecting the diffraction spots $(11-1)$ from InAs and Si in order to determine the possible existence of misfit dislocations. This is shown in Figure 2c. We indicate with arrows the positions where a misfit dislocation appears, shown by the discontinuity between the planes from Si to InAs. In the pyramidal region of the sample, dislocations are separated by about 2.5 ± 2 nm, in agreement with what was obtained by other groups with InAs nanowires on Si. Interestingly, the presence of dislocations in the region outside the pyramidal nucleus becomes more random and sporadic. We believe this is a consequence from the growth mechanism: the InAs nucleus grows directly on the Si substrate, while the wings grow/form directly on the facets of the pyramid. This is further supported by the strain analysis shown in Figure 2d,e. The pyramidal nucleus and the wings of the membrane exhibit a clearly different strain. In fact, the wings appear to be relatively relaxed, while the nucleus is highly strained.

A low-resolution HRTEM of a typical V-shaped membrane is shown in Figure 3a–c. The two wings

are separated by a grain boundary at the interface, as can be seen in Figure 3b,c. Stripes of different contrast are observed along the two arms perpendicular to the growth direction, indicating the presence of planar defects, discussed further in the following. Because silicon is a nonpolar semiconductor, whereas III–V semiconductors are polar, it is of interest to evaluate the polarity of the membranes. Convergent beam electron diffraction (CBED) was used for this purpose. The CBED patterns are shown in Figure 3d with the corresponding computer-simulated pattern used for confirming the interpretation. By comparing the simulated CBED pattern with the measured one, we confirm that the growth direction is along the $[000-1]$ direction, indicating that both arms grow with a B polarity (group-V-terminated). This procedure was repeated for several nanowings, and in every case, we found the growth direction to be $[000-1]$.

As it has been shown above, HRTEM micrographs of the interface of the membranes with the substrate reveal that the nucleus of the structure consists of a triangle defined by a (100) bottom facet and two $(11-1)$ and $(1-11)$ inclined facets (Figure 4a). The triangle crystal structure is pure zinc blende, as confirmed by the diffractogram (Figure 4b). Figure 4c corresponds to an atomic force microscopy (AFM) measurement of a nucleus obtained after 5 min of growth. A truncated pyramid with the facets parallel to the directions $\langle 011 \rangle$ and $\langle 0-11 \rangle$ is observed. The flat top of the pyramid contrasts with the perfect triangular shape observed in HRTEM. Now the question is what
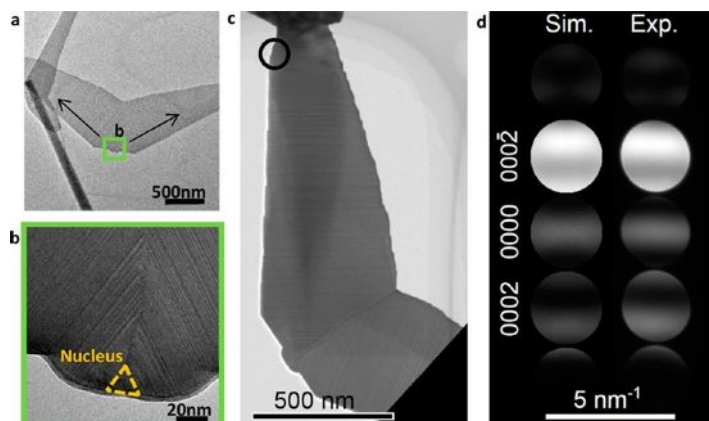
Figure 3. (a,b) TEM micrograph of a typical V-shaped InAs nanostructure. All the V-shaped InAs nanostructures analyzed exhibit distinguishing features: a nucleus region in the base and two arms coming out of this nucleus. (c) Bright-field TEM image of an arm of the V-shaped InAs nanostructures; (d) experimental and simulated ⟨14−50⟩ CBED patterns of the arm, respectively. CBED patterns were simulated for thicknesses of 30−150 nm with the JEMS software, and the best match was selected (in this case 45 nm).

the relation between the orientation of the nucleus and that of the membrane with respect to the substrate is.

In order to provide some insight on the possible orientation mechanisms of the membranes on the substrate, the initial stages of growth are discussed from the atomistic point of view: atomic models are constructed to illustrate the epitaxy between the InAs island and the Si(001) surface. A top view of this model showing a pyramidal seed oriented in the two [011] zone axes is shown in Figure 4d. The atomic modeling of the interface between the InAs pyramidal seed and the Si substrate needs to consider two elements: (i) the structure of the Si(100) formed by terraces (implying the presence of single or double steps) and (ii) the polarity of the interface between the seed and the substrate, being B or A depending if As or In atoms are the ones bonding directly with the Si substrate, respectively. The role of the Si surface structure and polarity is illustrated in Figure 5, where we sketch the cross section of the four types of structures cutting along a ⟨011⟩ direction.

Figure 5a,b illustrates the atomic configuration of As and In atoms on a silicon surface. In the cross section along the (011) planes of diamond and zinc blende structure, the atoms typically arrange in hexagons, forming a honeycomb network. Depending on where the Si(100) surface is cut, we have two types of configurations of the Si surface, as shown in Figure 5a,b. Other reports have shown that the two surface atomic configurations exist and that the surface is composed of terraces with one or the other configuration.[51−53] The oxide formation and subsequent removal in perfectly flat Si(100) also results in the creation of terraces.[54] The two configurations are related by a 90° rotation. Now, we consider at the atomic arrangement of the base of the InAs pyramid, arbitrarily fixing the interface as As−Si (A polarity

of the interface). This is illustrated in Figure 5a,b. For each type of Si terrace, only one configuration of the InAs island is possible: the one that allows the completion of the hexagon, as indicated in Figure 5a,b. This determines the relative orientation of the facets of the pyramid being B polar, which are the ones enabling the fast membrane growth. As a consequence, the (111)B facets of the islands (and the membranes) will be oriented in one [011] direction or rotated by 90° depending on the type of terrace they start growing on. A similar effect is observed if one considers that the interface is formed by As−Si bonds (A polarity at the interface), as illustrated in Figure 4c,d. In this case, the direction of the B polar facets will just be rotated by 90° with respect to the precedent one. The fact that the ratio between the two membrane orientations is about 50%, under the growth conditions detailed in the Methods section, lets us suspect almost all of the seeds may have the same polarity. In the case of GaAs nanowire growth on Si(111), however, the two polarities (A and B) at the interface have been observed on the same sample.[55] Furthermore, it has been shown that certain growth conditions influence in a deterministic manner the polarity at the interface with the substrate.[56,57] In our case, it will be necessary to perform statistical measurements of the seed polarity, obtained with a large set of different growth conditions, before one can confirm the prevalence of one scenario over the other.

The nucleation and growth of the InAs membranes may occur as follows. InAs growth is performed under temperature and flow conditions such that adatoms only incorporate in the areas of the substrate without oxide.[58] In the initial stages of growth, InAs grows epitaxially on the open Si openings of the mask. Following the theory of Stranski−Krastanov quantum dot formation, one can speculate that a defect-free pyramidal-shaped island should form after the deposition
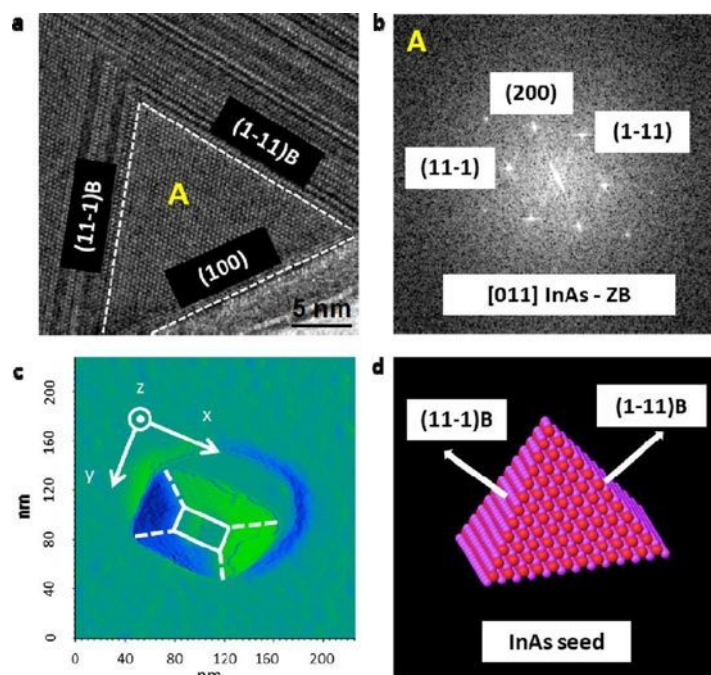
Figure 4. (a) HRTEM of the nucleus, indicating the interface with the substrate Si(100) and the membrane wings. (b) Power spectrum of the nucleus indicating zinc blende structure, (c) atomic force micrograph of the nucleus obtained after 5 min growth and the corresponding atomistic model in (d).
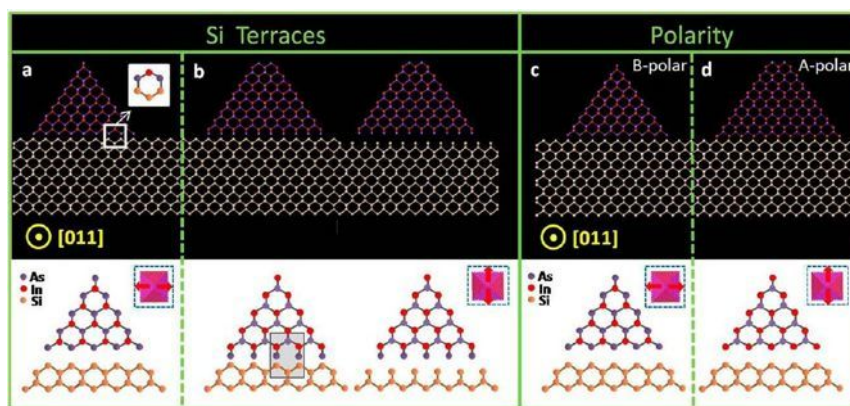
Figure 5. Atomistic model of the coupling between the [001] Si substrate and the InAs pyramid. The orange spheres represent Si atoms, while the blue and red represent, respectively, As and In. The coupling of the Si terrace with the InAs island depends on the type of termination on both sides of the interface. We plot the possible configurations depending on the type of Si terrace and polarity of the seed.

of 1 ML of InAs. This pyramid would be bound by low index surfaces to minimize its total surface free energy, in agreement with the {111} facets observed in this work. Subsequently, growth would proceed selectively on the two (111)B facets of the pyramid. On the two opposite {110} planes of the membrane, nucleation is relatively slow compared to the following step-flow, hence birth-and-spread growth mode is favored, and lateral growth takes the form of complete layers, explaining the absence of tapering (homogeneous thickness).

Light-Scattering Experiments and Electromagnetic Modeling. The light-scattering and localization properties of metal–dielectric nanostructures have recently attracted considerable attention due to the possibility of engineering light–matter coupling at the nanoscale for a number of nanophotonic device applications.[59,60] In particular, the shape-dependent resonances of conduction electrons in metallic nanostructures, known as nanoplasmonic resonances, are widely investigated for their ability to concentrate electromagnetic fields over
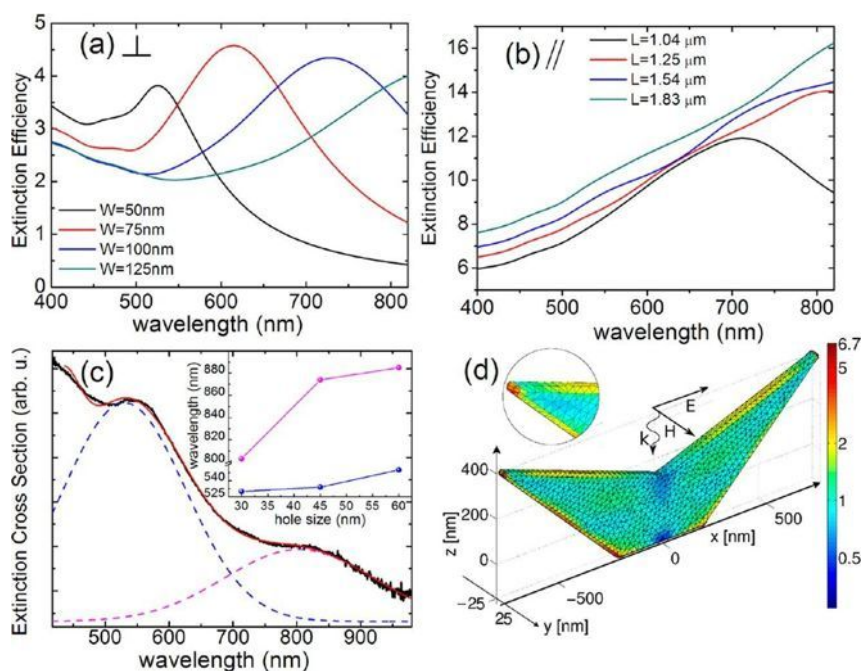
Figure 6. (a) Extinction efficiency spectrum for an isolated nanowing with fixed length $L = 1.54$ μm and for varying width W, excited by a plane wave propagating in the direction of the negative z-axis and polarized along y (transverse to the V, see panel d for the reference system). (b) Extinction efficiency for a nanowing with fixed width $W = 50$ nm and for varying length L, excited by a plane wave polarized along x (parallel to the V). (c) Scattering cross section as a function of the wavelength. The experimental spectrum has been fitted by two Gaussian line shapes (dotted lines), and their sum (red continuous line) is compared with the experimental data (black continuous line). (Inset) Peak wavelength of the two peaks extracted from the experimental data as a function of the hole size. (d) Distribution of the magnitude of the electric field calculated at $\lambda = 800$ nm (in logarithmic scale) on the surface of a nanowing with $L = 1.54$ and $W = 50$ nm excited by a plane wave polarized along x. In the inset of panel d, a zoom of the field distribution in proximity to the left corner is reported.

subwavelength regions, leading to significant electric field enhancement at the nanoscale. Moreover, resonant light scattering by nanoscale structures with high refractive index can also lead to largely tunable optical resonances in purely dielectric materials.[61−63] However, this approach is currently limited to the engineering of Mie scattering resonances in highly regular nanostructures, such as semiconductor nanowires, which offer great spectral tunability but only limited local field concentration.

The control of dielectric nanostructures with highly asymmetric shapes and irregular geometries featuring sharp tips, such as the ones demonstrated by V-shaped membranes, provides a largely tunable approach for the engineering of strongly confined resonant fields on Si. In the following, we investigate the distinctive light-scattering properties of these novel dielectric nanostructures using a highly accurate formulation of the surface integral equation (SIE) method.[49] Further details on the calculations are discussed in the Methods section.

In Figure 6a,b, we show the calculated wavelength spectra of the extinction efficiencies for a representative nanowing structure normally excited by a monochromatic plane wave with electric field polarization

either perpendicular (Figure 6a) or parallel (Figure 6b) with respect to the $x-z$ axis shown in Figure 6d. The results in Figure 6a correspond to structures with different widths W and a constant length $L = 1.54$ μm, as defined in Figure 6d. A clear resonant behavior, controlled by the thickness of the wall, is predicted for the scattering of the transverse excitation mode of the structure. These resonances gradually red shift by increasing the wall thickness. In the case of parallel excitation in Figure 6b, we obtain a similar resonant scattering behavior but shifted to longer wavelengths, consistently with the significantly larger polarizability probed along this polarization direction, resulting in the excitation of a longitudinal mode in the structure. In Figure 6b, the results are shown for different lengths of the walls, while keeping the thickness fixed at 50 nm.

In Figure 6c, we show the experimentally measured extinction spectrum of the nanowing structure excited by incoherent white illumination, which demonstrates the presence of the two well-defined resonances theoretically predicted and corresponding to the longitudinal and transverse modes of the structure. Moreover, the peak positions of the experimentally measured modes red shift by increasing the size of the nanowing structures, as demonstrated by the inset of Figure 6c

for a number of investigated structures. The spectral positions and the line shapes (obtained by Gaussian deconvolution) of these two modes have also been found to be in good agreement with our theoretical predictions. However, we notice that the experimental dark-field excitation conditions introduce a spectral broadening with respect to the theoretical spectra, which are calculated under normal incidence illumination.[64,65] Therefore, the agreement between the measured and calculated spectra, though well capturing all of the relevant features of the experimental scattering behavior of V-shaped membranes, should be considered only qualitatively. Finally, in Figure 6d, we plot the calculated electric field distribution on the surface of the nanowing structure, best representing the one measured in Figure 6c, at the resonant longitudinal frequency. The ability of the fabricated nanostructures to localize and to significantly enhance (*i.e.*, by over a factor of 6) the electric field at the tips of the nanowing is clearly demonstrated by Figure 6d. The highly tunable scattering response of the fabricated nanowing structures along with their ability to significantly localize and enhance electromagnetic radiation at controllable tip locations can provide an alternative approach for the manipulation of nanoscale optical fields on a Si substrate for a number of device applications, such as tip-enhanced nanosensors, light emitters, and nonlinear optical elements in a purely dielectric platform.

CONCLUSIONS

In conclusion, we have reported on a new form of III—V compound semiconductor nanostructures growing epitaxially as vertical V-shaped membranes on Si[001]. Precise position control of the InAs nanostructures in regular arrays has been demonstrated by bottom-up synthesis using molecular beam epitaxy in nanoscale apertures on a SiO_2 mask. The InAs V-shaped nanomembranes originate from the two opposite facets of a rectangular pyramidal island nucleus. At the same time, when the tip of the membranes merge, we observe the formation of a relatively large defect-free zinc blende island developing in the [001] direction. By tuning growth parameters and pattern geometry, the nanomembranes can be engineered to connect and thus create controllable hierarchical structures. We also determined the presence of distinctive shape-dependent optical resonances significantly enhancing the local intensity of incident electromagnetic fields over tunable spectral regions. These V-shaped nanomembrane structures have an interesting potential in applications as nanosensors, infrared light emitters, and nonlinear optical elements.

METHODS

Growth. The InAs membranes were synthesized by molecular beam epitaxy in a DCA P600 system. Growth has been performed on patterned $\langle 100 \rangle$ p-doped silicon wafers with cut off of $0 \pm 0.5°$ and a resistivity of $0.1-0.5$ Ωcm. The growth mask consisted of a 20 nm thick SiO_2 layer of thermal oxide, which was patterned following typical nanofabrication methods as reported elsewhere.[45,66,67] Special care was taken to ensure a perfectly clean and oxide-free surface in the holes. Prior to the introduction to the MBE reactor, we performed a 2 s dip in a solution of buffered HF (BHF, 7:1) and kept the sample in isopropyl alcohol until it was introduced in the load lock. The substrates were subsequently degassed at 600 °C for 2 h. Just before the growth, they were heated to 770 °C for 30 min to further remove possible surface contaminants. The growth was carried out at a nominal In growth rate of 0.2 Å/s, As_4 partial pressure between 0.8 and 1.15×10^{-5} Torr, at a temperature between 500 and 520 °C, and with 7 rpm rotation.

Electron Microscopy. To analyze the crystalline structure of the InAs membranes, we used a Phillips CM300 electron microscope operated at 300 kV from the Centre Interdisciplinaire de Microscopie Électronique (CIME) at EPFL Lausanne. For the determination of the polarity of the same membranes, we used the JEOL 3000F electron microscope at n-CHREM at Lund University, operating in TEM mode at 300 kV. CBED patterns were acquired in the wurtzite $\langle 14-50 \rangle$ zone axis and compared to patterns simulated by the Bloch wave method in JEMS. The $\langle 14-50 \rangle$ zone axis was chosen due to the clear asymmetric contrast in the (0002) and (000−2) discs and since it requires less tilt from the preferred $\langle 11-20 \rangle$ orientation of the nanowings than the alternative $\langle 1-100 \rangle$.

A perpendicular TEM lamella was prepared by standard means, using focused ion beam and a micromanipulator on protected as-grown V-shaped membranes, specifically to obtain information about the epitaxial relationship with the substrate. For all other analyses, we performed the simple sample preparation, where the InAs membranes were mechanically transferred to a holey carbon grid, to be then studied with the two electron microscopes.

Optical Scattering Measurements. Optical scattering measurements were performed under incoherent white light illumination (broad-band halogen lamp) using a custom-made dark-field microscope set up with a 50× long-working distance objective (NA = 0.75), and spatial filtering at the detector was used for background noise reduction. Scattered light was collected into a fiber-coupled CCD spectrometer (Ocean Optics QE65000). The same setup was used also for imaging and aligning the sample in order to ensure overlap between the illuminated area and the patterned structures. For this purpose, the output of the objective was sent also to a camera sensitive to visible light (Apogee Alta U4000 camera w/KAI-4022 CCD). All of the scattering spectra were background-corrected with respect to the normalized emission line shape of the excitation lamp, the detector sensitivity, and the system's collection efficiency.

Electromagnetic Simulation. Electromagnetic scattering calculations were performed according to a recently developed SIE method. The integral formulations of the Maxwell equations were very effective to treat the scattering from large arbitrary shaped particles since they require only the discretization of the spatial domain occupied by the scatterers, while the radiation conditions at infinity are naturally satisfied. In particular, the surface integral equations (SIE), which are based on the equivalent theorem for the electromagnetic fields, only require a discretization of the surface of the scatterers. Some of the most widely used SIE formulations are the PMCHWT (Poggio, Miller, Chang, Harrington, and Wu) formulation,[68] and the null field method (NFM).[69] Only in the past few years, those methods have been applied to the electromagnetic scattering by plasmonic nanostructures. In particular, the PMCHWT formulation has been investigated by Kern and Martin,[70] while the NFM has been studied in ref 71. A detailed comparison between several SIE formulations has been performed in ref 48, where their

convergence rate and accuracy have been carefully addressed. In this paper, we solve the PMCHWT with Rao Wilton Glisson (RWG) basis functions. In each of the SIE calculations presented in this work, more than 10k degrees of freedom have been used to numerically solve the scattering problem.

Conflict of Interest: The authors declare no competing financial interest.

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Growth mechanisms and process window for InAs V-shaped nanoscale membranes on Si[001]

E Russo-Averchi[1]**, A Dalmau-Mallorquí**[1]**, I Canales-Mundet**[1]**,
G Tütüncüoğlu**[1]**, E Alarcon-Llado**[1]**, M Heiss**[1]**, D Rüffer**[1]**, S Conesa-Boj**[1]**,
P Caroff**[2] **and A Fontcuberta i Morral**[1]

[1] Laboratoire des Matériaux Semiconducteurs, Ecole Polytechnique Fédérale de Lausanne,
1015 Lausanne, Switzerland
[2] Department of Electronic Materials Engineering, Research School of Physics and Engineering,
Australian National University, Canberra, ACT 0200, Australia

E-mail: anna.fontcuberta-morral@epfl.ch

Abstract

Organized growth of high aspect-ratio nanostructures such as membranes is interesting for
opto-electronic and energy harvesting applications. Recently, we reported a new form of InAs
nano-membranes grown on Si substrates with enhanced light scattering properties. In this
paper we study how to tune the morphology of the membranes by changing the growth
conditions. We examine the role of the V/III ratio, substrate temperature, mask opening size
and inter-hole distances in determining the size and shape of the structures. Our results show
that the nano-membranes form by a combination of the growth mechanisms of nanowires and
the Stranski–Krastanov type of quantum dots: in analogy with nanowires, the length of the
membranes strongly depends on the growth temperature and the V/III ratio; the inter-hole
distance of the sample determines two different growth regimes: competitive growth for small
distances and an independent regime for larger distances. Conversely, and similarly to
quantum dots, the width of the nano-membranes increases with the growth temperature and
does not exhibit dependence on the V/III ratio. These results constitute an important step
towards achieving rational design of high aspect-ratio nanostructures.

(Some figures may appear in colour only in the online journal)

1. Introduction

In recent years there has been strongly increasing interest in the growth and fabrication of nanostructures, motivated by the constant decrease in the characteristic size of electronic devices [1–3] but also due to the increase of functionality of materials when reduced to the nanoscale [4–8]. Nanoscale structures are most commonly obtained in the form of nanowires. Interestingly, growth at the nanoscale allows materials to form other peculiar structures such as nanotrees [9], tripods and tetrapods [10, 11], nano-membranes, nanowalls and nanoplates [12–20]. The possibility of modifying the shape of nanostructures in

bottom-up manner opens new perspectives in research areas where surfaces and shape is important such as: energy storage [21], energy generation [22, 23] and non-linear optics [24, 25]. For all this to become a reality, detailed studies on the formation mechanisms of novel nanoscale shapes are extremely important. At the same time, there has been a significant effort towards the growth of ordered nanostructures by a combination of top-down and bottom-up processes [26, 27], and towards the integration of III–V nanostructures on silicon [28–34]. The ordered growth of nanostructures on silicon opens many new perspectives as it enables to combine two very powerful platforms. The advantage of growing III–Vs in the form of a nanostructure

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is that the small footprint of nanostructures and their free-standing nature result in a very efficient strain relaxation at interfaces. As a consequence for moderate strain, coherent growth without misfit dislocation is possible [35] and when dislocations occur at larger misfit, they do not propagate in the vertical growth direction [36, 37]. A key requirement for the integration of nanostructures on silicon is the use of Si[001] as substrate. This is the platform in use in all the microelectronics industry, as CMOS fabrication on [110] or [111] surfaces have traditionally been hampered by their inferior gate oxide reliability. Only few groups have reported on the growth of III–V nanowires in the [001] direction [38–40], which has the additional advantage of suppressing the formation of extended planar defects and polytypism within the nanowires. We recently reported on a new form of III–V compound semiconductor nanostructures growing epitaxially as vertical wing-shaped membranes on [001] silicon substrates by solid source molecular-beam epitaxy (MBE) [24]. The nano-membranes are self-catalyzed and positioned in regular arrays of holes in a SiO_2 mask. We showed that they originate from two opposite facets of a rectangular pyramidal island and extend along two opposite $\langle 111 \rangle$ B directions, forming flat {110} walls. We also showed that these membranes scatter light in an extremely efficient manner, rendering them extremely interesting for intrinsic light management applications. While in this initial work we provided a microscopic model for the formation of the membranes, no discussion on the effect of the growth conditions on the morphology of the membranes was provided. Such a study is necessary in order to complete the understanding on the growth mechanisms and to distinguish it from the growth mechanisms of nanowires.

In this work we present a detailed study on the effect of the growth conditions on morphology of the V-shaped nano-membranes. In particular, we look into the role of the V/III ratio, substrate temperature, mask opening size and inter-hole distances in determining the size and shape of the membranes. We characterize the structures by Raman spectroscopy and we analyze the effect of the growth temperature on the crystal phase. This work opens a new path towards controlling the shape of bottom-up nanostructures.

2. Experiments

InAs membranes have been synthesized by molecular-beam epitaxy in a DCA P600 system. We have used [001] p-doped silicon wafers with a resistivity of 0.1–0.5 Ω cm, patterned with holes with diameters ranging from 100 to 180 nm and inter-hole distances (the same are also defined as pitches in the following) ranging from 200 to 2000 nm. The growth mask consisted of a 20 nm thick SiO_2 layer of thermal oxide. The pattern has been predefined in a ZEP resist with electron-beam lithography and has been transferred on the oxide layer by a 12 s 7:1 buffered HF wet etch. Prior to the introduction in the MBE chamber, a further 2 s dip in the buffered HF solution was performed in order to guarantee a pristine surface. The substrates were subsequently degassed at 600 °C for 2 h in UHV and then transferred to the growth chamber, where they

were again heated to 770 °C for 30 min to further remove possible surface contaminants. The growth was carried out at a nominal In growth rate of 0.2 Å s^{-1}, As$_4$ partial pressure between 0.2 and 1.15 $\times$ 10^{-5} Torr (BEP), temperatures between 440 and 540 °C, and with 7 rpm rotation. Once the growth temperature had been reached, both sources (As and In) were opened at the same time and then switched off simultaneously at the end of the growth. The samples were then cooled down to 200 °C and removed from the reactor.

The morphology of the samples was characterized by scanning electron microscopy (SEM). We used the image-processing package ImageJ [41] to automatically analyze the features shown in the pictures. Statistical information such as the length and width of the membranes are obtained by scanning top view images. The length is given by the Feret diameter, defined as the longest segment between any two points on the object (the membrane) perimeter. In the case of our membranes, this length represents the projection of the membrane's arms on the plane (001). The real length of the membranes is obtained by dividing the measured length by the cosine of the angle between the arm and the substrate (34°). The width is in turn determined by the length of a segment connecting the two points with the greatest orthogonal distance from the Feret diameter and orthogonal to their tangents. When considering the distribution of lengths in order to characterize their statistical properties, it must be taken into account that the sample may also include connected membranes [24]. In the simplest case of two connected membranes, the typical length of these structures is approximately twice the length of a membrane, in the case of three connected membranes it would be approximately thrice and so on. This requires a special care in computing the statistical properties of the sample: for example, if the multiple membranes are included in the calculation of the mean (of a single membrane) they would artificially increase the result. We handled this complication by modeling the distributions of lengths with a so-called Gaussian Mixture Model (GMM): mixture models are used in statistics when distinct subpopulations are present in a given population [42]. In our case the first subpopulation (or component, as they are also referred to) corresponds to all the single membranes (i.e. not connected with others), the second subpopulation corresponds to all the two connected membranes etc. Given that the only source of variation within each subpopulation is random, it is reasonable to model each subpopulation with a Gaussian distribution with its mean and variance. The whole population is then described as the (normalized) distribution given by the sum of all the Gaussian components (hence the name of the model). In our analysis, GMM have been fitted by using the expectation–maximization (EM) algorithm,[3] [43] with a procedure available in the statistical package R [44]. In

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[3] The EM algorithm computes efficiently the maximum likelihood estimation (MLE) in the presence of missing or hidden data by iterating two processes: the E-step, and the M-step. In the expectation, or E-step, the missing data of the complete data likelihood are estimated; in the M-step, the likelihood function (the expectation computed in the first step) is maximized. These two steps are repeated as necessary. The iteration is guaranteed to increase the likelihood and the algorithm is guaranteed to converge to a local maximum of the likelihood function.

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the following we will focus on the statistical properties of the single membranes component, leaving an analysis of the other components for future works.

Back-scattering micro-Raman spectra were taken on individual nano-membranes grown at temperatures from 440 to 540 °C. The measurements were taken at room temperature with the 520.8 nm Ar–Kr laser line as excitation source focused through a 63×objective (NA 0.75). The power was kept low enough to prevent heating of the structures. The crystalline structure of the InAs membranes has been analyzed with a Philips CM300 electron microscope operated at 300 kV from the Centre Interdisciplinaire de Microscopie Électronique (CIME) at EPFL Lausanne.

3. Temperature dependence

Examples of InAs V-shaped membranes grown at various temperatures ranging from 440 to 540 °C under an As_4 partial pressure of 8.5×10^{-6} Torr (BEP V/III = 51) are reported in figure 1. The scanning electron microscopy tilted images (30°) show the wing shape of the nanostructures with arms branching towards two ⟨111⟩ B directions [24]. The substrate temperature has a critical role on the size and the shape of the membranes. At 440 °C the tips of the membranes form flat surfaces. The section of the membranes reminds of a rectangular shape rather than a triangle. Since at these temperatures the diffusion length of In adatoms is low, the atoms depositing on the membranes cannot move easily and so they tend to accumulate in the valley formed between the arms increasing the interface height. At the higher temperatures of 480 and 500 °C, the arms of the membrane assume a triangular shape and the tip becomes sharper. It is suggested that the increased diffusion length of the In adatoms allows the atoms to reach the extreme regions of the membrane where nucleation occurs, thus explaining the wing shape and its elongation towards a sharper tip. For growth temperatures above 520 °C the tips become rounded, the arms assume again a rectangular shape and the interface height is further reduced. This shape evolution can be understood in terms of a temperature-activated group III adatom desorption mechanism; recent reports show that indium desorption from a (111) Si surface and from a pattern containing InAs nanowires becomes relevant at substrate temperatures between 520 and 570 °C [45]. At 540 °C, the nucleation yield drops since most of the In adatoms and InAs are desorbed. The nucleation is observed in only few membranes and these develop with very short and thicker arms.

Figure 2 summarizes the statistical analysis of the membrane morphology as a function of the growth temperature for a mask opening of 100 nm and a pitch of 1000 nm. Similar results are obtained for other opening sizes. We choose this pitch because a pitch-less dependence on the morphology is only observed for a pitch of 1000 nm or higher. The dependence of the morphology on the pitch will be discussed in more detail in section 4.

For a fixed growth time of 1 h, the membrane length reaches values of 1500 nm at 480 °C while both lower and higher temperature yielded maximum lengths below 700 nm.
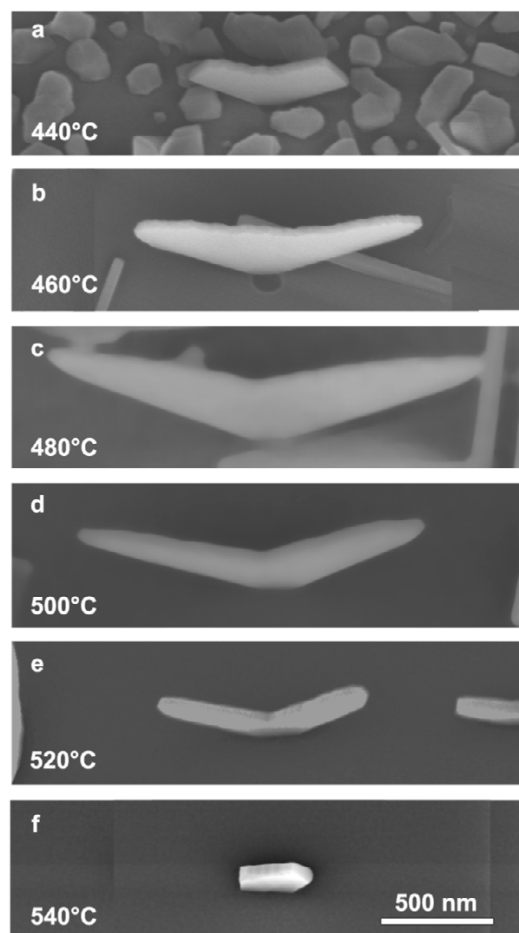
Figure 1. Scanning electron microscopy (SEM) tilted (30°) images of typical InAs membranes grown under an As partial pressure of 8.5×10^{-6} Torr and different substrate temperatures, from 440 °C (a) to 460 °C (b), 480 °C (c), 500 °C (d), 520 °C (e) and 540 °C (f). The length scale is the same for all temperatures. The images illustrate how the temperature strongly influences the length and shape of the arms of the membranes.

A similar trend has been observed several times in the growth of InAs nanowires [46–51]: the decreasing of the length by increasing the temperature above 480 °C is related to the increased thermal decomposition rate along the InAs⟨111⟩ growth direction, while the decreasing of the length by decreasing the temperature below 480 °C can be explained by the reduced diffusivity of adatoms and hence their decreased incorporation probability at the nanostructure tip, limiting the growth along the ⟨111⟩ B direction. As it has been done in other works [52], we fitted the length of the membranes as a function of the inverse temperature (not shown). The results of our fit between 440 and 480 °C show that in this range the ⟨111⟩ growth rate is surface kinetically limited with an activation energy of 21.5 ± 3.3 kcal mol^{-1} (0.94 ± 0.14 eV). This value is in good agreement with the activation energy obtained by Björk *et al* [52] for the same material system.

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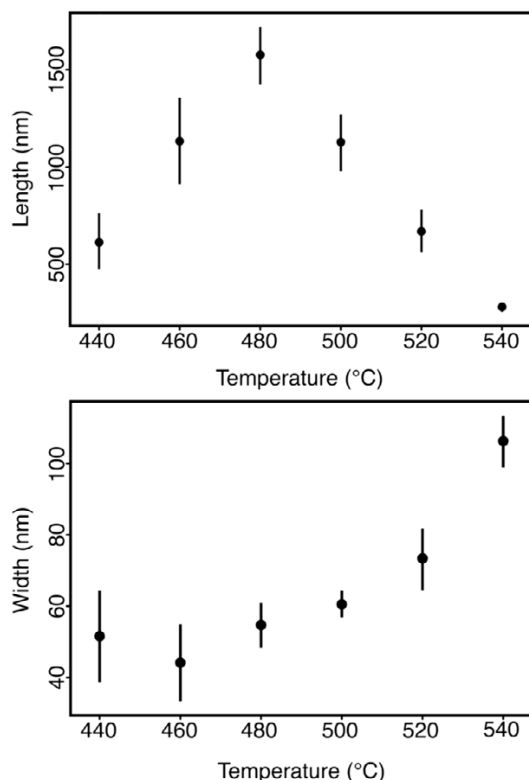
Figure 2. Temperature dependence of InAs membranes growth. The length and the width are plotted as a function of the substrate temperature, for pitch = 1000 and for opening size = 100 nm. Similar behavior is observed for other pitches and opening sizes. The length of the membranes first increases and then decreases with increasing temperature. In contrast, the width always increases with increasing temperature. At low temperature it reaches a plateau.

In contrast to the length, the width of the membranes increases with temperature. The variation with temperature is weak up to 480 °C, while above this value it becomes similar to what has been observed for self-catalyzed InAs nanowires [47, 53, 54], and shows a pronounced dependence on the temperature. This behavior of the membrane width could be explained by the temperature dependence of the formation of the initial nucleus from which the arms develop: a pyramidal quantum dot [24]. The arms consist of $(0\bar{1}1)$ and $(01\bar{1})$ surfaces. On these planes the nucleation is relatively slow compared to $\langle 111 \rangle$ B. Lateral growth occurs via step-flow, in agreement with the absence of tapering (homogeneous thickness). The width of the membrane is thus the distance between the two opposite {110} planes and it is mainly determined by the width of the initial quantum dot. Indeed the width of a nucleus obtained after 5 min growth at 520 °C is 69 ± 9 nm and the width of the membranes after 1 h growth in the same conditions is 73 ± 9 nm.

A vast literature exists on the formation of InAs quantum dots on Si and GaAs, some of the studies including the critical growth parameters on the morphology [55–61]. For substrate temperatures above 480 °C, one observes that the

quantum dot size increases with the temperature, with a scaling law similar to what we measure for the width of the membranes [60, 61]. This is explained by considering the mechanisms of quantum dot formation. After the formation of the quantum dot, the strain relaxation in the island results in a strain concentration at the island edge. The adatoms initially forming the wetting layer surface need to overcome an energy barrier $\Delta\mu$ before relax forming the island. An increase in the growth temperature leads atoms to overcome the energy barrier $\Delta\mu$ more frequently. As a consequence, the size of the quantum dot increases with the substrate temperature [62].

We turn now our attention to the evolution of the growth selectivity, namely the preferential growth of the membranes on the silicon surface of the openings rather than on the SiO$_2$ of the growth mask, as a function of the temperature. In figure 3 we see low magnification planar view SEM images of InAs membranes grown in the conditions previously described, on patterns with opening size of 100 nm and inter-hole distances 400 nm (a)–(f) and 1800 nm (g)–(n). The growth selectivity depends strongly on the growth temperature. At very low temperature, 440 °C, there is parasitic growth on the oxide in the form of InAs particles and the yield for the growth of membranes is around 20%. By increasing the substrate temperature up to 480 °C, the parasitic growth decreases while at the same time the yield improves significantly. For temperatures above 480 °C, the parasitic growth on the SiO$_2$ disappears completely, as the indium desorption rate on the oxide becomes significantly larger than the deposition rate [27, 63].

4. Dependence on the pitch and opening size

Figure 4 shows the length projected to the (001) plane and the width of InAs membranes grown at As$_4$ partial pressure of 8.5×10^{-6} and substrate temperature of 480 °C in function of the pitch and the hole size. The length of the membrane increases with the pitch up to a size of 800 nm and then saturates (figure 4(a)). Growth occurs in two different regimes depending on the value of the pitch. These two regimes correspond to: (i) competitive growth regime characterized by shorter membranes for small pitches and (ii) diffusion limited or independent growth regime for longer pitches. The switch between the two regimes is determined by the indium surface diffusion length on SiO$_2$ (λ_{SiO_2}). λ_{SiO_2} limits the sample area from which each membranes can collect the In species which are diffusing on the sample. For a small spacing (pitch < $2\lambda_{SiO_2}$), the indium adatoms are shared between the membranes. By increasing the spacing, the surface collection area available exclusively to each single membrane increases, resulting in a linear increase of the growth rate. In the opposite limit of a large spacing (pitch > $2\lambda_{SiO_2}$) the membranes can be treated as independent isolated islands. In this regime the surface collection area saturates and the growth rate is no longer dependent on the pitch. Similar observations have been done by other groups examining the growth of nanowires on pattern [46, 64, 65]. The width of the membranes does not show a significant dependence on the pitch (figure 4(b)). This can be related to the different
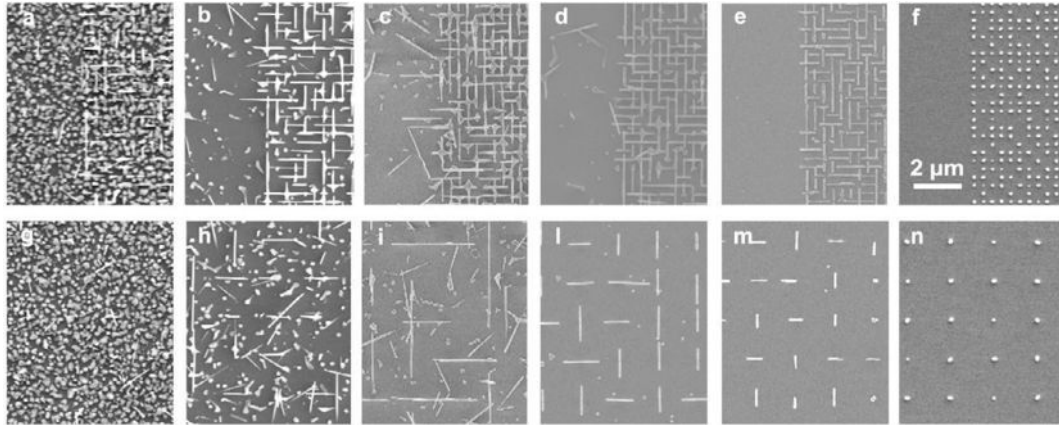
Figure 3. Planar view SEM images of InAs membranes grown under an As partial pressure of 8.5×10^{-6} Torr and different substrate temperatures, from 440 °C (a) and (g), to 460 °C (b) and (h), 480 °C (c) and (i), 500 °C (d) and (l), 520 °C (e) and (m) and 540 °C (f) and (n). In these images the inter-hole distances are 400 nm (a)–(f) and 1800 nm (g)–(n) and the opening size is 100 nm. The scale is the same in all images. The image shows how the membrane growth selectivity strongly depends on the growth temperature and improves as the temperature increases.
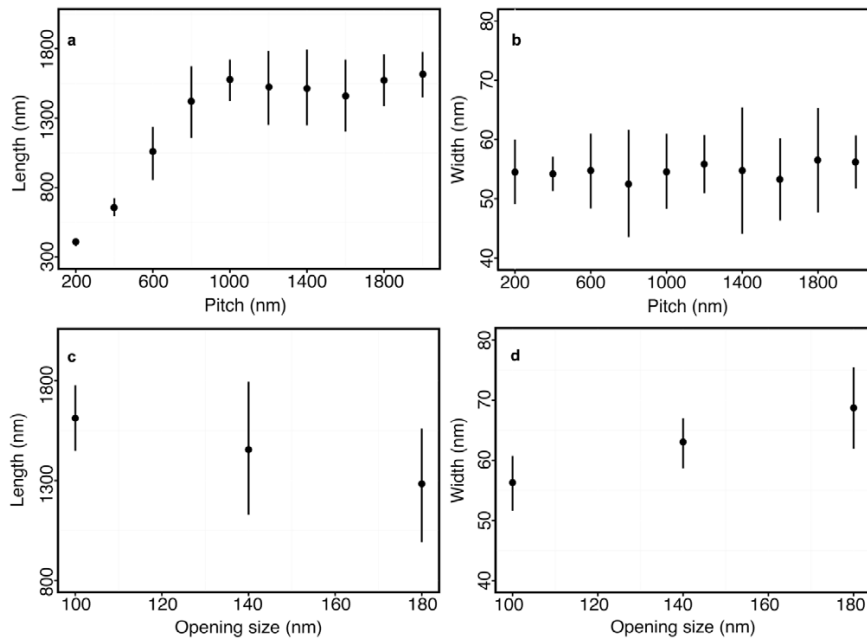
Figure 4. (a)–(b) Effect of inter-holes spacing on the length and width of InAs membranes grown under an As partial pressure of 8.5×10^{-10} Torr and substrate temperature of 480 °C. In these images the opening size is 100 nm. The length increases by increasing the pitch and saturates. The width does not depend on the pitch. (c)–(d) Plot of the membranes length and width as a function of the opening size (inter-hole distance is 2000 nm). The length slightly decreases with the opening size while the width increases with it.

growth rate dependences of (111) B and {110} surfaces on the growth conditions, as already shown by Björk *et al* [52]. In general, the length of the membranes increases with the pitch for all temperatures grown. One should note that: (i) in the competitive regime, the higher is the temperature the lower is the overall variation of the membrane length. One can also say that the variation between the length at 200 nm and the one at 2000 nm decreases by increasing the temperature; (ii)

in the independent regime, the maximal length decreases by decreasing the temperature, consistently with figures 1 and 2.

The role of the hole size is analyzed in figures 4(c) and (d): the length of the membranes slightly decreases with larger opening sizes, while their width increases. To explain this behavior we focus on the growth mechanism of the membranes. Since the InAs island is formed at the very beginning of the process, we speculate that a major

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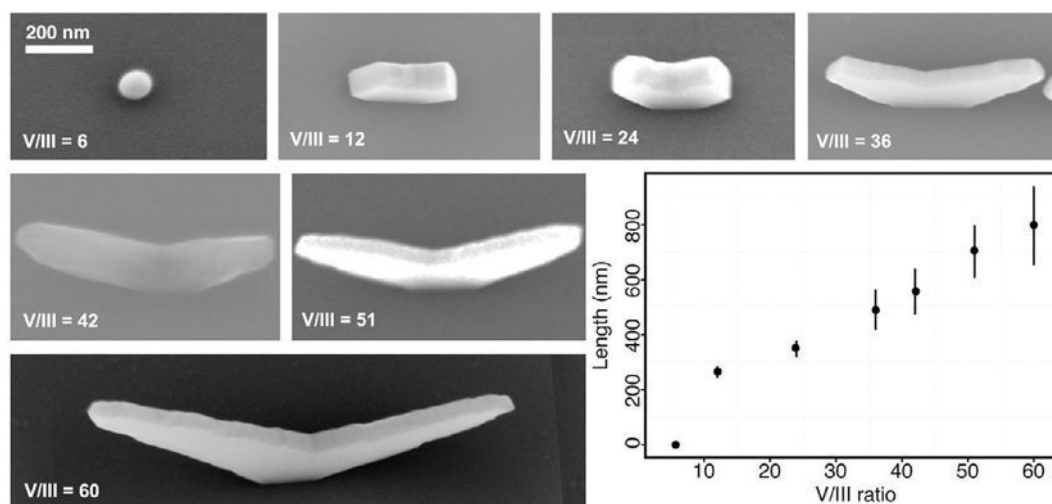
Figure 5. Tilted (30°) SEM images of InAs membranes grown at 520 °C and under different V/III BEP ratios. The growth time is 1 h. The length scale is the same for all pictures. At V/III = 6 we do not observe any growth. Above this value the length increases with the V/III ratio, as for group V-limited growth.

contribution to the formation of the quantum dot is given by the indium diffusing on the ⟨001⟩ Si surface, i.e. the indium deposited directly into the holes. The size of the opening will thus determine the dimension of the quantum dot and in turn the width of the membrane. This has been observed by other research groups before [66, 67, 27] and our measurements confirm the findings (data not shown).

The opening size will also determine the size of the lateral facets on which the wings of the membrane grow as they scale with the size of the initial seed. One should note that the increase in width and decrease in length of the membranes with the hole size means that the total volume of the membrane is conserved and does not depend on the hole size.

5. V/III ratio dependence

For these experiments we have chosen 520 °C as substrate temperature as it has shown zero parasitic growth and a good yield. In the set of high magnification 30° tilted SEM images reported in figure 5, we varied the V/III ratio from 6 to 60, by keeping the growth time for all samples equal to 1 h. At a V/III ratio 6 we do not observe any growth of membranes. We find only indium droplets on the surface and no island, nanowire or membrane formation. It has been seen in the past that a too low V/III ratio could lead to an indium-terminated (001) Si surface which in turn would inhibit the formation of InAs islands [68, 52]. The length of the membranes increases with the V/III ratio (graph in figure 5). We did not observe any saturation of the length for the V/III ratios used. This behavior is in agreement with group V-limited growth mechanism. The width of the membranes is independent of the V/III ratio (data not shown).

6. General structural characterization by Raman spectroscopy

Having determined the effect of the growth conditions on the morphology of the V-shaped nano-membranes, we now characterize the crystal structure by Raman spectroscopy. Raman spectroscopy reports on the phonon spectrum of a material, which constitutes a fingerprint of the crystal structure. This technique has often been used in the characterization of polytypism in III–V nanostructures [69–71]. It possesses the advantage that it allows a fast non-destructive measurement and therefore the realization of a high number of measurements and statistics on a same sample. Figure 6 shows the normalized typical spectra obtained for single membranes grown at different temperatures. Most of the spectra show a main Raman feature at around 210 cm^{-1} and a less intense peak at ∼232 cm^{-1}.

Membranes grown at the lowest temperature of 440 °C are not considered for consistency, since the high degree of parasitic growth does not allow to optically discerning nano-membranes from the rest of deposited material. Membranes grown at mid-temperatures reveal virtually identical spectra where the frequency of the main peak corresponds to that of the E$_{2h}$ mode of wurtzite InAs [71]. This indicates the wurtzite crystalline phase of membranes grown at such temperatures, which was further confirmed by polarization-dependent measurements on single nano-wings (not shown). In the case of membranes grown at the highest temperature (540 °C) the main peak clearly blue-shifts, approaching the value of the TO mode in zinc-blende InAs. This could be due to an increased zinc-blende proportion in the membranes for such temperature. In order to confirm so, high-resolution transmission electron microscopy (HRTEM) was performed. Figure 6(b) is an HRTEM analysis on a representative InAs nano-membrane. The electron diffraction pattern of the framed area, indicates that zinc-blende crystalline structure is

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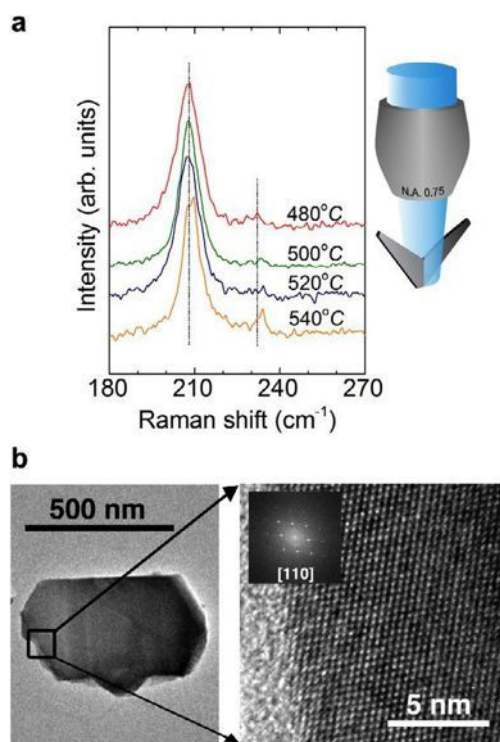
Figure 6. (a) Raman spectra obtained on single membranes as a function of the growth temperature. Dotted lines indicate the frequency position of the main phonon modes of wurtzite InAs. (b) HRTEM image of a V-shaped InAs membrane grown at 540 °C exhibiting a zinc-blende crystalline structure, as shown by the corresponding diffraction pattern, where all reflections can be indexed according to zinc-blende structure in [110] zone axis.

the main phase in the membrane wing. This constitutes the initial steps towards crystal-phase control in self-catalyzed InAs nanostructures on Si, which is predicted to be the key development for crystal-phase engineering [72].

7. Conclusions

We recently reported on a new form of III–V compound semiconductor nanostructures growing epitaxially as vertical V-shaped membranes on Si[001]. Here we studied how to control the morphology of the membranes by changing the growth conditions. In particular we have systematically examined the role of the V/III ratio, substrate temperature, mask opening size and inter-holes distances in determining the size and shape of the structures. We found that the membranes form by combining growth mechanisms of nanowires and Stranski–Krastanov type quantum dots. In analogy with nanowires, the length of the membranes strongly depends on the growth temperature and the V/III ratio; the inter-hole distance of the sample determines two different growth regimes: a competitive growth for small distances and an independent regime for larger ones. In analogy with quantum dots, the width of the membranes increases with the growth temperature and does not exhibit dependence

on the V/III ratio. Our results constitute an important step towards controlling the design of these nanostructures. Lastly, we characterized the crystal structure of the membranes by Raman spectroscopy. We found that the percentage of zinc-blende material in the arms of the membranes depends on the temperature. The membranes grown at temperatures between 480 and 520 °C have identical spectra where the frequency of the main peak corresponds to that of the E_{2h} mode of wurtzite InAs. For a temperature of 540 °C the peak is slightly blue-shifted, towards the position of the TO mode in zinc-blende InAs and indicating an increase in the zinc-blende proportion, as confirmed by HRTEM. This result constitutes the initial steps towards crystal-phase control.

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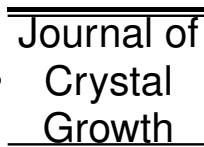
Bottom-up engineering of InAs at the nanoscale: from V-shaped nanomembranes to Nanowires.

E. Russo-Averchi[a], G. Tütüncüoglu[a], A. Dalmau-Mallorqui[a], I. Canales Mundet[a], M. de la Mata[b], D. Rüffer[a], J. Arbiol[b,c], S. Conesa-Boj[a], A. Fontcuberta i Morral[a,*]

[a]*Laboratoire des Matériaux Semiconducteurs, Ecole Polytechnique Fédérale de Lausanne, 1015 Lausanne, Switzerland*
[b]*Institut de Ciència de Materials de Barcelona (ICMAB-CSIC), Campus de la UAB, 08193 Bellaterra, CAT, Spain*
[c]*Institució Catalana de Recerca i Estudis Avanats (ICREA), 08010 Barcelona, CAT, Spain*

Abstract

The ability to rationally tune the morphology of nanostructures is a fundamental milestone in nanoscale engineering. In particular, the possibility to switch between different shapes within the same material system represents a further step in the development of complex nanoscale devices and it increases the potential of nanostructures in practical applications. We recently reported a new form of InAs nanostructures growing epitaxially on Si substrates as vertical V-shaped membranes. Here we demonstrate the possibility of modifying the shape of these nanomembranes and turning them into nanowires by modulating the surface roughness of the substrate by varying the surface treatment. We show that the growth of nanomembranes is favored on smooth surfaces. Conversely rough surfaces enhance the growth of nanowires. We also show that the V/III ratio plays a key role in determining the absolute yield, i.e. how many nanostructures form during growth. These results envisage a new degree of freedom in the engineering of bottom-up nanostructures and contribute to the achievement of nanostructures networks.

1. Introduction

Nanoscale structures with controlled size and morphology have attracted extensive interest over the past years. The miniaturization of integrated circuits down to sub-micrometric scales has been key in the developments of increasingly more advanced microelectronic devices which are ubiquitous in our daily life [1]. In recent years, however, the pace of miniaturization has considerably slowed down as the customary "top-down" fabrication methods are reaching the limit of their capability [2]. Two issues in particular are hindering the development of even smaller electronic components: the failure of semiconductor physics in nanometer-scale devices and the fundamental limitations of conventional photolithography, which constitutes a key step in the top-down approach. An alternative methodology, called "bottom-up", has shown promising results in overcoming these limits. Nanostructures created "bottom-up", i.e. built from their smallest possible components, atoms and molecules, are regarded as the fundamental building blocks of future electronics devices. Examples of non-planar nanostructures can be as simple as nanowires [3, 4] or more complex structures such as nanomembranes [5, 6, 7, 8, 9], nanowalls [10], nanoplates [11], nanosheets [12, 13],

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nanotrees [14], tripods and tetrapods [15, 16, 17, 18]. Besides electronics, non-planar nanostructures have also found many novel applications in research areas such as energy storage [19], energy generation [20, 21], lasers [22, 23] and non-linear optics [8, 24]. Here what makes the "bottom-up" approaches particularly interesting is that they offer a way to synthesize nanocrystals with controlled size and shape.

The last few years have also seen an increased interest in III-V materials and in the integration of III-Vs on silicon which is facilitated by nanowires [25, 26, 27, 28, 29, 30, 31]. Nanoscale electronics, optoelectronics, photonics and photovoltaics would benefit from this integration because nanoscale structures could be eventually engineered on silicon, a mature and less expensive platform and with complementary functionality. III-V nanostructures are promising as they offer an efficient elastic relaxation of the strain thanks to their small footprint and free-standing nature [32, 33, 34].

In order to bring the integration of III-V materials and silicon closer to the existing technological platforms, the nanostructures should be obtained in an ordered manner on (001) substrates. Silicon (001) is the platform in use across the microelectronics industry, as CMOS fabrication on [110] or [111] surfaces have inferior gate oxide reliability. One should also note that nanowire growth along (001) results in a reduction of structural defects and suppression of polytypism [35, 36]. The ordered growth of III-V nanostructures has been intensively studied very recently in different material systems [26, 35, 37, 38, 39, 40, 41, 42, 43, 44]. Different techniques such as electron beam, nanosphere, nano-imprint or phase-shift lithography have been used for the definition of the patterns [45, 46, 47, 48, 49, 50]. Only a few groups report on ordered growth of nanostructures on silicon (001) [35, 51, 52].

An important milestone in nanoscale engineering is the understanding of the underlying mechanisms that allow for the fabrication of different shapes. Several groups have shown the ability to rationally change the shape of the structures for example by inducing new branches [14, 53, 54, 55] or by directly crystallizing the material in different configurations [56, 57]. In these cases the different shapes are achieved by simply changing the growth conditions. Utama et al. have recently suggested the possibility to manipulate the shape of the non-planar nanostructures in van der Waals epitaxy by changing the surface treatments prior to growth, although they did not fully unravel the underlying mechanism [18, 58].

We recently reported on a new form of InAs nanostructures, vertical wing-shaped membranes [8]. A microscopic model for the formation of the membranes and a detailed study on the effect of the growth conditions on their morphology were also reported [8, 9]. In this work we demonstrate that it is possible to modify the shape of InAs nanostructures simply by modulating the surface roughness of the substrate. We examine the role of the V/III ratio, etching and cleaning steps in the relative occurrence of nanomembranes and nanowires. We show that, among these factors, fine sample preparation can be used to favor the presence of one or the other type of nanostructure which rely on two different growth mechanisms. We also show that the V/III ratio plays a key role in determining the absolute yield, i.e. how many nanostructures form during the growth. The ability to manipulate the shape of nanostructures is a further step in the fabrication of advanced nanodevices and nanosystems as it gives a new degree of freedom in the engineering of bottom-up nanostructures.

2. Experiments

The InAs nanostructures were grown by MBE in a DCA P600 system. The growths were performed on [001] p-doped silicon wafers with a resistivity of 0.1-0.5 Ωcm. To achieve precise positioning of the nanostructures, we defined regular arrays of nanoscale holes on a thermally oxidized Si(001) wafer, with diameters ranging from 30 to 350 nm and pitches (the inter-hole distances) ranging from 200 to 2000 nm. The thermal oxide layer was grown in a Centrotherm furnace at 900°C; before loading into the furnace, the wafers have been cleaned with a RCA process to remove organic and metallic contaminants. The pattern was predefined in a ZEP resist with electron-beam lithography and had been transferred to the 20 nm thick oxide layer using a 12 s 7:1 buffered HF (BHF) wet etch or by a He/CHF$_3$ reactive ion etch. Prior to the introduction in the MBE chamber, a further dip in a wet etching solution was performed in order to guarantee a pristine surface. The samples with patterns defined in the 7:1 BHF solution were dipped in the same wet etching solution for a further 1s before loading. The patterns prepared with the He/CHF$_3$ dry etch were dipped in three wet etch solutions: a 7:1 BHF; a customized, highly diluted BHF wet etch for a more controlled etching rate; a typical isotropic polysilicon etch in nitric and hydrofluoridric acid. The reason for using different etching solutions was to deliberately change the surface roughness of the silicon substrate. After the last dip it was observed that the oxide thickness is reduced to 10 nm. The different sample preparations are summarized in table 1.

2

Chapter 3. Results

Sample Prep.	Main Etch	Final Dip (wet)	Dilution
N.1	BHF (wet)	NH_4F (40%):HF (49%)	7:1
N.2	CHF_3/He (dry)	NH_4F (40%):HF (49%)	7:1
N.3	CHF_3/He (dry)	NH_4F (40%):HF (49%)	500:1
N.4	CHF_3/He (dry)	HNO_3 (70%):HF(49%):H_2O	50:3:20

Table 1. Summary of the different sample preparations.

The substrates were subsequently degassed at 600°C for 2 *h* in UHV and transferred to the growth chamber. There, they were again heated to 770°C for 30 *min* to further remove possible surface contaminants. After this steps, the HF treated silicon surfaces are Hydrogen free as the Hydrogen desorbs already at 510°C [59]. The growth was carried out at a nominal In growth rate of 0.2 Å/s, As_4 partial pressure ranging between 0.1 x 10^5 and 1.4 x 10^5 *Torr* (V/III beam equivalent pressure -BEP- ratios from 6 to 90), temperature 520°C, and with 7 *rpm* rotation. In a previous work [9] we showed that at this temperature there is optimal growth selectivity: the nanostructures preferentially nucleate in the openings where the silicon surface is exposed, rather than on the SiO_2 of the growth mask [41]. Once the growth temperature had been reached, both sources (As and In) were opened at the same time and then switched off simultaneously at the end of the growth. The samples were then cooled down to 200°C and removed from the reactor. The morphology of the samples was characterized by scanning electron microscopy (SEM) and by transmission electron microscopy (TEM) in a TECNAI F20 operated at 200 *kV* from the Institut Català de Nanociència i Nanotecnologia (ICN2) at UAB Campus, Bellaterra, Barcelona; in a Phillips CM300 operated at 300 *kV* and a FEI Tecnai OSIRIS operated at 200 *kV* from the Centre de Microscopie Electronique (CIME) at EPFL Lausanne. TEM cross-sections were prepared by using a Focus Ion Beam (FIB).

3. Results

In this section we analyze the influence of the substrate preparation on the relative occurrence of nanomembranes and nanowires. The first subsection is dedicated to the description of the effects of a full wet chemical etch. Then we move to analyze the growth on patterns defined through dry etching. The results obtained by varying the final dip are presented in a further subsection.

3.1. Analysis of sample prep. N.1: wet etch + BHF dip

As an initial step in the analysis of the experimental results we examine the growth of InAs nanostructures on a first substrate obtained by defining the pattern with a main etch and dip in a 7:1 BHF etch (sample preparation N.1). Fig. 1 shows scanning electron microscopy (SEM) planar and tilted images of the samples grown under an As_4 partial pressure of 1.15 x 10^5 (V/III BEP ratio = 60) for 2 hours. It is worthwhile to note that the sample had been prepared and grown in the same experimental conditions employed in the previously reported works on V-shaped nanomembranes [8, 9]. Interestingly, as we show in Fig. 1 (a), it can be seen that in addition to the V-shaped nanomembranes (Fig. 1 (b-c)), nanowires (Fig. 1 (c-d)) and tripods (Fig. 1 (e)) are also present. Under these particular growth conditions the nanomembranes represent 90% of the structures grown while the nanowires are typically 9%. Only a small occurrence of tripods (<0.5%) is detected.

We now proceed to determine if the V/III BEP ratio can influence the occurrence of any of these nanostructures. To this purpose we performed another set of growths using the sample preparation N.1 and varying the V/III BEP ratios from 6 to 90. For simplicity we will write V/III ratio instead of V/III BEP ratio. Representative planar view SEM images are displayed in Fig. 2.

Here the inter-hole distance is 1000 *nm* and the opening size is 90 *nm*. At very low V/III ratio (V/III = 6, shown elsewhere [9] and not shown here) we find only indium droplets. This is in agreement with the observation that the formation of indium terminated Si(001) surfaces inhibits the formation of InAs islands [60]. By increasing the V/III ratio up to 12, the nanostructures start to form. At this V/III ratio we have many islands but by increasing the V/III ratio, islands progressively give way to nanomembranes and nanowires. We conclude then that the yield of the nanostructures depends strongly on the V/III ratio. Another observation stemming from the SEM images in Fig. 2 is that the length of the nanowires and nanomembranes increases with the V/III ratio. Indeed, similarly to nanowires,
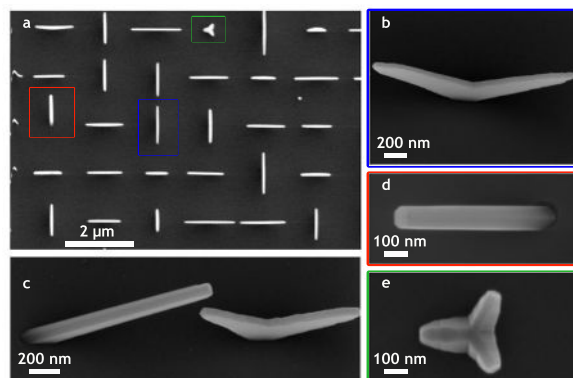
Figure 1. Scanning electron microscopy (SEM) images of InAs nanostructures grown at 520°C under an As$_4$ partial pressure of 1.15 x 10^5 Torr. (a) A low magnification planar view image illustrates the outcome of the growth: V-shaped nanomembranes, nanowires and tripods; (b) a tilted view (20°) of an InAs nanomembrane showing arms branching towards two <111>B directions; (c) a tilted view (20°) of a nanowire with a nanomembrane; (d) a planar view of an InAs nanowire; (e) a planar view of an InAs tripod.
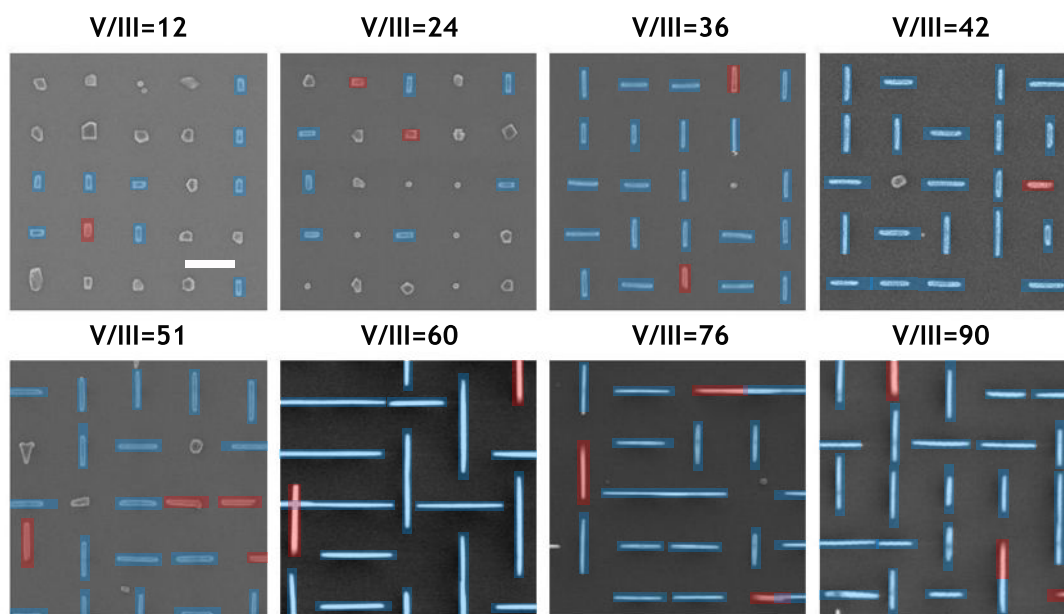
Figure 2. Planar view SEM images of InAs nanomembranes and nanowires grown at 520°C and under different V/III beam equivalent pressure ratios, from 12 to 90. In the images, the hole diameter is 90 nm and the inter-hole distance is 1 μm. The V-shaped nanomembranes are highlighted in blue while the nanowires in red. The picture illustrates how the yield of the nanostructures depends on the V/III ratio and improves as the V/III ratio increases. The scale bar is 1 μm and is the same for all images.

the length of the arms of the nanomembranes depends on the V/III ratio, consistent with a group V-limited growth regime [9]. In Fig. 3 we summarize the statistical analysis of the yield of the nanomembranes (Fig. 3 (a)) and of the nanowires (Fig. 3 (b)) as a function of the V/III ratio for different hole diameters. In agreement with Fig. 2, the yield is low for small V/III ratios and increases with the V/III ratio. The yield depends inversely on the hole diameter (i.e. it decreases with larger holes). Conversely, the results do not show a dependence of yield on the inter-hole distance

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108   (see Supporting Information for further details).

109   Having looked at the yield of nanostructures in the different patterns, we turn our attention to the relative occur-
110 rence of nanomembranes against nanowires (Fig. 3 (c)). Across all patterns with different V/III ratios we observe a
111 general an increased occurrence of nanomembranes, between 90 and 98%. This shows that, while the V/III ratio has
112 a role in determining the overall yield of the nanostructures, it does not significantly impact the relative occurrence of
113 nanomembranes. Conversely we see that the relative occurrence of nanomembranes seems to show a dependence on
114 the hole diameter and it decreases as the hole size decreases (Fig. 3 (c)).

115 *3.2. Analysis of sample prep. N.2: dry etch + BHF dip*

116   In order to determine if the hole size really limits the yield of nanostructures and if it could potentially increase
117 the nanowire formation, we fabricated arrays with smaller holes. In order to reach smaller diameters, we replaced
118 the standard wet etch (isotropic, inevitably enlarges the diameter) with a dry etch (anisotropic). A 7 *s* He/CHF$_3$
119 reactive ion etch (RIE) and a fast dip in a BHF solution (sample prep. N.2) allowed us to obtain holes as small as
120 30 *nm* in diameter, three times smaller than the smallest we could achieve in the previous sample preparation N.1.
121 We then performed a new growth keeping the same growth conditions (T=520 °C, BEP V/III = 60 and a nominal In
122 growth rate of 0.2 Å/*s*) of our first sample with preparation N.1. As shown here below, the novel sample preparation
123 drastically changes the outcome of the growth. The first difference we observe with the new preparation is that the
124 absolute yield (defined as the sum of yield of nanomembranes and yield of nanowires) is reduced. For a hole diameter
125 of 90 *nm*, with the previous sample preparation in a wet chemical etch, a yield of 95% was achieved. With the new
126 preparation, the yield at the same hole diameters decreases to 45%. Even at smaller hole diameters (which did not
127 exist in the previous sample) the yield increases but only up to 70% for the smallest hole size of 30 *nm*. We look
128 now at the relative occurrence of nanomembranes against nanowires as a function of the hole diameters. These results
129 are reported in Fig. 4 (a). We observe a significant drop in the nucleation of the nanomembranes especially at small
130 holes. In line with the previous sample preparation, the relative occurrence decreases by decreasing the opening size.
131 Interestingly, for hole diameters below 175 *nm* the relative occurrence of nanomembranes is less than 50% while for
132 sample preparation N.1 it was in a range between 88% and 96%.

133   In summary, we can confirm that small holes favor the growth of nanowires rather than nanomembranes. In
134 addition, for the same hole size the occurrence of nanowires is enhanced by the use of a dry etch. This different
135 behavior suggests that the two etching procedures produce holes with different features.

136 *3.3. Analysis of sample prep. N.3 (dry etch + highly diluted BHF dip) and sample prep. N.4 (dry etch + polySi dip).*
137   *The role of surface roughness.*

138   To further investigate the effect of the etching procedures on the characteristics of the holes, we grew another set of
139 samples on patterned substrates prepared by dry etching followed by different etching solutions. Our hypothesis here
140 is that surface roughness might be key in the initial stages of growth, thereby allowing one growth mode or the other.
141 We chose etching solutions having a strong influence on the silicon surface roughness. There is extensive literature on
142 the effect of etching solutions on the surface roughness of silicon. Higashi *et al.* found that the microscopic roughness
143 of the silicon surface can be altered by varying the pH of the HF solutions [61]. In particular, a high pH HF solution
144 shows a smoothening effect on Si(111) surfaces. On other silicon surface orientations such as (001) the solution
145 develops (111) facets, thereby increasing the surface roughness [62]. One way to increase the pH is to add NH$_4$F
146 [63, 64]. In this case, etching Si(001) with NH$_4$F starts with the formation of small (100) terraces and pyramids with
147 (111) facets and continues with the uncorrelated etch of the terraces. This process leads to a continuous increase in
148 surface roughness during the etching process [62]. Conversely, in microelectronics, a widely used process to reduce
149 surface roughness is a wet chemical etching of silicon in HNO$_3$:HF solutions with high concentrations of HNO$_3$
150 (solution called polysilicon etch) [65]. This etch consists of a two-step chemical process: 1) oxidation of Si to form
151 SiO$_2$ by the acid HNO$_3$ and 2) dissolution of SiO$_2$ by HF and release of a new silicon surface. This is conceptually
152 similar to the sacrificial oxidation performed in microelectronics to remove the RIE damaged silicon [66].

153   In order to create a rougher surface, we modified the final dip we had used in sample preparation N.1 and N.2 (a
154 common buffered HF composition of 7:1 NH$_4$F (40%)-HF (49%), with a pH of 5 [67]) by adding NH$_4$F. We prepared a
155 highly diluted solution: 500:1 NH$_4$F (40%)-HF (49%) which we found to have a pH = 8. Dry etching followed by this
156 solution is referred to as sample preparation N. 3 listed in the table in section 2. In order to perform a complementary
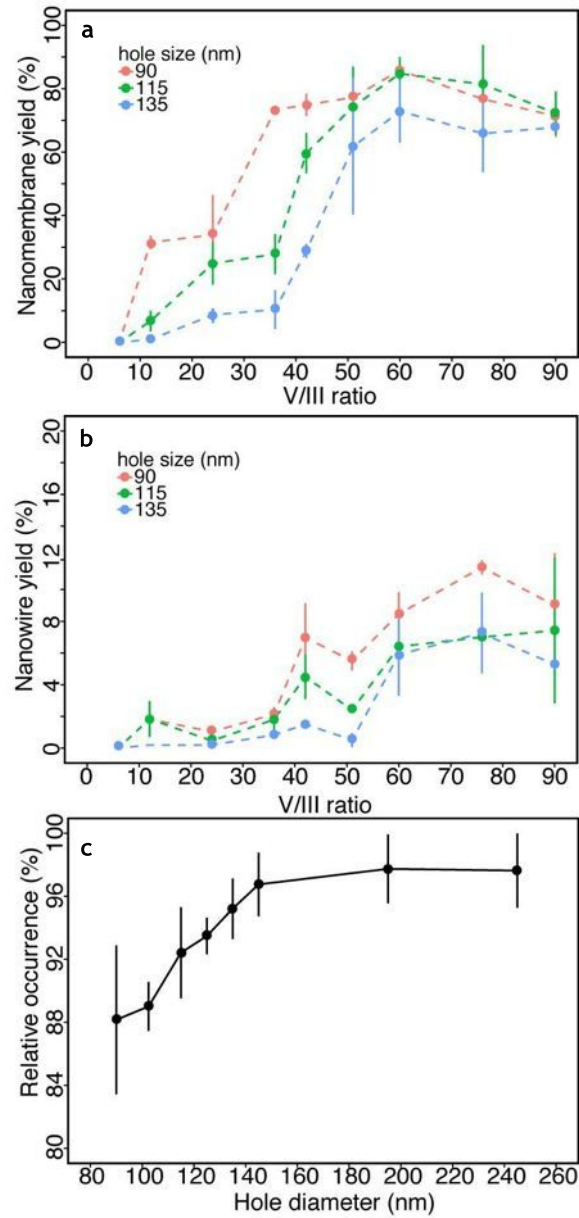
Figure 3. The yields of InAs nanomembranes (a) and nanowires (b) are plotted as a function of the V/III BEP ratio, for opening size 90, 115 and 135 *nm*. The yields of both nanostructures increase by increasing the V/III ratio until they reach a plateau. The results do not depend on the inter-hole distances. (c) Relative yield of nanomembranes at V/III ratio=60 as a function of the opening size: a small decrease is observed for smaller hole diameters.

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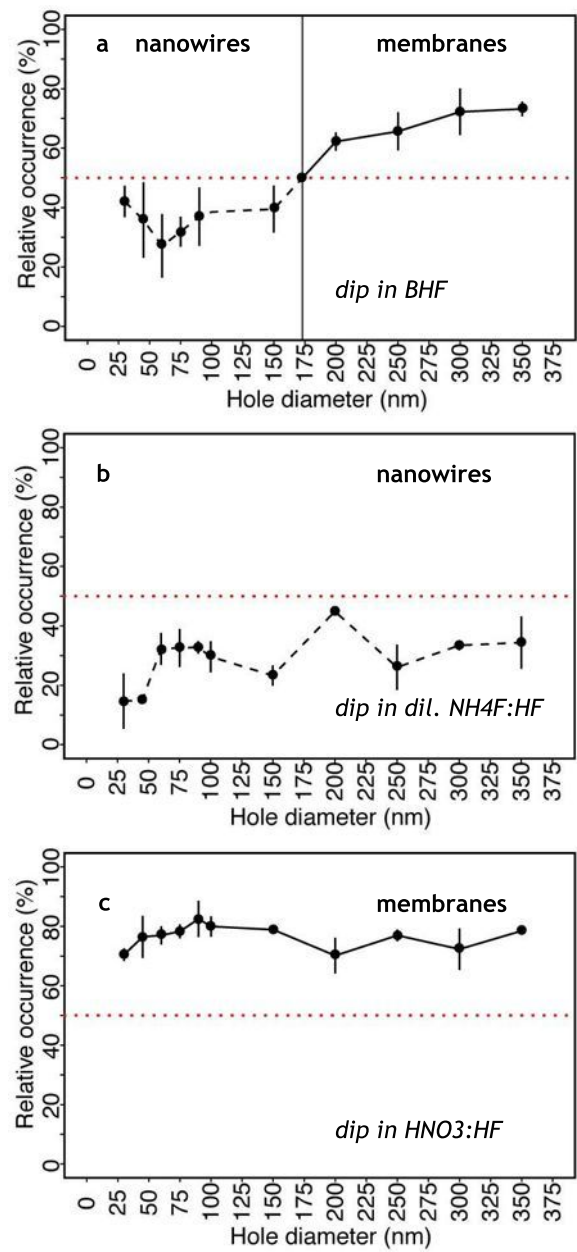
Figure 4. The relative occurrence of nanomembranes against nanowires for different sample preparation: a) dry etch followed by a standard BHF; b) dry etch followed by a dip in a highly diluted $NH_4F:HF$ solution; c) dry etch followed by a dip in a $HNO_3:HF$ solution. Different sample preparations can lead to a similar occurrence of nanomembranes and nanowires as in (a), favor nanowires as in (b) where the relative occurrence of nanomembranes drops to 20-30% or favor the nanomembranes as in (c) where their relative occurrence is as high as 70-80%.

test on a smoother surface, we substituted the BHF dip with a HNO_3:HF etch. Dry etching followed by a dip in HNO_3:HF:H_2O 50:3:20 solution is referred to as sample preparation N.4.

Fig. 4 (b) and (c) show the relative occurrence of nanomembranes against nanowires obtained with these solutions. Data are plotted as a function of the hole diameter, in analogy with Fig. 4 (a). Examining the results of the growth on the rough surface (sample prep. N.3) we found that the occurrence of nanowires is larger not only for small holes but also for large holes, where we had seen a majority of nanomembranes with the sample preparation N. 2. As we can see in Fig. 4 (b) the relative occurrence of nanomembranes against nanowires is always below 50%, even for holes larger than 200 *nm*. This strongly suggests that the increased roughness of the sample promotes the growth of nanowires. On the other hand, growth on the smoother surface (sample prep. N.4) gave a complementary result and indicated that a smooth surface promotes the occurrence of nanomembranes. The occurrence of nanomembranes has indeed increased to above 70% for all the hole diameters investigated (Fig. 4 (c)), similarly to what was obtained with the wet etch in sample preparation N.1. As a result, the occurrence of nanowires is reduced accordingly. We note that we obtained a high occurrence of nanomembranes also with another surface treatment consisting of oxidation and of dissolution of oxide and as such yielding smooth surfaces. In this case, after the reactive ion etch in He/CHF_3, the silicon surface has been oxidized in water in a clean room environment. Then, the thin layer of SiO_2 has been dissolved by a dip in buffered HF. This result (not shown) would support our hypothesis that by changing the roughness of the silicon surface it is possible to tune the type of nanostructure to be grown.

Fig. 5 shows a column chart with the absolute yield of nanomembranes as a function of the sample preparation (top). The same figure shows top view SEM micrographs of the different sample preparations where nanomembranes are highlighted in blue and the nanowires in red. The absolute yield of nanostructures obtained on the rough surface (sample prep. N.3) is similar to the what was obtained with sample preparation N. 2. Interestingly, the absolute yield is much higher on the smoother surface and it is very close to the values obtained with a full wet etching preparation (sample prep. N.1).

4. Discussion.

We turn now to the analysis on the role of the substrate preparation in the yield of nanowire and nanomembrane growth. We start by discussing the dependence of the relative occurrence on the hole diameter observed on the samples prepared with a full BHF etch and with the dry etch followed by a dip in BHF (sample prep. N.1 and N.2). To answer the question as to why the growth of nanowires is favored at the expenses of the nanomembranes for smaller hole sizes and rougher Si surfaces, we looked in more detail at the initial stages of growth for the two types of nanostructures.

In a previous publication [8] we showed that the InAs V-shaped nanomembranes stem from the two opposite facets of a nanoscale nucleus with a rectangular pyramidal shape. In the early stages of growth a Stranski-Krastanov (SK) type of quantum dot (QD) with {111} facets nucleates as a consequence of the high lattice mismatch between InAs and Si (11.6%). Subsequently, the growth proceeds selectively on the two (111)B facets of the QD forming the arms of the nanomembranes. The lateral growth of the arms, that consist of (0-11) and (01-1) surfaces, proceeds via step-flow in the <011>directions, slowly compared to <111>B. The width of the nanomembrane is thus given by the distance between the two opposite {110} planes and as such it is mainly determined by the width of the initial quantum dot [9]. An example of this is shown in Fig. 6 (a). Here, a cross sectional high-resolution TEM image taken at the interface between the InAs V-shaped nanomembrane and the Si substrate reveal the characteristic nucleus.

In Fig. 6 (b) we show a representative TEM image of the bottom part of a nanowire. In this case, we could never find a pyramidal nucleus from which the nanowire should originate. This result is in agreement with the extensive existing literature. The area where the initial stage of the growth takes place exhibits zinc-blende crystalline structure, as we can see in the associated Fast Fourier Transform in Fig. 6 (c). The absence of this pyramidal nucleus at the base of nanowires suggests that the SK growth of QDs is being suppressed in the holes. Moreover, the more frequent appearance of nanowires at smaller hole sizes indicates that the suppression of SK is more likely for smaller holes. It is worth noting that the SK growth mode on a confined area (like the apertures of the mask oxide) is different from that on a large unpatterned surface. As SK growth is a mechanism to release mismatch strain, there is a critical size for the hole below which the SK mechanism is suppressed [68]. This can explain why smaller holes tend to favor the growth of nanowires.

We now turn our attention to the role of the surface treatment (roughness) on the relative occurrence of nanomembranes/nanowires. An enhancement of the nanowire growth was obtained by substituting the wet etch in BHF with

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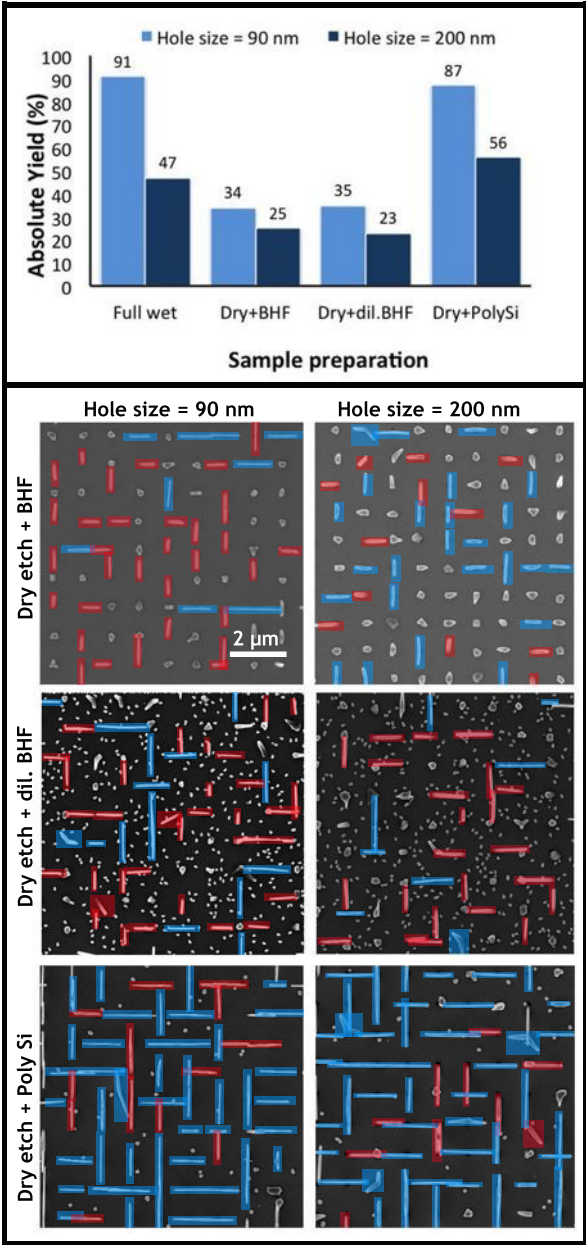
Figure 5. Top. Column chart reporting the absolute yield of nanomembranes as a function of the sample preparation. Hole size 90 *nm* and 200 *nm* have been chosen for representing the growth outcome in small and large holes. Bottom. Top view SEM micrographs of samples prepared with a dry etching in He/CHF$_3$ followed by different dips in wet etching solutions: in standard BHF, in a highly diluted NH$_4$F:HF, and in a HNO$_3$:HF solution for. The inter-hole distance is 1000 *nm* and the hole diameters are 90 *nm* and 200 *nm*. The V-shaped nanomembranes are highlighted in blue while the nanowires are highlighted in red. The relative occurrence of nanomembranes with respect to nanowires changes with the sample preparation.

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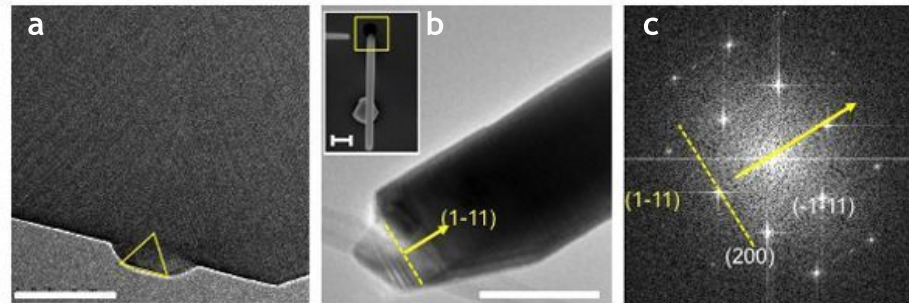
Figure 6. (a) High-resolution TEM image of the bottom part of a nanomembrane exhibiting the characteristic nucleus, which could be formed by a Stranski Krastanov growth. The scale bar is 100 *nm*. (b) Low magnification TEM image showing the bottom part of a representative nanowire; Inset: SEM top view micrograph of the nanowire with the bottom part marked in the yellow square. The scale bars of the TEM and SEM images are respectively 100 *nm* and 200 *nm*. c) Associated Fast Fourier Transform (power spectrum) showing that the crystalline structure of the nanowire at the initial stages of growth is zincblende.

the dry etch in CHF_3/He (from sample prep. N.1. to sample prep. 2). For a given hole diameter, the percentage of nanowires obtained with dry etching is higher than that obtained with wet etching.

Atomic Force Microscopy (AFM) measurements of the silicon oxide under the different treatments showed that its roughness does not vary. This prompted us to perform TEM analysis in order to study the morphologies of the holes obtained with the two etching procedures.

Cross-sectional low magnification HRTEM images of the nanoscale holes obtained by dry and wet etching followed by a dip in BHF are reported in Fig. 7. Fig. 7 (a), (d) and (g) are false color images showing the different morphology of the holes defined with wet etching (a) and dry etching ((d) large size hole and (g) small size hole). Fig. (b)-(c), (e)-(f) and (h)-(i) show the profile of the holes at different magnifications. In the case of dry etching the hole shows a deep dig in the crystalline silicon as the etching does not land selectively on the silicon substrate. The dig in silicon is reduced by decreasing the hole size due to the aspect ratio dependent etching (ARDE) phenomenon [69]. In Fig. 7 it can also be seen that, on the other hand, the silicon dioxide is selectively removed in the hole defined with a full BHF wet etch. We believe that the surface at the bottom of the holes for sample prep. N.2 (dry etching) is rougher than that obtained with the sample prep. N.1 (wet etching). CHF_3-based dry etching is known to modify the silicon surface, in part due to the ion bombardment of the RIE process, which can even sputter material off the surface. As a consequence, the silicon exposed to plasma is generally damaged [70], while concentrated and buffered HF wet etching does not affect the crystal order of the Si(001) surface [71, 72].

We have also tried to characterize the roughness of the silicon surface after the four sample preparations with AFM analysis. Unlike the TEM analysis reported above, in the AFM measurements the roughness of the silicon surface has been measured on large areas of the sample and not in the nanoscale holes: indeed, measuring roughness inside nanoscale holes is not within reach of the existing state-of-the-art AFM techniques. The AFM measurements proved inconclusive as we could not detect any difference in roughness on the large areas within the experimental error: this however does not disprove the TEM analysis conducted within the holes and is compatible with ARDE, the effect where the etch rate depends on the aspect ratio (depth/width) of the features to be etched [69].

In conclusion, we believe that the main driver favoring the formation of nanowires or nanomembranes is not as much the hole size *per se* but the roughness of the substrate: a small hole size simply increases the probability of having only a small area available for the SK transition which in turn favors the growth of nanowires since -as we have explained above- it is not relying on SK unlike in the growth of nanomembranes. An equal or better level of control can be achieved by directly acting on the roughness of the substrate: by increasing the roughness we can reach the critical size below which SK is suppressed. This gives us a way to control the relative occurrence of nanomembranes independently from the hole size in the array, effectively providing a new extra degree of freedom. Removing the constraint on the size of the array is an important step in obtaining more control on the design of nanosystems and in determining the size of the nanostructures.
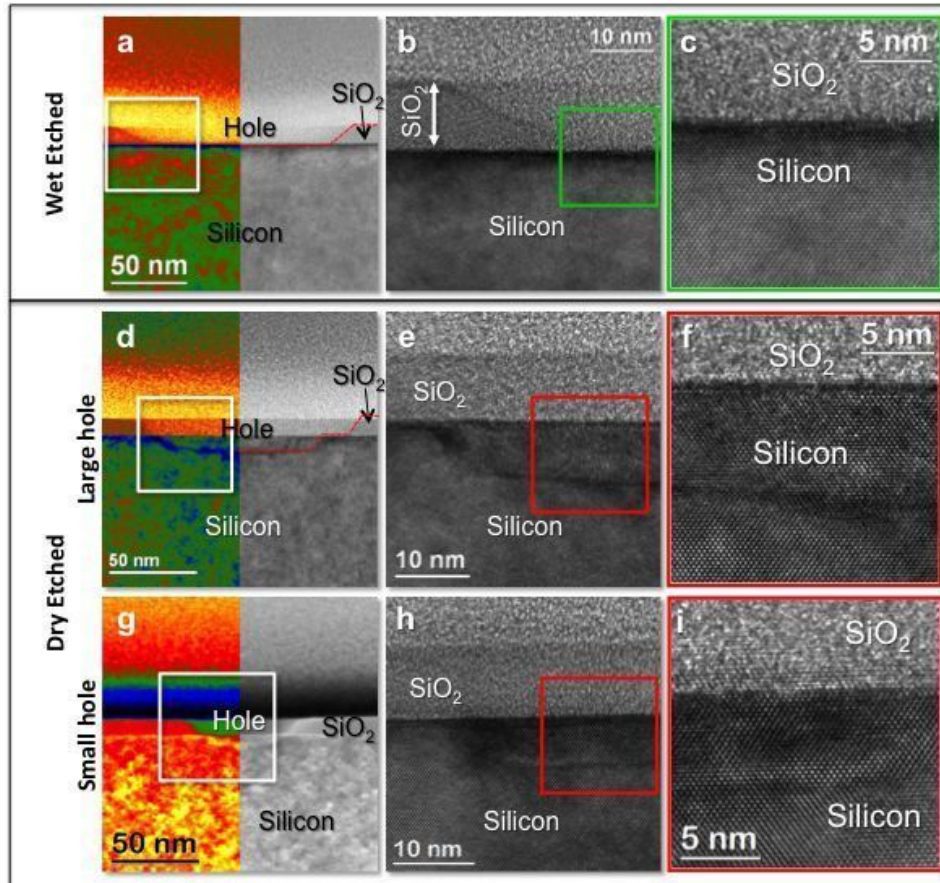
Figure 7. (a/d/g) Low magnification HRTEM/HAADF images of the patterned silicon substrate under wet/dry etched conditions. The left side of the images is false colored to enhanced the hole morphology. (b/e/h) HRTEM images of one corner of the holes. (c/f/i) Magnified details of the squared regions in (b/e/h) evidencing the silicon damage under the hole from the dry etching treatment (with the presence of crystal defects and recrystallization).

5. Conclusions.

In summary, we have investigated the role of the growth conditions and sample preparation parameters for the growth of InAs nanowires and nanomembranes. In particular we showed for the first time the role of the sample preparation (etching and cleaning steps) in favoring the occurrence of nanomembranes or nanowires. We showed that the formation of InAs V-shaped nanomembranes is quenched by increasing the roughness of the substrate since the formation of Stranski Krastanov quantum dots from which the nanomembranes stem is suppressed under these conditions. This quenching of the nanomembranes in turn favors the growth of nanowires. Conversely, the preparation of a smooth surface enhances the growth of nanomembranes at the expenses of nanowires growth. This work is a further step towards fabrication of nanostructure networks and the achievement of high complexity on the same substrate.

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Acknowledgement

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Papers not included in my thesis work

During my Ph.D. at EPFL I have produced hundreds of samples on which a large part of the research of LMSC has been conducted. In addition to my own research, as part of my daily work I have been collecting the requirements of team members which needed to grow samples for their experiments; I have translated those requirements into recipes for MBE growths and I have realized the samples themselves. Samples have been also sent to external collaborators.

This led to the publication of the following articles:

1. **Polarization reponse of nanowires à la carte**
   A. Casadei, E. Alarcon Llado, E. Russo-Averchi, D. Rüffer, M. Heiss, L. Dal Negro and A. Fontcuberta i Morral
   Scientific Reports 5 (2015) 7651
   I grew and doped the NWs studied in this paper.

2. **Tuning the *g*-factor of excitons and charged excitons confined to self-assembled (Al,Ga)As shell quantum dots**
   P. Corfdir, Y. Fontana, B. Van Hattem, E. Russo-Averchi, M. Heiss, A. Fontcuberta i Morral and R. T. Phillips
   Appl. Phys. Lett. 105 (2014) 223111
   I grew the samples investigated in this work.

3. **Probing inhomogeneous composition in core-shell nanowires by Raman spectroscopy**
   F. Amaduzzi, E. Alarcon-Llado, E. Russo-Averchi, F. Matteini, M. Heiss, G. Tütüncüoglu, S. Conesa-Boj, M. de la Mata, J.Arbiol and A. Fontcuberta i Morral
   J. Appl. Phys 116 (2014) 184303
   I took part to the growth of the wires and contributed to some parts of the text.

4. **Quantum dot opto-mechanics in a fully self-assembled nanowire**
   M. Montinaro, G. Wüst, M. Munsch, Mathieu, Y. Fontana, E. Russo-Averchi, M. Heiss, A. Fontcuberta i Morral, R. Warburton and M. Poggio
   Nano Lett. 14 (2014) 4454
   I grew the wires analyzed in the manuscript.

5. **Anisotropic magnetoresistance of individual Ni and CoFeB nanotubes with values of up to 1.4% at room temperature**
   D. Rüffer, M. Slot, R. Huber, T. Schwarze, F. Heimbach, G. Tütüncüoglu, F. Matteini, E. Russo-Averchi, A. Kovacs, R. Dunin-Borkowski, R. R. Zamani, J. Arbiol, A. Fontcuberta i Morral and D. Grundler
   APL Mat. 2 (2014) 076112
   I took part to the growth of the wires.

6. **Exciton Footprint of Self-assembled AlGaAs Quantum Dots in Core-Shell Nanowires**
   Y. Fontana, P. Corfdir, B. Van Hattem, E. Russo-Averchi, M. Heiss, S. Sonderegger, C.

Magen, J. Arbiol, R. T. Phillips and A. Fontcuberta i Morral
Phys. Rev. B 90 (2014) 075307
I grew the GaAs NWs studied in the paper.

7. **Characterization and analysis of InAs/p-Si heterojunction nanowire-based solar cell**
A. Dalmau Mallorqui, E. Alarcon-Llado, <u>E. Russo-Averchi</u>, G. Tütüncüoglu, F. Matteini,
D. Rüffer and A. Fontcuberta i Morral
J. Phys. D: Appl. Phys. 47 (2014) 394017
I grew the arrays of InAs NWs.

8. **Nanoskiving Core-shell Nanowires: A New Fabrication Method for Nano-optics**
D. Watson, R. Martinez, Y. Fontana, <u>E. Russo-Averchi</u>, M. Heiss, A. Fontcuberta i Morral,
G. Whitesides and M. Loncar
Nano Lett. 14 (2014) 524
I grew the wires reported in the paper.

9. **Photonic-Plasmonic Coupling of GaAs Single Nanowires to Optical Nanoantennas**
A. Casadei, E. F. Pecora, J. Trevino, C. Forestiere, D. Rüffer, <u>E. Russo-Averchi</u>, F. Matteini,
G. Tütüncüoglu, M. Heiss, A. Fontcuberta i Morral and L. Dal Negro
Nano Lett. 14 (2014) 2271
I grew the GaAs NWs and wrote part of the text.

10. **Plastic and Elastic Strain Fields in GaAs/Si core-shell Nanowires**
S. Conesa-Boj, F. Boioli, <u>E. Russo-Averchi</u>, S. Dunand, M. Heiss, D. Rüffer, N. Wyrsch, C.
Ballif, L Miglio and A. Fontcuberta i Morral
Nano Lett. 14 (2014) 1859
I grew the GaAs NWs studied in the paper.

11. **Enhanced second harmonic generation from InAs nano-wing structures on silicon**
E. F. Pecora, G. F Walsh, C. Forestiere, A. Handin, <u>E. Russo-Averchi</u>, A. Dalmau-Mallorqui,
I. Canales-Mundet, A. Fontcuberta i Morral and L. Dal Negro
Nanoscale 5 (2013) 10163
I grew the nanomembranes, did part of SEM characterization and I analyzed the behavior and the dimension of the nanostructures. I contributed to some illustrations, to the discussion of the paper and I wrote part of the text.

12. **Self-assembled quantum dots in a nanowire system for quantum photonics**
M. Heiss, Y. Fontana, A. Gustafsson, G. Wüst, C. Magen, D.D. O'Regan, J. W. Luo, B.
Ketterer, S. Conesa-Boj, A. V. Kuhlmann, J. Houel, <u>E. Russo-Averchi</u>, J. R. Morante, M.
Cantoni, N. Marzari, J. Arbiol, A. Zunger, R. J. Warburton and A. Fontcuberta i Morral
Nature Materials 12 (2013) 439
I grew the samples and I took part in the discussion of the paper.

13. **Hybrid axial and radial Si-GaAs heterostructures in nanowires**
S. Conesa-Boj, S. Dunand, <u>E. Russo-Averchi</u>, M. Heiss, D. Rüffer, N. Wyrsch, C. Ballif and

A. Fontcuberta i Morral
Nanoscale 5 (2013) 9633
I grew the GaAs NWs and wrote some parts of the text.

14. **Electrical transport in C-doped GaAs nanowires: surface effects**
A. Casadei, J. Schwender, E. Russo-Averchi, D. Rüffer, M. Heiss, E. Alarcó-Lladó, F. Jabeen, M. Ramezani, K. Nielsch and A. Fontcuberta i Morral
Phys. Status Solidi RRL 7 (2013) 890
I grew and doped the GaAs NWs, I analyzed their morphology and wrote some parts of the manuscript.

15. **Reversal mechanism of an individual Ni nanotube simultaneously studied by torque and SQUID magnetometry**
A. Buchter, J. Nagel, D. Rüffer, F. Xue, D. P. Weber, O. F. Kieler, T. Weimann, J. Kohlmann, A. B. Zorin, E. Russo-Averchi, R. Huber, P. Berberich, A. Fontcuberta i Morral, M. Kemmler, R. Kleiner, D. Koelle, D. Grundler and M. Poggio
Phys. Rev. Lett. 111 (2013) 067202
I grew the NWs investigated in the paper.

16. **Nanoscale multifunctional sensor formed by a Ni nanotube and a scanning Nb nano-SQUID**
J. Nagel, A. Buchter, F. Xue, O. F. Kieler, T. Weimann, J. Kohlmann, A. B. Zorin, D. Rüffer, E. Russo-Averchi, R. Huber, P. Berberich, A. Fontcuberta i Morral, D. Grundler, R. Kleiner, D. Koelle, M. Poggio and M. Kemmler
Phys. Rev. B 88 (2013) 064425
I grew the NWs studied in the manuscript.

17. **Cantilever Magnetometry of Individual Ni Nanotubes**
D. P. Weber, D. Rüffer, A. Buchter, F. Xue, E. Russo-Averchi, R. Huber, P. Berberich, J. Arbiol, A. Fontcuberta i Morral, D. Grundler and M. Poggio
Nano Lett 12 (2012) 6139
I grew the NWs investigated in the paper.

18. **Magnetic states of an individual Ni nanotube probed by anisotropic magnetoresistance**
D. Rüffer, R. Huber, P. Berberich, S. Albert, E. Russo-Averchi, M. Heiss, J. Arbiol, A. Fontcuberta i Morral and D. Grundler
Nanoscale 4 (2012) 4989
I grew the GaAs NWs and contributed to some parts of the text.

In review/preparation

1. **Tubular spin-wave nanocavities for 3D integrated nanomagnonics**
D. Rüffer, J. Mendil, S. Wang, T. Stückler, R. Huber, T. Schwarze, F. Heimbach, G. Tütüncüoglu,

F. Matteini, <u>E. Russo-Averchi</u>, R. R. Zamani, J. R. Morante, J. Arbiol, A. Fontcuberta i Morral and D. Grundler
submitted
I took part to the growth of the NWs object of this study.

2. **Three-dimensional nanoscale study of Al segregation and quantum dot formation in GaAs/AlGaAs core-shell nanowires**
L. Mancini, Y. Fontana, S. Conesa-Boj, I. Blum, F. Vurpillot, L. Francaviglia, <u>E. Russo-Averchi</u>, M. Heiss, J. Arbiol, A. Fontcuberta i Morral and L. Rigutti
submitted
I grew the NWs investigated in the paper.

4 Conclusion

The main topic of this thesis has been the investigation of the dynamics of the growth of gold-free III-V semiconductor nanowires (NWs) and nanomembranes on silicon substrates by molecular beam epitaxy. We have analyzed several aspects of the growth ranging from the nucleation to the organization in ordered arrays, with a particular attention on the early stages of growth. A detailed understanding of the growth process is a mandatory step in the integration of the III-V materials on the silicon platform, which would pave the way for applications in a broad range of electronic, optoelectronic and energy harvesting devices.

The first aspect of the growth that we have studied in detail is the control of the orientation of nanowires. We investigated and explained the appearance of non vertical wires in the growth of Ga-assisted GaAs NWs on Si(111) substrates. In particular we studied the occurrence of growth directions different from the ones predicted by the existing theory through a detailed analysis of the initial stages of growth of tilted wires. We proposed a new theoretical model, called *Three dimensional multiple order twinning*, according to which twinning and further growth on the lateral facets of the initial single seed result in the formation of secondary seeds. This in turn ends in the formation of new {111}B facets and allows the growth of the NWs in multiple discrete directions. The three-dimensional twinning phenomenon can be tuned as a function of the growth conditions. We demonstrated that this mechanism can be even be suppressed and that a 100% yield of vertical NWs can be obtained. Several questions are still open and some of them are currently addressed in our group. As an example, the nucleation of the nanowires depends on the physical properties of the substrate. To fully describe the dynamics of the process, a more detailed theory that considers also other major drivers like the cleaning steps, the roughness of the surface, the stoichiometry and thickness of the oxide still needs to be formulated.

Another key requirement for the use of NWs in the fabrication of nanoscale devices is the ability to control the growth of NWs on precise locations. In this work we have realized regular arrays of NWs on silicon substrates and we showed our capability to grow reproducible ordered InAs NWs arrays with yield of vertical wires between 91 and 96%. We highlighted the challenges in growing GaAs NWs on patterned Si(111) substrates and we showed that a successful growth

critically depends on the size and contact angle of Ga droplets and on their interaction with the substrate. We suggested how to improve the wetting properties at the open surface of the holes in order to achieve a high yield of vertical NWs. This requires a reconsideration of the typical nanofabrication methods for the realization of nanoscale holes and more challenging process flows could be required. Regular arrays are an ideal setting for studying growth mechanisms and fundamental matters for the use of NWs in applications; as an example, the possibility to optimize light absorption for an ideal array configuration suggests that NWs may have a role in the field of photovoltaics and encourages further studies in this direction. Furthermore, recent results in Raman spectroscopy indicates the NWs arrays as optimal setting to study structural and functional properties of the NWs, thanks to the enhancement of the LO phonon scattering.

As a third and final step, we took on the challenge of growing InAs nanostructures on oriented (001) substrates, yet another necessary step for the integration of III-V nanostructures in the existing technological processes . The research along this line led us to the discovery of a new class of nanostructures, that we called V-shaped nanomembranes. These structures grow vertically aligned with respect to the substrate and possess a unique morphology, with a peculiar V-shape. We shed light on their morphology, crystal structure, epitaxial relationship with the substrate and on the polarity of the arms through an in-depth scanning electron microscopy and transmission electron microscopy analysis. We provided a microscopic model for their formation, according to which they originate from two opposite facets of a Stranski-Krastanov type of quantum dots and extend along two opposite <111>B directions. We also provided a complete study of the effect of the growth conditions on the morphology of the membranes and we showed that they seem to grow by combining the growth mechanisms of NWs and QDs. As further step in the engineering of bottom-up nanostructures, we demonstrated the ability to manipulate their shapes, in moving from the growth of V-shaped nanomembranes to the growth of NWs without changing the growth conditions but by modulating the surface roughness of the substrate. The InAs nanomembranes possess interesting optical properties: they can significantly enhance electromagnetic radiation and second harmonic emission. As such, the V-shaped nanomembranes show an interesting potential as tip-enhanced nano sensors, light emitters and are good candidates to study non linear optical properties on the silicon platform.

More generally, we are convinced that III-V semiconductor nanostructures have interesting potentiality and possess many features which look promising as the field of microelectronics faces the challenges of down-scaling, which are becoming increasingly more important and have been getting more and more attention in these last years. We think that the work performed in this thesis has contributed in showing how a fundamental understanding of the nanostructures growth is key in the development of future applications and how open the field still is to new and sometimes surprising discoveries such as the V-shaped nanomembranes.

A Appendix

In this appendix I report the growth conditions of the samples on which this thesis work is based.

The growth of samples discussed in paper I and II has been performed on undoped 2 in. Si(111) wafers. These wafers have been introduced directly in the MBE machine without any surface treatment or removal of the native oxide.

The growth of nanostructures in arrays has been performed on 4 in. silicon wafers with different crystallographic orientations: Si(111) for the growth of NWs (paper III-IV) and Si(001) for the growth of V-shaped nanomembranes (paper V-VII). The sample preparation for the realization of the patterns is presented in detail in each paper.

The InAs and GaAs growth rate reported in the tables are obtained with a RHEED calibration at 520° and 580° respectively.

Three-dimensional twinning of self-catalyzed GaAs nanowires on Si substrates

Sample name	Ga Temp (°C)	Ga rate (A/s)	As tank Temp (°C)	As press (Torr)	As valve(%)	V/III ratio	T manip (°C)	T substrate (°C)
D1-11-03-02-A	900	0.3	383			15	720	618
D1-11-03-02-B	900	0.3	383			30	725	621
D1-11-03-04-A	900	0.3	383	4.50E-06	44	60	723	620

Suppression of three dimensional twinning for a 100% yield of vertical GaAs nanowires on silicon

Sample name	Ga Temp (°C)	Ga rate (A/s)	As tank Temp (°C)	As press (Torr)	As valve(%)	V/III ratio	T manip (°C)	T substrate (°C)
D1-11-03-02-A	900	0.3	383			15	720	618
D1-11-03-02-B	900	0.3	383			30	725	621
D1-11-03-04-A	900	0.3	383	4.50E-06	44	60	723	620
D1-11-06-06-A	900	0.3	383	4.50E-06	44	60	730	649

III-V nanowire arrays: growth and light interaction

Sample name	In Temp (°C)	In rate (A/s)	As tank Temp (°C)	As pressure (Torr)	As valve(%)	T manip (°C)	T substrate (°C)
D1-12-02-21-C	805	0.3	383	6.00E-06	46	580	500

Sample name	Ga Temp (°C)	Ga rate (A/s)	As tank Temp (°C)	As press (Torr)	As valve(%)	T manip (°C)	T substrate (°C)	Comments
D1-12-09-01-A	990	1	383	2.00E-06	27	690	630	
D1-12-09-01-B	990	1	383	2.00E-06	27	690	630	no degassing
D1-12-09-05-B	990	1	383	2.00E-06	27	690	630	
D1-12-09-07-A	990	1	383	2.00E-06	27	690	630	Oxide=21nm
D1-12-09-07-B	990	1	383	2.00E-06	27	690	630	Oxide=18nm
D1-12-09-07-C	990	1	383	2.00E-06	27	690	630	Oxide=13nm

Amorphous silicon mediates a high yield in GaAs nanowire arrays on Si obtained by the Ga-assisted method

Sample name	Ga Temp (°C)	Ga rate (A/s)	As tank Temp (°C)	As press (Torr)	As valve(%)	T manip (°C)	T substrate (°C)	Comments	
D1-13-12-18-A	990	1	405	2.00E-06	27	705	630	with a-Si	Ga predeposition
D1-13-12-18-B	990	1	405	2.00E-06	27	705	630		
D1-14-02-26-A	990	1	360	2.00E-06	31	705	630	with a-Si	
D1-14-02-26-B	990	1	360	2.00E-06	31	705	630	with a-Si	Ga predeposition
D1-12-09-20-A	990	1	405	2.00E-06	27	705	630		
D1-14-10-29-A	1007	1	only droplet deposition			685	620	a-Si PECVD on 2"	Ga predeposition
D1-14-11-06-B	1007	1	only droplet deposition			695	620	crystalline 2"	Ga predeposition

Vertical III-V V-shaped nanomembranes epitaxially grown on a patterned Si[001] substrate and their enhanced light scattering

Sample name	In Temp (°C)	In rate (A/s)	As tank Temp (°C)	As press (Torr)	As valve(%)	V/III ratio	T manip (°C)	T substrate (°C)
D1-12-02-21-A	790	0.2	383	8.00E-06	58	42	572	520
D1-12-02-16-A	790	0.2	383	1.15E-05	80	60	572	520
D1-12-02-28-A	790	0.2	383	8.00E-06	58	42	572	520

Growth mechanisms and process window for InAs V-shaped nanoscale membranes on Si[001]

Temperature serie

Sample name	In Temp (°C)	In rate (A/s)	As tank Temp (°C)	As press (Torr)	As valve(%)	V/III ratio	T manip (°C)	T substrate (°C)
D1-13-05-07-A	790	0.2	388	6.46E-06	70	51	492	440
D1-13-04-23-A	790	0.2	388	6.46E-06	70	51	512	460
D1-12-09-28-C	790	0.2	383	8.50E-06	54	51	532	480
D1-12-09-13-C	790	0.2	383	8.50E-06	54	51	552	500
D1-12-10-02-A	790	0.2	383	8.50E-06	54	51	572	520
D1-12-08-25-C	790	0.2	383	8.50E-06	54	51	592	540

Comment: the In BEP at the fixed temperature = 790 °C changed with time. In the temperature serie the As flux has been adjusted to keep constant the V/III ratio.

V/III BEP serie

Sample name	In Temp (°C)	In press (Torr)	As tank Temp (°C)	As press (Torr)	As valve(%)	V/III ratio	T manip (°C)	T substrate (°C)
D1-12-09-11-D	790	1.66E-07	383	2.00E-06	27	12	572	520
D1-12-09-13-A	790	1.66E-07	383	4.00E-06	34	24	572	520
D1-12-09-13-B	790	1.66E-07	383	6.00E-06	42	36	572	520
D1-12-02-21-A	790	1.66E-07	383	8.00E-06	58	42	572	520
D1-12-10-02-A	790	1.66E-07	383	8.50E-06	54	51	572	520
D1-12-02-16-A	790	1.90E-07	383	1.15E-05	80	60	572	520

Bottom – up engineering of InAs at the nanoscale: from V-shaped Nanomembranes to Nanowires

V/III BEP serie

Sample name	In Temp (°C)	In press (Torr)	As tank Temp (°C)	As press (Torr)	As valve(%)	V/III ratio	T manip (°C)	T substrate (°C)
D1-12-09-11-D	790	1.66E-07	383	2.00E-06	27	12	572	520
D1-12-09-13-A	790	1.66E-07	383	4.00E-06	34	24	572	520
D1-12-09-13-B	790	1.66E-07	383	6.00E-06	42	36	572	520
D1-12-02-21-A	790	1.66E-07	383	8.00E-06	58	42	572	520
D1-12-10-02-A	790	1.66E-07	383	8.50E-06	54	51	572	520
D1-12-02-16-A	790	1.90E-07	383	1.15E-05	80	60	572	520
D1-13-04-22-A	790	1.30E-07	383	9.90E-06	90	76	572	520
D1-14-04-07-A	790	1.40E-07	370	1.30E-05	100	90	590	520

Sample preparation serie

Sample name	In Temp (°C)	In press (Torr)	As tank Temp (°C)	As press (Torr)	As valve(%)	V/III ratio	T manip (°C)	T substrate (°C)	Preparation
D1-13-05-15-A	790	1.29E-07	388	7.76E-06	100	60	572	520	wet+BHF
D1-13-06-03-A	790	1.55E-07	393	9.77E-06	100	60	572	520	wet+BHF
D1-13-06-30-A	790	1.55E-07	393	9.77E-06	100	60	572	520	dry+BHF
D1-13-08-07-A	790	1.55E-07	393	9.77E-06	100	60	572	520	dry +polySi
D1-13-08-16-A	790	1.55E-07	393	9.77E-06	100	60	572	520	dry+dil BHF

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Eleonora Russo Averchi

Chemin de Pierrefleur 23B ● 1004, Lausanne (VD), Switzerland
078 670 43 82 ● eleonora.russo@epfl.ch

10 years of experience in semiconductor physics and clean room processes, both in industry and academia • Highly efficent, result-driven work ethics and methodology • Broad international experience and proven team work attitude.

ECOLE POLYTECHNIQUE FEDERALE DE LAUSANNE (EPFL)

Ph.D. in Materials Science and Engineering…………………………..….*2011-present*

- **Conducted** experimental research on III-V compound semiconductor nanostructures, focusing on the early stages of the nanostructure growth
- **Developed** several process flows through a systematic approach to Molecular Beam Epitaxy (MBE) growth parameter optimization, leading to original results such as 100% yield of vertical self-catalyzed III-V nanowires on silicon
- **Discovered** a new class of nanostructures (called "V-shaped nanomembranes")
- **Published** over 20 papers and presented results in several conferences in Switzerland and abroad

STMICROELECTRONICS

Technology R&D Engineer………………………………………………..….*2008-2011*

- **Developed** oxide dry etching processes for smart power devices down to 0.13 μm technology.
- **Worked** on development of processes both in FEOL and BEOL, from isolation to final bonding.
- **Contributed** to integration of *deep trench isolation*, *copper interconnections*, *through-silicon-vias* and *SOI substrates* on smart power process flow.

Process Engineer………………………………………………………….*2005-2008*

- **Engineered** plasma-etching R&D processes to achieve efficient and reliable large scale industrialization
- **Actively partecipated** in process technology transfer from R&D site to production facilities, in particular flash NOR 90 nm and 65 nm, embedded flash memories 0.18 μm and 90 nm
- **Managed** start up of new 200 mm equipments for dry etching at R&D facility in Italy and of the line for copper back-end in Singapore.

TETHIS S.r.l. (Start-up company in Nanotech)

Collaborator………………………………………………………………*2004 –2005*

- **Designed** an optimized apparatus for deposition of carbon and TiO2 nanoclusters thin films
- **Autonomously built** and put into production the same apparatus, later sold to a customer company

UNIVERSITA' DEGLI STUDI DI MILANO

Bachelor and Master degree in Physics (*cum laude*)…………………..….*1998-2004*

- **Master thesis work:** redesigned and put into production a high-intensity nanoparticle source for carbon nanoclusters thin films. Work conducted at CIMaINa (Prof. Paolo Milani), recognized as "academic center of excellence in nanotechnology"

Nationality: Italian; holder of Swiss B permit ● **Languages:** English (fluent), Italian (native), 153 French (advanced) ● **Interests:** Traveling, Reading, Cooking, Fitness, Interior Design