Crystalline Silicon Solar Cells with Co-Annealed Electron and Hole Selective SiC_x Passivating Contacts

Gizem Nogay, Andrea Ingenito, Esteban Rucavado, Quentin Jeangros, Josua Stuckelberger, Philippe Wyss, Monica Morales-Masis, Franz-Josef Haug, Philipp Löper and Christophe Ballif

***Abstract*—We present electron and hole selective passivating contacts based on wet-chemically grown interfacial SiO_x and overlying *in-situ* doped silicon carbide (SiC_x) deposited by PECVD. After annealing at 850 °C, excellent surface passivation on *p*-type planar c-Si wafer is obtained for both electron and hole selective contacts. Their potential is demonstrated at the device level by employing a simple process flow in which the junction formation of the two polarities is achieved with a single co-annealing step. Both-sides-contacted patterning-free planar *p*-type cells with an area of 4 cm^2 and screen printed metallization reach a *FF* of 83.4 % and a V_{oc} of 726 mV. Zirconium-doped indium oxide with excellent optoelectrical properties is used as front electrode. The decrease in the parasitic absorption in the front electrode results in higher photogenerated current. By realizing front-side-textured and rear-side-planar *p*-type cells, an efficiency of up to 22.6 % is achieved.**

***Index Terms*— Passivating contact, silicon solar cells, SiC_x, interfacial oxide, co-annealing, charge carrier transport, zirconium-doped indium oxide**

I. Introduction

Today's commercial crystalline silicon (c-Si) solar cells are limited by recombination losses at the direct metal-absorber interfaces. The current industrial trend is to define partial rear contacts. However, a reduced contacted area leads to increased series resistance and generates a trade-off between open circuit voltage (V_{oc}) and fill factor (*FF*) [1], [2]. A possible way to mitigate such a trade-off is offered by "passivating contacts", which consist of a thin buffer layer for surface passivation, capped with doped layers that selectively collect one type of carriers. A prime example of passivating contacts integration is the silicon heterojunctions (SHJ) cell technology which holds the current world record efficiency for the single junction c-Si solar cells [3]. However, as the electronic quality of intrinsic amorphous silicon layer deteriorates at temperatures above 250 °C, SHJ cell production requires high quality material and it is incompatible with industrial firing through metallization schemes. Recently the contact structure that combines a thin oxide (SiO_x) with a heavily doped Si-based layer is attracted considerable attention under the name of TOPCON [4], [5], poly-Si [6], [7] or POLO [8], [9]. In the 1970's similar structures were extensively investigated for bipolar junction transistors [10]–[14] and in the 1980's for solar cells [15]–[20]. The main advantages of the contact scheme are i) a full-area surface passivation, ii) an efficient charge-carrier transport and iii) the compatibility with industrial high temperature processes such as $POCl_3$ diffusion and contact firing. The approach is based on an annealing that forms a highly doped region in the c-Si wafer by dopants in-diffusion from the doped Si-based layer. As thin SiO_x is not necessarily self-passivating, a hydrogenation step is commonly applied to reduce the electronic defect states in the SiO_x and at the c-Si/SiO_x interface that may have appeared during the thermal treatment [21], [22]. However, it is still not well defined how these junctions can be integrated into a solar cell in a simple manner. Different strategies have been demonstrated, either based on the combination of a diffused homojunction front side with a poly-Si electron-selective passivating contact at the rear, or by integrating both electron and hole selective passivating contacts in an interdigitated back contacted solar cell architecture. Both approaches lead to excellent conversion efficiencies above 25.7 % [23], [24]. Another option is to realize the front and rear contacts with poly-Si-based layers. This is especially attractive as it would minimize the need for structuring step, enabling a lean fabrication process. Recently, both-sides-contacted poly-Si based solar cells were demonstrated on *n*-type wafer with an efficiency of 22.3 % using ion implanted poly-Si layers [25]. Especially for Czochralski (CZ) materials process step at high temperature for

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dopant in-diffusion can be used for impurity gettering from the bulk and to deactivate thermal donors which is more difficult to implement in low thermal budget passivating contacts such as in the SHJ solar cells [26]. Additionally, crystallization of the deposited layers induced by the high temperature treatment can reduce the series resistance — resistive losses — within the solar cell thanks to the high doping efficiency and mobility of partially crystallized layers [27], [28]. This can improve the contact resistivity in between transparent conductive oxide (TCO) and doped layer, consequently contributes to the lateral charge carrier transport which can enable to use more transparent (i.e. less doped) or cost effective (i.e. Indium-free) TCOs.

In this contribution, we present the development of *in-situ* doped SiC_x-based passivating contacts and their application over the full rear and front areas of the *p*-type c-Si solar cells i.e. patterning-free process. To that end, parallel plate plasma enhanced chemical vapor deposition (PECVD) is used as it is a versatile technique that enables to precisely control the electrical, micro-structural and compositional properties of the deposited layer. Moreover, it offers one-side process flexibility. The application of the Si-based alloys prepared by PECVD was reported [29], [30]. In this work the choice of SiC_x is motivated by its high resilience to blistering and stability to wet chemistry used for cell fabrication [21], [31]. Additionally, alloying with carbon offers the possibility to control the optical properties of the layer [32]. A lean fabrication process is ensured by forming front and rear junctions simultaneously in a *single* annealing step. Screen-printed front metallization is applied as it gives a possibility to use all the advanced metallization technologies such as multi-wire interconnection or multi-busbar, etc.

II. Experimental

Passivating contacts were investigated using 200-µm-thick chemically polished 4-inch *p*-type float-zone <100> c-Si wafers with a resistivity of 2 Ω·cm. After wet-chemical cleaning, a thin SiO_x layer (~1.2 nm) was formed by wet-chemical oxidation in hot nitric acid (69 % w.t at 80 °C) solution by submerging the wafers for 10 min. Subsequently, *in-situ* doped layers were deposited on both sides of the wafer at a temperature of 200 °C by parallel plate PECVD operated at an excitation frequency of 40.6 MHz, either the same layer on both sides of the wafer — symmetric samples — or electron- and hole-selective layers on opposite sides of the wafer — cells precursors — the latter is illustrated in Fig. 1 with step II. As process gases, silane (SiH_4), hydrogen (H_2), and methane (CH_4) were used together with phosphorous or boron containing gases for doping. The samples were then annealed in a quartz tube furnace under an inert gas atmosphere at temperatures between 850 and 925 °C. The heating ramp was kept as 10 °C/min, directly followed by a cooling ramp of 2 °C/min, i.e. without any dwell time at the final temperature. The hydrogenation process was applied to passivate the electronic defects at the chemical SiO_x/c-Si interface using a SiN_x:H donor layer on both sides, which releases atomic hydrogen upon annealing at 450 °C for 30 min on hot plate. After that, the SiN_x:H was removed in 5 % diluted HF. The interface passivation quality was monitored by injection dependent minority-carrier lifetime measurements using Sinton Instruments WCT-120TS [33], which gives an access to the implied operating voltages in open-circuit conditions (iV_{oc}) and at the implied maximum-power point (iV_{mpp}) [34]. The structural evolution of the boron-doped $SiC_x(p)$ upon annealing was analyzed by transmission electron microscopy (TEM). To that end, thin lamellae were extracted using the conventional focused ion beam (FIB) lift-out method and thinned to their final thickness using a gallium ion voltage of 2 kV (in a Zeiss NVision40 workstation). High-resolution TEM and scanning TEM (STEM) images were recorded, for the latter a high-angle annular dark-field (HAADF) detector at 200 kV in a double Cs-corrected FEI TITAN Themis microscope was used. The layer thicknesses were determined using variable angle spectroscopic ellipsometry (SE, HORIBA Jobin Yvon, UVISEL) in the energy range from 0.6 to 6 eV.

To investigate the potential of the passivating contacts at the device level, both-sides-contacted *p*-type solar cells featuring front $SiC_x(n)$ and rear $SiC_x(p)$ were prepared either on planar or on front-side-textured, rear-side-planar wafers by co-annealing. For the front-side-textured cells the chemical SiO_x was replaced with dry-grown UV-ozone (UV-O_3) oxide generated by photo-oxidation using a mercury vapor lamp with emission lines at 184.9 nm and 253.7 nm (Jelight, UVO-Cleaner 42). Following the preparation of the cell precursors, transparent conductive oxide (TCO) layers (either indium-doped tin oxide, ITO, or zirconium-doped indium oxide, IO:Zr) were sputtered on both sides to extract the collected carriers efficiently and to increase

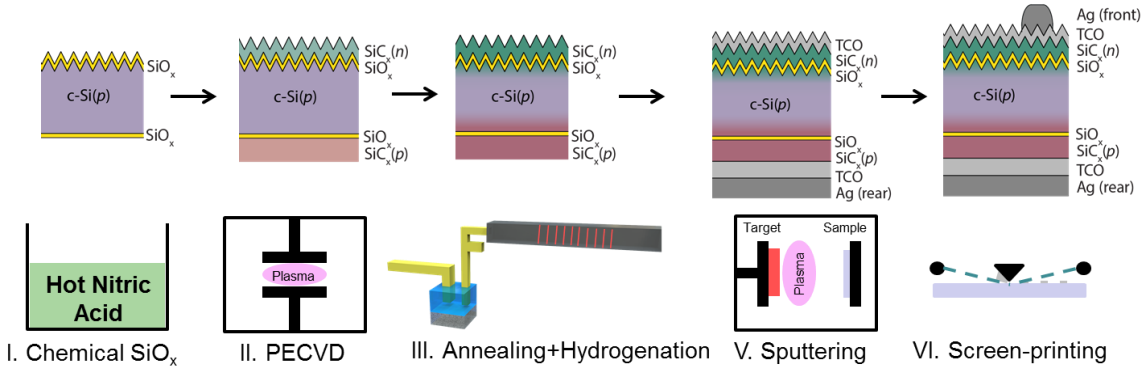


Fig. 1. Process flow for both sides-contacted poly-Si based *p*-type silicon solar cells.

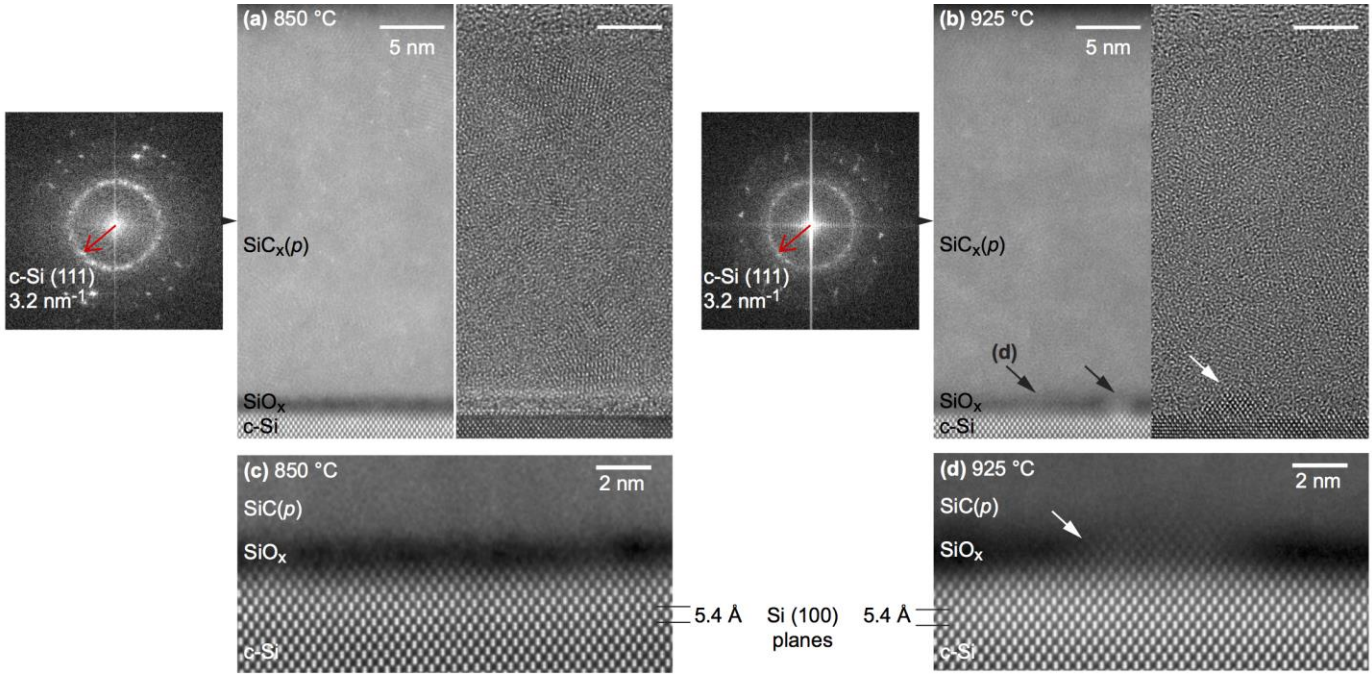


Fig. 2. High-resolution STEM HAADF (left panel) and TEM (right panel) image of the cross-section of the passivating contact stack after annealing at (a) 850 and (b) 925 °C (images of different regions). Fourier transforms of the STEM HAADF image taken at the position of the contact, i.e. excluding the wafer, are shown as insets. Arrows in (b) highlight the presence of crystalline protrusions appearing after annealing at 925 °C at the position of the thin interfacial SiO_x. (c-d) Higher magnification STEM HAADF images of the SiO_x, demonstrating in (d) its local rupture and the epitaxial growth of Si from the c-Si wafer towards the $SiC_x(p)$ contact layer.

the light in-coupling into the wafer. The solar cell size was determined by depositing the TCO layers through a 2.2 × 2.2 cm^2 shadow mask. A silver reflector/contact was sputtered onto the rear side and low temperature silver paste based on nanoparticle filler was screen-printed to realize the front metallization grid, followed by curing for 30 minutes at 210 °C on a belt furnace. Current density-voltage (*J-V*) characteristics of the cells were measured at 25 °C with a source meter (Keithley, 2601A), using an AAA solar simulator (Wacom) calibrated to 100 mW cm^{-2} with a c-Si reference cell. Suns-V_{oc} measurements were carried out with Sinton Instruments WCT-120 [35] on the individual cells at 25 °C to extract the series resistance (R_s)-free pseudo *J-V* curve. The external quantum efficiency (EQE) and reflectance (R) were measured using the Loana (pv-tools) tool on the full cell area including the metallization, and the internal quantum efficiency (IQE) was deduced accordingly [IQE =EQE/(1 − R)].

III. Results

A. $SiC_x(p)$ Rear Contact: Structural Evolution

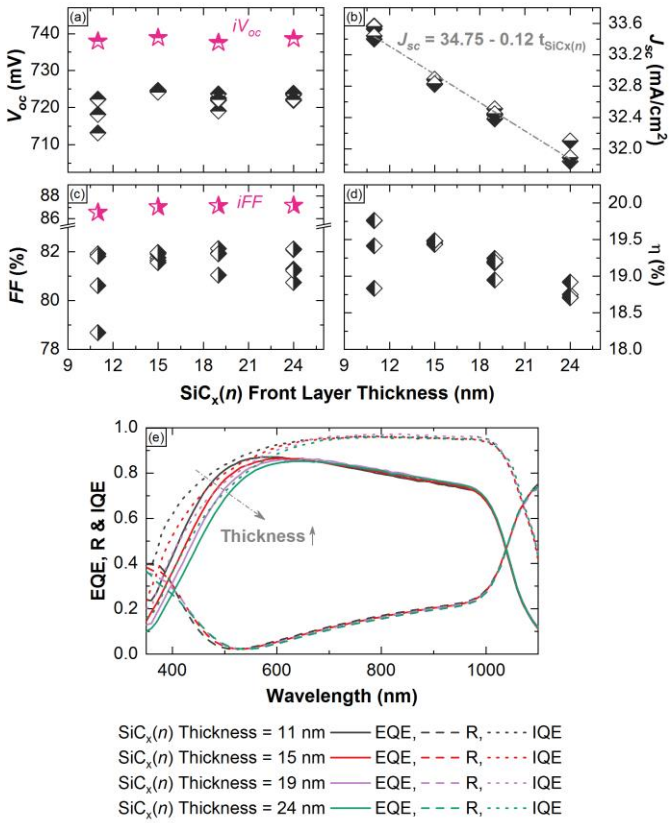
Structural changes occurring in the $SiC_x(p)$ rear contact upon annealing at 850 and 925 °C were assessed by atomic resolution STEM HAADF and TEM imaging (Fig. 2). The contact structure maintains its integrity after annealing at 850 °C, as indicated by the presence of a continuous dark SiO_x region between the crystalline (100)-oriented c-Si wafer (viewed along the [011] zone axis) and the $SiC_x(p)$ contact in the HAADF images [see Fig. 2(a) and (c)]. Indeed, the SiO_x appears darker as the contrast in HAADF images scales with the mean atomic number — we note that the sample thickness is an another source of contrast, which is constant here — [36]. The high-resolution TEM image that is shown in the right panel of Fig. 2(a) highlights the amorphous nature of thin interfacial SiO_x.

After annealing at 925 °C, the interfacial SiO_x is observed to break up locally, forming pinholes. Indeed, as indicated by the white arrows in Fig. 2(b) and (d), Si crystalline protrusions appear after annealing at 925 °C at the position of the interfacial SiO_x. This effect gives rise to the apparition of regions with a brighter HAADF contrast and that exhibits lattice fringes in the TEM images at the interfacial SiO_x position. A higher magnification STEM HAADF image of one of these regions is shown in Fig.2(d) and reveals Si atomic columns that are epitaxial with the c-Si wafer (so viewed along the [011] zone axis). Consequently, in this region $SiC_x(p)$ is directly in contact with the c-Si. Overall, Fourier transforms, acquired at the position of the $SiC_x(p)$ contact, indicate that the $SiC_x(p)$ layer contains randomly oriented crystalline Si domains after annealing at the temperature of both 850 and 925 °C.

In terms of surface passivation, the sample annealed at 850 °C reaches an iV_{oc} of 735 mV while the one annealed at 925 °C shows a strong degradation to values below 680 mV. This severe drop is likely linked to the local rupture of the SiO_x and the formation of pinholes, as revealed in Fig. 2(b) and (d). It is important to note that, even if no pinholes could be observed by TEM after annealing at 850 °C, their presence cannot be fully excluded. However, the pinhole density is significantly higher at 925 °C as many pinholes could be observed within the 5 μm long TEM lamella.

Fig. 3. (a) V_{oc}, (b) J_{sc}, (c) *FF*, and (d) efficiency of the planar both-sides contacted solar cells with different $SiC_x(n)$ front layer thicknesses extracted

from one-sun *J-V* characteristics. The implied values before metallization are indicated with stars in panel (a) and (c). (e) EQE, R and IQE of the cells.



B. *Planar solar cells: Impact of front layer thickness*

Aiming for a lean cell fabrication process, the front phosphorous-doped $SiC_x(n)$ is optimized to provide high surface passivation after a thermal treatment compatible with the one of the rear boron-doped $SiC_x(p)$ which is found to be 850 °C. More detailed information about compositional optimization of the front $SiC_x(n)$ layer will be presented elsewhere.

To determine the optimum front layer thickness, a set of planar solar cells featuring the same $SiC_x(p)$ as rear passivating contact and a front $SiC_x(n)$ with different thicknesses was realized. The thickness of the front $SiC_x(n)$ layer was altered from 11 to 24 nm as measured after the thermal treatment by means of spectroscopic ellipsometry. Transparent electrodes of 70- and 110-nm-thick ITO were sputtered at the front and rear, respectively.

The extracted cell parameters from the one-sun *J-V* characteristics as a function of $SiC_x(n)$ front layer thickness are shown in Fig. 3. The iV_{oc} and *iFF* values derived from the minority-carrier lifetime curves measured from the cell precursors before the metallization are indicated in Fig. 3(a) and (c) with pink stars. Prior to metallization, all both-sides-contacted planar *p*-type solar cells reveal iV_{oc} values between 737 – 739 mV which correspond to total J_0 values of 4.8 – 5.0 fA/cm^2. The pseudo-V_{oc} values extracted from suns-V_{oc} measurement are 728 mV for the best cell out of five on each wafer that features different thicknesses. Fig. 3(a) shows that the final V_{oc} values are in range of 720 to 725 mV for most of the cells. Thus, they are not significantly affected by the $SiC_x(n)$ thickness, except the cell featuring the thinnest front layer that reveals strong V_{oc} inhomogeneity over the five cells on the wafer. Overall, the difference between iV_{oc} and V_{oc} is ca. 13 mV and remains unaffected by the thickness variation. This loss in V_{oc} compared to the iV_{oc} might be attributed to sputtering induced damage, dark diode formation or a local ideality factor higher than one as iV_{oc} is perceptively affected by the local ideality factor, which is assumed to be unity.

According to Fig. 3(b), short-circuit current density (J_{sc}) drops linearly with increasing thickness, which is a direct consequence of parasitic absorption in the visible and UV regions. By calculating the slope of this gradual decline, the related J_{sc} loss is determined to be approximately 0.12 mA/cm^2 per nm. The EQE curves shown in Fig. 3(e) provide a consistent description for the trend of decreased J_{sc} with increased thickness, highlighting the optical losses at wavelengths below 600 nm when going from 11- to 24-nm-thick $SiC_x(n)$ front layer. Except for very short wavelengths below 400 nm, no variation is detected in the reflection data of the presented cells.

Regarding the charge-carrier transport, Fig. 3(c) reveals that the *iFF* values before metallization are increasing slightly but systematically from 86.5 to 87.2 % with $SiC_x(n)$ front layer thickness. However, the final *FF* values of the cells are in the range of 81 to 82 % and they do not exhibit a clear trend with thickness. The pseudo-FF values extracted from suns-V_{oc} measurements are increasing incrementally from 84.3 to 85.3 %. Overall, the conversion efficiency is dominated by the decrease in J_{sc} associated with the increased layer thickness. As the *FF* and V_{oc} values suffer from strong fluctuations for the cells with thinnest front layer, the 15-nm-thick $SiC_x(n)$ is selected for the following experiments.

C. *Impact of carbon concentration of the $SiC_x(p)$ rear contact*

A further cell optimization was conducted by changing the flow ratio of the CH_4 to SiH_4 gas precursors during the rear $SiC_x(p)$ layer deposition. In the previous section this ratio was set to 0.33, here it is varied between 0.25 and 0.80. Two sets of solar cells were prepared to assess additionally the impact of annealing temperature (850 and 875 °C). The front as well as the rear TCO was made of ITO. Fig. 4 shows the measured *J-V* characteristics of the cells.

According to Fig. 4(a), our optimum V_{oc} value is obtained with a CH_4/SiH_4 ratio of 0.29, reaching values of 726 and 723 mV for the cells annealed at 850 and 875 °C, respectively. It is observed that further increase in CH_4/SiH_4 ratio results in a gradual drop which appears to be more drastic for the cells annealed at 875 °C. Prior to hydrogenation, the measured iV_{oc} values of the cell precursors produced with the ratio of 0.29 were 714 and 706 mV after annealing at 850 and 875 °C, respectively. Following the hydrogenation process, the extracted iV_{oc} values reached to 735 and 733 mV. Overall, it is observed that the cells annealed at higher temperature benefit more from the hydrogenation-induced defect passivation.

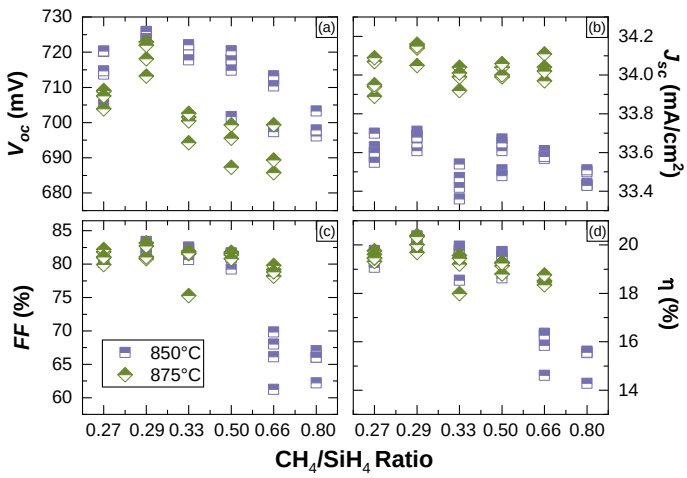


Fig. 4. The cell parameters extracted from one-sun *J-V* characteristic of the planar both-sides-contacted solar cells featuring the same front contact and $SiC_x(p)$ rear contacts prepared with different CH_4 to SiH_4 ratios (carbon concentrations).

Fig. 4(b) reveals that the cells annealed at 875 °C reach higher J_{sc} values compared to the ones annealed at 850 °C. The maximum J_{sc} difference is measured as 0.6 mA/cm^2. This can be explained with the increased crystalline fraction of the front $SiC_x(n)$ contact at higher temperature accordingly the parasitic absorption of the front layer reduces. Apart from that, the J_{sc} values do not seem to be significantly affected by the variation of the carbon concentration in the rear $SiC_x(p)$. The highest J_{sc} obtained is 34.1 mA/cm^2, which is promising considering the fact that these are planar solar cells with a very poor light in-coupling.

The *FF* attains maximum values of 83.4 and 83.2 % after annealing at 850 and 875 °C, respectively, for the CH_4/SiH_4 ratio of 0.29 [see Fig. 4(c)]. With further increase in carbon concentration, the *FF* values reveals a gradual decrease which can be attributed to the bandgap widening and corresponding increase in the valence band offset that poses a barrier to hole extraction. The extracted *iFF* from the effective lifetime curves before metallization were 86.9 and 86.5 % for the precursors produced with relative carbon flow of 0.29, annealed at 850 and 875 °C, respectively. For relative carbon flows of 0.66 and 0.80, *FF* degrades severely to values below 70 %. For both annealing temperatures very similar *FF* trends as a function of carbon concentration are observed.

We conclude that for the cells annealed at 875 °C, the *FF* and V_{oc} degradation dominates over the improved optics due to more crystalline $SiC_x(n)$ front layer resulting in a J_{sc} gain. Consequently, similar conversion efficiency values with the cells annealed at 850 and 875 °C are obtained. The highest efficiency is attained with the ratio of 0.29 resulting in 20.4 % for both annealing conditions but with different cell parameters. The cell annealed at 850 °C attains a V_{oc} of 726 mV, a J_{sc} of 33.7 mA/cm^2 and a *FF* of 83.4 % while the cell annealed at 875 °C attains a V_{oc} of 718 mV, a J_{sc} of 34.1 mA/cm^2 and a *FF* of 83.2 %. From the results, we conclude that the notably high *FF* value of 83.4 % indicates a reduced series resistance in $SiC_x(p)$ rear contact layers with lower carbon concentrations.

D. *Application of IO:Zr as front TCO*

In an effort to replace ITO with an alternative TCO, we tested IO:Zr as it features higher conductivity and higher transparency over a broad spectral range, from UV to NIR. Recently it was reported that the application of IO:Zr as front TCO in SHJ solar cells leads to a remarkable improvement in J_{sc} compared to the cells with ITO [37].

Both-sides-contacted planar *p*-type solar cells featuring $SiC_x(n)$ front and $SiC_x(p)$ rear contact produced with CH_4/SiH_4 ratio of 0.29 were used. The cells were annealed at 850 °C. As rear TCO, 110-nm-thick ITO was applied while as front TCO, 85-nm-thick IO:Zr with different oxygen concentrations were sputtered. During the IO:Zr sputtering, oxygen flow was varied from 0.5 to 1.6 sccm. The obtained electrical parameters are listed in Table I for 100-nm-thick IO:Zr layers. In the *as-deposited* state IO:Zr exhibits only an amorphous phase, yet after annealing at 200 °C it shows large crystals and well-ordered atomic structure which leads to high mobility values above 100 cm^2/Vs. More detailed information about the IO:Zr development and its optoelectronic properties can be found in Ref [37].

TABLE I
SUMMARY OF THE 100-NM-THICK IO:ZR PROPERTIES WITH O_2 FLOW AFTER ANNEALING AT 200 °C ON HOT PLATE UNDER AIR AMBIENT.

O_2 Flow [sccm]	Mobility [cm^2/Vs]	Free Carrier Density [cm^{-3}]	R_{Sheet} [Ω/□]
0.5	75	4.1×10^{20}	20
1.1	105	2.5×10^{20}	25
1.6	100	1.5×10^{20}	40

Fig. 5 shows the output characteristics of the planar cells featuring the front IO:Zr with different oxygen content. The extracted iV_{oc} and *iFF* values from the minority-carrier lifetime curves of the cell precursors before metallization are indicated with green stars in panel (a) and (c). The solar cell precursors reveal iV_{oc} values of ~ 740 mV. It is observed that the difference between iV_{oc} before metallization and final V_{oc} is not affected significantly.

For the cell produced with lower oxygen flow, the obtained J_{sc} values are fairly comparable with the cells produced by employing ITO as a front TCO (presented in previous sections). According to Fig. 5(b), by increasing the oxygen flow during the sputtering process the J_{sc} exhibits drastic improvement, resulting in values above 34.4 mA/cm^2. The reason for this improvement is a reduction in free-carrier absorption in the spectral range of 600 to 1000 nm (EQE, R and IQE measurements are not shown here). It is important to note that this is the highest current value obtained in the scope of this work for planar solar cells without double anti-reflective coating. The J_{sc} value above 34.4 mA/cm^2 is a promising value for planar solar cells, especially compared with an upper limit of 36.5 mA/cm^2 simulated with Wafer ray tracer [33] for an ideal planar device using nitride / c-Si / nitride / Ag on a 200-μm-thick wafer including 3 % shading losses.

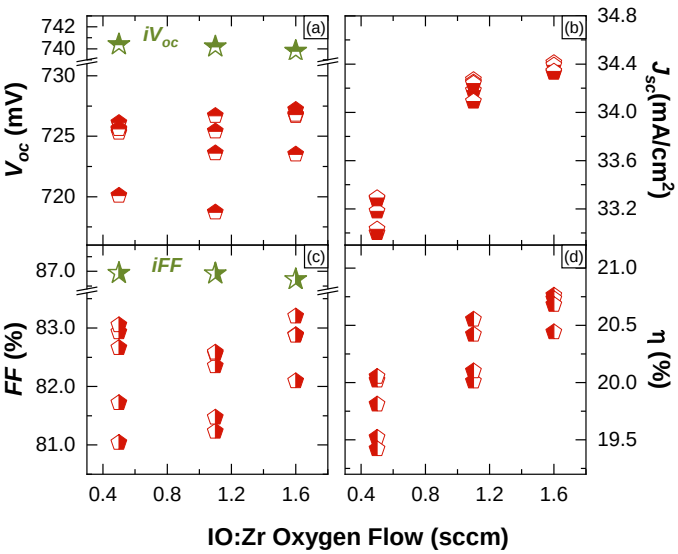


Fig. 5. The extracted cell parameters from one-sun *J-V* characteristic for the planar cells prepared by varying the oxygen concentration of the front IO:Zr. Measured implied values before metallization are indicated with stars.

It is observed that with increasing oxygen content of the IO:Zr layers, the corresponding sheet resistance is increasing, however this does not come at the expense of reduced *FF* at the device level as seen in Fig. 5(c). Before metallization the extracted *iFF* values are around 86.7 – 86.9 %. It appears the best *FF* of 83.2 % is obtained with the cell featuring the IO:Zr layer produced with the oxygen flow of 1.6 sccm. However, we note that *FF* values of the cells exhibit some fluctuation, probably due to the inhomogeneous IO:Zr deposition throughout the 4-inch c-Si wafer in the small lab-scale sputtering tool used in this work. The conversion efficiency of the cells shows an increasing trend with oxygen content of the front IO:Zr [see Fig. 5(d)]. The best cell reaches an efficiency of 20.8 % with V_{oc} of 727 mV, J_{sc} of 34.4 mA/cm^2 and *FF* of 83.2 %. To the best of our knowledge, this value is one of the highest conversion efficiency obtained with planar *p*-type c-Si solar cells without double anti-reflective coating.

E. Cells with textured front and planar rear

Following the verification of the excellent surface passivation and charge carrier extraction achieved with planar cells, the front $SiC_x(n)$ was further transferred to textured surfaces to improve the light in-coupling and to overcome the efficiency limitation due to J_{sc}. It is essential to note that transferring the *p*-type contact layer to textured surfaces is more challenging since it suffers more from the difference in the c-Si/SiO_x recombination velocity for <111> and <100> surface orientation [38], [39]. However, this is not an obstacle for commercialization as rear side planarization is commonly used in production lines of PERC solar cells [40], [41].

The obtained cell parameters from a preliminary test performed by applying standard ITO as front and rear TCO to the front-side-textured cell precursor are indicated in the first column of Fig. 6. The best cell indicated with pink star attains to a V_{oc} of 718 mV, a J_{sc} of 38.03 mA/cm^2, a *FF* of 79.7 % and an efficiency of 21.8 %. As one of the efficiency limiting parameters for this cell appears to be J_{sc} due to high parasitic absorption in the ITO and $SiC_x(n)$ front layer, the ITO is replaced with IO:Zr to reduce optical losses, in a first experiment only for the front side of the cells. Additionally, to investigate the potential J_{sc} improvement by minimizing the parasitic absorption of the front $SiC_x(n)$ layer, its thickness is reduced to 10 nm, indicated with purple triangles in Fig. 6.

The second column of Fig. 6 shows the comparison of the cells with different $SiC_x(n)$ front layer thickness featuring the same IO:Zr front and ITO rear TCOs. Before metallization the iV_{oc} – *iFF* values were extracted from lifetime curves using an optical factor of 0.9 as 729 mV – 85.4 % for the cell with standard $SiC_x(n)$ front and 722 mV – 86.2 % for thin $SiC_x(n)$ front layer. A possible interpretation can be that by thinning down the doped layer, the reservoir of dopant atoms in the layer decreases, leading to insufficient dopant diffusion. Following that, the IO:Zr front and ITO rear TCOs were sputtered on the cell precursors. It is observed that in the case of using 10-nm-thick $SiC_x(n)$, the V_{oc} is around 704 mV whereas for the standard 15-nm-thick $SiC_x(n)$ layer it reaches to 714 mV. As the difference between iV_{oc} before metallization and final V_{oc} is slightly higher for thinner $SiC_x(n)$ front — 18 mV for thin $SiC_x(n)$, 16 mV for standard $SiC_x(n)$ —, it suggests that the thinner passivating contact layer is more prone to degradation during TCO sputtering. The dark diode losses are determined to be 6 mV for both cells. Overall, it is observed that the textured surfaces are more sensitive to the damage induced by the TCO sputtering.

Fig. 6 (b) reveals a clear J_{sc} improvement with front IO:Zr compared to the cells featuring ITO on both sides. Regarding the impact of $SiC_x(n)$ layer thickness, it is seen that with decreased thickness from 15 to 10 nm, a J_{sc} gain up to 0.8 mA/cm^2 can be achieved due to the reduced front parasitic absorption. This observation indicates a clear trade–off between V_{oc} and J_{sc}; thinning down the $SiC_x(n)$ front layer leads to higher J_{sc} values; on the other hand, it causes a significant loss in V_{oc}, leading to similar final efficiencies.

Impressively high mobility values were already reported for IO:Zr in Table I, therefore it is expected that its superior electrical transport properties would be translated in to high *FF* values at the device level. Compared to the cells with ITO on both sides, the *FF* values reveal improvement with IO:Zr. The best *FF* of 81.8 % is reached with the cell featuring thin $SiC_x(n)$ front layer. The measured pseudo *FF* from suns-V_{oc} is 83.8 % and the calculated dark diode loss is around 0.8 %. The reason of the lower *FF* values of these cells compared to fully planar cells presented in previous sections might be related to the UV-O_3 oxide which is supposed to be more stoichiometric and denser compared to chemical SiO_x. Consequently, less efficient charge carrier transport manifests itself with low *FF*. We note that the previous optimizations were performed with chemical SiO_x, thus the observed *FF* limitation of front-side-textured cells with UV-O_3 oxide can be probably overcome by simply increasing the doping concentration of the PECVD layers, annealing temperature or annealing dwell time. Overall, Fig. 6 shows that the application of IO:Zr is beneficial for both electrical and optical performance of the front-side-textured *p*-

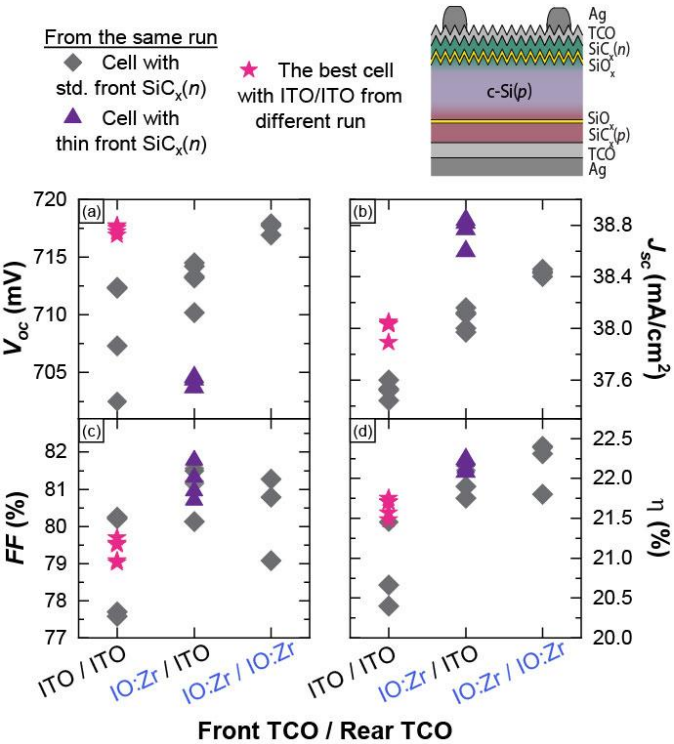


Fig. 6. Cell characteristics of the both-sides-contacted, front side textured, rear side planar cells with various TCOs. Grey and purple symbols are the cells from the same batch employed front $SiC_x(n)$ layer with standard and thinner thicknesses respectively while the pink stars indicate the best ITO/ITO cell from a different run.

type solar cells. The most pronounced effect is observed for the J_{sc}, thanks to the higher optical transparency of IO:Zr compared to ITO [37]. After replacing the front and rear ITO with IO:Zr, a conversion efficiency of 22.4 % is achieved with V_{oc} of 717 mV, *FF* of 81.3 % and J_{sc} of 38.4 mA/cm^2.

TABLE II
SUMMARY OF THE PARAMETERS FOR THE BOTH SIDES-CONTACTED FRONT SIDE-TEXTURED P-TYPE SOLAR CELLS WITH MgF_2.

Cell Description	V_{oc} [mV]	J_{sc} [mA.cm^{-2}]	FF [%]	η [%]
15-nm-front-SiCx (n)	719.0	38.3	80.9	22.3
After MgF_2	719.6	38.8	80.9	22.6
10-nm-front-SiCx(n)	704.6	38.6	81.8	22.2
After MgF_2	704.7	39.2	81.7	22.6

With the intention of minimizing the reflection loss, selected front-side-textured *p*-type solar cells were subjected to a second anti-reflection coating (ARC) of 85-nm-thick thermally evaporated MgF_2. The obtained cell parameters before and after MgF_2 deposition are summarized in Table II. Comparison of the J_{sc} values indicates a gain of 0.5 – 0.6 mA/cm^2 due to the double ARC. The highest J_{sc} achieved is 39.2 mA/cm^2 with the cell featuring 10-nm-thick $SiC_x(n)$ front layer, IO:Zr as a front TCO and ITO as a rear TCO. In combination with the V_{oc} of 704.7 mV and the *FF* of 81.7 %, this cell yields a conversion efficiency of 22.6 %. The cell with standard 15-nm-thick $SiC_x(n)$ front layer, IO:Zr as front and rear TCOs also attains to 22.6 % with V_{oc} of 719.6 mV, *FF* of 80.9 % and J_{sc} of 38.8 mA/cm^2.

IV. CONCLUSION

We demonstrated both-sides-contacted, screen printed cells featuring thin interfacial SiO_x covered with *in-situ* doped SiC_x layers deposited by PECVD. The solar cells were realized by employing a simple approach based on a single co-annealing step that serves to simultaneously form the junction of both electron and hole selective passivating contacts. Even though the full-area front side contact limits conversion efficiency due to parasitic light absorption, with this approach we demonstrated *p*-type planar solar cells reaching a V_{oc} of 726 mV and a *FF* of 83.4 %. Contrary to the commonly reported high-V_{oc} *n*-type solar cells, here we present a simple process for high-V_{oc} *p*-type solar cells which enables an excellent charge carrier transport as well. To increase the conversion efficiency further, the front $SiC_x(n)$ layer was adapted to textured surfaces by replacing the chemical oxide with UV-O_3 oxide. Front-side-textured and rear-side-planar *p*-type solar cells were realized by replacing the standard ITO with IO:Zr layer. Thanks to the higher transparency in the near-IR and better electrical properties of IO:Zr, both *FF* and J_{sc} gain were obtained concurrently. The optics of the selected cells was further improved by applying a second anti-reflective coating of MgF_2 and efficiencies up to 22.6 % were attained.

ACKNOWLEDGMENT

This work was supported in part by the Swiss National Science Foundation under Grant 200021_14588/1 and Grant IZLIZ2_156641, in part by the Swiss Federal Office for Energy under Grant SI/501253-01, and in part by the European Commission in the project Horizon 2020 under Grant 727529. The interdisciplinary center for electron microscopy of EPFL is acknowledged for the use of the electron microscopes. The authors thank W. Wu for MgF_2 depositions.

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