High fill-factor miniaturized SPAD arrays with a guard-ring-sharing technique

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Abstract: We present a novel guard-ring-sharing technique to push the limit of SPAD pixel miniaturization, and to demonstrate the operation of SPAD arrays with a 2.2 μm-pitch, the smallest ever reported. Device simulation and preliminary tests suggest that the optimized device design ensures the electrical isolation of SPADs with guard-ring sharing. 4×4 SPAD arrays with two parallel selective readout circuits are designed in 180 nm CMOS technology. SPAD characteristics for the pixel pitch of 2.2, 3, and 4 μm are systematically measured as a function of an active diameter, active-to-active distance, and excess bias. For a 4 μm-pitch, the fill factor is 42.4%, the maximum PDP 33.5%, the median DCR 2.5 cps, the timing jitter 88 ps, and the crosstalk probability is 3.57%, while the afterpulsing probability is 0.21%. Finally, we verified the feasibility of the proposed technique towards compact multi-megapixel 3D-stacked SPAD arrays.

1. Introduction

In recent years, CMOS-compatible single-photon avalanche diode (SPAD) technology has attracted a wide range of scientific and industrial applications, thanks to its single-photon sensitivity and picosecond photoresponse. Its application fields cover light detection and ranging (LiDAR) sensors for autonomous and semi-autonomous vehicles and robots [1–4], solid-state detectors for medical imaging, time-resolved cameras for fluorescence lifetime imaging microscopy (FLIM) [5,6], and optical receivers for visible light communications [7], as well as single-photon sensitive scientific imaging [8,9]. As in conventional CCD and CMOS image sensors, pixel array size contributes to signal-to-noise ratio and dynamic range, ultimately determining image quality. When the sensor format is fixed, larger array sizes can only be achieved by shrinking pixel pitch. For over 15 years, there has been a continuous effort to increase the size of SPAD arrays and thus reducing pixel pitch has been a great part of that effort. The highest SPAD array size to date is 1 Mpixel with 7 to 13.4% fill factor [10], while comparable resolution has been reported for other photon counting approaches including CMOS-based ultra-low-noise pixels [11,12] and vertical APDs [13,14]. The smallest SPAD pixel pitch reported is 3 μm for test structures with 14% fill factor [15]. Due to the existence of guard-ring structures, where no photons can be detected, shrinking SPAD pixel pitch below 10 μm could lead to the reduced fill factor. Several countermeasures to this issue have been proposed recently, such as well-sharing [16], on-chip microlens [17–19], and 3D-stacking [3,4,20,21], which enable better fill factor in small SPAD pixels. Yet, the fundamental limit of SPAD pixel miniaturization lies in the photon-insensitive guard-ring and pixel isolation structures.

In this paper, we demonstrate a novel guard-ring-sharing technique to push the limits of SPAD pixel miniaturization. The SPAD performance has been verified in guard-ring-shared 4×4 arrays of 2.2 μm-pitch SPAD, the smallest pixel pitch ever reported. In addition, significant improvement of fill factor, dark count rate (DCR), photon detection efficiency (PDE), and timing jitter performance with respect to the state-of-the-art small SPAD pixels is observed in the

guard-ring-shared 3 μm and 4 μm pixels. The 2.2 μm-pitch SPAD pixels showed excellent performance in afterpulsing and timing jitter, while the DCR and PDP are deviated from larger pixels. Combined with on-chip microlens and 3D-stacking approaches, the proposed technique provides a promising solution to achieve a compact multi-megapixel SPAD array.

2. Device structure, simulation and preliminary test

To address the physical limit of SPAD pixel miniaturization, the need of pixel circuitry adds uncertainty to pixel pitch and fill factor, given that the circuit area is highly dependent on technology node, architecture, and layout. Thanks to recent progress in 3D-stacked technologies though, this uncertainty is largely removed and SPADs can be assumed to be densely packed, thus the influence of pixel circuit area is not taken into account in this paper, unless otherwise noted. The discussion can be naturally extended to monolithic 1D [22] or small-scale 2D arrays [1,23], where pixel circuits are located outside the array.

A schematic cross-section of the p-i-n SPAD [24], combined with well-sharing technique [16], is shown at the top of Fig. 1(a), where the p-well defines the active area of the photosensor. Key parameters in pixel miniaturization are active diameter D_a, active-to-active distance L_{a-a}, and pixel pitch L_p, where $L_p = D_a + L_{a-a}$. Assuming circular active area, the SPAD fill factor is given as:

$$FF = \frac{\pi D_a{}^2}{4L_p{}^2} = \frac{\pi D_a{}^2}{4(D_a + L_{a-a})^2}. \tag{1}$$

For a given pixel pitch L_p, smaller L_{a-a} is desirable to improve fill factor. In the well-shared SPADs, L_{a-a} consists of isolation well (n-well) width and twice the guard-ring width. Typically, the guard-ring width is designed to be at least 1 μm to avoid premature edge breakdown, whereas the minimum isolation well width is 0.5 μm due to process requirements. Hence, L_{a-a} smaller than 2.5 μm is not practically useful to guarantee reasonable photon detection probability (PDP) and dark count rate (DCR), as well as high levels of manufacturability. Under the above assumptions, when targeting 20% fill factor, the theoretical limit of well-shared SPAD pitch is 5 μm, irrespective of fabrication technology. Pixel pitch smaller than this limit has been investigated previously [15], whereas the measured low PDP and high DCR suggest that the device suffered from premature edge breakdown.

To overcome these limitations, we propose a novel guard-ring-sharing technique. The schematic cross-section of guard-ring-shared SPAD is shown at the bottom of Fig. 1(a). Compared to the conventional well-shared structure, the isolation well between neighboring pixels is eliminated. The pixel is virtually isolated by the shared guard-ring region with a shallow trench isolation (STI). Assuming the shared guard-ring width of 1 μm, the theoretical limit of pixel pitch can be reduced to 2 μm for 20% fill factor. In Fig. 1(b), the electric field distribution is extracted by 2D-TCAD simulation. In contrast to well-shared devices (top), guard-ring-shared devices feature neighboring active regions in close proximity (bottom). The corresponding simulated electrostatic potential distribution is shown in Fig. 1(c). The potential profiles on the white dashed lines in Fig. 1(c) are plotted in Fig. 1(d). For well-sharing (top), potential barrier height between two active area is determined by cathode voltage V_C, typically in the order of 15 to 30 V.

In contrast, the minimum required potential barrier to operate the SPAD is determined by excess bias V_{ex}; when reducing the potential barrier height, an increase in the punch-through current between neighboring p-wells may induce electrical coupling of output signals, thus leading to the electrical crosstalk. The punch-through current is maximized when the potential difference between the p-wells is maximum, i.e. when one SPAD is quenched and the adjacent SPAD is not quenched. The maximum bias difference is V_{ex}, and hence a potential barrier higher than V_{ex} is sufficient to block punch-through. For guard-ring sharing (bottom), the isolation region between p-wells is fully depleted, and the potential barrier is reduced below 10 V, but it can be higher than V_{ex}, typically 1 to 6 V. Careful design of the potential barrier by optimizing doping
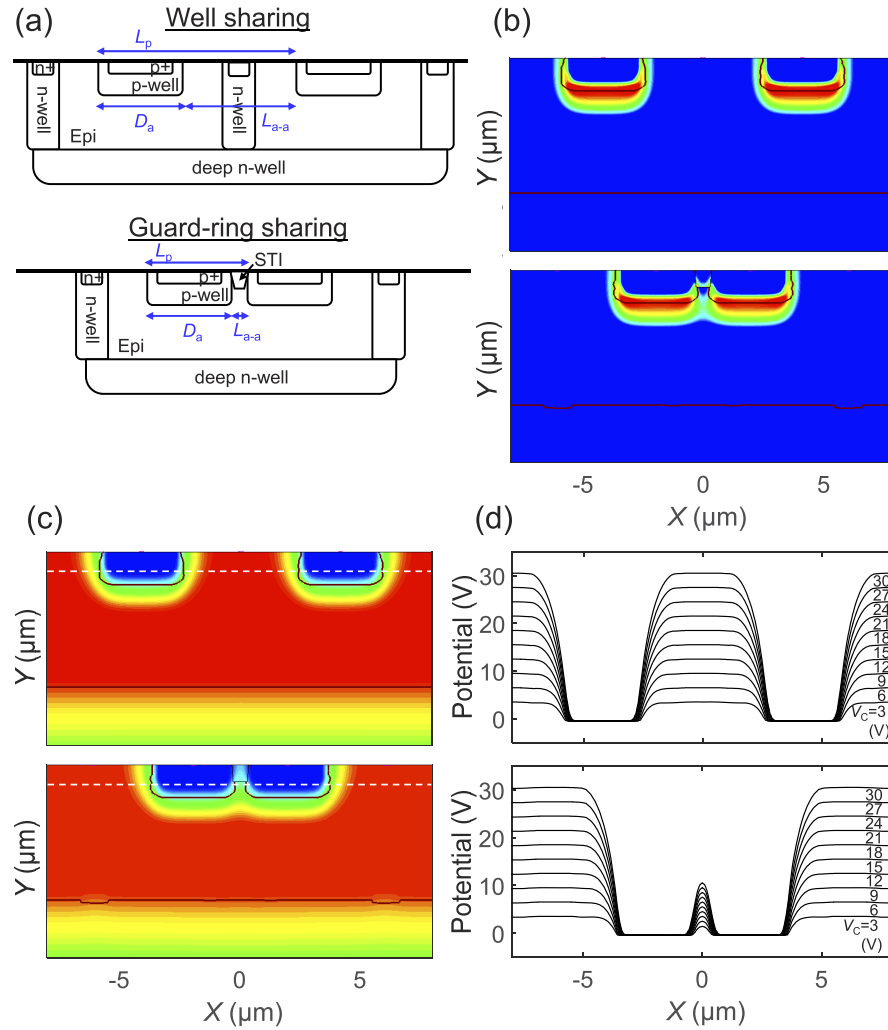
Fig. 1. Comparison of well-sharing (top) and guard-ring-sharing techniques (bottom). (a) Cross-sectional views of p-i-n SPADs. (b) Simulated electric field distributions. (c) Simulated electrostatic potential. (d) 1D potential profile on the white dashed line in (c) for cathode voltage $V_C = 3$ to $30\,\mathrm{V}$ with 3 V-step.

conditions enables the significant reduction of active-to-active distance without degradation of the crosstalk and other SPAD properties.

To experimentally confirm the feasibility of the guard-ring-sharing technique, preliminary tests were performed with a 3-terminal two-SPAD device. Figure 2 shows the measured results. As shown in the inset of Fig. 2(a), two guard-ring-shared SPADs are designed, where cathode voltage V_C and anode voltages V_{A1} and V_{A2} can be applied externally. In the experiment, V_{A2} is fixed at 0 V, and V_{A1} is swept from -8 V to 8 V for several different values of V_C (8 to 15 V with 1 V-step). The breakdown voltage of this SPAD is above 23 V, and no avalanche current is expected in the measured range. D_a and L_{a-a} for the measured device were 3 µm and 1 µm, respectively. As shown in Fig. 2(a), no significant current to anode 1 (I_{A1}) is observed for $V_{A1} < 3$ V. Exponential increase of I_{A1} is observed for positive V_{A1}, indicating punch-through current. The rising value of I_{A1} is dependent on V_C. The critical voltage for punch-through, V_{PT}, can be defined as V_{A1} giving $I_{A1} = 100$ pA. Note that the absolute value of current to anode 2 (I_{A2}) was equivalent to I_{A1}, whereas cathode current (I_C) was below the measurement limit of 10 pA over the measured range. Figure 2(b) shows the V_C dependence of V_{PT}, exhibiting linear increase of V_{PT} for V_C. The result is consistent with our simulations, where potential barrier height increases with increasing cathode voltage. Linear fitting of the data is shown as a dashed line, indicating that in the Geiger mode, with V_C above 20 V, the potential barrier is high enough to suppress the punch-through current with V_{ex} at up to 10 V. The results strongly suggest that in an optimized process and device conditions, adjacent p-wells *can be electrically isolated without isolation well*. Note that the proposed structure is distinct from STI-bounded SPADs [25], where the STI has a direct contact with the multiplication region and its surface traps degrade the noise performance. In our device, the STI is spatially isolated from the buried multiplication region to avoid influence on the noise performance. The STI between p-wells is introduced to suppress punch-through and to enhance V_{PT}. Separate measurements were carried out with a guard-ring-shared device without the STI isolation (not shown), which showed a similar trend but with slightly lower V_{PT}.
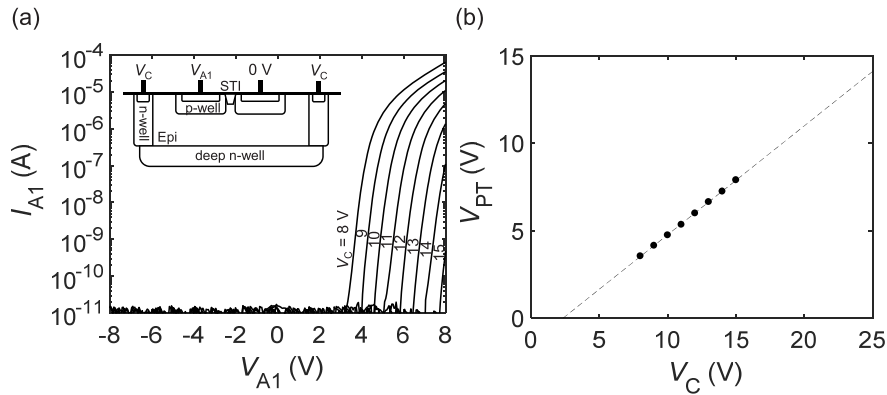

Fig. 2. Results of preliminary test with 3-terminal two-SPAD device. (a) I-V characteristics for anode 1 with V_{A2} fixed at 0 V and V_C at 8, 9, 10, 11, 12, 13, 14, and 15 V. Inset shows a schematic cross-section of the test device. (b) Punch-through voltage V_{PT} as a function of V_C, where V_{PT} is defined as V_{A1} giving $I_{A1} = 100$ pA. Dashed line is the linear fit.

3.   Experimental results with 4×4 SPAD arrays

3.1.   Chip design

4×4 SPAD arrays with selective readout circuits were designed with monolithic 180 nm CMOS process, which was customized for low noise SPAD, to verify the Geiger-mode operation of guard-ring-shared SPADs. Figure 3(a) shows a circuit diagram; 8 different types of 4×4 SPAD arrays were designed in a single chip. The anode terminal of each SPAD in an array is connected to an array of pixel circuits in one-to-one correspondence. The pixel circuit comprises a quenching and a cascode transistor [26], followed by a level-shifting inverter and two parallel tristate inverters. Using demultiplexers and multiplexers, pulsed photon counting signals from two arbitrary SPADs in a single 4×4 array of interest can be streamed out through OUT1 and OUT2. The two parallel output configuration enables direct measurement of inter-avalanche time correlation for two SPADs, as well as the parallel measurement of DCR, PDP, afterpulsing probability and timing jitter for single SPAD.
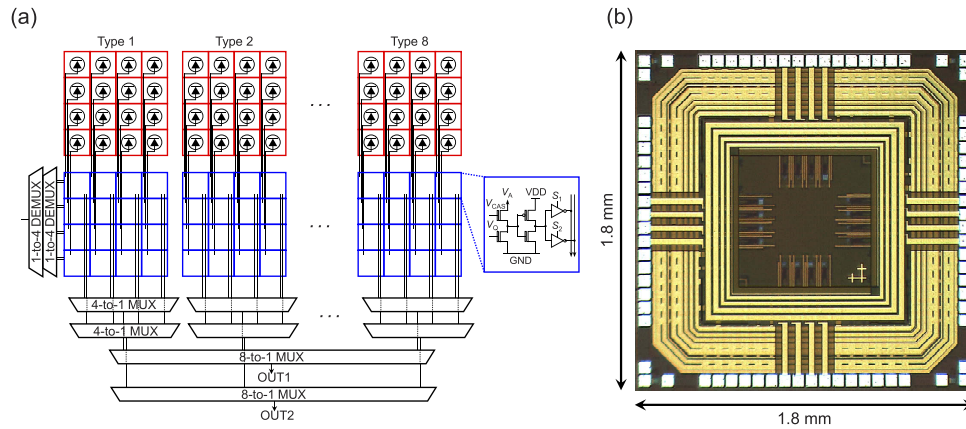

Fig. 3. Architecture of eight 4×4 SPAD arrays. (a) Circuit diagram of 4×4 SPAD arrays with two parallel selective readout circuits. (b) Chip micrograph with the size of 1.8 mm×1.8 mm.

Figure 3(b) shows the chip micrograph. The size of a single chip is 1.8 mm×1.8 mm, and four dies with the same format and readout circuit, but with different SPAD structures and dimensions are designed. A single die contains two sets of devices shown in Fig. 3(a). In total, 64 different types of SPADs are tested. Three pads at the corners of the chip are for the preliminary test devices discussed in the previous section.

3.2.   Fill factor and PDP

Figure 4(a) shows a geometrical fill factor of designed SPADs. The fill factor is defined as the drawn active area subtracted by the area of metal layers overlapping the active area. Active diameters $D_a = 1.2$, 2, and 3 µm are designed in combination with active-to-active distances $L_{a-a} = 1$, 1.6, 2.2, 2.8, and 3.4 µm. Owing to the guard-ring-sharing technique, fill factors of up to 19.5%, 32.3% and 42.4% were achieved for the pixel pitches $L_p = 2.2$, 3, and 4 µm, respectively. Note that, when adopting this technique to 3D-stacking process, the fill factor can be further enhanced due to the lack of shadowing effect by metal interconnects.

Figure 4(b) shows the measured PDP as a function of wavelength. The plotted PDP is calculated as an average of PDPs from two pixels in an array. As in the conventional SPAD without guard-ring sharing, the PDP increases by increasing the excess bias voltage V_{ex}. For the SPAD with 3 µm active diameter and 1 µm active-to-active distance, maximum PDP of
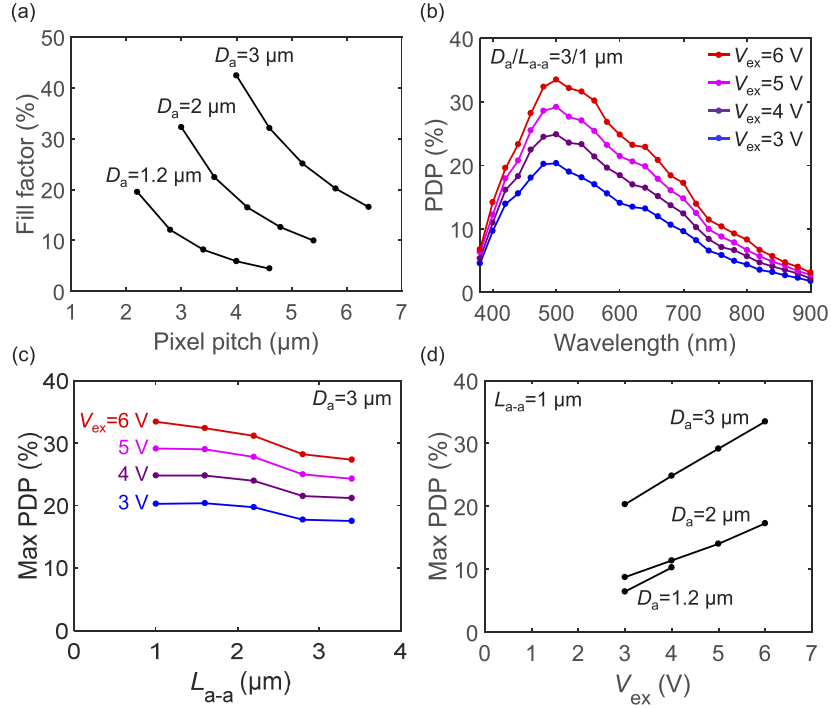
Fig. 4. Fill factor design and PDP measurement results for guard-ring-shared SPADs. (a) Fill factor of designed SPADs with different active diameters and pixel pitches. (b) Measured PDP for SPAD with $D_a = 3\,\mu m$ and $L_{a-a} = 1\,\mu m$ as a function of wavelength. (c) Maximum PDP as a function of L_{a-a}. (d) Maximum PDP as a function of excess bias and D_a.

33.5% is obtained with $V_{ex} = 6$ V at $\lambda = 500$ nm. The corresponding photon detection efficiency (PDE), defined as a product of PDP and fill factor, is 14.2%, which is considerably higher than state-of-the-art miniaturized SPADs. Relatively broad spectrum is observed, and the PDP with $V_{ex} = 6$ V at $\lambda = 900$ nm is measured at 3.1%. The trend is consistent with prior art based on the p-i-n SPADs [10,24], *indicating that the guard-ring sharing has no significant impact on PDP*.

Figure 4(c) shows the measured maximum PDP as a function of the active-to-active distance L_{a-a}. Slight increase of the maximum PDP is observed with reducing L_{a-a}. This could be caused by a deformed electric field distribution for smaller L_{a-a}, leading to the reduced loss of photocharge detection around the corner of the active area. Figure 4(d) shows the excess bias dependence of the maximum PDP for different active diameters. The maximum PDPs for $D_a = 1.2\,\mu m$ and $2\,\mu m$ are smaller compared to that of $D_a = 3\,\mu m$, likely due to the border effect for reduced active diameters [27].

3.3. DCR

Figure 5 shows the measured room temperature DCR performance. The plotted DCR is a median of 16 pixels in an array. Active-to-active distance dependence of DCR for $D_a = 3\,\mu m$ is plotted in Fig. 5(a). For $V_{ex} = 3$ V, no significant dependency of DCR is observed for smaller L_{a-a}. For $V_{ex} = 6$ V, the DCR is slightly increased at $L_{a-a} = 1\,\mu m$, whereas the absolute values of the DCR are still much smaller compared to the prior art thanks to small active area and low noise process.

Figure 5(b) shows the excess bias dependence of room temperature DCR for different active diameters. Smaller DCR for $D_a = 2\,\mu m$ is observed with respect to $D_a = 3\,\mu m$ due to reduced active area. Limited increase of DCR is observed up to $V_{ex} = 6$ V, which implies that tunneling-induced

DCR component is well-suppressed. The DCR for $D_a = 1.2$ µm is higher than that of larger active diameters, indicating that the aggressive design of the active area results in the higher risk of premature edge breakdown.
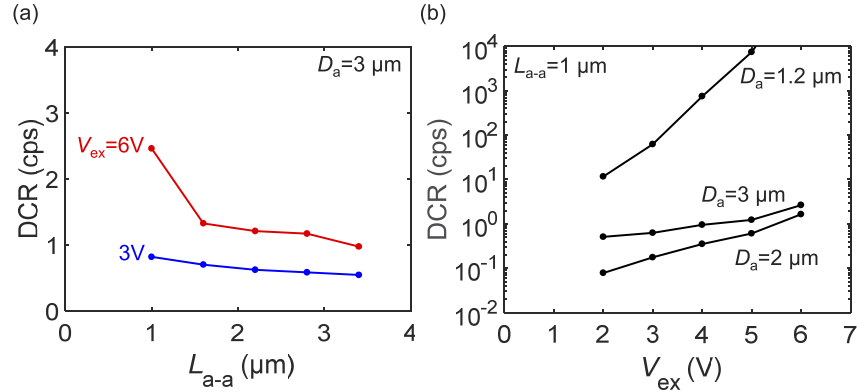

Fig. 5. DCR characteristics for guard-ring-shared SPADs. (a) Measured room temperature median DCR for SPAD with $D_a = 3$ µm as a function of L_{a-a}. (b) Median DCR as a function of excess bias and D_a with $L_{a-a} = 1$ µm.

3.4. Crosstalk

As discussed previously, crosstalk is one of the most critical properties in miniaturized SPADs, which could potentially be influenced by guard-ring sharing. In general, crosstalk in SPADs can be classified in optical and electrical crosstalk [28,29]. Optical crosstalk in SPAD is caused by avalanche-induced light emission, i.e. emitted photons travel towards nearby pixels and generate secondary electron-hole pairs, thus inducing other avalanche multiplication events. Electrical crosstalk is caused by avalanche-generated excess charges. One possible mechanism is an avalanche-induced hot carrier traveling across the pixel isolation to induce the additional avalanche multiplication event in the adjacent pixels. Another cause is a punch-through current between adjacent active regions; when a SPAD detects a photon, the voltage at the anode (or cathode in case of the reversed p-n configuration) swings with an amplitude of nearly V_{ex}. The punch-through current can pull the anode voltage of the adjacent pixel, which could go beyond the threshold of pixel circuit and generate an output pulse. The difference between the two electrical crosstalk mechanisms is whether the secondary output pulse is generated by avalanche effect or direct macroscopic leakage current. In typical SPAD arrays, both of the electrical crosstalk components are suppressed due to sufficiently high potential barrier at the pixel isolation.

Quantitative evaluation of optical and electrical crosstalk was experimentally performed by comparing well-shared and guard-ring-shared SPAD structures. Figure 6(a) shows the cross-sections of well-shared and guard-ring-shared SPADs with identical pixel dimensions; when the active diameter and the active-to-active distance are identical for both structures, the effect of optical crosstalk should be identical because the amount of light emission per single avalanche event stays the same, and propagation of emitted photons is not affected by the doping profile of pixel isolation. Thus, differences in crosstalk for the two structures can be caused solely by electrical crosstalk.

In 4×4 SPAD arrays, crosstalk is measured by inter-avalanche time histogramming [15]. Assuming ideal SPAD array with no correlation of photon detection events between two pixels, an inter-avalanche time histogram shows exponential decay. The crosstalk component can be extracted as a deviation from the exponential behavior. Figure 6(b) shows the histogram of measured inter-avalanche time for two adjacent pixels with $D_a = 3$ µm and $L_{a-a} = 1$ µm, taken
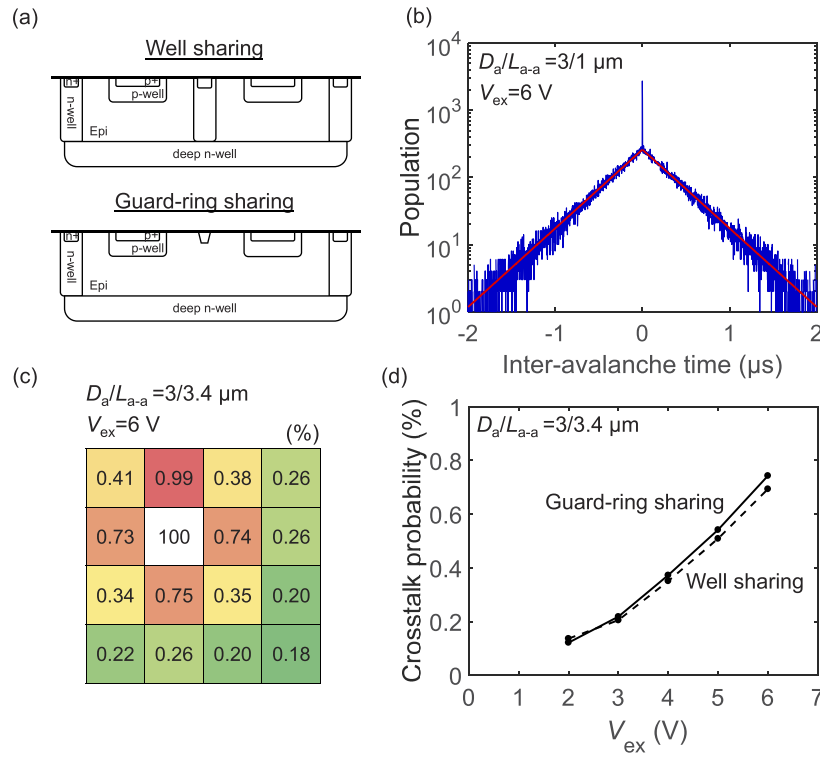
Fig. 6. Comparison of crosstalk between well sharing and guard-ring sharing. (a) Cross-sectional views of well-shared SPADs (top) and guard-ring-shared SPADs (bottom) with identical D_a and L_{a-a}. (b) Inter-avalanche time histogram for two adjacent pixels with $D_a = 3\,\mu m$ and $L_{a-a} = 1\,\mu m$. Red curve is the exponential fit. (c) Crosstalk map in a 4×4 array with $D_a = 3\,\mu m$ and $L_{a-a} = 3.4\,\mu m$. (d) Crosstalk probability as a function of excess bias with $D_a = 3\,\mu m$ and $L_{a-a} = 3.4\,\mu m$.

under low light condition. The time bin width for the histogram is set at 2 ns. A central peak indicates the time-correlated crosstalk events. The tails are fitted with exponential functions (red lines). Figure 6(c) shows the crosstalk map for a 4×4 guard-ring-shared pixel array with $D_a = 3\,\mu m$ and $L_{a-a} = 3.4\,\mu m$ at $V_{ex} = 6\,V$. Each crosstalk probability is independently estimated from the corresponding inter-avalanche time histogram. The crosstalk probability is higher for pixels closer to a reference pixel (shown in white). Figure 6(d) shows the calculated crosstalk probability as a function of the excess bias. The plotted crosstalk is the median of 4 pixels adjacent to a single reference pixel. No critical difference is observed between the well sharing and the guard-ring-sharing devices. *This result strongly suggests that guard-ring sharing leads to no significant degradation of electrical crosstalk with respect to the conventional well-sharing technique.*

Detailed analysis of the crosstalk in the guard-ring-shared SPAD arrays is performed. Figure 7(a) shows the active-to-active distance dependence of the measured crosstalk probability for different excess biases. The crosstalk probability is increased with decreasing L_{a-a} and increasing V_{ex}. The highest crosstalk probability of 3.57% is smaller than typical crosstalk probability of 5% to 10% in CMOS image sensors. The level of crosstalk is acceptable for most of the applications mentioned in this paper, while it could limit key performance in some specific applications, whereever correlated noise has a major impact [1,30]. Figure 7(b) shows the crosstalk probability as a function of the excess bias for different active diameters. Analogous to the trend for DCR,

the lowest crosstalk probability is obtained at $D_a = 2\,\mu m$. Degradation of crosstalk is observed at $D_a = 1.2\,\mu m$. Quadratic increase of the crosstalk probability stems from two factors: linear increase of photon emission for V_{ex}, and linear increase of PDP for V_{ex}. Note that the crosstalk probability can be further suppressed by employing the 3D-stacking process, where reduction of parasitic capacitance for anodes regulates the avalanche-induced light emission.
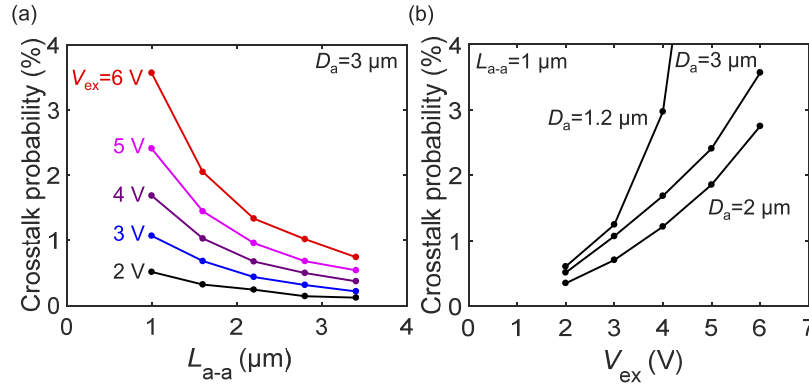

Fig. 7. Measured crosstalk for guard-ring-shared SPADs. (a) Crosstalk probability for SPAD with $D_a = 3\,\mu m$ as a function of L_{a-a}. (b) Crosstalk probability as a function of excess bias and D_a with $L_{a-a} = 1\,\mu m$.

3.5. Afterpulsing and timing jitter

Figure 8(a) shows the measured inter-avalanche histogram for a single pixel with $D_a = 3\,\mu m$ and $L_{a-a} = 1\,\mu m$, taken under low light condition. In contrast to the crosstalk measurement, where inter-avalanche time for two different pixels is extracted, the inter-avalanche time between two adjacent output pulses in the same SPAD is monitored to evaluate afterpulsing probability. The SPAD dead time is fixed at 10 ns. The histogram shows exponential decay in the population. The red line shows the fitting result with the ideal case. Magnified view for shorter inter-avalanche time is shown in the inset. No positive deviation of the histogram from the ideal trend indicates that the afterpulsing is suppressed in the measured device. Calculated afterpulsing probability is 0.21%, close to the measurement limit. Similar afterpulsing probability was observed for different active diameter and active-to-active distance.

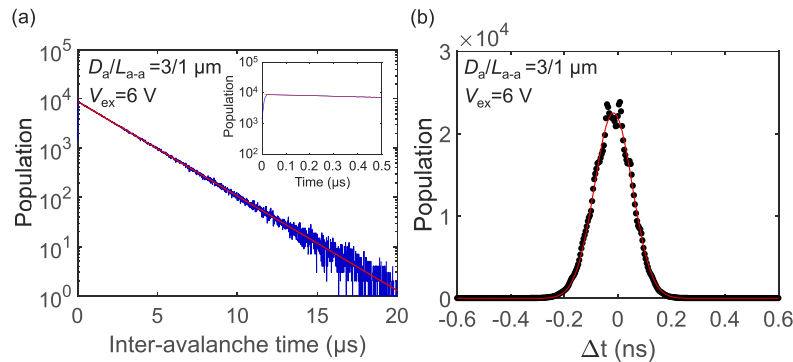**Fig. 8.** Correlated noise analysis for guard-ring-shared SPAD with $D_a = 3\,\mu m$ and $L_{a-a} = 1\,\mu m$. (a) Inter-avalanche histogram for extraction of afterpulsing probability. Red curve is the exponential fit. (b) Timing jitter histogram. Red curve is the Gaussian fit.

Figure 8(b) shows the measured histogram for timing jitter. A 785 nm laser pulsed at 25 MHz (average power: 5 mW, optical pulse width: 80 ps, ALS GmbH, Berlin, Germany) illuminated the SPAD array through ND-filter, so as to observe the timing jitter of output pulses. The obtained histogram was fitted by Gaussian distribution as shown in a red curve. The raw timing jitter was 147 ps (FWHM) at $V_{ex} = 6$ V, which comprises SPAD jitter and circuit-induced jitter. The latter component can be independently measured by monitoring an identical SPAD signal through two different paths towards OUT1 and OUT2. The readout circuits are designed symmetric for the two paths, and the timing jitter between OUT1 and OUT2 gives $\sqrt{2}$ times the circuit jitter. The circuit jitter component is estimated to be 117.7 ps. As a result, SPAD timing jitter for $D_a = 1.2$, 2, and 3 μm is calculated to be 72, 70, and 88 ps, respectively.

The measured afterpulsing probability and timing jitter are similar or better than the state-of-the-art SPAD devices, suggesting that the guard-ring sharing has no impact on those performance measures.

4. Conclusions

We proposed a novel guard-ring-sharing technique enabling high fill factor, miniaturized SPAD pixels, thus paving the way to very large format SPAD imagers. Feasibility of the guard-ring-sharing technique is verified by device simulation, preliminary I-V test and detailed measurement of 4×4 SPAD arrays. A pixel pitch of 2.2 μm was demonstrated, the smallest ever reported for a SPAD. Table 1 shows state-of-the-art comparison of performance and specifications in miniaturized SPAD arrays. In spite of an extremely small pixel pitch of 2.2, 3, and 4 μm, the guard-ring-shared SPAD arrays showed excellent fill factor, PDP, PDE, DCR, afterpulsing, and

Table 1. State-of-the-art comparison of performance and specifications in miniaturized SPAD arrays.

	[21]	[36]	[15]	This work		
Process technology	65/40 nm 3D-BSI CMOS	90 nm CMOS	130 nm CIS	**180 nm CMOS**		
Pixel pitch (μm)	7.83	5	3	**2.2**	**3**	**4**
Active diameter (μm)	-	2	1	**1.2**	**2**	**3**
Drawn fill factor (%)	45	12.5	14[b]	**19.5**[a]	**32.3**[a]	**42.4**[a]
Sensor resolution	128×120	3×3	4×4	**4×4**	**4×4**	**4×4**
Breakdown voltage (V)	12	10.3	15.8	**32.35**	**23.6**	**22.1**
Max. PDP (%)	27.5 (V_{ex}=3 V)	36 (V_{ex}=0.6 V)	15 (V_{ex}=3.2 V)	**10.3 (V_{ex}=4 V)**	**17.3 (V_{ex}=6 V)**	**33.5 (V_{ex}=6 V)**
Max. PDE (%)	12.4 (V_{ex}=3 V)	4.5 (V_{ex}=0.6 V)	2.1 (V_{ex}=3.2 V)	**2.0 (V_{ex}=4 V)**	**5.6 (V_{ex}=6 V)**	**14.2 (V_{ex}=6 V)**
Median DCR (cps)	11,000 (V_{ex}=3 V)	250 (V_{ex}=0.6 V)	150 (V_{ex}=1 V)	**751 (V_{ex}=4 V)**	**1.6 (V_{ex}=6 V)**	**2.5 (V_{ex}=6 V)**
Crosstalk (%)	-	<0.1 (V_{ex}=0.6 V)	0.13-0.22 (V_{ex}=1 V)	**2.97 (V_{ex}=4 V)**	**2.75 (V_{ex}=6 V)**	**3.57 (V_{ex}=6 V)**
Afterpulsing probability (%)	-	-	0.18 (V_{ex}=1 V)	**<0.20 (V_{ex}=4 V)**	**0.20 (V_{ex}=6 V)**	**0.21 (V_{ex}=6 V)**
Timing jitter (ps)	136 (V_{ex}=3 V)	107 (V_{ex}=0.6 V)	107 (V_{ex}=3 V)	**72 (V_{ex}=4 V)**	**70 (V_{ex}=6 V)**	**88 (V_{ex}=6 V)**

[a]Drawn p-well area subtracted by overlapped metal area.
[b]Honeycomb structure

timing jitter performance with respect to prior art. Crosstalk probability is relatively high due to aggressive miniaturization of active-to-active distance and much higher excess bias. Note that the concept of guard-ring sharing is not limited to p-i-n SPADs, but it is also applicable to other SPAD structures, such as a p+/n-well SPAD, a p-well/buried-n-well SPAD, and a SPAD for enhanced near-infrared PDP [31,32,33].

Note that a large array of guard-ring-shared SPADs could suffer from voltage drop through a single shared deep-well. One of the scalable solutions for this issue is a hybrid approach: guard-ring shared in vertical and horizontal directions and not shared in diagonal directions. In such a case, the SPADs are well-shared in diagonal directions, and thus the cathode contacts can be placed in every corner between pixels. Another solution is to make a small SPAD sub-array (e.g. 8×8 pixels) to form a large-scale array, where every small sub-array can be surrounded by well-ring for cathode contact. This solution effectively reduces the average pixel pitch, while changing the periodicity of the pixels.

The guard-ring sharing technique is even more effective when combined with other miniaturization techniques, such as on-chip microlens and 3D-stacking. For 3D-stacked SPAD sensors, the dimension of pixel circuitry is predicted to be under 1 µm by employing advanced logic processes, such as 11 nm-CMOS [34], and thus the limiting factor of SPAD pixel scaling is considered to reside in the SPAD arrays rather than the circuits. Note that in such a small SPAD pixels whenever implemented in an advanced logic process, a cascode transistor or poly-resistor could be necessary for level-shifting photon count signals, so as to ensure high excess bias and low voltage operation of logic circuit. The guard-ring sharing can go beyond the limit of the conventional SPAD technologies, and could play a critical role for achieving compact multi-megapixel SPAD sensors, and ultimately 1 µm-pitch SPAD 'arrays towards a next generation of quanta image sensors [35] in the near future.

Disclosures

EC: Fastree3D SA (I,S) and Pi Imaging Technology SA (I,S), and KM: Canon Inc. (F,E,P).

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