SEMI-AUTOMATED DESIGN OF A MOS CURRENT-MODE LOGIC STANDARD CELL LIBRARY FROM GENERIC COMPONENTS

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ABSTRACT

This paper describes the design and semi-automated generation of a MOS current-mode logic standard cell library. A set of generic components implementing a wide range of combinational and sequential functions is proposed. The layout of the generic components being parameterized for process design rules and transistor dimensions, the library can be mapped to different generations of CMOS processes. An implementation in 0.18um CMOS technology is presented.

1. INTRODUCTION

MOS current-mode logic (MCML) has received a growing attention during the last five years, thanks to its promising potential applications in mixed-signal integrated circuits. MCML offers speed performance competitive with CMOS, while potentially reducing the supply switching and substrate noise by orders of magnitude and keeping power consumption acceptably low, especially at high operating speed.

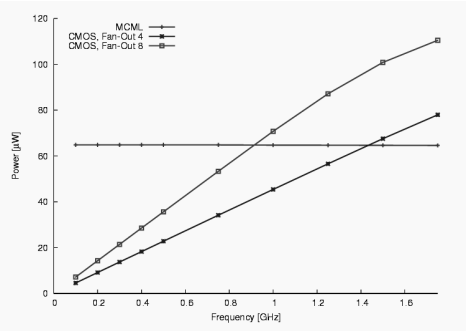


Figure 1 Power dissipation of MCML gates remains independant of switching frequency, which makes them preferable to CMOS at high speed

MCML has been identified in earlier works as a candidate to implement digital building blocks [1]. However, most MCML circuits that have been reported implement very specific hardware, mostly as part of or applied to digital communication front-ends. Examples of such realizations include ring oscillators [2] or high-speed multiplexers [3] [4].

A majority of researchers have focused on the analysis and design of basic MCML components [5],[6],[7], highlighting several challenges in the design and application of MCML for digital logic circuits. Few integrations have been reported so far, and the practical value of MCML in this area largely remains to be proven.

In order to successfully be adopted by designers of digital circuits, a logic style should be applicable to the conventional top-down design-flows that CAD tools utilize. Hence, the building blocks should bear the form of a standard cell library. Many issues need to be addressed to fulfil this requirement, ranging from the compatibility with synthesis software to placement and routing. The specificities of MCML impose new design constraints and challenges, such as differential signal routing, bias voltage distribution, continuous supply current, matching.

This paper addresses the design of a standard cell library of MCML gates. The design approach is generic, allowing freedom in the choice of the design parameters and targets as well as the technology design rules. The result is a set of tools allowing to rapidly design and implement a standard-cell MCML library in a given technology, as well as a quick turn-around allowing a realistic estimation of the resulting performance in a trial-and-error approach to the choice of the design parameters.

The paper is organized as follows : in section 2, the set of generic components that compose the library is described. In section 3, the design parameters and the transistor-level sizing of the components is explained, followed by the layout in section 4. Finally, in section 5, results are presented. Section 6 concludes and highlights future works to be done.

2. GENERIC COMPONENTS FOR A MCML STANDARD CELL LIBRARY

In the MCML current-mode approach, logic functions are realized in a way different than CMOS. Notably, MCML gates implement multiplexers in a natural and efficient way. Also, since inverted and non-inverted outputs are available, and the negation of one input of a gate is achieved by switching the positive and negative ends of

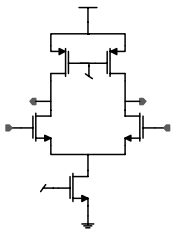
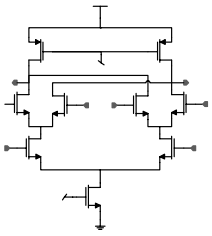
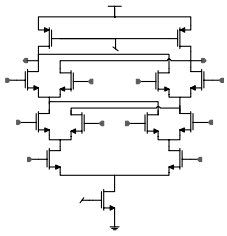
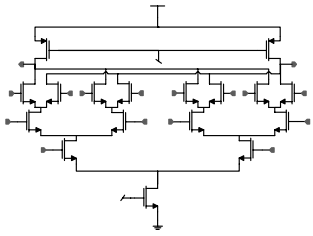
Generic component				
	1-level 1-diff. pair	2-level 3-diff. pairs	3-level 5-diff. pairs	3-level 7-diff. pairs
Main functions implemented	Inverter Buffer	2-input AND / NAND 2-input OR / NOR 2-input XOR / XNOR 2-to-1 MUX D-Latch	3-input AND/NAND 3-input OR / NOR 3-input XOR / XNOR 3-input AND-OR 3-input OR-AND Full Adder (2 gates)	4-to-1 Multiplexer SR Latch D-latch with Set/Reset

Figure 2 Generic components selected for the MCML standard cell library

the differential signal, the function implemented by a gate can be varied in multiple ways. For example, a gate realizing the 2-input AND function will also realize the NAND function, as well as many functions resulting of inverting the inputs and output in all combinations, as shown on Table 1.

$A \cdot B$	$\overline{A \cdot B}$	$A + B$	$\overline{A + B}$
$\overline{A} \cdot B$	$\overline{\overline{A} \cdot B}$	$\overline{A} + B$	$\overline{\overline{A} + B}$
$A \cdot \overline{B}$	$\overline{A \cdot \overline{B}}$	$A + \overline{B}$	$\overline{A + \overline{B}}$
$\overline{A} \cdot \overline{B}$	$\overline{\overline{A} \cdot \overline{B}}$	$\overline{A} + B$	$\overline{\overline{A} + B}$

Table 1 Functions obtained from the MCML 2-input AND gate, with input/output inversions

2.1 Selected Set of Generic Components

The previous observations suggest that a small number of MCML components can realize a broad range of functions. Thus, a set of 4 generic components were selected as a basis to implement the library. The chosen components are depicted in Figure 2, together with the functions that they were chosen to implement. The components were selected according to two criteria :

1. The number of stacked differential pairs should not exceed 3
2. The components should be symmetrical

The first requirement follows from simulating gates with an increasing number of stacked differential pairs, and observing that the delay of a gate with more than three levels exceeds the delay of the equivalent circuit with 3-level gates followed by a multiplexer. The second requirement, excluding asymmetrical components, reduces the set without reducing the available functions, since asymmetrical components are obtained by setting one or more inputs to a fixed value in the symmetrical counterpart. Moreover, this choice has a positive impact on the switching noise [8].

2.2 Sequential Functions and Flip-Flops

Since the generic components are capable of realizing level-sensitive sequential functions (i.e. latches) by feedback from the output to one of the inputs, flip-flops can be implemented with two gates in a master-slave configuration. Simple D flip-flop is implemented with two D-latches, and flip-flops with Set/Reset inputs are implemented with a combination of simple D-latches and/or D-latches with Set/Reset. In order for the Set/Reset to be asynchronous, both master and slave must implement Set/Reset. Implementing Set/Reset only in the master stage of the flip-flop will result in a synchronous behavior.

3. TRANSISTOR-LEVEL SIZING

Once the generic components have been chosen, each one must be sized in order to meet the design targets. The design targets must be chosen so as to maximize speed and minimize area while ensuring a reliable operation.

3.1 Design Parameters

The three parameters governing MCML gates design are the differential voltage swing V_{SWING}, the bias current I_{BIAS} and the noise margins NM [9]. Noise margins are related to the small-signal voltage gain [10], and together with I_{BIAS} impose a minimum size on the gate width of the differential pairs. The differential voltage swing is the product of the bias current and the equivalent on-resistance of the PMOS loads, and hence relates to the gate width of the loads. The gate lengths of the transistors

are usually fixed to the minimum allowed value, in order to save silicon area.

3.2 Design Procedure

Analytical formulas have been derived to express the relationships between the three design parameters [9]. However, in order to achieve the highest accuracy, and since the computing time is acceptable, we decided to size the components using transistor-level simulation.

The design procedure, takes as inputs the netlist of a component and the netlist of a bias generator. The latter generates the voltages applied to the gates of the NMOS current source and the PMOS loads, and sets the unit bias current which is equal for all gates. The NMOS bias voltage will usually be the gate to source voltage of an NMOS connected in a diode configuration, so that the current source in each gate mirrors the reference current. For matching reasons, the current source transistor dimensions will be fixed, and possible bias currents are limited to multiples of the unit reference current.

In a first step, the gate width of the loads is computed. A test bench is generated, and DC simulation is run in a loop until the target voltage swing is achieved. The largest load size obtained across process corners is selected, resulting in a voltage swing always smaller or equal to the target.

Next, the gate widths of the differential pairs are computed in order to satisfy the target noise margins. Another test bench is generated, and DC simulation is run until the resulting noise margin is equal to or greater than the target. The smallest dimensions satisfying the requirements across process and supply voltage corners are selected.

Each level of differential pairs is sized separately, since the deeper the a pair is located, the smaller its drain to source voltage and hence the wider it needs to be to reach the target. The order in which they are sized is relevant : since the voltage swing and the bias current are fixed, the choice of a gate dimension will determine the gate to source voltage, which in turn will impact the drain voltage of the transistors in the next lower level. Therefore, the differential pairs must be sized from the top down.

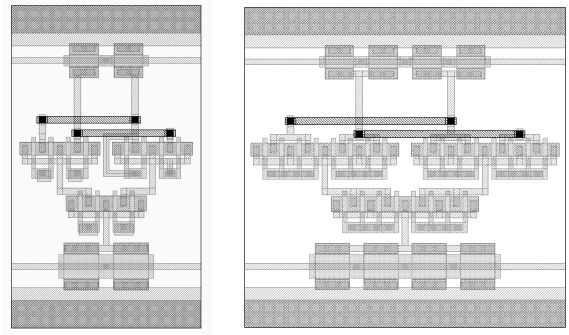
4. LAYOUT GENERATION

Once the transistor dimensions have been determined through the above procedure, their layout can be generated. In order to accommodate different sets of design targets, as well as different technologies, parameterized layouts have been developed for each of the generic components. Two examples of the 2-input AND layout are shown on Figure 3, for two different drive strengths.

A requirement for standard cells is that gates all share the same height. Hence, the transistors are drawn fingered, and higher drive strengths can be achieved by multiplying the number of fingers, yet keeping the same cell height. Bias voltages are distributed with rails parallel to the power supply rails.

For each gate to be generated, the generator is supplied the type of generic component from which it is derived, a set of mapping for input and output ports that turn it into the desired function, and a set of drive strengths to be generated. Constant inputs are implemented by tying one input of the differential pair to the source and the other to the drain.

The layout engine is also capable of simple routing, allowing it to generate gates from two generic components, in order to realize flip-flops in a master-slave configuration.



(a) *(b)*

Figure 3 Mask layout of a 2-input AND gate, with unit drive strength (a) and double drive strength (b).

5. IMPLEMENTATION OF A RC4 ENCODER IN 0.18*μm* CMOS

A library of MCML standard cells has been implemented in a 0.18μm technology using the procedure described in the previous sections. The library has been characterized for timing using commercial CAD tools, in order to be fed to a logic synthesis software.

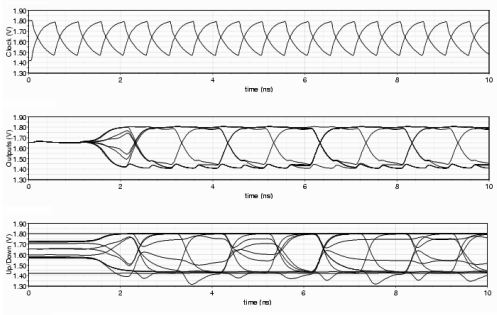


Figure 4 Sample simulated output of a counter with the MCML library at 1GHz clock frequency.

Using this library, an RC4 encoder has been designed following the design-flow described in [11]. The design-flow allows to accommodate logic synthesis, placement,

routing with differential wiring and verification. The resulting layout is shown on Figure 5. The design, totalizing more than 4000 gates, has been sent to fabrication along with a CMOS version of the same design implemented using a commercial CMOS standard cell library. The area occupied by the MCML block is about 1 mm^2, which is about 4 times larger than its CMOS counterpart.

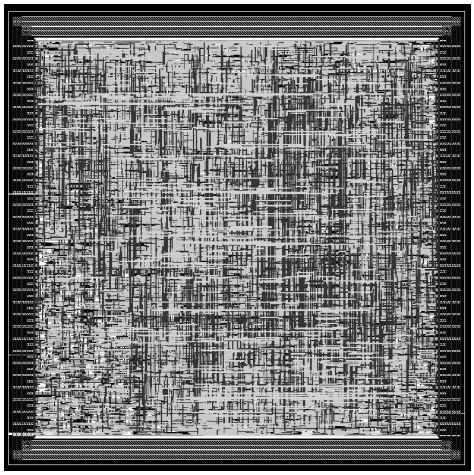


Figure 5 Mask layout of the implemented RC4 encoder

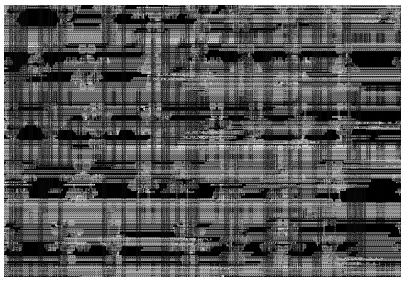


Figure 6 Close-up view of the RC4 layout, showing the standard cells and true differential routing between the cells

6. CONCLUSION

A procedure for semi-automated design of a MCML standard cell library has been proposed. A set of tools has been developed to implement it, and used to realize a standard cell library in a 0.18µm CMOS technology. A 4k-gates RC4 encoder has been implemented using the resulting library and a commercial CMOS library, thus, speed and noise performance comparison will be possible on a realistic environment. The area of the MCML cells, resulting in a layout about 4 times larger than its CMOS counterpart, is a potential area of improvement and will be further investigated. Future works also include investigation of optimal design parameters and extension of the set of generic components in order to improve performances.

7. REFERENCES

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