A Novel Analog-Digital Flash Converter Architecture Based on Capacitive Threshold Gates

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Abstract

In this paper, the circuit architecture and operation of a novel analog-digital flash converter is presented, which is based on cascade-connected capacitive threshold gates. The circuit structure, which is realized using conventional CMOS technology, offers a very small overall layout area, simple operational requirements, and very high input-to-output response speed. Fabricated four- bit flash ADC circuits have been tested to exhibit highly accurate DC transfer characteristics, and typical transient response times in the order of 40 ns. Four-bit and five-bit flash ADC variants can be used as building blocks in high-speed pipelined ADC architectures with higher accuracy.

1 Introduction

The requirements of analog-digital (A/D) conversion in mixed high-throughput signal processing architectures (such as artificial neural networks or ANNs) may impose unique specifications on analog/digital converter (ADC) circuit performance which are quite different from classical ADC performance requirements. The silicon area occupied by the ADC should be minimized, since a large number of such units are typically needed in parallel, to process multiple inputs at the same time. The sampling speed should be as high as possible, in order to accommodate fast-changing input signals such as those encountered in real-time image processing and pattern recognition. The required accuracy (resolution), on the other hand, may be lower than that used in most of the classical ADC applications, since the inherently error-tolerant properties of ANN operation typically compensate for the lower resolution of the processed signal.

Here, we present a very compact flash ADC circuit architecture which is based on the Capacitive Threshold Logic (CTL) concept introduced earlier [1], [2]. The circuit is CMOS compatible, operates on a single two-phase non-overlapping clock scheme, and it requires no externally generated reference voltage levels other than VDD and GND for its operation. Its main features such as the high response speed and very small overall silicon area required for its realization uniquely coincide with the requirements described above for a very significant class of ADC architectures. In addition, these features also make it a perfect building block for higher- accuracy, very high speed pipelined ADC realizations. In the following, the circuit structure and its operation are described in Sections 2 and 3. Silicon realization of sample test circuits and the corresponding test results are presented in Section 4. Finally, Section 5 provides a summary of our results and conclusions.

2 Description of the ADC Circuit Architecture

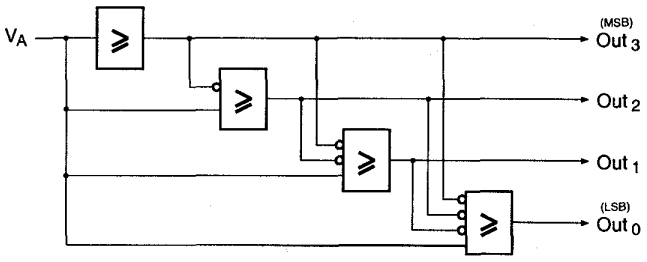

Figure 1: Block diagram of the 4-bit ADC.

The proposed analog-digital converter architecture essentially consists of threshold logic gates, which can accommodate analog and digital input signals simultaneously and produce a digital output signal as the result of a simple thresholding function. The capacitive threshold logic

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gates are actually connected in a cascade configuration; the gate that generates the most significant bit (MSB) output is directly driven by the analog input signal, whereas the gates that generate the lesser significant bits are driven by the analog input as well as by the higher-order digital output signals. The block diagram of a four-bit threshold-logic based ADC is given in Fig. 1. Here, each rectangular block represents a mixed-input thresholding function. At the functional level, the operation of the four threshold logic gates can be described as follows:

$$
\begin{aligned}
V_{out3} = V_{DD} \quad if \quad V_A &> \frac{8}{16}V_{DD} \\
V_{out2} = V_{DD} \quad if \quad V_A &> \frac{12}{16}V_{DD} - \frac{8}{16}\overline{V_{out3}} \\
V_{out1} = V_{DD} \quad if \quad V_A &> \frac{14}{16}V_{DD} - \frac{8}{16}\overline{V_{out3}} - \\
&\quad \frac{4}{16}\overline{V_{out2}} \\
V_{out0} = V_{DD} \quad if \quad V_A &> \frac{15}{16}V_{DD} - \frac{8}{16}\overline{V_{out3}} - \\
&\quad \frac{4}{16}\overline{V_{out2}} - \frac{2}{16}\overline{V_{out1}}
\end{aligned}
\tag{1}
$$

Note that the four output bits (V_{out0} through V_{out3}) are generated by four threshold decisions, each of which is performed by a mixed-input threshold gate. The inherently recursive nature of the decision process described in (1) implies that the LSB-delay is proportional to the number of bits in the output word, and that the higher-order outputs create a ripple effect for the lower-order bits. Yet, the entire conversion operation given in (1) can be completed in a single clock cycle (flash converter operation).

As opposed to earlier, similar charge-based ADC architectures [3], this circuit does not require a subsequent decoder circuitry to convert a thermometer code output of voltage comparators into a conventional binary output word.

3 Realization of the ADC Architecture with CTL gates

For the realization of mixed-input threshold functions described in (1), a slightly modified version of the charge-based Capacitive Threshold Logic (CTL) gate structure is being used. The simplified circuit diagram of the four-bit ADC is shown in Fig. 2.

In the following, we examine the operation of a single mixed-input CTL gate, which comprises the basic building block of the four-stage capacitive ADC structure shown in Fig. 2. Note that each CTL gate consists of a row of weighting capacitors, and a chain of inverters which functions as a voltage comparator (see Fig. 3).

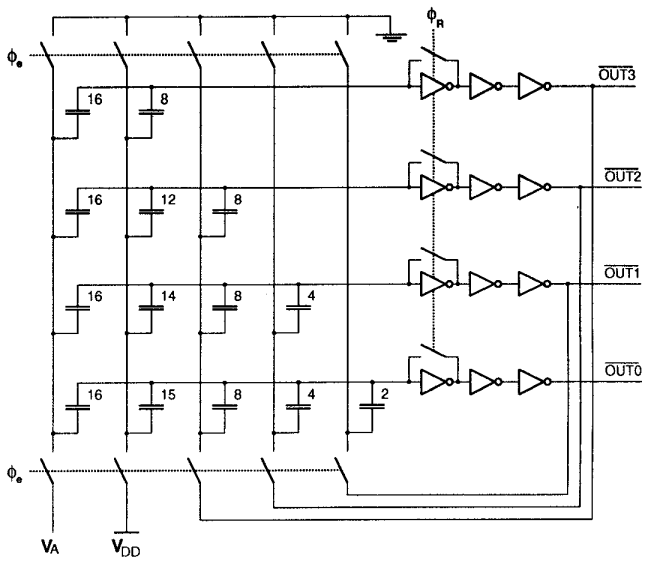

Figure 2: Simplified circuit schematic of the 4-bit ADC circuit

Here, C_A denotes the weight capacitor of the analog input V_A, C_i denote the weight capacitors of the digital inputs, and C_T denotes the threshold capacitor (note that all of these capacitors are realized as integer multiples of a unit capacitor).

The mixed-input CTL gate operates with a two-phase non-overlapping clock scheme consisting of a reset (precharge) phase and an evaluation phase. During the reset phase, the total charge accumulated in the capacitive row is given by:

$$
\begin{aligned}
Q_{row(reset)} = V_{th_1} \cdot C_A + \left(V_{th_1} - V_{DD}\right) \cdot C_T \\
+ V_{th_1} \sum_{i=1}^{m} C_i
\end{aligned}
\tag{2}
$$

where V_{th_1} is the logic threshold voltage of the first inverter within the voltage comparator chain. During the evaluation phase, all inputs (analog and digital) are applied to the bottom plates of the respective capacitors, while the threshold capacitors are connected to ground. The amount of total charge in the capacitive row is now given by

$$
\begin{aligned}
Q_{row(eval)} = (V_{row} - V_A) \cdot C_A + (V_{row} - 0) \cdot C_T \\
+ \sum_{i=1}^{m} (V_{row} - V_i) \cdot C_i
\end{aligned}
\tag{3}
$$

Since the total row charge during the reset phase must be equal to the row charge during the evaluation phase (due

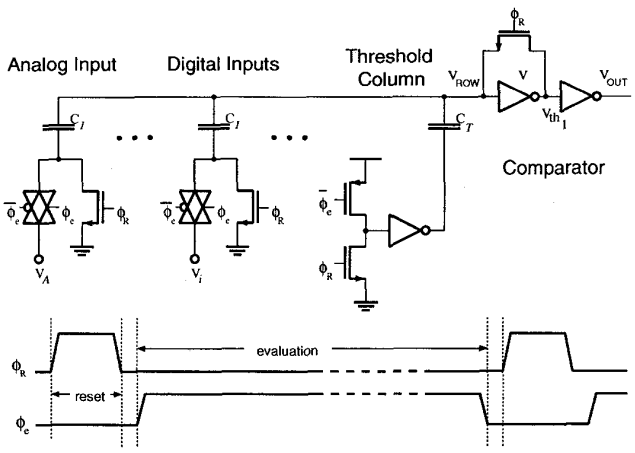

Figure 3: Circuit diagram of a mixed-input CTL gate.

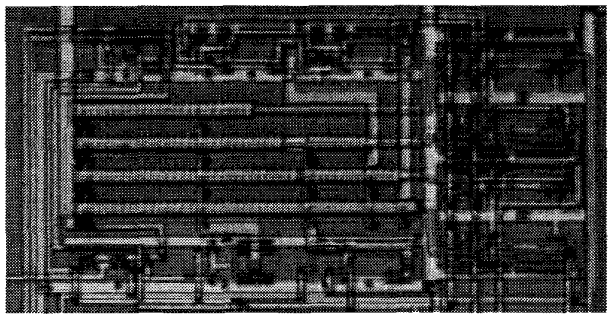

Figure 4: Microphotograph of the 4-bit flash ADC.

to charge conservation), the row voltage must exhibit a certain amount of perturbation during the evaluation phase. This row voltage perturbation can be found as:

$$\triangle V_{row} = \frac{1}{\left(C_A + \sum_{i=1}^{m} C_i + C_T\right)} \cdot \sum_{i=1}^{m} V_i \cdot C_i \qquad (4)$$
$$+ V_A \cdot C_A - V_{DD} \cdot C_T$$

Note that the first inverter of the comparator circuit is biased exactly at inversion threshold (which is also the operating point with the highest gain) at the beginning of the evaluation phase. Depending on the direction of the voltage perturbation ($\triangle V_{row}$), the inverter output will switch either to Logic 0 or Logic 1. Thus,

$$V_A \cdot C_A + \sum_{i=1}^{m} V_i \cdot C_i > V_{DD} \cdot C_T \quad \rightarrow \quad V_{out} = V_{DD} \qquad (5)$$

$$V_A \cdot C_A + \sum_{i=1}^{m} V_i \cdot C_i < V_{DD} \cdot C_T \quad \rightarrow \quad V_{out} = 0 \qquad (6)$$

It can be seen that (5) and (6) correspond to the basic mixed-input threshold equations that are needed to implement the recursive threshold decisions described in (1). This mixed-input (analog/digital) CTL gate constitutes a versatile generalization of the digital-input CTL gate, which was introduced earlier for various compact high-speed logic applications with large fan-in [1], [2], [4]. Note that the circuit requires no analog reference voltage levels for its operation, and the circuit response is independent of the exact value of comparator inversion threshold voltage. Also, the circuit operation depends on ratios of capacitances, rather than absolute capacitances values. Hence, the input - output characteristics are immunne to most process-related variations. All capacitors are realized as integer multiples of a rectangular-shaped unit capacitor, which consists of a Poly1/Poly2 overlap region (unit capacitance value $C_U = 15fF$).

4 Silicon Realization and Test Results

The 4-bit flash ADC structure described in Fig. 2 has been realized using a 0.8 micron double-polysilicon CMOS process. Figure 4 shows the microphotograph of the ADC, which measures 250 μm by 135 μm. With further layout compaction, the area of the ADC can be reduced by an additional 15-20%, resulting in an overall area of less than 0.03 mm^2 for the 4-bit ADC. This compares very favorably with the overall area required by a conventional 4-bit flash ADC realization, which typically consists of 16 individual voltage comparators and the necessary logic for converting the thermometer-code output of the voltage comparators into a 4-bit binary word.

The measured DC input-output characteristic of the ADC is shown in Fig. 5. It can be seen that the circuit exhibits correct monotonic output behavior over the entire range, with no missing output codes. Despite of an inadvertent layout error in the test circuit which led to slightly different capacitance values than actually intended, the integral nonlinearity error of the circuit is found to be less than 1/2 LSB over the full range. The measured transient response times of the four output bits are plotted as a function of the input level in Fig. 6. The typical measured input-to-output transient response time of the ADC does not exceed 60 ns, which qualifies the simple charge-based ADC architecture for high-speed applications. With these operational characteristics, the proposed flash-converter circuit structure also represents a very feasible building block for higher-accuracy, pipelined ADC architectures.

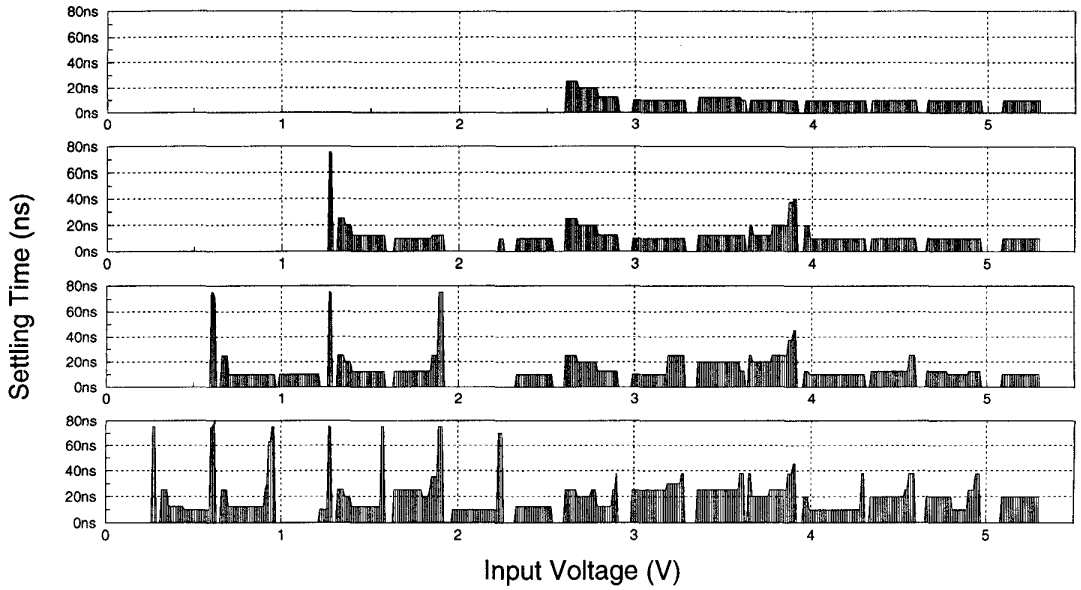

Figure 6: Measured settling times for individual outputs

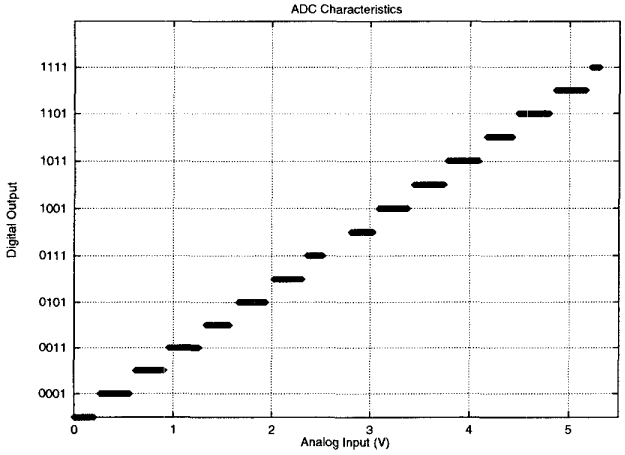

Figure 5: Measured input/output characteristic of the ADC

5 Conclusions

In this paper, the circuit architecture and operation of a novel analog-digital flash converter has been presented, which is based on cascade-connected capacitive threshold gates. The circuit structure, which is realized using conventional CMOS technology, offers a very small overall layout area, simple operational requirements, and very high input-to-output response speed. Fabricated four-bit flash ADC circuits have been tested to exhibit highly accurate DC transfer characteristics, and typical transient response times in the order of 40 ns. Four-bit and five-bit flash ADC variants can be used as building blocks in high-speed pipelined ADC architectures with higher accuracy.

References

[1] H. Ozdemir, A. Kepkep, B. Pamir, Y. Leblebici, U. Cilingiroglu, "A capacitive threshold gate", *IEEE J. Solid-State Circuits*, Vol. 31, pp. 1141–1150, August 1996.

[2] Y. Leblebici, H. Ozdemir, A. Kepkep, and U. Cilingiroglu, "A compact parallel (31,5)-counter circuit based on capacitive threshold logic gates", *IEEE Journal of Solid State Circuits*, Vol. SC-31, pp. 1177–1183, August 1996.

[3] B. Onat, J. McNeill, and U. Cilingiroglu, "Implementation of a charge-based neural Euclidian classifier for a 3-bit flash analog-to-digital converter", *IEEE Transactions on Instrumentation and Measurement*, Vol. 46, No. 3, pp. 672–677, June 1997.

[4] Y. Leblebici, F.K. Gurkaynak, "Modular realization of threshold logic gates for high-performance digital signal processing applications", presented at the 11th *Annual IEEE International ASIC Conference*, September 1998.