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High-Performance III-V MOSFETs and Tunnel-FETs Integrated on Silicon

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I was taught that the way of progress
was neither swift nor easy.
— Marie Curie

Alla mia Famiglia.

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Abstract

Silicon transistor scaling is approaching its end and a transition to novel materials and device concepts is more than ever essential. High-mobility compound semiconductors are considered promising candidates to replace or complement silicon, targeting low-power logic and high-speed electronics. However, to enable large scale and cost-effective integration, it is crucial to address the challenge of integrating III-V devices on silicon substrates and to ensure CMOS processing compatibility. In this work, possibilities and limitations of III-V-on-silicon electronics are explored experimentally. A material platform, suitable for 3D and co-planar integration of InGaAs-based devices with multiple functionalities and featuring CMOS compatible process modules is here presented. Scaled InGaAs FinFETs showing record high on-current of 350 µA/µm (I_{OFF} = 100 nA/µm and V_{DD} = 0.5 V), for III-V FETs on Si are demonstrated. Comparable device performance is also achieved in a 3D sequential integration fashion, where InGaAs transistors are fabricated on top of a Si CMOS device layer. The designed fabrication flow, targeting high-performance devices, can be adapted to the heterogeneous integration of multiple III-V compounds. Hence, following the same approach, the first sub-thermionic heterojunction InGaAs/GaAsSb Tunnel-FETs on silicon are reported. Tunnel-FETs belong to the category of *steep-slope* devices and can overcome MOSFET fundamental limitations taking advantage of quantum transport laws. In this work, some of the key technological challenges to fabricate III-V Tunnel-FETs are addressed and their impact on performance is experimentally demonstrated.

Keywords: III-V, MOSFET, TFET, silicon, integration, TASE, bonding

Sommario

Il continuo ridimensionamento dei transistori a base di silicio sta gradualmente raggiungendo livelli intollerabili e nuovi materiali o dispositivi diventano sempre più necessari. I semiconduttori III-V, essendo caratterizzati da una più elevata mobilità dei portatori di carica, sono considerati oggi dei candidati promettenti per la sostituzione del silicio, in particolare per applicazioni a basso consumo e ad alta frequenza. In ogni caso, per rendere possibile l'introduzione di questi materiali innovativi su larga scala ed a basso costo, è importante elaborare nuove soluzioni per poterli integrare direttamente su substrati di silicio ed utilizzare processi compatibiliti con l'esistente industria dei semiconduttori. In questa tesi, possibilità e limitazioni della tecnologia basata su semiconduttori III-V saranno esplorate sperimentalmente. In particolare sarà presentato lo sviluppo di una piattaforma tri-dimensionale (3D), caratterizzata da dispositivi differenti e con varie funzionalità. Tutti i dispositivi elettronici sono stati fabbricati seguendo procedure compatibili con gli standard industriali. Abbiamo ottenuto il transistore basato su indio-arsenurio di gallio con la più alta corrente in stato di accesione che sia stato dimostrato fin ora. Simili performances sono state ottenute in una versione del dispositivo realizzata su più livelli, in cui il livello sottostante è costituito da standard transistori a base di silicio. Il flusso di processo che è stato progettato ha come obiettivo il miglioramento delle performance dei dispositivi elettronici a base di semiconduttori III-V. Seguendo lo stesso approccio, abbiamo anche dimostrato il primo transistore *tunnel*, integrato su silicio e che raggiunge una pendenza sotto soglia inferiore a 60 mV/dec. Questo risultato è stato raggiunto andando ad individuare le principali criticità dei dispositivi tunnel-FET.

Parole chiave: III-V, MOSFET, TFET, silicio, integrazione, TASE, bonding

Résumé

Alors que la miniaturisation des transistors à base de Silicium touche à sa fin, la transition vers de nouveaux matériaux et concepts devient de plus en plus importante. Grâce à leur haute mobilité, les composants semi-conducteurs à haute mobilité sont considérés comme des candidats potentiels pour remplacer le Silicium dans les applications logiques à basse puissance et pour de l'électronique à haute fréquence. Cependant, afin de permettre une intégration à large échelle, il est crucial d'intégrer des composants III-V sur des substrats de Silicium et d'assurer une compatibilité avec les procédés CMOS actuels. Ce travail de thèse a pour but d'explorer expérimentalement l'intégration de matériaux III-V sur Silicium et de discuter les possibles améliorations et limitations de cette technologie. Une plateforme à base d'InGaAs, compatible avec l'intégration monolithique 3D et coplanaire est présentée. Utilisant des procédés CMOS standards, elle permet d'intégrer des composants électroniques de diverse fonctionnalité. Des FinFETs ultra-miniaturisés à base d'InGaAs ont démontré des courants ON record 350 µA/µm (I_{OFF} = 100 nA/µm et V_{DD} = 0.5 V) pour des transistors à effet de champ sur Silicium. Des performances comparables ont pu être obtenues dans une intégration séquentielle 3D, où des transistors InGaAs ont pu être fabriqués au dessus d'un wafer CMOS contenant des transistors en Silicium. Le procédé de fabrication, développé pour des composants hautes performance, peut être adapté afin d'intégrer d'autre matériaux III-V. En utilisant une approche similaire, un transistor à effet tunnel sub-thermionique à base d'hétérostructure InGaAs/GaAsSb a pu être démontré sur Silicium pour la première fois. Les transistors à effet tunnel (Tunnel-FETs) font partie de la catégorie des composants à forte pente. Grâce à leurs propriétés de transport quantique, ils permettent de surmonter les limitations fondamentales des transistors MOSFETs. Dans ce travail de thèse, les enjeux technologiques liés à la fabrication de transistors III-V à effet tunnel sont discutés et leur impact sur les performance des composants sont démontrés expérimentalement.

Mots-clés: III-V, MOSFET, TFET, silicium, intégration, TASE, bonding

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Acronyms

2D two-dimensional.

3D three-dimensional.

AC alternating current.

AFM atomic force microscopy.

Al_2O_3 aluminum oxide.

ALD atomic layer deposition.

APD anti-phase domains.

ART aspect-ratio trapping.

BJT bipolar junction transistor.

BOX buried oxide layer.

BTBT band-to-band tunneling.

CELO confined-epitaxial lateral overgrowth.

CF4 tetrafluoromethane.

CHF4 trifluoromethane.

CMOS complementary metal-oxide-semiconductor.

CMP chemical mechanical polishing.

CN-FET carbon nanotube field-effect transistor.

CPU central processing unit.

DC direct current.

DE digital etching.

DG dummy gate.

DIBL drain-induced barrier lowering.

DOS density of states.

DWB direct wafer bonding.

EDX electr-diffraction x-ray.

ELO epitaxial lateral overgrowth.

EUV extreme ultra-violet.

FBE floating body effect.

FGA forming gas anneal.

GAA gate-all-around.

GaAs gallium arsenide.

GaAsSb gallium arsenide antimonide.

GaSb gallium antimonide.

Ge germanium.

GF gate first.

H_2O water.

HBT heterojunction bipolar transistor.

HCl hydrochloric acid.

HF hydrofluoric acid.

HfO_2 hafnium oxide.

HK high-κ.

HKMG high-κ metal-gate.

HSQ hydrogen silsesquioxane.

IC integrated circuit.

ICP inductively-coupled plasma.

ILD inter-layer dielectric.

InAlAs indium aluminum arsenide.

InAs indium arsenide.

InGaAs indium gallium arsenide.

InP indium phosphide.

IPA isoproyl alcohol.

IR infrared.

M1 metal 1.

MBE molecular beam epitaxy.

MD misfit dislocations.

MOCVD metal-organic chemical vapor deposition.

MOS metal-oxide-semiconductor.

MOSFET metal-oxide-semiconductor field-effect transistor.

NC-FET negative capacitance field-effect transistor.

NDR negative differential resistance.

NW nanowire.

OI on-insulator.

PBE parasitic bipolar effect.

PECVD plasma-ehnanced chemical vapor deposition.

PMMA Poly(methyl methacrylate).

PVCR peak-to-valley current ratio.

RF radio frequency.

RIE reactive ion etching.

RMG replacement metal gate.

RSD raised source drain.

RTA rapid thermal anneal.

SiO_2 silicon oxide.

SAG selctive area growth.

Sb antimonide.

SCE short-channel effect.

SEM scanning electron microscopy.

Si silicon.

SiGe silicon germanium.

SiN silicon nitride.

Sn Tin.

SOI silicon-on-insulator.

SRB strain-relaxed buffer.

SRH Shockley-Read-Hall.

STDT source-to-drain tunneling.

STEM scanning transmission electron microscopy.

STT surface tunnel transistor.

TASE template-assisted selective epitaxy.

TAT trap-assisted tunneling.

TBAs tertiarybutylarsine.

TCAD technology computer-aided design.

TD threading dislocations.

TFET tunnel field-effect transistor.

TiN titanium nitride.

TMGa trimethylgallium.

TMIn trimethylindium.

TSV TSV through-silicon via.

UTB ultra-thin body.

VLSI very large scale integration.

W tungsten.

WKB Wentzel-Kramers-Brillouin.

XeF_2 xenon difluoride.

XRD x-ray diffraction.

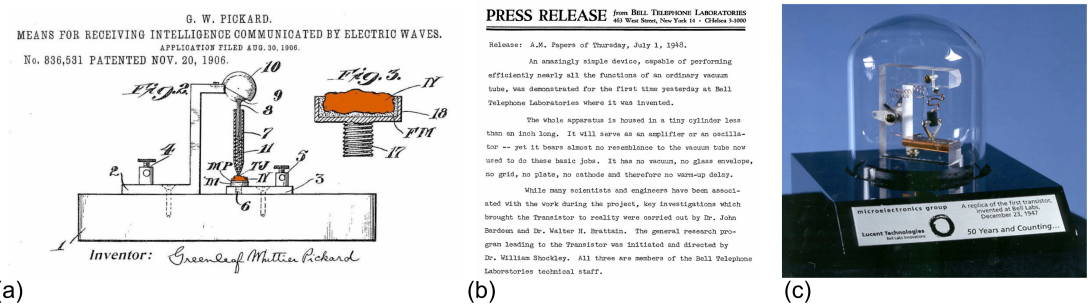
Zn zync.

1 Introduction

1.1 The Atoms of Modern Computing

In November 1906, one of the first patents in semiconductor technology history is granted to Mr. G. W. Pickard [1]. The patent is about "means for receiving intelligence communicated by electronic waves" (Fig. 1.1a) and it is based on a semiconductor device capable to convert an alternating current (AC) into a direct current (DC) hence a rectifying junction diode. The device makes use of mineral silicon as detecting material and found soon applications in radio-receiving sets. The rise of semiconductor electronic devices will, a few years later, radically change our world and lead to the extraordinary technological progress of the modern era. However, from Pickard's patent, still 40 years of research would have been necessary to achieve the next breakthrough. Meanwhile, another electric device gained popularity, known as the *vacuum tube*. Invented in 1920, it emits electrons from an heated cathode and enables signal amplification. Vacuum tubes found applications in "consumer electronics" goods such as radio and television, but also in more advanced radar systems or early digital computers. Although they are nowadays considered obsolete, a modern and more advanced version is still used for high-power RF transmitters, particle accelerators and MRI scanners, due to their superiority in power generation compared to semiconductor devices.

A major breakthrough occurs in December 1947, when Walter Brattain, John Bardeen and William Shockley, three scientists working at the Bell Telephone Laboratories, invent the *point-contact transistor*. "An amazingly simple device, capable of performing nearly all the functions of an ordinary vacuum tube", as announced in the first press release in 1948 (Fig. 1.1)b. The name *transistor*, introduced one year later by J. Pierce, results from the combination of the words *varistor* and *transconductance*, describing a device that can generate gain. The structure consists in a germanium crystal positioned on a copper base and two gold foils placed on its sides. When the semiconductor material and the two metal plates are in contact, a small current applied on one plate amplifies the one flowing on the other side. This very simple but



(a) (b) (c)

Figure 1.1 – (a) Schematic of the first patented semiconductor device in history. Based on mineral silicon the device is known as *cat whisker* detector [2][1]. (b) Sections of the first transistor press-release announcement, made by the Bell Labs director in 1948. (c) Replica of the first transistor invented in 1947. It is made of two gold plates bound to a spring system and a germanium crystal placed on a metal plate.

brilliant invention is worth the Physics Nobel Prize in 1956 and drastically changed the world. The first fully *transistorized* computer is announced by IBM in 1955 as the IBM 608.

Although the cost and performance advantages over vacuum tubes are tremendous, machines made of thousands of discrete transistors still require tedious wiring and are not easy to scale. This is the case until Jack Kilby, a scientist working for Texas Instruments, understands that *transistors can be made all at once, with a parallel and planar process, on the surface of a semiconductor substrate.* It is the invention of the monolithic integrated circuit (IC). In parallel, R. Noyce at Fairchild Semiconductor finds a way to replace manual metal wiring with integrated interconnects toward a fully automated IC process. During this time, junction transistors are being replaced by metal-oxide-field-effect transistors (MOSFETs) – a more scalable device capable of high-performance and low-power consumption – and a few years later by complementary-MOS (CMOS) technology.
In 1971, Intel reaches the market with the first microprocessor, containing 2250 transistors with minimum feature size of 10 µm and based on the so-called PMOS technology. In the early eighties, CMOS will finally overtake both NMOS and PMOS technologies.

Gordon E. Moore, one of the founders of Fairchild Semiconductor and years later of Intel, describes the rising trend of transistor miniaturization and area density increase in his historical article called "Cramming more components onto integrated circuits", published in 1965 in occasion of the 35th anniversary edition of Electronics magazine [3]. He observes that the IC complexity for minimum component cost is doubling every two years, and he projects this observation to the next ten years. This prediction, validated over the next century, will be later known as Moore's law and will become a driving principle for the whole semiconductor industry. Every second year, foundries announce the next *technology node*, labeled by a number that refers to the smallest

Constant-Field Scaling	Parameter	Scaling Factor
Hypothesis	Channel Length	$1/\kappa$
	Doping	κ
	Voltages	$1/\kappa$
Device Parameters	Electric Field	1
	Depletion Charge	1
	Capacitance	$1/\kappa$
	Current	$1/\kappa$
Circuit Parameters	Integration Density	κ^2
	Dissipated Power	$1/\kappa^2$
	Delay	$1/\kappa$
	Dissipated Power Density	1
	Power-delay Product	$1/\kappa^3$

Table 1.1 – Constant-Field scaling summary.

transistor feature. The most recent generations of microprocessors contain nowadays tens of billions of transistors.

1.2 Limitations and Possibilities of Transistor Scaling

Robert H. Dennard, researcher at IBM, formulates in 1972 the MOSFET scaling laws, also known as Dennard scaling [4]. In his paper he provides guidelines to miniaturize the transistor while maintaining or enhancing its performance. Scaling rules soon became necessary since decreasing the length of a MOSFET cause a number of undesired effects known as short-channel effects (SCE), including velocity saturation, channel length modulation, drain induced barrier lowering (DIBL) and breakdown phenomena. Dennard's rules state that voltage and current should be scaled linearly with the transistor dimensions such that the electric field inside the channel remains unchanged. Such scaling approach is known as *constant-field scaling* and it is summarized in Table 1.1. MOSFET dynamic power consumption is proportional to the frequency (related to the transistor switching speed), capacitance and the square root of the applied voltage. Hence, when both capacitance and bias decrease with the device dimensions, there is room for working at higher frequencies. Furthermore, decreasing the occupied wafer area allows to achieve higher integration densities. However, these guidelines were successfully implemented only for a few technology nodes, and soon voltage scaling became unsustainable. Consequently, since the early 2000s, microprocessors clock frequency has saturated around 5 GHz and power densities approximately at 100 W/cm^2, initiating the power-constrained scaling era [5].

As geometric scaling is slowing down, several technology boosters are being explored, impacting the device physical structure itself. Named as equivalent or effective scaling approaches, we can mention the use of strained silicon and silicon-germanium channels for mobility enhancement, the introduction of materials with higher dielectric constant κ or high-κ oxides – enabling further gate oxide scaling compared to SiO_2 – and novel, non-planar geometries such as high-aspect-ratio fins, nanowires and nanosheets. FinFETs for instance, industry-standard technology since 2011 (Intel, 22 nm node), are characterized by an excellent electrostatic control, enabling reduced static leakage at scaled gate lengths and increased drive current density. Furthermore, a key enabler in the ultra-scaling era is played by the development of extreme ultraviolet (EUV) lithography, since 2019 part of the 7 nm production line. All the listed solutions have been literally pushing Moore's law limits, certainly not without performance compromises at device level, and the last technology node we can foresee is the 1.4 nm in ten years from now. After that, a radical paradigm shift in CPUs technology will be needed. Three major routes can be identified in this direction:

- **High-mobility channel materials.** Among the valid alternatives to silicon, III-V semiconductors are the most promising, in terms of technology readiness and performance [6, 7]. As alloys of elements from the third and fifth group of the periodic table, they are characterized by exceptional optical properties hence they are already of wide use in lasers, light-emitting diodes and detectors. The InGaAs system, at different In and Ga concentrations, is also known for a superior electron mobility, and finds applications in high-frequency and high-mobility electronic systems [8]. The already established ecosystem around these materials makes the integration of III-V logic with existing CMOS production lines a plausible reality. However, achieving low-power consumption III-V logic will require outperforming precise Si metrics that will be discussed in the next section.

- **Steep-slope devices.** When operating voltage (V_{DD}) reduction is no longer sustainable for standard CMOS technology, a device featuring steeper turn-on would be desirable. The transport mechanism of a MOSFET relies on Boltzmann statistics that sets a harsh limitation on the required voltage to increase the current by one order of magnitude. A family of devices under the name of *steep-slope devices*, targets to overcome this limitation by exploiting alternative operating principles, such as quantum-mechanical transport. Tunnel field-effect transistors (TFETs) belong to this category [9, 10].

- **3D Integration.** 3D integration is a powerful concept that can be applied from the single transistor level to a fully packaged IC, resulting in shorter metal interconnects and reduced circuit delay. By exploiting the third dimension,

a circuit density increase of about 60 % is predicted compared to the use of 2D co-planar schemes [11, 12]. In particular, 3D sequential techniques enable the independent optimization of each level, in terms of process, design and functionality.

The electron devices presented in this thesis project will exploit synergies of these three technological solutions. From InGaAs MOSFETs co-integrated with Si CMOS in a 3D sequential integration fashion to TFETs based on III-V compounds.

1.3 MOSFET: basics and metrics

A structure schematic of a planar MOSFET is shown in Fig. 1.2a, highlighting as well its main geometrical parameters. Source, drain and gate are the three main terminals while the bulk contact is frequently connected to the source. In an n-MOSFET, the transistor body is p-doped and the source/drain region is n-doped (vice-versa for the p-MOSFET). Complementary-MOS (CMOS) digital circuits make use of both transistor types to implement logic functions. A thin oxide layer (gate-oxide) separates the channel from the gate electrode, and these three elements form the metal-oxide-semiconductor (MOS) structure, the building block of a MOSFET [13]. The doping gradient inside the body leads to the formation of an energy barrier, whose height can be modulated by applying a voltage between the gate and the source terminals (V_{GS}). For simplicity, the following description applies to n-MOSFETs only, as p-MOSFETs behavior can be easily derived by inverting the voltage polarities. A sufficiently high V_{GS} inverts the carrier population in the channel and creates a conductive tunneling path for electrons, bridging source and drain contacts (inversion layer). Hence, in presence of a positive source-to-drain drive bias (V_{DS}), a current flows across the structure and the transistor is turned-on. If no V_{GS} is applied, the channel-drain p-n junction is reversely polarized and only a small current (leakage) can flow. The threshold voltage V_{th} is the V_{GS} point at which the transistor turns-on.

The relationship between on and off-state and their associated figures of merit are of crucial importance to assess the performance of a logic switch [14]. The drive current I_D, the current flowing from source to drain, is schematically plotted in Fig. 1.2b against V_{GS}, in logarithmic and in linear scale. The sub-threshold transistor behavior can be better observed in the first, as in a good switch the current is supposed to increase by several orders of magnitude in the minimum voltage range. The efficiency of this mechanism is described by the inverse subthreshold slope (or sub-threshold swing) SS, defined as:

$$SS \equiv \left(\frac{\partial log(I_D)}{\partial V_{GS}} \right)^{-1} \tag{1.1}$$

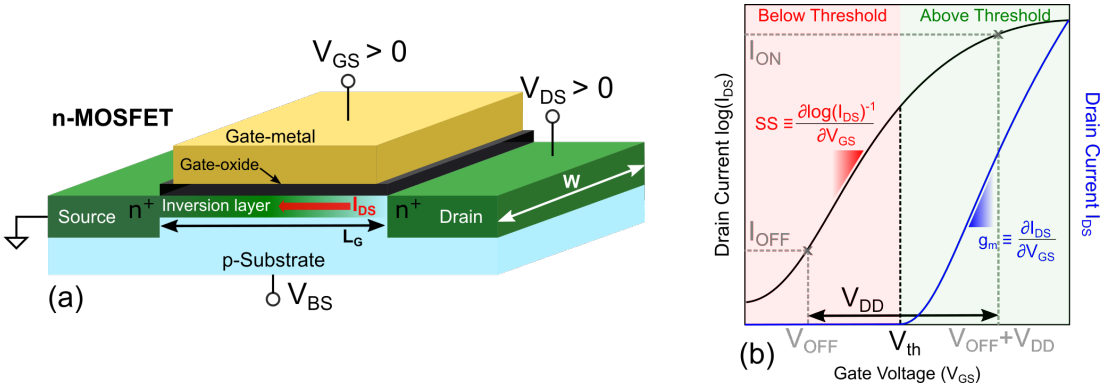


Figure 1.2 – (a) Metal-oxide-semiconductor field-effect-transistor (MOSFET) illustration. (b) Schematic representation of a MOSFET subthreshold characteristic showing how the application of V_{DD} brings the transistor from off-state to on-state. The schematic extrapolation of the on-current (I_{ON}) is also shown. The efficiency of the switching mechanism is ruled by the inverse subthreshold slope and the transconductance.

While SS quantifies the transistor turn-on (or turn-off) efficiency below threshold, the transconductance g_m, represents a measurement of the drive current delivered per V_{GS}, above threshold (Fig. 1.2b). Its formal definition is:

$$g_m \equiv \frac{\partial I_D}{\partial V_{GS}} \tag{1.2}$$

From a technological standpoint, transitioning from planar to scaled gate length (L_g) structures featuring 3D channel geometries such as fins, nanowires and nanosheets, represents a path to achieve minimum SS and maximum g_m, due to the improved electrostatic control [15]. Other than the switching efficiency itself, the absolute values of I_{ON} and I_{OFF} are also of importance. The "I_{OFF} target" is generally fixed to values that depend on the device power range and provides a reference point to the definition of I_{ON}. As graphically drawn in Fig. 1.2b, I_{ON} can be extrapolated as the current at V_{OFF} plus V_{DD}.

By looking at the transfer characteristic in Fig. 1.3 we can easily understand why voltage scaling in planar MOSFETs became unsustainable in the early 2000s [10]. I_{ON} is proportional to the square of the gate voltage overdrive ($V_{DD} - V_{th}$), hence it is important to maximize this quantity by scaling both V_{DD} and V_{th} at the same rate, to guarantee high current and fast switching. On the other hand, V_{th} scaling causes an exponential increase in I_{OFF}, responsible for static leakage power, i.e. the power consumed while the transistor is in the off-state. In a MOSFET, SS is fundamentally limited to 59.5 mV/decade at room temperature (300 K), therefore scaling the voltage – and keeping the overdrive constant – unavoidably increases I_{OFF}.

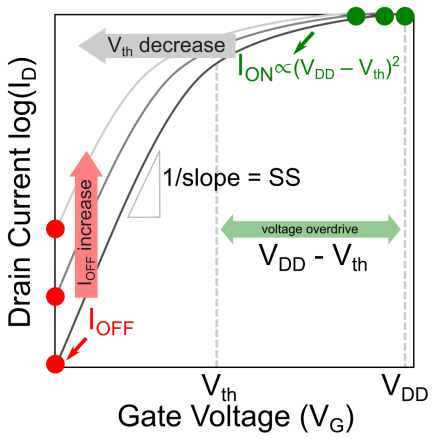


Figure 1.3 – MOSFET subthreshold characteristic showing that threshold voltage scaling induces off-current increase due to the fixed slope SS. Contrarily, reducing the voltage overdrive decreases the I_{ON}. Adapted from [10].

1.3.1 High-mobility channel materials

Mobility and velocity saturation are the main features of classical diffusive transport. However, as transistors are scaled down and the channel length becomes comparable to the scattering length, ballistic or near-ballistic transport takes place and a new description is required. In the so-called top-of-the-barrier model, developed by Natori and Lundstrom [16, 17], source and drain are represented by two electron reservoirs separated by an energy barrier. A crucial role in the ballistic picture is played by the *virtual source*, the location featuring the highest energy barrier point, schematized in Fig. 1.4a. In an ideal ballistic conductor electrons injected at the right and left contact reach the opposite side without undergoing any scattering, as the scattering length is larger than the channel length. In this case, the quantity that dominates is the injection velocity (v_{inj}) at the virtual source [16]. Hence the I_{ON} in a near-ballistic MOSFET is given by the product of the inversion charge carrier density N_{inv} and the velocity v_{inj}. III-V semiconductors are characterized by a low effective mass m^*, that is inversely proportional to v_{inj}. InGaAs v_{inj} for instance, is about twice as high as silicon at half the operating voltage [6]. However, for scaled devices operating in the ballistic limit, the relationship between the I_{ON} and the channel material parameters is no longer trivial. The inversion charge density N_{inv} is a monotonically increasing function of the effective mass. A material with large m^* will be limited by a low injection velocity while a lower m^* effectively limits the density of states at the virtual source [18]. This phenomenon is known as the III-V DOS bottleneck [19]. In Fig. 1.4b the effective coupling capacitances at the virtual source are schematized. An optimum I_{ON} trade-off point can be achieved when the condition $C_{INV} \approx C_Q = 2C_{OX}$ is met.

Consistent research efforts are being dedicated to demonstrating the use of III-V

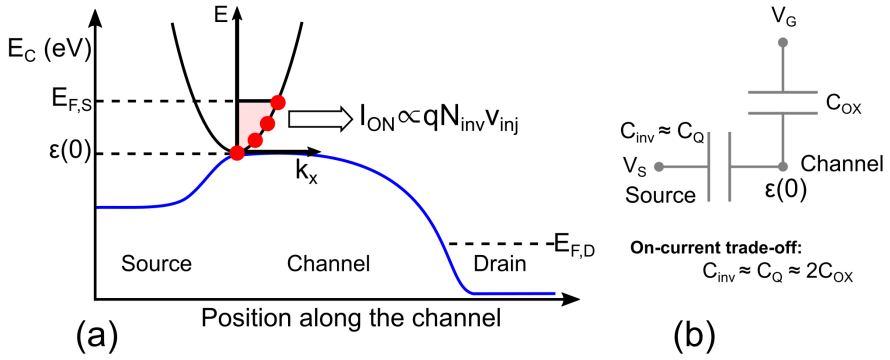


Figure 1.4 – (a) Conduction band profile of a MOSFET in the ballistic regime. At $T = 0\,\mathrm{K}$, only carriers with positive wavevector K_x and energy below the source Fermi level can contribute to the total current. The highest barrier point is known as virtual source. (b) Effective coupling capacitances at the virtual source of a ballistic MOSFET.

for logic applications. The In(Ga)As system is the most popular choice for n-MOSFETs whereas Sb-based materials are more suitable for p-type devices. InGaAs/InAs planar FETs have been reported by Lin *et al.* [20] featuring high g_m of 3.45 mS/µm. Lee *et al.* [21] instead, explored the use of Al_2O_3/ZrO_2 gate dielectric combined with InAs channel resulting in high I_{ON} at 25 nm L_g. Huang *et al.* [22] has demonstrated very low I_{OFF} with the implementation of vertical InP spacers. Moving to non-planar channel geometries, a tri-gate InGaAs n-MOSFET with a record I_{ON} of 650 µA/µm ($V_{DD} = 0.5\,\mathrm{V}$ and $I_{OFF} = 100$ nA/µm) has been reported by Zota *et al.* [23]. Excellent electrostatic control has been achieved in the gate-all-around (GAA) InGaAs FETs demonstrated from Gu *et al.* [24].

All the listed examples demonstrate the potential of this material to outperform silicon logic. However, beyond device performance, other important aspects are the integration on silicon and the manufacturing costs. Several integration methods have been explored in this direction, and they will be widely discussed in the next chapter. Although the fabrication complexity unavoidably increases when going from a native III-V substrate (such as InP) to Si, encouraging results have been already reported. Waldron *et al.* [25], for instance, has demonstrated high-g_m gate-all-around (GAA) devices on Si using a replacement-fin technique. Huang *et al.* [26], instead, has reported the use of buffered layer growth to obtain high-mobility channel InGaAs MOSFETs. Selective epitaxial techniques enabled the demonstrations of scaled transistors as in the work of Schmid *et al.* [27] or Czornomaz *et al.* [28]. Finally, wafer bonding has also been explored for the fabrication of InGaAs MOSFETs, as reported by Djara *et al.* [29] and Hahn *et al.* [30].

1.4 Steep-slope devices

Highly scaled CMOS technologies suffer from a tremendous power density bottleneck, due to the inability of reducing the operating voltage without increasing the off-current (I_{OFF}) or degrading the on-state. As mentioned above, the turn-on steepness in a MOSFET, measured by the inverse subthreshold slope (SS), is fixed to 59.5 mV/decade at 300 K, commonly referred to as 60 mV/decade barrier. The switching efficiency of a MOSFET is strictly dependent on Fermi-Dirac statistics, setting the amount of carriers qualified (in energy) to contribute to the total current. The minimum value depends only on the temperature and cannot be changed by the use of different materials or device geometry. To overcome this limitation, a disruptive change in the current mechanism or the device structure is required. Guidelines for designing a steep-slope solid-state switch can be derived starting from the SS formal definition [10]:

$$SS = \frac{\partial V_{GS}}{\partial log(I_D)} = \frac{\partial V_{GS}}{\partial \Psi_S} \frac{\partial \Psi_S}{\partial log(I_D)}, \tag{1.3}$$

where Ψ_S is the surface potential in the channel, induced at the interface with the gate-oxide. The first partial derivative, $\frac{\partial V_{GS}}{\partial \Psi_S}$, is the transistor body factor m and expresses the coupling between the voltage applied on the gate and the channel surface potential. The second term, instead, refers to the current conduction mechanism itself, hence to the variation in drain current induced by the channel potential. The two terms can be simplified as follows [31]:

$$SS \approx \underbrace{\left(1 + \frac{C_S + C_{it}}{C_{ox}}\right)}_{\text{m}} \underbrace{\frac{k_B T}{q} ln(10)}_{\text{n}}. \tag{1.4}$$

C_S is the semiconductor depletion capacitance whereas C_{ox} and C_{it} are the gate-oxide and the interface states capacitances, respectively. The expression for the body factor m is derived from a simple capacitor divider model (see Appendix A). In the second term instead, we identify the Boltzmann constant k_B, the temperature T and the elementary charge q. The complete n factor derivation is reported in Appendix A.

Steep-slope devices are a category of solid state switches that aim to reduce SS to a value smaller than the thermal limit of 60 mV/decade by decreasing the factors m and n in equation 1.4. A sub-unity body factor device can be achieved, for instance, by replacing the conventional gate insulator material with a ferroelectric one, as done in negative-capacitance FETs (NC-FET) [32, 33]. Novel current mechanisms, other than thermionic emission, are instead required to decrease the n factor, exploiting for instance quantum-mechanical tunneling. Tunnel-FETs (TFETs) are among the most promising options to deliver the necessary performance, in terms of on-state and energy efficiency and their basic operation will be described in the next section. The

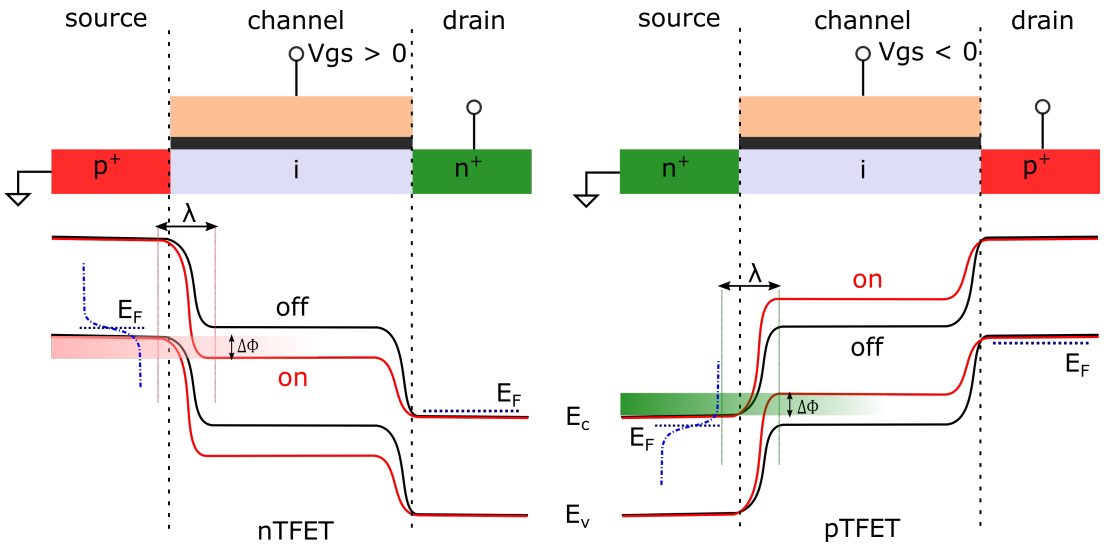


Figure 1.5 – Illustration of a tunnel field-effect-transistor (TFET) energy band diagram. Both n-TFET (left) and p-TFET (right) are represented. A voltage applied on the gate terminal opens the tunneling window $\Delta\Phi$ and turns on the transistor. For the nTFET, tunneling is enabled when the Fermi level in the source is aligned with the channel conduction band edge. Adapted from [31].

two concepts of TFET and NC-FET can also be combined in the same device, where the factors m and n are simultaneously optimized, as shown by Saedi *et al.* in [34].

1.4.1 Physics of tunnel-FET

A basic TFET structure resembles the one of a MOSFET, with two doped contact regions and a gated, intrinsic channel. But unlike in a MOSFET, source and drain are oppositely doped, as schematized in Fig. 1.5 [31]. Depending on the sign of the voltages applied and the doping, p- or nTFETs can be obtained. This description, as well as the experimental results presented in the next chapters, will focus mostly on the nTFET. In Fig. 1.5 the corresponding energy band diagram is drawn. In normal TFET operation the p-i-n junction is reversely polarized hence a positive V_{DS} is applied. In absence of gate bias, the Fermi level in the source and the channel conduction band-edge are misaligned and ideally no current flows. However, structural non idealities can contribute to the presence of a small leakage current, through diffusion of minority carriers or defect-mediated processes such as Shockley-Read-Hall (SRH) generation and trap-assisted-tunneling (TAT) [35]. Similarly to a MOSFET, a gate voltage, V_{GS} turns-on the transistor but carriers enter the channel with a totally different mechanism. For increasing positive V_{GS}, the Fermi level in the source starts aligning with the channel conduction band-edge. Only electrons within the energy window $\Delta\Phi$ can tunnel into the available states in the channel, by a mechanism called

band-to-band-tunneling (BTBT). A very important role is played by the source doping level: an highly degenerate source can prevent the filtering of a large part of the Fermi tail, degrading the SS but at the same time can increase the electric field at the source-channel junction, yielding an higher I_{ON} [35]. The SS versus I_{ON} trade-off optimization represents one of the crucial aspects in the design of a TFET switch. The BTBT I_{ON} is directly proportional to the tunneling probability T_{WKB}, that can be expressed within a semi-classical Wentzel-Kramers-Brillouin (WKB) approximation as [36]

$$T_{WKB} \approx exp\left(-\frac{4\lambda\sqrt{2m^*}\sqrt{E_g^{\frac{3}{2}}}}{3q\hbar(E_g+\Delta\Phi)}\right), \tag{1.5}$$

where m^* is the carrier effective mass, E_g is the energy band gap, λ is the tunneling length. These three parameters can be engineered by proper channel geometry and material selection such that T_{WKB} is brought as close as possible to unity. A large E_g material would exhibit a lower tunneling rate – hence smaller I_{ON} – but superior off-state performance. This trade-off must be carefully considered in the TFET design. Among the possible material choices, silicon is certainly the most interesting from a industry-standard compatibility standpoint. However, the indirect and relatively large E_g (1.12 eV) makes it unsuitable for BTBT. A smaller E_g can be obtained with other group IV materials such as Ge and SiGe or in III-V semiconductors, such as InGaAs, InP, InGaSb and many other compounds. In particular, heterostructures combining different materials offer great possibilities in terms of on-off optimization: a smaller E_g at the source junction and a larger one at the channel-drain is desirable to maximize the I_{ON} while limiting the direct source-to-drain and ambipolar tunneling mechanisms [31]. In Fig. 1.6, different types of band alignment are schematized. In a heterostructure TFET, the transmission probability T_{WKB} is hence proportional to an effective $E_{g,eff}$, that can be carefully tuned by proper material choice. Staggered and broken-gap configurations are the most favorable to achieving an optimum band alignment. A particularly interesting III-V heterostructure for this purpose is the $In_{53}Ga_{47}As/GaAs_{50}Sb_{50}$ system, being also lattice-matched to InP, a common III-V native substrate [37]. Technological aspects and experimental results relating to such structure will be presented in the following chapters. Moreover, a crucial aspect to enable steep SS is to achieve good electrostatic control. This is the case for scaled, 3D channel geometries such as GAA, tri-gate fins and nanowires along with gate oxides featuring low equivalent oxide thickness (EOT). The simple semi-classical description in Eq. (A.10) does not capture many parasitic mechanisms that can occur in TFETs. Although III-V semiconductors appear to be the optimum choice, several techno-

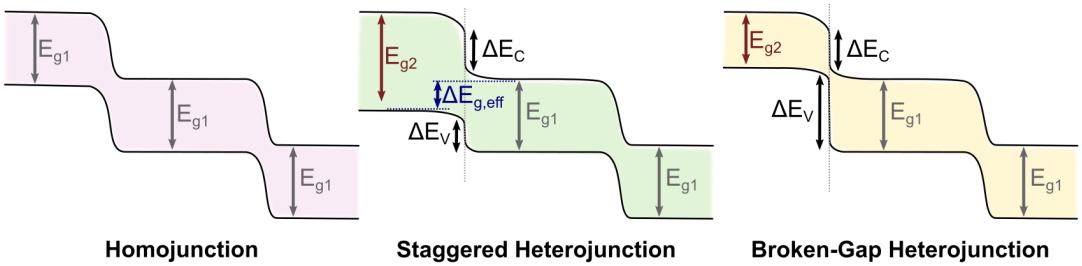


Figure 1.6 – Schematic illustration of three possible TFET band alignments. From the left, homojunction, staggered heterojunction and broken-gap heterojunction alignment. The latter is ideal in terms of on-off trade-off.

logical challenges need to be addressed. Besides the integration and compatibility with silicon – where solutions are readily available – a very important role is played by defects located at the tunneling junction and at the oxide/channel interface (D_{it}). In Fig. 1.7, a schematic band-edge diagram describes some of the most common traps-mediated leakage mechanisms in a TFET. Both direct and phonon-assisted tunneling can contribute to steady-state trap occupation, negatively impacting the device electrostatics, hence degrading *SS*. These mechanisms have been studied particularly on the Si/InAs p-TFET system, where the high lattice mismatch is responsible for a defective tunnel junction [38, 39]. The role of interface traps in the *SS* is evident as well from eq. 1.4, where C_{it} is taken into account. III-V semiconductors, compared to silicon, are characterized by poor-quality native oxide. However, the discovery of aluminum oxide (Al_2O_3) as excellent gate stack for the InGaAs system (and for Si as well) opened new possibilities in this direction and devices with D_{it} approaching Si/SiO_2 values have been reported [40, 41]. Furthermore, the relatively small density of states (DOS) that characterizes III-V materials translates into less carriers available for tunneling to occur. Consistent research efforts have been dedicated in the last years to identify the right recipe, in terms of materials and geometries, to enable an optimum SS/I_{ON} and I_{OFF}/I_{ON} balance. A short overview from the pioneering activities to the most recent demonstrations will be provided in the following section.

1.4.2 TFET state-of-the-art

In 1934, C. M. Zener reported for the first time the occurrence of a tunneling mechanism in a reversely biased p-n junction, based on an impact ionization mechanism [42]. The characteristic negative differential resistance (NDR), fingerprint of the tunneling diode, is instead first measured by Leo Esaki in 1958 [43]. In 1987, Banerjee *et al.* [44] are able to demonstrate tunneling in a three terminal MOS structure. A few years later, the surface tunnel transistor (STT) is proposed by Baba *et al.*, featuring a III-V gated p-i-n diode [45]. After that, several similar device concepts and proto-

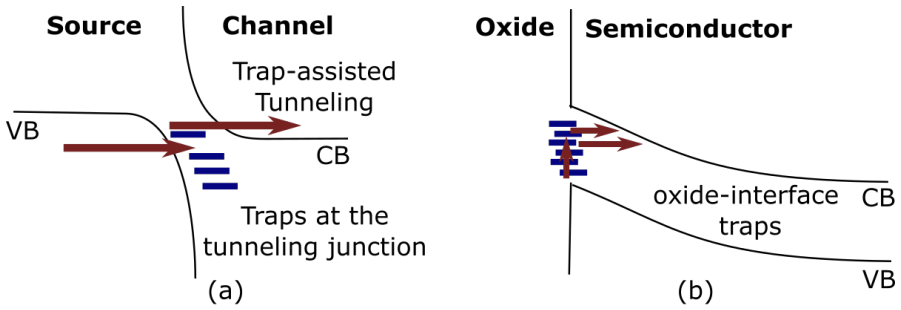


Figure 1.7 – TFET schematic band diagram illustrating the traps-mediated parasitic mechanism at the (a) source-channel tunnel junction and (b) oxide-channel interface. Both direct and phonon-assisted tunneling can contribute to the occupation of traps. Adapted from [31].

types have been proposed, but the key feature of the steeper inverse subthreshold slope remained unexplored until 2004. The discussion was independently initiated by Appenzeller [46], Wang [47] and Bhuwalka [48] and the first sub-thermionic TFET (SS<60 mV/decade) was demonstrated by IBM researchers in a carbon nanotube FET (CNFET). From that moment, a plethora of TFET structures exploiting different materials and geometries have been reported, as displayed in Fig. 1.8 [31]. The observation of how I_{ON} and SS have evolved in the last years is particularly useful to trace the technological development in this field. Although silicon devices have shown initially promising SS, the best and most recent improvements relate to III-V-based TFETs. Among the existing architectures, it is possible to identify three categories: mesa-like, lateral and vertical TFETs. Mesa structures take advantage of growth techniques such as molecular beam epitaxy (MBE) to obtain crystalline materials with low defect densities. One of the best TFET demonstrations to date is an air-bridge structure proposed by Intel [49] and later explored [50]. Following a similar approach, the first complementary III-V TFET platform was demonstrated [51]. However, integration on silicon and scalability represent major limitations for such device geometries. Noguchi *et al.* [52] have reported instead the first planar TFET structure using InGaAs, where doping regions are obtained with Zn-diffusion, enabling an accurate junction formation process. Their device was approaching the thermionic limit with an I_{ON} of 10 µA/µm at V_{DD} = 1 V. The use of a quantum well in the channel was also explored in a later implementation [53]. A complementary planar TFET platform has also been demonstrated by colleagues at IBM, following an integration scheme called template-assisted selective epitaxy (TASE). III-V lateral nanowires (NW) are directly grown on silicon (InAs/GaSb for n-TFET and Si/InAs for p-TFET) with compatible processes [54]. The reported p-TFET shows stronger performance, with average SS of about 70 mV/decade. Further optimization on several aspects is required to improve the n-TFETs, and this will partially be the scope of this thesis. Excellent results

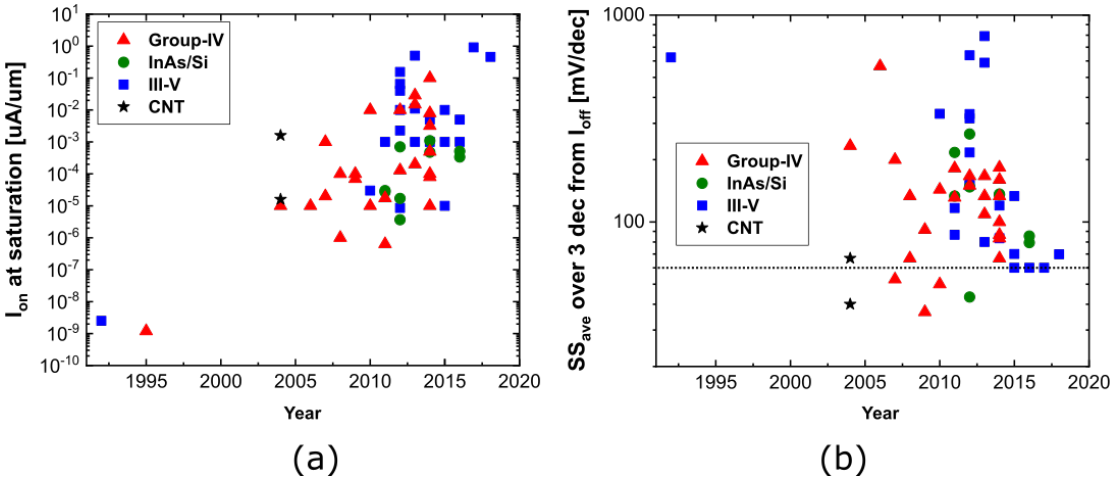


Figure 1.8 – Chronological development of TFETs from the first demonstrations until today. The two most important metrics, SS and I_{ON} are extracted from various publications and not from raw data hence minor deviations might be present. The color code corresponds to different material systems. III-V TFETs have shown the best results in the latest years. Adapted from [31].

have also been demonstrated using vertical architectures. As mentioned before, GAA scaled structures are of great advantage to improve device electrostatics and achieve less-defective interfaces. One example is the work of Memisevic *et al.* [55], reporting sub-thermionic n-TFET operation in vertical III-V NWs fabricated with vapor-liquid-solid (VLS) metal-catalyzed technique. Etched-out InGaAs vertical TFETs have been demonstrated by Zhao *et al.* [56], achieving 53 mV/decade. The lowest SS record value of 47 mV/decade for III-V TFET has been reported by Alian *et al.* [57] using pocketed vertical InGaAs/GaAsSb NW TFETs. TASE has also been explored for the fabrication of vertical InAs/Si p-TFETs, as reported by Cutaia *et al.* [58].

The recent results, achieved through multiple architectures and materials are very promising for the future of steep-slope devices. Low defect densities and excellent electrostatics are clearly key requirements and a perfectly balanced performance trade-off is yet to be demonstrated. Moreover, the emerging use of III-V materials introduces further technological challenges that remain unsolved to date and require focused research efforts.

1.5 Thesis Structure

The present thesis is divided into three main parts:

- **Chapter 2** focuses on the InGaAs-on-silicon platform developed during my project. An overview on the explored methods to integrate this material in silicon substrates is followed by a detailed description of the implemented FET process flow, compatible with CMOS standards. The same fabrication scheme is first applied to InGaAs MOSFETs, then exploited in a 3D sequential integration approach and finally, adapted to the fabrication of Tunnel-FETs.

- **Chapter 3** provides a description of the major performance limitations in InGaAs MOSFETs such as the excessive off-state current. Target process modules are implemented to address such limitations and their impact on device performance is discussed through electrical data. Results relating to high-performance InGaAs MOSFETs, integrated on silicon with two different approaches, are discussed. Finally, electrical characterization of a 3D sequentially integrated Si/III-V platform is provided.

- **Chapter 4** reports electrical characterization of sub-thermionic InGaAs/GaAsSb Tunnel-FETs, fabricated on silicon substrates with the process described in chapter 2. A benchmarking against competing technologies is provided as well.

- **Chapter 5** The final chapter includes a summary of the whole thesis project, including final considerations and future directions.

- **Appendix A** contains the analytical derivation of the MOSFET inverse subthreshold slope m and n factors. An expression for the TFET SS, highlighting the complex dependence on several device and material parameters, is also discussed.

- **Appendix B** highlights the main feature of an activity based on InGaAs 1-transistor DRAM memory cells, carried on in collaboration with University of Granada. Device working principle and the most important experimental results are presented.

1.6 Personal Contribution

All the experimental work presented in this thesis has been conducted at IBM Research – Zurich, under the guidance of the thesis director Prof. Adrian M. Ionescu and the IBM thesis co-director Dr. Kirsten Moselund. At IBM I received supervision also from Dr. Lukas Czornomaz and Heinz Schmid. In this section I describe my contribution to the presented, distinguishing the steps that I did independently from the ones where I received external support.

- **Process design:**
  - **InGaAs MOSFETs**: Many steps of the InGaAs MOSFET replacement-metal gate (RMG) process have been previously established by L. Czornomaz, V. Deshpande and D. Caimi. I introduced the use of source-drain spacers combined with doped extension regions. This process module has enabled record I_{ON} performance and improved off-state.
  - **InGaAs/GaAsSb TFETs**: I designed the entire fabrication flow as there was no previous example of VLSI-compatible III-V TFET based on RMG process. I developed the self-aligned tunnel junction positioning module that was key to achieving sub-thermionic performance.
- **Mask design:**

  I personally designed all the masks used in this work. I implemented a Python script to generate dense layouts featuring a complex sweep of several design parameters.
- **MOCVD growth:**
  - **InGaAs MOSFETs** I performed the MOCVD growth of all the samples except for the TASE InGaAs wafer that has been grown by H. Schmid.
  - **InGaAs/GaAsSb TFETs** I developed the GaAsSb growth recipe, with support from Y. Baumgartner, and achieved excellent lattice-matched condition between GaAsSb and InGaAs. The obtained material quality was key to achieve high-performance TFET devices. I have also performed the channel and raised source drain MOCVD growth steps.
- **Wafer bonding:**

  The direct wafer bonding (DWB) process has been established by L. Czornomaz and D. Caimi. The DWB for my device has been performed entirely by D. Caimi.

- **TASE template fabrication:**

  The TASE process has been established at IBM by H. Schmid, L. Czornomaz, K. Moselund and M. Borg. I have fabricated the InGaAs templates and adapted the process to Sb-based compound materials, achieving crystalline GaSb material quality inside the templates.

- **Device fabrication:**

  I have personally done the device fabrication of both MOSFETs and TFETs from beginning to end, including fin etching, dummy gate formation, RSD, and BEOL. All the electron-beam lithography steps have been performed by A. Olziersky. The Si CMOS layer used for the 3D sequential integration demonstrator has been processed at CEA Leti Institute.

- **Material analysis:**

  Each sample had to be prepared for Transmission Electron Microscopy (TEM) using a focused-ion-beam (FIB) tool. This was done primarily by M. Sousa. TEM analysis was performed by M. Sousa, P. Staudinger and in some cases by N. Bologna, under a collaboration with the Swiss National Laboratories for Microscopy Studies (EMPA). I have done all the scanning electron microscopy (SEM) and atomic force microscopy (AFM) characterizations shown. The x-ray diffraction measurements were done by Y. Baumgartner.

- **Electrical characterization:**

  All the electrical measurements shown in this work have been performed primarily by me. During the measurements and the data analysis I received support from L. Czornomaz, C. Zota and K. Moselund. Only exceptions are the pulsed I-V measurements done by P. Paletti (Notre Dame University).

- **Device simulation analysis:**

  The TCAD simulation analysis has been performed by S. Sant under the supervision of Prof. Schenk at ETH-Zurich.

2 InGaAs-on-Silicon: a 3D Technology Platform

2.1 Introduction

The present chapter focuses on the technological features of the InGaAs-on-silicon 3D platform developed during this project. Two main aspects can be identified, the III-V-on-silicon integration methods and the transistor device processing. After a general overview on the existing material integration techniques, direct wafer bonding and template-assisted selective epitaxy are described in more detail. All the devices presented in this thesis have been fabricated following a standard CMOS-compatible replacement-metal gate process, independently of the approach selected to obtain the active device layer on the silicon substrate. Therefore, details on the InGaAs MOSFET process are provided here, with a special focus on key process modules and on their impact on device performance. The heterojunction TFET fabrication flow, instead, is the result of minor modifications to the standard MOSFET process, as shown in the following. Finally, as in the scaling era non-planar integration schemes are becoming key-enablers for technological advancement, a 3D sequential integration approach exploiting the advantages of direct wafer bonding is presented.

2.2 III-V-on-Silicon Integration

Compound semiconductors are nowadays widely used in electronics for different applications, thanks to their interesting optical and electrical properties [7]. A major feature is the small, direct band gap and the higher mobility compared to silicon at scaled dimensions. Although their commercial use is now established within the radio-frequency and optoelectronics industries, their integration in CMOS technology, targeting low-power applications, is still only a vision. In fact, several performance and technological marks must be met in order to make III-V semiconductors a sustainable choice for the well-established silicon industry. For instance, low fabrication costs and compatibility with standard CMOS process modules needs to be preserved, along with good material quality and device performance. Extremely encouraging results

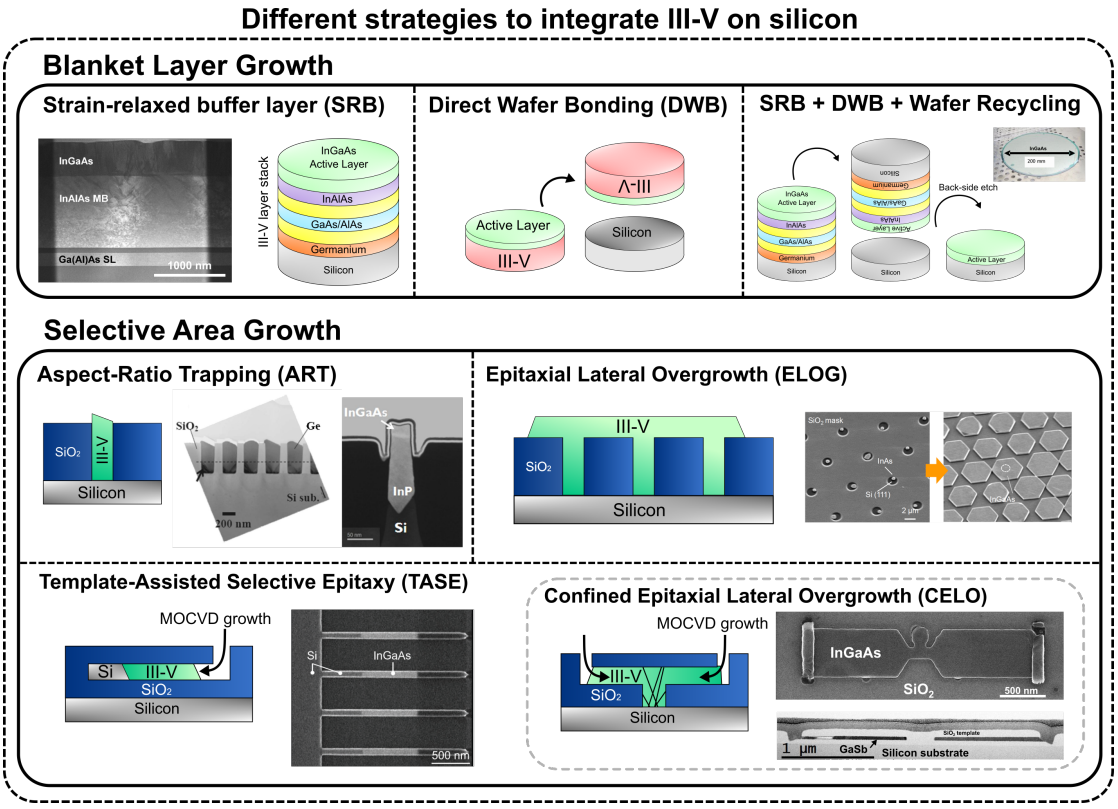


Figure 2.1 – Overview of several available approaches to integrate III-V on silicon substrates. Two main categories are identified: blanket-layer techniques are more suitable for the transfer of large-area III-V layers and for 3D sequential integration schemes whereas selective area growth is versatile for the local co-integration of different nanostructures featuring reduced defect densities.

have been shown using III-V FETs fabricated using native substrates. Nevertheless, a true challenge consists in achieving comparable performance on devices directly integrated on Si, as the obviously more complicated process would favor the formation of defects and impurities. There are several fundamental problems linked to the direct epitaxy of a III-V layer on Si substrate, also known as monolithic integration, and material scientists are nowadays working on strategies to mitigate them. Focusing on InGaAs, the main compound exploited in this work, three main issues can be identified [59]:

- $In_{50}Ga_{50}As$ and Si are characterized by very different lattice parameters, featuring a mismatch of about 8 %. This difference translates into plastic deformation as consequence of the formation of misfit and threading dislocations (MD, TD). Crystalline defects can develop in proximity of abrupt hetero-interfaces or in the presence of gradual strain relaxation and they can cause a complete failure of the device performance.

- The different crystal polarity between Si and III-V materials leads to the formation of domains of opposite charge (also known as anti-phase domains (APDs)), originating at monoatomic steps at the Si interface [60]. The meeting of two APDs, leads to anti-phase boundaries, where wrong bonds between two group V or group III atoms can form, resulting in trapping and scattering of charged carriers.
- Another source of defects formation is the difference in thermal expansion coefficient, larger for most of the III-V materials with respect to Si. InGaAs epitaxy is typically performed at elevated temperatures. Therefore the high temperature gradient that is generated while quenching to room temperature induces tensile layer stress.

To overcome these challenges, a number of integration methods have been explored, starting from the 1980s. Solutions consists of engineered epitaxial techniques to reduce and sometimes prevent the formation of defects. Fig. 2.1 provides an overview on the existing approaches, highlighting two major routes: blanket-layer growth and selective area growth techniques. Each category presents advantages and disadvantages, that might be specific for the target applications.

The application of strain-relaxed buffer (SRB) layer, for instance, enables gradual relaxation of the lattice constant mismatch by alternating several layers where stress distribution is carefully engineered. Direct wafer bonding (DWB) [61, 62], instead, allows to transfer any material from a donor wafer to the Si substrate. The donor wafer can be either a Si substrate (resulting in the combination of SRB and DWB [63] or simply a lattice-matched native III-V wafer. Moreover, DWB is particularly suitable for SOI wafer technologies, interesting for many high-frequency applications [64]. However, III-V native wafers are expensive and limited in size (a 2" InP wafer can cost up to 2000 $). Therefore, only the combination of SRB and DWB, meaning the growth of a III-V layer on a Si donor wafer and the transfer of this layer on another silicon substrate, can potentially allow for III-V-on-insulator (III-V-OI) wafers at any arbitrarily large size.

The large-area native wafer availability problem (and the related high cost) can be overcome with selective area growth (SAG) techniques, that make use of a dielectric mask to confine the epitaxial growth within accessible regions. The core idea relies on combining epitaxial processes with nano-fabrication techniques. This way, defects can be spatially confined and III-V nanostructures can be obtained only where desired, yielding lower fabrication costs. However, with this method active layers larger than a few microns can hardly be achieved. As described in Fig. 2.1, several implementations of SAG have been explored in the last twenty years. For instance, the growth of III-V materials into narrow, high-aspect ratio SiO_2 cavities on Si, known as aspect ratio trapping (ART), targets defects propagation termination at the trench sidewalls. ART

was proposed first for germanium epitaxy [65] and later exploited in III-V material systems [66, 67, 68]. However, in ART the propagation of planar dislocations in the {111} plane, parallel to the trench sidewall, cannot be prevented, at any cavity aspect-ratio. To overcome this problem, a recent technique called template-assisted selective epitaxy (TASE) have been developed at IBM Zurich [27, 69]. The III-V epitaxial growth takes place inside 3D cavities (namely templates), allowing for a growth confinement in both lateral and vertical direction. This technique is suitable for fabricating devices on (100)-oriented SOI substrates. The empty template contains a silicon structure that can be recessed resulting in well-defined {111} planes. Larger III-V volumes can instead be achieved with a well-known technique called Epitaxial Lateral Overgrowth (ELO) [70, 71]. The material growth proceeds laterally on a SiO_2 layer, starting from a small opening patterned inside an oxide mask. The principle of lateral overgrowth can be exploited in TASE cavities as well, giving rise to Confined Epitaxial Lateral Overgrowth (CELO) technique [28]. For simplicity, all the epitaxial techniques inside empty cavities will be from now on classified as TASE.

Devices fabricated with both DWB and TASE will be shown in the following chapter. Therefore, in the next section, we will provide a detailed description of the two approaches.

2.2.1 InGaAs-on-insulator: Direct Wafer Bonding

The process starts with the epitaxial growth of a III-V stack on a 2" semi-insulating high-grade (100)-oriented InP donor wafer. The stack comprises the InGaAs active layer (of thickness t_{ch}) and an etch-stop heterostructure with alternating InGaAs, InAlAs and InP thin films. The layer sequence has been carefully engineered in order to ensure a safe active layer transfer on the target substrate. The epitaxy is performed using a metal-organic chemical vapor deposition (MOCVD) reactor at 500 °C. A schematic overview of the process is displayed in Fig 2.2. Following, a SiO_2 buried oxide layer (BOX) is deposited directly on the active InGaAs layer. This allows for a better control of the III-V/oxide interface quality, that is crucial to minimize the density of interface traps (D_{it}).

Previous studies performed at IBM Research show Al_2O_3-Al_2O_3 is the combination with the highest bonding strength (1.5 J/m^2 at 250 °C) within the temperature process window that prevents the InP substrate from breaking during annealing (below 400 °C) [72]. Therefore, 10 nm of Al_2O_3 is deposited on the III-V wafer by atomic-layer deposition (ALD) at 250 °C. Next, the hosting substrate is prepared. The target wafer is a 4" (100)-oriented n-type Si wafer. First a buried oxide layer (BOX) consisting of 25 nm of SiO_2 is deposited by plasma-enhanced chemical vapor deposition (PECVD) followed by the deposition of the Al_2O_3 thin bonding oxide. The surface on both wafers is prepared with a wet cleaning recipe based on ozone-rich de-ionized water (DIO_3),

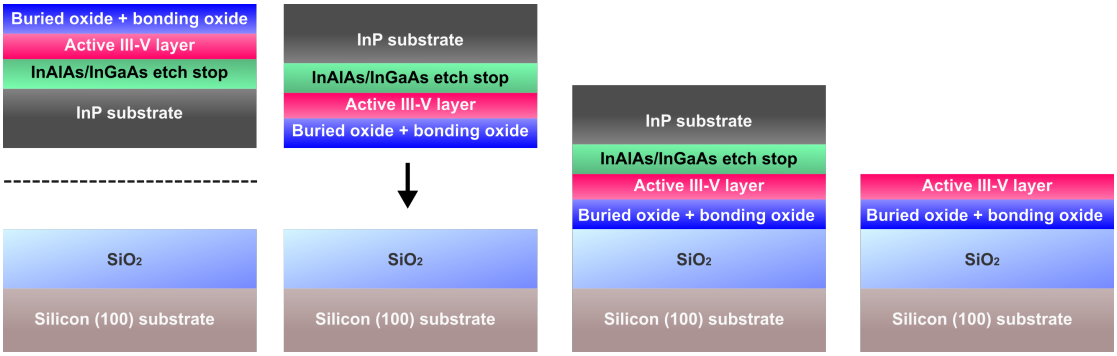


Figure 2.2 – Schematic illustration of direct wafer bonding performed to obtain a III-V-on-insulator as final result. The substrate surface topography and the oxides bonding strengths play a crucial role in the process.

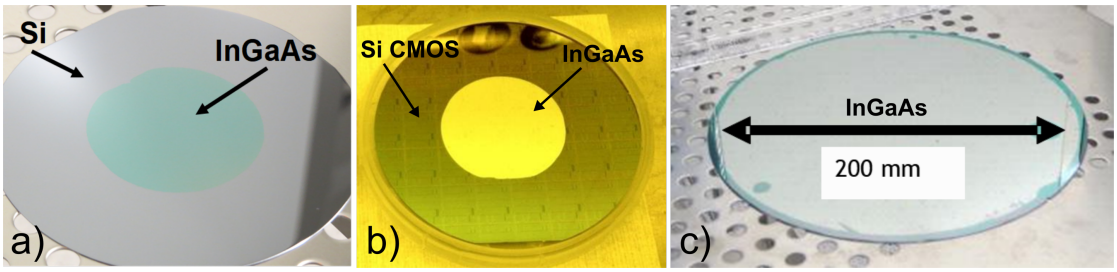


Figure 2.3 – Photographs of a) 20 nm thick InGaAs bonded on Si, b) 20 nm thick InGaAs bonded on pre-processed Si-CMOS wafer and c) InGaAs layer bonded on 200 mm Si wafer, the largest we have demonstrated.

before and after the oxide depositions. Shortly after the cleaning, the two wafers are brought into intimate contact at room temperature and ambient atmosphere to initiate the bonding. The bonding energy is then increased by annealing the wafers for 3 hours at 250 °C. The active III-V layer is subsequently released from the donor substrate using a fast wet etching process based on concentrated hydrochloric acid (HCl). The etching stops on the InGaAs/InAlAs layers. They are hence wet-etched using diluted acids that feature a slower etch rate, such that the remaining layers can be removed without damaging the active one. This step completes the DWB process [73]. DWB is a key enabling technology for 3D sequential integration schemes. A very similar process can be implemented to transfer a III-V layer on a pre-processed Si substrate. For instance, the hosting wafer can include Si-CMOS devices in a bottom layer. In this case, the target wafer must be additionally planarized before the bonding, to achieve a surface roughness smaller than 0.5 nm. This is obtained by planarizing the SiO_2 layer using chemical mechanical polishing (CMP).

This microfabrication technique has been historically developed to fabricate silicon-on-insulator (SOI) substrates. It represents a very versatile, cost-efficient technique and it can be up-scaled to large wafer size. Most of the cost-advantage has been ex-

ploited with the development of SmartCut^{TM}, an industry-standard method involving the full recycling of the donor wafer. Previous work done at IBM Research shows that a SmartCut-like approach can be implemented in the described InGaAs-OI bonding process and the bonding of wafers up to 200 mm has been demonstrated [63]. Fig. 2.3 shows pictures of fabricated wafers examples. In the experiments reported in this thesis, the wafer recycling was not performed since it adds process complexity and it goes beyond the scope of this work.

2.2.2 Selective Epitaxial Growth of InGaAs on silicon

Although DWB represents a very convenient method for transferring entire layers of high-quality materials on foreigner substrates, it still implies high production costs for very large scale integration (VLSI). As a matter of fact, a more local technique, that would allow to place III-V material only in pre-defined areas would eliminate the excessive cost related to III-V substrates and would open new paths for hybrid solutions. Several approaches have been successfully explored in this direction. The ELO method, for instance, does not provide a sufficient control of the III-V thickness and of the fin height, therefore is not suitable for ultra-scaled structures. Moreover, threading dislocations can easily reach the device layer as the {111} glide planes are not efficiently trapped within the elongated mask openings. With the ART technique, instead, it can be challenging to grow III-V nanowires inside very narrow trenches, for instance with a diameter smaller than 20 nm. In this case, the gas precursors can hardly reach the bottom nucleation seed and the growth rate decreases rapidly. These problems can be addressed by TASE, where a 3D oxide structure provides growth confinements in multiple directions [74]. For instance, researchers at IBM have reported the observation of defects-free GaAs nanowires using this technique [75]. The process to fabricate InGaAs µm-sized structures integrated on Si will be described in detail. Fig. 2.4 shows an overview of the template fabrication process and highlights the major phases. To start, a 25 nm thick SiO_2 layer is deposited on a 4" (100)-oriented n-type Si wafer (Fig. 2.4a). An e-beam lithography step allows to pattern small openings (diameter of 50 nm) in the oxide layer and to expose the underlying Si substrate. The resist used is Poly(methyl methacrylate), also known as PMMA, and the oxide is dry-etched with reactive-ion etching (RIE) (Fig. 2.4b). Then the wafer is covered by a sacrificial layer, namely 30 nm of amorphous silicon deposited using a sputtering technique (Fig. 2.4c). This layer represents a key-player in the process as its thickness and morphology will mirror the final III-V structure properties. The next e-beam lithography step consists in patterning structures to be transferred in the III-V layer. Hydrogen silsesquioxane (HSQ) is a negative resist, and it is used in this step to define a µm-sized hard mask, in correspondence of the previously defined openings. The sacrificial layer is dry-etched using inductively-coupled plasma (ICP)

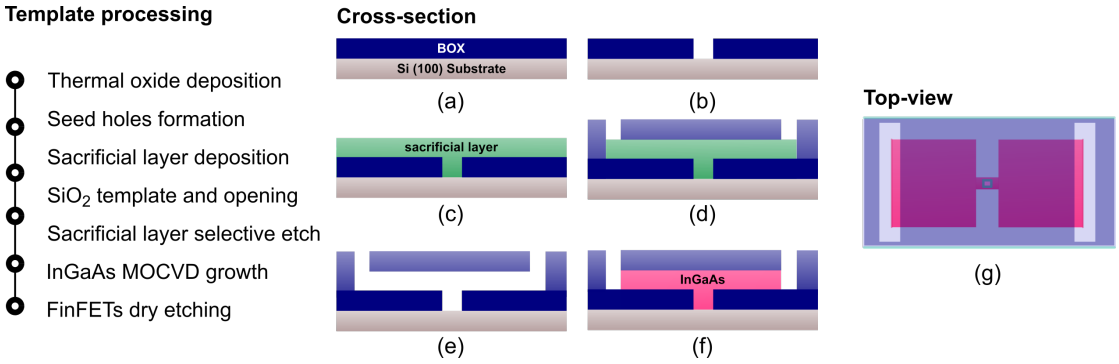


Figure 2.4 – Fabrication flow describing the template-assisted selective epitaxy (TASE) process. (a-e) Fabrication of the SiO_2 template, (f-g) InGaAs growth by MOCVD. Optionally fins can be dry-etched by patterning a mask on the platelet shown in (f). The growth expands first vertically and then laterally in the cavity, hence an effective defect filtering takes place.

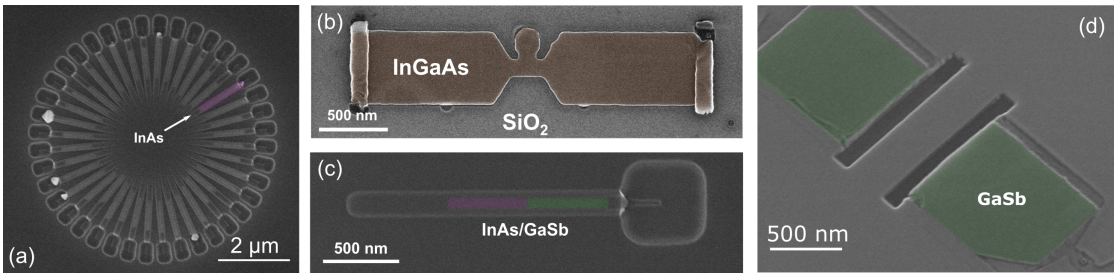


Figure 2.5 – Different examples of III-V nanostructures fabricated using TASE. (a) SEM image showing InAs nanowires designed in a star-like pattern. The picture highlights how different orientations feature different growth rates. (b) InGaAs platelet expanding from the central seed to the two sides. (c) Example of in-situ heterostructure growth (InAs/GaSb) and (d) GaSb platelets.

etching. A second oxide layer, the oxide template, is deposited by PECVD (100 nm of SiO_2) (Fig. 2.4d). Two extremes of the template are opened using PMMA resist and RIE etching. The amorphous Si present inside the cavity is hence selectively removed with a XeF_2 dry-etching process (Fig. 2.4e). Finally, an empty micro-cavity is obtained, exposing a small silicon seed. The Si native oxide is removed with HF etching, shortly before the III-V growth starts. The wafer is loaded into a MOCVD reactor, where trimethylgallium (TMGa), trimethylindium (TMIn) and tertiarybutylarsine (TBAs) are used as precursors gases to grow InGaAs (the growth is done at 550 °C), as shown in Fig. 2.4e.

Examples of structures featuring different materials and geometries, fabricated using this technique are shown in Fig. 2.5 [76]. This method enables an efficient defect filtering as the growth proceeds first vertically and then expands laterally within the template, where the compound crystal is geometrically confined. The oxide layer is removed using both wet and dry etching and the III-V resulting micron-sized crystal

can be patterned and etched into smaller fins (see next section), nanowires or it can provide a virtual substrate to perform further heteroepitaxial growth [77, 78]. The fin dry-etching process, common to TASE and DWB devices, will be described in the next section.

2.3 Replacement-Gate InGaAs MOSFETs on Silicon

Here we present the self-aligned replacement metal gate (RMG) InGaAs MOSFET fabrication flow. A micron-sized InGaAs crystal on a Si substrate represents the starting point of this process and it can be obtained equivalently with the two integration methods just described (TASE and DWB). Electrical results from both approaches will be shown in later chapters and compared.

The main advantage in using an RMG scheme, as opposed to gate-first approach, is that the transistor high-K metal-gate (HKMG) layer is deposited at the end of the process, hence does not see the high-temperature steps. Achieving a high quality gate-oxide/channel interface (with low D_{it}) is extremely challenging in III-V materials, and because of the poor quality of their native oxides, specific materials such as Al_2O_3 needs to be artificially deposited within very controlled conditions. This is not the case for silicon, for instance, that form pristine interfaces with its native oxide, SiO_2. Therefore, for InGaAs it is of crucial importance to avoid any possible source of oxide interface quality degradation. After providing an overview of the fabrication flow, a detailed process module description will focus on key-aspects of the realization of high-performance InGaAs MOSFETs on Si.

2.3.1 InGaAs MOSFETs: device processing

The RMG process developed in this work is a CMOS-compatible self-aligned flow. Fig. 2.6 shows an overview of the process, a device cross-section schematic and a summary of the integration routes implemented in this work to demonstrate InGaAs MOSFETs. The active device area pattern is transferred into a SiO_2 hard mask (3 nm) implementing two separate electron beam (e-beam) lithography steps. First, high-resolution negative resist, HSQ, is used to obtain fins with a width (W_{FIN}) between 10 nm and 200 nm. Structures with a number of parallel fins between 1 and 8 are obtained. All the devices presented in the thesis will be referred to as "FinFETs" although the gate oxide thickness is the same on the top and on the side facets (this type of architecture is often labeled as tri-gate).

The larger area is instead patterned in a subsequent lithography step using a lower resolution positive resist, PMMA. SEM pictures after the e-beam resist development are shown in Fig. 2.7. The resulting pattern is transferred into the oxide hard mask using RIE. The exposed III-V area is therefore dry-etched with an inductively-coupled

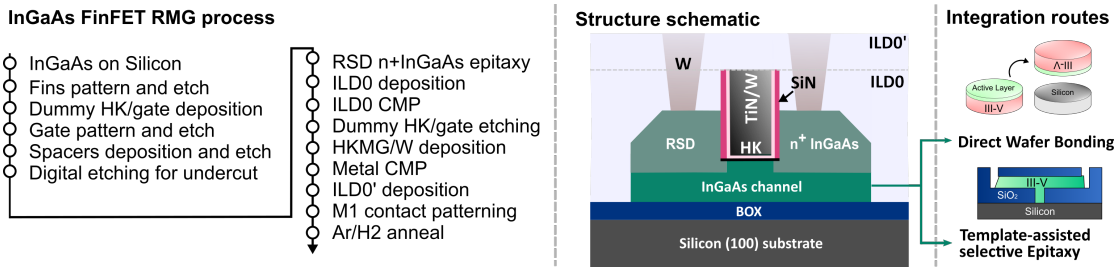


Figure 2.6 – Schematic description of the replacement metal gate (RMG) process flow, used to fabricate all the devices reported in this work. The InGaAs channel has been obtained following two different integration routes, as schematized on the right. Each transistor features raised-source-drain contacts, gate sidewall spacers and doped extensions.

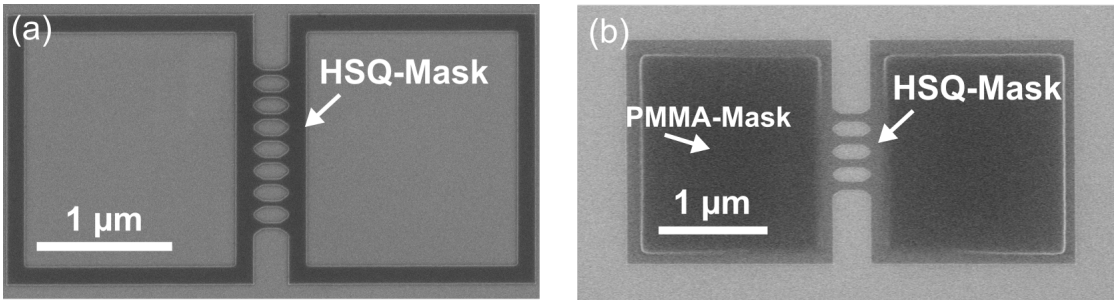


Figure 2.7 – SEM images showing (a) the HSQ mask used to pattern the high-resolution features by e-beam lithography (b) and the PMMA mask for the low-resolution regions.

plasma etching process (ICP-RIE), using a cycling plasma. The mask is then stripped by reactive ion etching (RIE). SEM pictures of the dry-etched InGaAs fins are shown in Fig. 2.8. Although TASE offers the alternative to directly shape the empty cavities into fins, this approach turned out to be more challenging to implement and led to lower device yield. This can be attributed to the more complex template shape that introduces obstacles to the gas precursors path toward the nucleation seed. The dummy gate structure, that will be subsequently replaced by actual high-K (HK) and metal-gate layers, is obtained by depositing 3 nm of Al_2O_3 by ALD and 150 nm of amorphous Si by sputtering. A HSQ hard mask is used to transfer the gate pattern to the a-Si layer, that is dry etched with a HBr-based ICP-RIE process. Gate lengths (L_G) as small as 14 nm have been achieved.

Sidewall spacers that separate the gate from the subsequent raised-source-drain (RSD) contacts, are obtained by depositing a SiN layer by ALD and then etching using a CHF_3-O_2 RIE process. After removing the protecting Al_2O_3 using diluted HF, source-drain extensions regions are formed underneath the spacers. More details on this step will be provided in the next sub-section. The wafer is then introduced into a MOCVD reactor and Sn-doped n^+-InGaAs contacts are grown at 550 °C. Raised contacts increase the channel material volume near the source/drain regions and

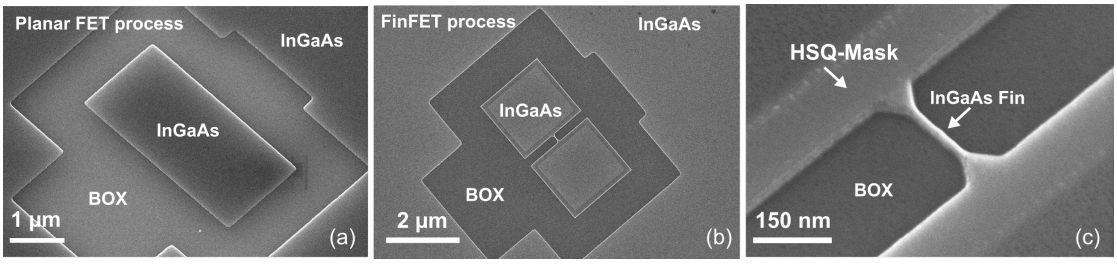


Figure 2.8 – SEM images showing (a) a planar InGaAs structure, (b) an InGaAs FinFET and (c) a zoom on the InGaAs fin showing the edge HSQ mask used for the patterning. From picture (b) it is also visible that the transistor area is surrounded by a large III-V area. This is done to ensure a more uniform RSD growth.

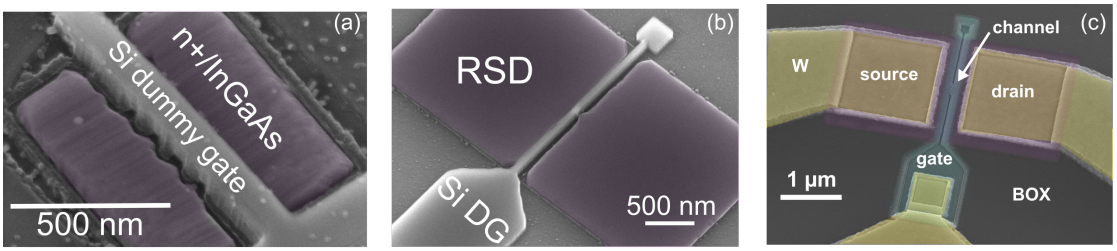


Figure 2.9 – SEM images showing InGaAs MOSFETs after the doped contact regrowth step (RSD) obtained using (a) TASE and (b) DWB. (c) Finalized transistor top-view with tungsten metal contacts for source, drain and gate.

therefore lower the channel resistance. Fig. 2.9a,b show two FETs after the RSD step, for the transistor fabricated with TASE and with DWB, respectively.

Subsequently, the devices are encapsulated by an inter-layer dielectric (ILD0) consisting of 250 nm SiO_2 that is deposited by PECVD and mechanically planarized by CMP. The purpose of this planarization is to reduce the topography and allow to access the top-side of the dummy gate. Once the dummy gate is exposed, the a-Si native oxide is etched in HF and a selective dry etching process based on XeF_2 etching is performed. A scaled HK bi-layer (Al_2O_3/HfO_2) is deposited by ALD, including additional 20 nm of TiN deposited *in-situ* and acting as metal gate. Following, W is sputtered and planarized by CMP. A second oxide layer, namely ILD0', is deposited by PECVD. A final e-beam lithography step is done to open vias (the mask used is PMMA) into the oxide such that source, gate and drain can be accessible for metallization. Finally, 100 nm of W is sputtered and metal 1 (M1) contact pads are patterned using a negative resist mask and dry etched with RIE. The wafer is heated under forming gas anneal (FGA) at 300 °C for 30 min using a rapid thermal anneal (RTA) system. The SEM image of a finalized device is shown in Fig. 2.9c.

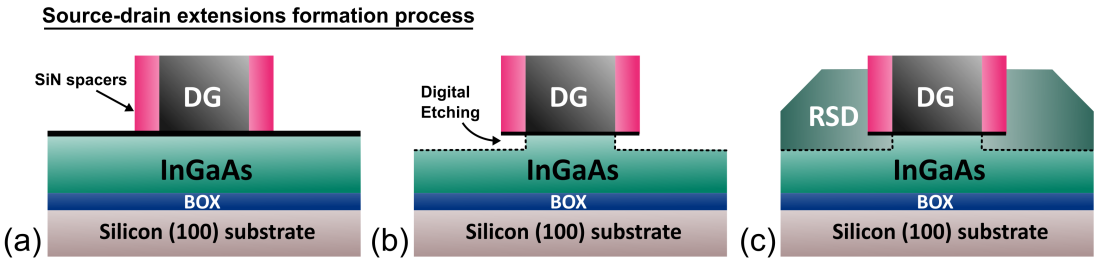
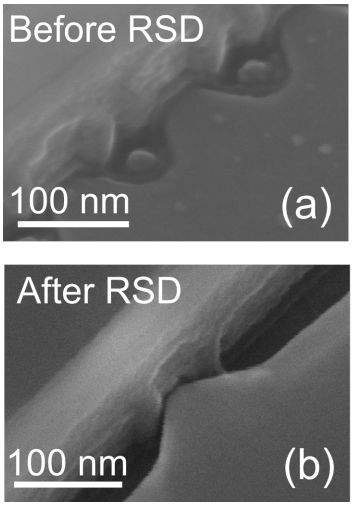


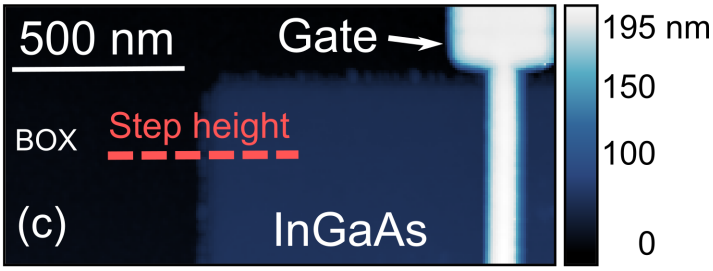
Figure 2.10 – Schematics illustrating the main steps in the source-drain extensions formation process. The InGaAs is selectively removed beneath the oxide spacers with digital etching allowing for an extremely accurate control of the extensions position.

2.3.2 Raised source/drain doped extension

Achieving excellent electrostatic control and limiting the series resistance contribution coming from the source-drain regions are crucial factors to match the target performances for scaled MOSFET technology nodes. Notably, III-V FETs suffer from large I_{OFF}, caused by favored band-to-band tunneling (BTBT) due to the narrow band gap. Electrostatic control and current densities can be maximized using 3D transistor geometries such as fins or nanowires, but in many of these designs the channel is confined on the back side by an insulating back-barrier. This is the case for all the InGaAs devices presented in this work, where the underlying SiO_2 BOX represents a crucial component to implement both integration routes. The floating body nature of such devices can negatively affect III-V MOSFET performance triggering the so called parasitic bipolar effect (PBE). PBE occurs as consequence of accumulation of holes in the channel that, due to the lack of body contact, lower the potential energy barrier between source and drain and contribute to the amplification of I_{OFF}. The physics behind this effect will be described in section 3.2.1.

Simulation studies performed at ETHZ suggest the implementation of gate sidewall spacers to mitigate both BTBT as well as trap-assisted tunneling (TAT) occurring at the oxide/channel interface [79]. Simultaneously, the access resistance degradation due to the presence of ungated channel regions can be engineered by replacing the low-doped InGaAs channel in those regions with n-doped InGaAs. This solution was already established in Si transistor processes and it is known as *raised source-drain extension* [13]. In this work, a specific process module is designed for InGaAs FETs and its detailed description is the focus of this subsection. Afterwards, electrical results supporting the technological implementation will also be discussed. A schematic overview of the process module is shown in Fig. 2.10. A SiN layer is deposited by ALD and it is exposed to the etching process, without any etch-mask. The spacers are formed as result of the anisotropicity of the dry etching process that features a slower etching rate in the lateral direction. Therefore, the final spacer thickness corresponds





Number of DE cycles	0	3	6
RMS roughness [pm]	930	672	284
Step height [nm]	38	35	32

(d)

Figure 2.11 – SEM zoom on the InGaAs fins (a) before and (b) after the RSD step. Picture (a) highlights the slight recess of the InGaAs following the digital etching (DE) process. (c) AFM image showing the transistor dummy gate and the source side. AFM is used to keep track of the DE rate. (d) Table showing the data collected from the AFM scan. For increasing number of DE cycles a reduced surface roughness is achieved and and etch-rate of 1 nm/cycle is obtained.

to 70% of the nominal deposited layer thickness. An Al_2O_3 etch-stop layer protects the channel from the spacer dry-etching (Fig. 2.10a). A digital etching (DE) process is used to form the extensions, allowing to achieve low and controllable etching rates. The DE is performed in two steps: 8 min of dry-oxidation inside an UV-Ozone chamber at room temperature followed by 15 s etching in HCl:H_2O (1:10) solution (and 1 min rinse in de-ionized water) (Fig. 2.10b). Shortly after the last cycle, the wafer is loaded into the MOCVD reactor and the RSD epitaxial growth can take place (Fig. 2.10c). Fig. 2.11a,b show gated InGaAs fins, after DE and RSD steps respectively. The etching rate has been calibrated by measuring the InGaAs thickness variation using atomic force microscopy (AFM) (Fig. 2.11c) and a value of 1 nm/cycle has been obtained. Similar values have been reported in another work for InP DE [81]. The achieved etching rate is very stable due to the saturated oxidation of the InGaAs surface, in accordance with what is predicted from the Lukeš rate law for GaAs [82]. The HCl, at this dilution, only etches the formed III-V-oxide and it is selective to the remaining InGaAs. Surface roughness has also been estimated through AFM measurement (Fig. 2.11d): A significant improvement for increasing number of performed cycles is obtained. In Fig. 2.12 a, on-resistance (R_{ON}) versus L_G for InGaAs FinFETs fabricated with DWB, (W_{FIN} = 40 nm) is shown. In this case, the spacer thickness is 10 nm and 10 cycles of DE were performed. The access resistance (R_{acc}) is obtained by linear extrapolation and it is equal to 220 Ω/µm. The effectiveness of the implemented process, i.e. the use of doped extension regions, is assessed by comparing this value for different spacer

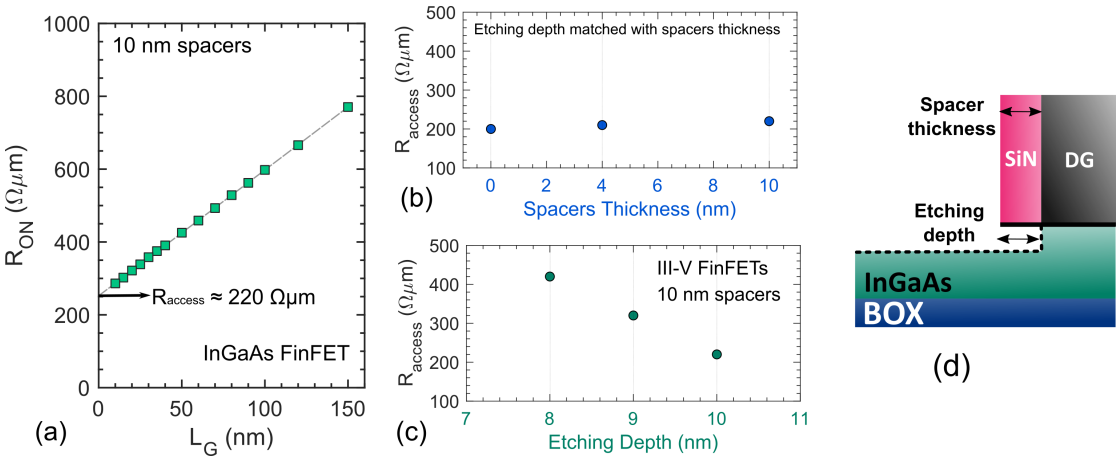


Figure 2.12 – (a) On-resistance versus gate length for an InGaAs FinFET featuring 10 nm spacers. An access resistance R_{acc} of 220 Ω µm is obtained through extrapolation with the y-axes intercept. R_{acc} for devices with different spacer thicknesses (b) and etching depth (c). The etching depth is determined by the number of etching cycles performed, as shown in (d). R_{acc} is minimized for an etching depth matching exactly the spacer thickness.

thicknesses (Fig. 2.12b) and etching depth (Fig. 2.12c). The result is that a low R_{acc} can be achieved by carefully matching the depth of the formed cavity with the spacer thickness. A mismatch of only 1 nm results in approximately 100 Ω µm of increase in access resistance. High-resolution TEM images of fabricated transistors featuring 0, 4 and 10 nm spacers are displayed in Fig. 2.13. The same process has been applied on TASE-grown InGaAs FETs. Fig. 2.14a, b show electron-diffraction X-ray (EDX) maps corresponding to the device cross-section in Fig. 2.14c. The unintentionally higher indium content in the contact regions allows to clearly visualize the extension of the source-drain regions below the spacers.

In this section we have described the RMG InGaAs MOSFET fabrication flow featuring key new technology modules:

- **source-drain spacers**, to limit the influence of PBE on the off-current;
- **doped contact extension regions** to eliminate the access resistance contribution coming from the region beneath the spacers;
- a minimum **gate length of 14 nm**, particularly exceptional for RMG processes where dimensional scaling is not as simple as for gate-first schemes.

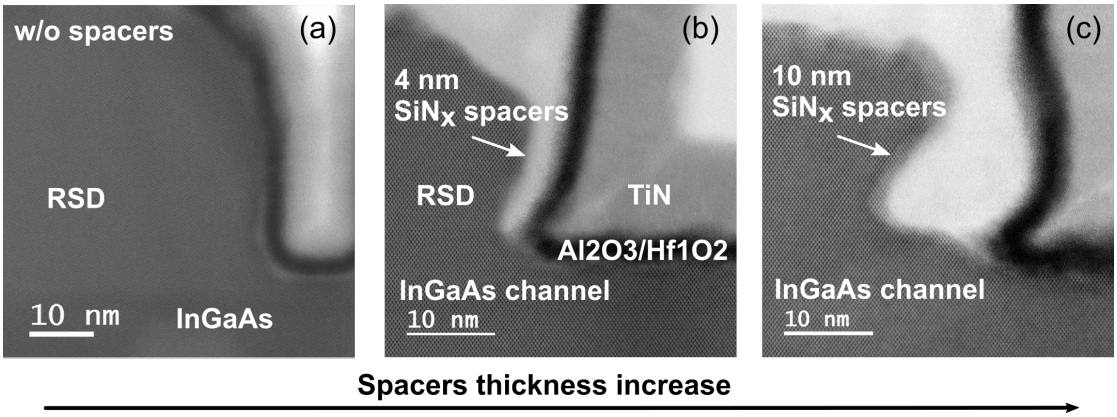


Figure 2.13 – Cross-sectional high-resolution TEM images showing InGaAs MOSFETs with three different spacer thicknesses: (a) no spacers, (b) 4 nm and (c) 10 nm spacers. The use of spacers targets a suppression of the parasitic bipolar effect causing high off-current leakage in III-V FETs. Adapted from [80].

2.4 Replacement-Gate InGaAs/GaAsSb Tunnel FETs on Silicon

TFETs are considered as a promising alternative to standard CMOS technology at ultra-low voltages [31]. The excellent transport properties with the possibility for band alignment engineering make III-V semiconductors particularly suitable for TFETs design. InGaAs/GaAsSb is an attractive combination as heterostructure material choice and several sub-thermionic TFETs have been demonstrated using this system [55, 57]. Although the best performances have been achieved primarily in vertical nanowire geometries on Si (111) or III-V native substrates, the technological relevance of a III-V TFET platform will be also evaluated on the feasibility to integrate these devices on Si (100) substrates, using process modules compatible with standard CMOS technologies. The III-V technology platform described in the previous sections represents the baseline for the TFET process. The same flow has been thoroughly adapted to fulfill all the necessary requirements to achieve an high-performance InGaAs/GaAsSb heterojunction TFET:

- The D_{it} must be minimized in order to prevent TAT from occurring at the oxide/channel interface;
- The structure must be highly scalable and electrostatically efficient;
- The defect density at the heterojunction tunneling interface must be minimized;
- Gate-to-source misalignment is responsible for defect-mediated parasitic tunneling at the heterointerface. Therefore, a self-aligned architecture would be

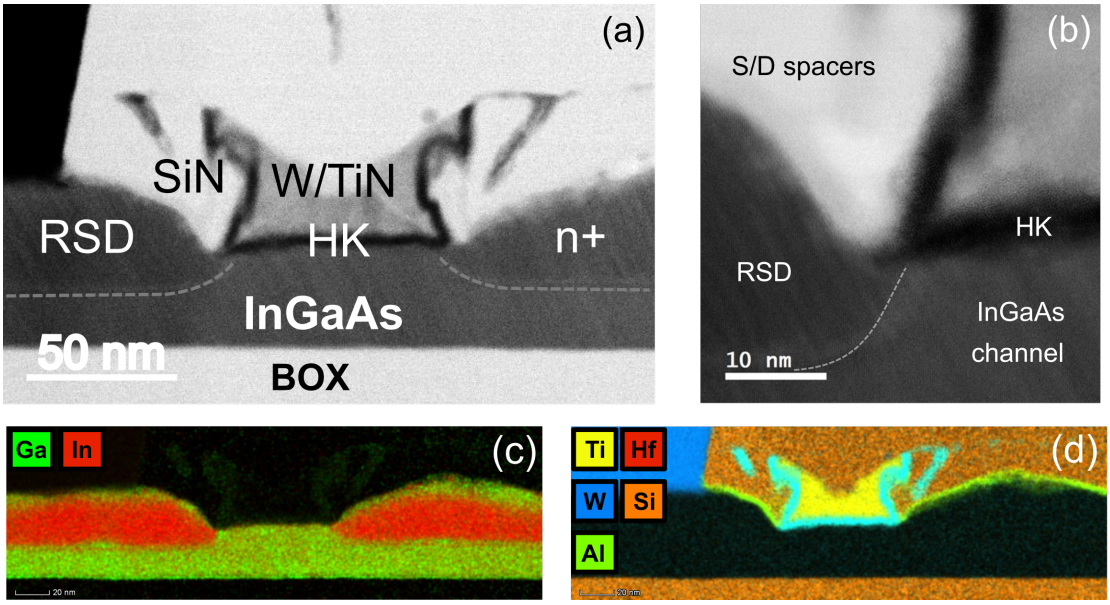


Figure 2.14 – (a) TEM cross-section of an InGaAs FinFET fabricated with TASE. The RSD region extending beneath the spacers is drawn by a dotted gray line. (b) Zoom-in on the channel-contact junction. (c,d) EDX compositional maps where the extension regions position is perfectly highlighted by the difference in In content between channel and doped contacts.

desirable [83];

- All the Sb-based compound materials (essential to build a TFET III-V heterostructure) are very sensitive to oxidation and show very poor selectivity with most of the standard etching solutions. A fabrication flow compatible with this materials has yet to be developed.

Some of the listed requirements follow previously published simulation results, some are conclusions based on actual technological challenges encountered during the experiments developed in this work. Fig. 2.15 illustrates the TFET processing steps and highlights the variations with respect to the standard InGaAs MOSFET fabrication flow. *The described approach has enabled the demonstration of the first sub-thermionic III-V TFET integrated on silicon in a fully compatible CMOS process.* The DWB integration route is selected to fabricate the starting heterostructure. Since TFETs are complex devices from a technological standpoint, a more mature III-V integration approach has been selected. Nevertheless, exactly the same process can be straightforwardly reproduced on InGaAs structures directly grown using TASE. Furthermore, *the implemented flow made possible the parallel co-planar integration of InGaAs n-MOSFETs and InGaAs/GaAsSb n-TFETs on the same substrate.*

The TFET RMG process starts with a III-V bi-layer of InP (20 nm)/ $In_{75}Ga_{25}As$ (20 nm). The bottom InP acts as back-barrier to separate the InGaAs channel from

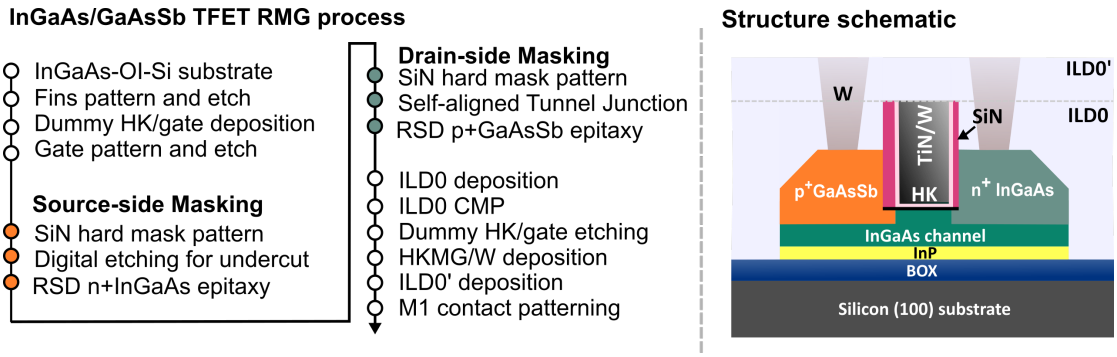


Figure 2.15 – Detailed process flow describing the main fabrication steps for InGaAs/GaAsSb TFET. Steps in orange and green are highlighting the variations compared to the standard MOSFET process, necessary to obtain source and drain made of different materials. On the left the finalized TFET structure is schematized. The InGaAs starting layer is obtained with direct wafer bonding.

the defective BOX bonding interface. The major difference compared to the MOSFET process is that source and drain need to be grown independently, therefore two separate growth-runs are required for the RSD module. After the InGaAs fins are patterned and dry-etched, the dummy gate is formed (L_G down to 10 nm have been achieved). Hence, the source side of the transistor is protected with a SiN hard mask. As in the spacer formation process described above, the SiN anisotropic etching used to pattern the source side will also result in 3 nm thick spacers on the drain sidewall. Moreover, the SiN mask provides high selectivity during the III-V growth, hence no parasitic deposition can occur. The dummy HK located on the drain side is removed using HF wet etching, and a DE process (see section 2.3.2) allows to form doped extensions below the spacers. In this case, only 3 cycles were necessary to create a recess af about 3 nm. The drain is formed by regrowing n^+ Sn-doped $In_{53}Ga_{47}As$ at 520 °C, with a doping concentration of 1×10^{19} cm^{-3}. The doping density has been previously calibrated on blanket layers [72]. A SEM image of a TFET after the first regrowth step is shown in Fig. 2.16a. Once the two RSD steps are done, the process is completed following the standard steps described in the MOSFET section. A second SiN mask, of the same thickness, is deposited on the wafer, protecting this time the drain side. Fig. 2.16b shows the drain side protected by the lithography mask used to be transferred into the SiN layer. The formation of the GaAsSb source (Fig. 2.16c) represents the core innovation of this process and the key-enabler for high-performance TFETs. Therefore, a detailed description of the self-aligned source/channel junction formation as well as the development of the hetero-epitaxial growth of GaAsSb lattice-matched to InGaAs will be presented in the following subsections. The MOSFETs fabricated on the same substrate are only exposed to the n-type RSD step, whereas they are protected during the p-type regrowth (Fig. 2.16d). The final TFET structure fulfills

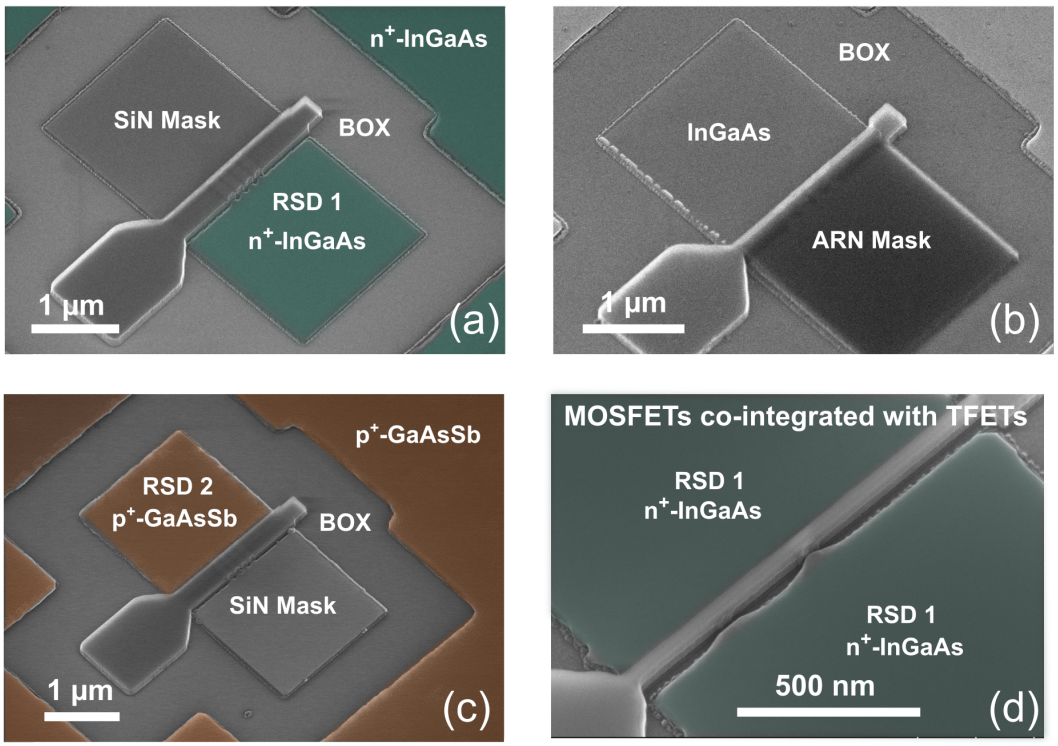


Figure 2.16 – SEM top-view of the TFET (a) after doped InGaAs drain regrowth (the source side being protected by a SiN hard mask), (b) drain side protection and (c) doped GaAsSb regrowth. The surrounding blanket III-V area is exposed to both growth steps and is removed at the end with a wet-etching process. (d) InGaAs MOSFET co-integrated with TFETs and processed in parallel. During the GaAsSb regrowth the MOSFETs are protected by a SiN hard mask.

most of the technological requirements listed above, including the scalability aspect and the material compatibility, making these devices particularly suitable for VLSI applications.

2.4.1 Self-aligned tunnel junction formation process

Previous studies on heterojunction III-V TFETs suggest that channel scaling and gate alignment are the two major routes to enable reduced hetero-interface TAT [83]. In this work, for the first time, self-alignment between gate and source is demonstrated in a lateral, CMOS-compatible TFET on silicon. The RMG scheme itself is intrinsically characterized by having the contact regions self-aligned to the gate. However, design guidelines from simulation studies indicate that the tunneling interface must be sharply aligned with the gate and a few nm of misalignment would have a detrimental impact on the device performance. Technological solutions such as Zn diffusion doping or metal alloying do not allow for sufficient control of the junction positioning

[84]. In this work, we propose a method based on the doped extension process described in section 2.3.2, applied to the heterostructure III-V system. This module is the key enabler for high-performance heterostructure TFET. The developed process is documented in a patent invention [85].

The detailed process of self-aligned tunnel junction formation is illustrated in Fig. 2.17. When the second SiN mask is created on the InGaAs drain side, a spacer of 3 nm adds on the previously obtained one, resulting in a total thickness of 6 nm and of 3 nm on the drain (Fig. 2.17d). Therefore, in order to carefully align the tunnel junction to the gate, a number of DE cycles corresponding to an etching depth of 7 nm is performed. The same digital etching parameters described in section 2.3.2 have been used. After the DE, the InGaAs surface is ready for the second epitaxial growth, where p+ Zn-doped $GaAs_{50}Sb_{50}$ is regrown at 525 °C. More details about the growth conditions are provided in the next section.

Cross-sectional STEM images of source-channel, HK-channel and channel-drain interfaces are shown in Fig. 2.18. By comparing Fig. 2.18a and b, the difference in spacer thickness can also be appreciated. The high atomic resolution allows assessing that the material is everywhere crystalline but the three regions can be hardly distinguished by simple electron transmission microscopy. Compositional analysis is hence performed to evaluate the effectiveness of the implemented process module. Particularly, the positioning accuracy of the tunneling junction is investigated with EDX elemental analysis. In Fig. 2.19a-d, maps of the tunneling region reveal the higher Ga composition that characterizes the source side (the nominal composition is $GaAs_{50}Sb_{50}$ for the source and $In_{75}Ga_{25}As$ for the channel). A line signal profile across the GaAsSb/InGaAs junction is shown in Fig. 2.19a. The Ga concentration, maximum in the source, drops at the interface with the channel and increases again in the drain where the InGaAs is expected to have 50% In content.

2.4.2 GaAsSb on InGaAs epitaxy: growth parameter optimization

To form a self-aligned TFET source, epitaxial growth of lattice-matched GaAsSb on InGaAs is required. The interface between the two layers constitutes the tunneling junction, therefore it is of crucial importance to minimize the strain and match the target composition. Moreover, it is important to identify the critical thickness above which plastic deformation occurs in the layer [86].

The GaAsSb/InGaAs/InP system has been extensively studied in the last thirty years because of the type-II band alignment, interesting for several applications such as mid-infrared (mid-IR) sources and heterojunction bipolar transistors (HBTs) [87, 88]. Working with these compounds is challenging since ternary or quaternary alloy systems such as $GaAs_{1-y}Sb_y$ or $Al_{1-x}Ga_xAs_{1-y}Sb_y$ are known to have a significant solid-phase miscibility gap, meaning that no alloys can form within a certain range of solid

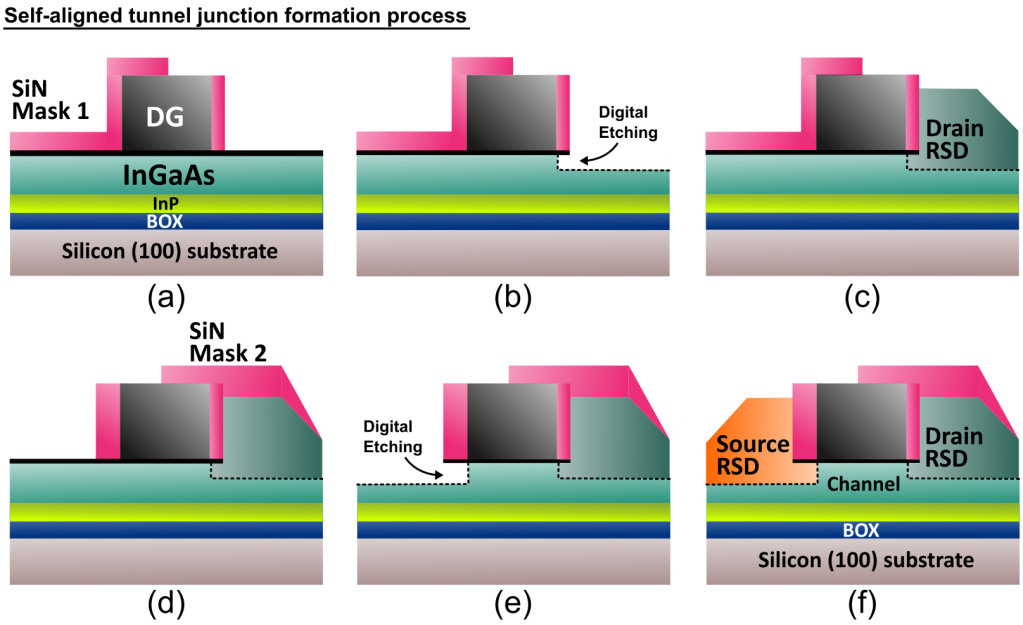


Figure 2.17 – Illustrations of the process steps required to position the tunnel junction self-aligned to the gate. Similarly to what described for the MOSFETs, the channel on the two sides is recessed using a digital etching process (b,e). Source and drain are alternatively protected during the MOCVD growth steps.

composition. The existence of the miscibility gap and its temperature dependence were calculated by Stringfellow *et al.* and confirmed by several experimental demonstrations [89]. For $GaAs_{1-y}Sb_y$ the gap is predicted to be around $0.05 < y < 0.8$, thus including the InP lattice-matched $GaAs_{50}Sb_{50}$. Nonetheless, Cherng *at al.* [90] in 1984 demonstrated the possibility to obtain GaAsSb compositions in the range of solid immiscibility by using a ratio between the group V and the group III gas precursor flow (V/III ratio) smaller than 1. This finding relates to the impact of V/III ratio on the Sb distribution coefficient, that must be kept close to unity, to ensure an efficient incorporation of all the As and Sb reaching the growth facet.

The present epitaxial growth calibration is performed on 2-inch semi-insulating InP (001) substrates. $GaAs_{50}Sb_{50}$ is expected to be equivalently lattice-matched to InP and InGaAs. Once the right parameters are identified, the full InGaAs/GaAsSb system is tested and then reproduced in the source formation TFET process module. Another important aspect of the optimization is that the blanket layer growth calibration well mirrors the process conditions on the actual device wafer. In fact, during the isolation of the III-V active device area, only a contour within a few µms is actually removed. This can be very well observed in Fig. 2.16. Therefore, the loading factor for the precursors during the RSD step will be directly comparable to the calibration runs performed on blanket layers. This holds for both processes (MOSFETs and TFETs)

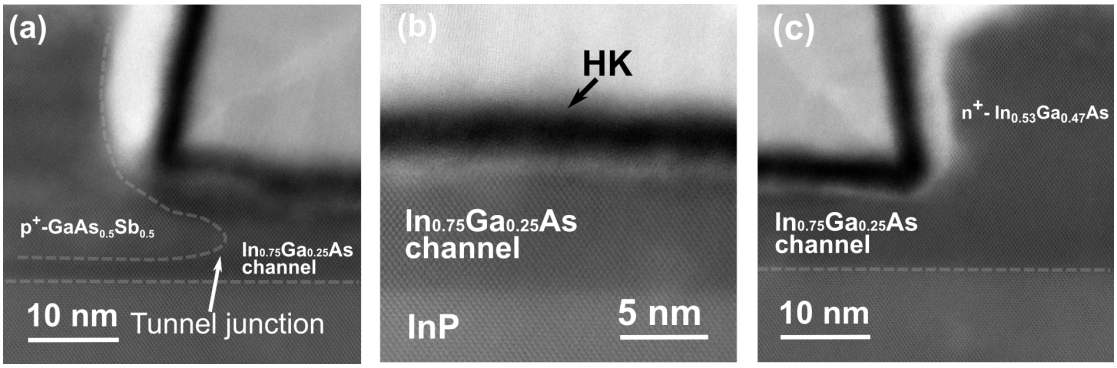


Figure 2.18 – High-resolution STEM pictures showing the (a) source/channel tunneling junction (b) gate-oxide/channel and (c) channel/drain interfaces. The tunneling junction is highlighted by a dotted gray line and it is formed by selective removal of InGaAs channel portions and regrowth of doped GaAsSb.

previously described, obviously only whenever the III-V layer is obtained by DWB.

In all the growth runs we keep the V/III ratio at the constant value of 0.9. The precursors used are trimethylgallium (TMGa), tertiarybutylarsine (TBAs) and trimethylantimony (TMSb). The obtained GaAsSb layers quality is characterized by high-resolution x-ray diffraction (XRD). $\omega - 2\theta$ angle scans around the (004) reflection are performed (Fig. 2.20). The peak with highest intensity corresponds to the (004) reflections of the InP substrate. The other peaks refer to GaAsSb layers grown under different conditions and from their angular position it is possible to extrapolate the layer lattice parameter.

First we performed several runs at 550 °C (only one representative shown in Fig. 2.20a). The precursor flow was slightly varied at each run, targeting the lattice match condition. However, all the trials would result in either an Sb-rich (left-shifted peak) or As-rich (right-shifted peak) layer. When decreasing the growth temperature by only 25 °C (2.20b), the layer results As-rich but we obtain a better layer roughness (not shown). This is a sign that the optimum spot might be close. By slightly reducing the As flow and increasing the Sb (constant V/III = 0.9) the layer peak results to be almost aligned with the substrate and an excellent layer roughness is obtained. Once we have achieved a reasonable material lattice-matching and quality, the p-type doping must be incorporated.

2.4.3 Zn-doped GaSb

The effect of p-type doping on GaSb surface morphology have been investigated on 3 inch semi-insulating GaAs (001) substrate with 97 nm of unintentionally-doped GaSb grown by molecular beam epitaxy (MBE). The substrates were provided by University of Glasgow. The highly resistive starting heterostructure substrate is ideally suited for evaluation of doped GaSb epitaxial layers. Shortly before the growth, the surface

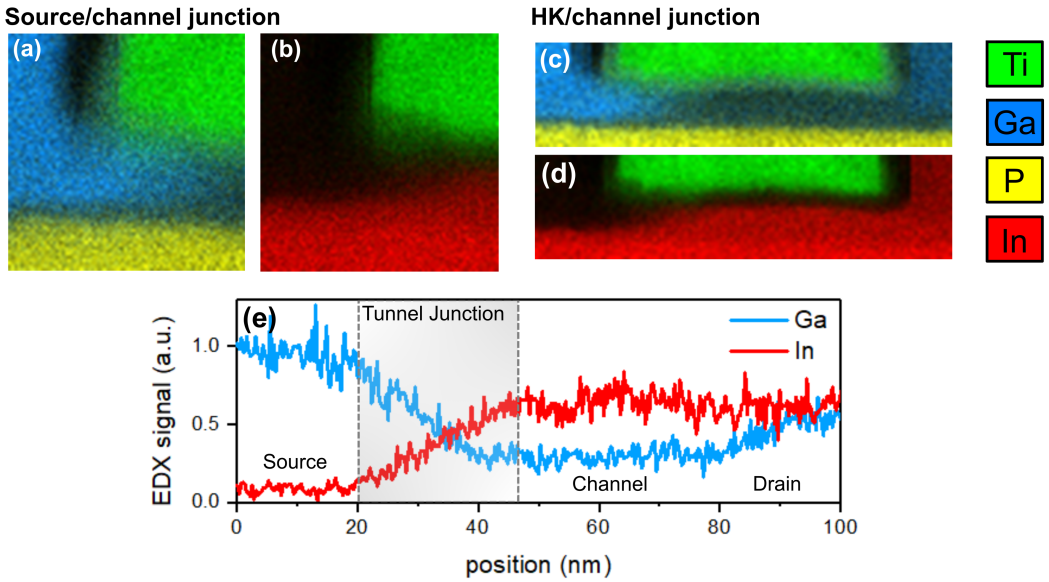


Figure 2.19 – EDS elemental analysis maps showing the material composition at the (a-b) source/channel tunneling junction and (c-d) gate-oxide/channel interface. (e) EDS signal profile from the GaAsSb source to the InGaAs drain. The different Ga composition marks the three TFET main regions and highlights the position of the tunneling junction.

is prepared with a wet chemical cleaning process. The die is dipped in HCl:H_2O (1:5) solution for 4 min, rinsed in H_2O and IPA, blow-dried using a nitrogen flow and immediately loaded into the MOCVD reactor. For this doping series, we set the growth temperature to 550 °C and select a V/III of 1. The p-type dopant used is diethylzinc (DEZn). The resulting deposited film shows a smooth morphology throughout the explored Zn doping range, with some Sb crystals appearing aligned along the <0-10> direction. The samples surface topography is analyzed using AFM, as shown in Fig. 2.21. Doping concentration and carrier densities are measured through Hall measurements in Van der Pauw configuration. The obtained results are in good agreement with studies reported elsewhere [91]. The encouraging finding is that no material degradation is observed at higher doping densities.

2.4.4 Etching of Sb-based compounds

Sb-based compounds are known for being sensitive to oxidation agents and to most of the common wet etching solutions available in micro fabrication. This represents a problem for several FET process steps, such as the removal of oxide layers. In this section we analyze possible ways to safely etch SiO_2 selectively to GaSb. In Fig. 2.22, a GaSb platelet structure fabricated with TASE and still protected by the template oxide is displayed. To assess the starting material quality and debug every possible

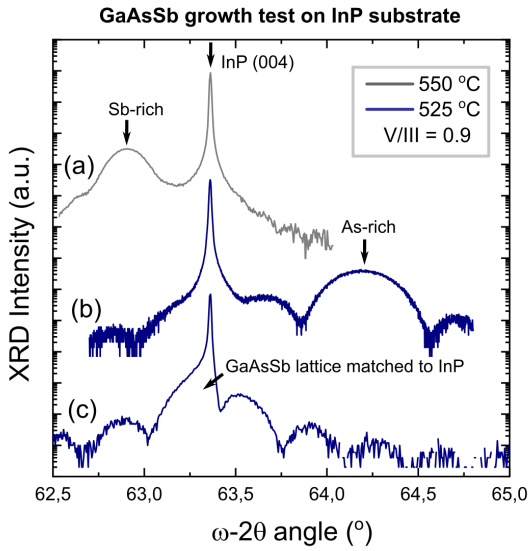


Figure 2.20 – X-ray diffraction (XRD) $\omega - 2\theta$ angle scans around the (004) reflection of InP substrate. The side peaks refer to the GaAsSb layer grown by MOCVD. The goal of this growth study is to obtain lattice-matching between GaAsSb and InP (translating into lattice matching with InGaAs). The optimum growth conditions are achieved in (c).

crystal damaging contribution, high-resolution TEM cross-sectional analysis is done right after the growth (Fig. 2.22b,c). A crystalline GaSb platelet is achieved inside the SiO_2 cavity, as also confirmed by previously published results on high-mobility GaSb nanostructures [76, 92]. To remove the oxide template, several HF etching solutions have been tested, such as buffered HF, diluted HF and a solution containing ethanol. As shown in Fig. 2.23, they are all causing serious material damages. Moreover, the etching effect is more pronounced in presence of an heterojunction such as InAs/GaSb, a phenomenon that can be attributed to the presence of electrochemical etching reactions. These results show that wet-etching is not a feasible option for GaSb processing. The next experiment is performed using only RIE (CF_4-O_2 gas mixture) to etch 100 nm of SiO_2. To a first inspection by SEM, the GaSb surface appears smooth and without physical damages. However, a deeper analysis performed by TEM, revealed the presence of polycrystalline/amorphous regions (Fig. 2.24).

The lack of a safe process to remove an oxide from the GaSb surface, makes any TASE-based approach unsuitable for this material, or at least for those devices where removing the template oxide is unavoidable. Same applies to DWB, when the active device layer is GaSb. Despite GaSb p-FETs are extremely interesting devices for complementary full-III-V technology (due to the high hole mobility in Sb-based compounds) they are not practically suitable for the integration in a lateral, CMOS-compatible flow, due to the several processing challenges just illustrated. Nevertheless,

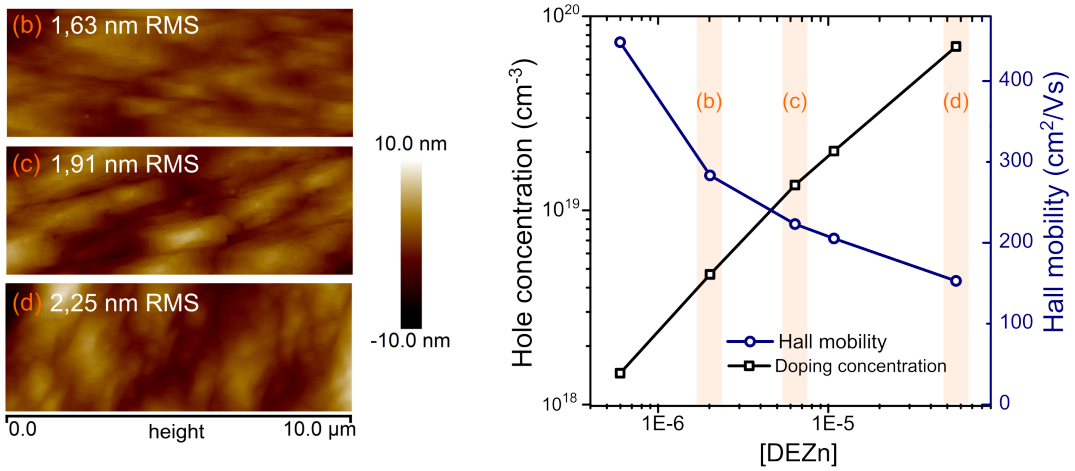


Figure 2.21 – Doping calibration performed on GaSb blanket layers grown on GaAs substrates. Three different runs (a,b,c) are characterized both by AFM and Hall measurements. No material degradation is observed for the highest Zn doping concentration where a mobility of 150 cm^2/Vs and a doping density of 7×10^{19} cm^{-3} are achieved.

a careful device process design enabled the successful fabrication of InGaAs/GaAsSb heterojunction TFETs. In fact, in the TFET flow previously described, the GaAsSb source is deposited just before the RMG process and the material stays protected underneath the inter-layer dielectric oxide. The source contact is accessed by opening small vias (while the channel area is protected) using exclusively a dry etching process. The absence of crystal damages in the source contact region is assessed with TEM analysis on a TFET device. As shown in Fig. 2.25, the GaAsSb appears purely crystalline already 2 nm away from the interface with the W contact via.

In this section we have described the technological aspects of the designed TFET fabrication flow and its most important features:

- the tunnel junction can be self-aligned with respect to the gate, by selective regrowth of the source material after the gate formation. The **self-alignment** is a key enabler for high performance TFETs, since it reduces the *SS* degradation caused by parasitic tunneling at the junction interface [83];

- InGaAs **MOSFETs** and InGaAs/GaAsSb **TFETs** are experimentally demonstrated **on the same Si substrate** with a parallel optimized process, differing only in the source material.

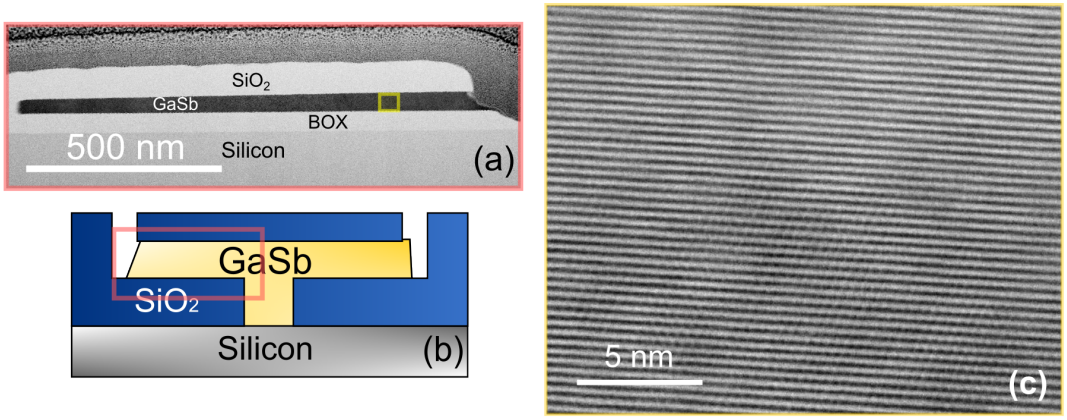


Figure 2.22 – (a) TEM cross-section of a GaSb platelet surrounded by an oxide template. The cavity overview is illustrated in (b). A zoom-in on the GaSb reveals a crystalline material. This characterization is done to assess the material quality before the process starts.

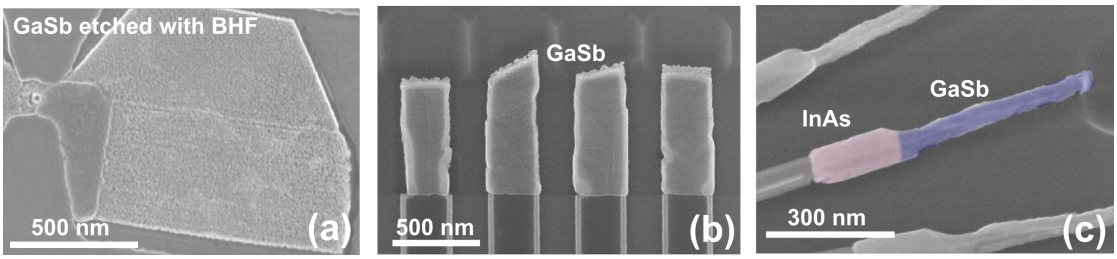


Figure 2.23 – (a-c) Examples of GaSb structures featuring evident material damages after exposure to different HF-based solutions. The effect is particularly visible in (c), where the InAs segment results immune to the HF etching, in contrast to the evidently eroded GaSb.

2.5 3D Sequential Integration

2.5.1 Industrial interest in 3D sequential integration

The need for high performance and aggressive scaling is shifting the industrial interest towards 3D geometries such as Tri-Gate or FinFETs and, in a near future, stacked nano-sheets. But very compact and power-efficient chip designs can be achieved by exploiting the third dimension at different levels, without need to scale the individual modules [11, 12]. Single transistors or alternatively 2D standard cells can be stacked in different layers that are vertically connected. 3D integration can enable "more than Moore" approaches, such as the heterogeneous integration of different functionalities, including electronics, sensing, radio-frequency, photonics and optoelectronic components, and each layer can be somewhat independently optimized for specific processes. Three major routes can be identified in 3D integration:

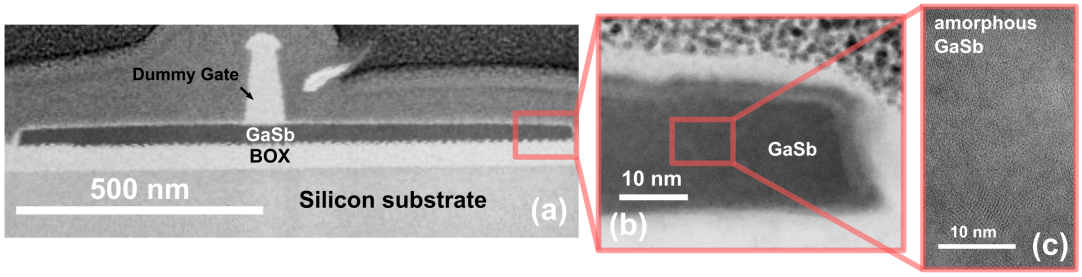


Figure 2.24 – STEM cross-section of the GaSb platelet grown by TASE after exposure to a reactive-ion-etching (RIE) process. The presence of amorphous region is revealed by a closer look inside the material (b-c). RIE is used to remove the SiO_2 template, since wet-etching cannot be used. We attribute this crystal damage to the physical action of ions during the dry etching process.

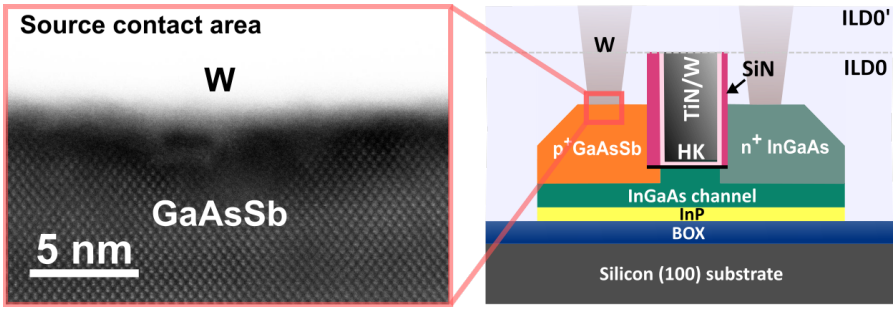


Figure 2.25 – TEM zoom-in on the interface between GaAsSb and the W plug, in the source region. As part of the new, optimized TFET process, the GaAsSb appears perfectly crystalline and unaffected by the transistor fabrication.

- **3D-IC packaging**, including the staking of different dies with wire bonding or of several packaged ICs. This is the most mature technology and it is already commercialized through several products.
- **Parallel 3D-IC integration**, where the different chips vertically integrated are connected using through silicon vias (TSV), a breakthrough invention for 3D integration. TSV offers a serious advantage in terms of electrical performance, power consumption, area density and form factor.
- **3D-silicon integration** or **3D sequential integration (3DSI)** consists in the wafer-to-wafer stacking, also in this case making use of TSV connections. The whole ICs are processed in a continuous fashion, and most importantly each layer shares the same alignment marks. Thermal budget compatibility between different tiers might represent an issue that needs to be addressed.

TSMC, one of the biggest players in the semiconductor business, has planned the production of 3D IC technology chips by 2020 while Samsung has recently demonstrated

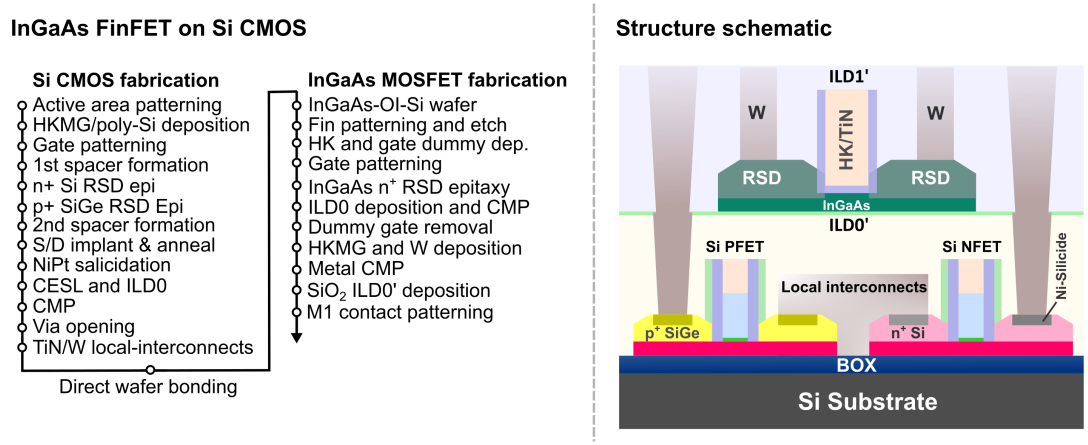


Figure 2.26 – Process flow schematic describing the fabrication of InGaAs MOSFETs sequentially integrated on a Si CMOS device layer. The thermal budget limited to 520 °C, required for the InGaAs processing, is perfectly compatible with the Si bottom layer and does not induce any performance degradation.

the first 12-Layer 3D-TSV chip packaging technology. Therefore, the industrial interest in this direction is clear. Parallel TSV integration is limited by the layer alignment accuracy, and the TSVs need to be designed large enough to compensate for this, thus limiting the maximum area density. 3D sequential integration allows instead to further decrease the vias pitch and diameter since the alignment of different levels has the same accuracy as achievable in 2D. The challenge of such a scheme is to make sure that the top layer fabrication does not have any impact on the bottom devices performance. A clever process design implies a decreasing thermal budget from bottom to top. In the next section an example of an integration approach addressing this issue will be described.

2.5.2 InGaAs-on-CMOS: 3D direct wafer bonding

A typical Si FET processing can reach a thermal budget of about 1000 °C but the transistor stability can be preserved only around 400 °C, that is approximately the thermal budget of the metallization process. Therefore, a Si 3DSI platform would be seriously affected by bottom layer performance degradation. III-V semiconductors are characterized instead by a processing thermal budget of 520 °C hence III-V FETs may be fabricated on top of a Si or SiGe CMOS wafer. The DWB integration method described in the previous sections is a key-enabler of this technology. With DWB, large-area wafers integration can be achieved, exploiting a bonding temperature of only 250 °C. In this work we have fabricated a 3DSI stack made of InGaAs FETs on top of fully-depleted SOI (FDSOI) CMOS layer, provided by CEA LETI institute.

A process flow and structure schematic describing the fabrication of the 3D plat-

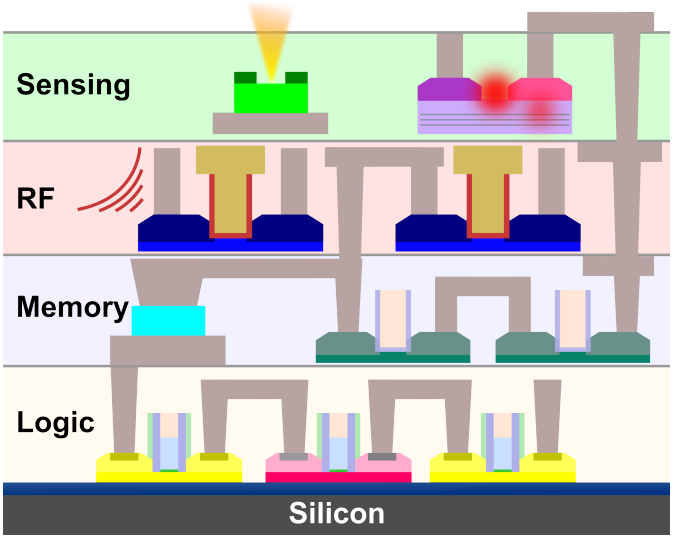


Figure 2.27 – Schematic illustration of a potential 3D sequentially integrated stack of different devices and functionalities, including sensors, RF modules, memories and logic components.

form is shown in Fig. 2.26. TiN/W TSVs are used to electrically connect the two levels, whereas local interconnects are located in the bottom layer. A standard gate-first process is used to fabricated the Si CMOS in the first tier. A comprehensive description of the process is reported in [93]. The starting substrate is an SOI wafer where the active device area is patterned first. Hence the gate stack comprising HK dielectric, metal gate and poly-Si is deposited on the obtained structures. After the gate spacers are formed, RSD is carried out in two steps to obtain p^+-SiGe and n^+-Si contacts. Doping implantation and silicidation are performed to obtain highly doped contacts. An inter-layer dielectric is deposited, planarized by CMP such that vias filled with TiN/W metal can access the RDS regions and form the 3D inter-layer contacts. Subsequently, a second oxide layer (ILD0') is deposited and planarized to host the bonded III-V layer. As mentioned in Section 2.2.1, the hosting substrate layer roughness needs to be minimized in order to obtain a good layer quality. DWB is hence used to transfer a 20 nm thick InGaAs layer on the Si CMOS wafer. The InGaAs FETs are processed as described in Section 2.4. The only relatively high-temperature step is the InGaAs RSD, performed at 500 °C. The electrical characterization shown in the next chapters will evaluate the impact of the top layer processing on the bottom devices performance.

2.6 Conclusion and Outlook

Several aspects concerning the integration of compound semiconductors on silicon are first addressed. Both DWB and TASE techniques are used to experimentally demonstrate III-V electron devices. A standard RMG process is used to fabricate MOSFETs (planar and FinFETs). The flow is described in detail and each critical process module is highlighted. The formation of doped contact extensions using a digital etching process enables improved performance: an R_{acc} as low as 220 Ωμm is achieved in the InGaAs FinFETs. We also conclude that a misalignment of only 1 nm results in 100 Ωμm increase of R_{acc}. The same module is adapted to enable the *fabrication of a self-aligned TFET*. The challenges related to epitaxial growth of GaAsSb on InGaAs are described: this is needed to fabricate the self-aligned TFET source contact. Moreover, blanket layer analysis reveals that the GaSb surface does not degrade with increasing Zn-doping concentration. Finally, a solution to overcome Sb-based compound etching sensitivity is presented. *The designed process has enabled the co-planar integration of III-V MOSFETs and TFETs on the same substrate, without additional processing.*

Recent trends in 3D integration are explored with a special focus on 3DSI. The benefits of DWB combined with the low thermal budget that characterizes III-V processing, makes it an ideal system for 3DSI of III-V FETs on Si CMOS. This concept is demonstrated with a platform realized in collaboration with CEA LETI institute. The possibilities offered by this process can be further exploited by combining more than just logic functionalities: RF devices, optoelectronic, sensing units as well as memories can be envisioned as different levels of a unique 3D technology platform (Fig.2.27).

3 III-V MOSFETs

3.1 Introduction

The electrical characterization of replacement metal-gate (RMG) InGaAs FinFETs integrated on silicon is discussed in this chapter. We analyze the impact of several process modules introduced in the previous chapter, targeting off-state performance improvement. A major goal of this work is to bridge the performance gap between commercial silicon technologies and high-performance III-V devices fabricated on native substrates. The integration aspects play a crucial role, since implementing a CMOS compatible flow on an external substrate implies the use of modules not necessarily tailored for III-V materials. The same device architecture is then pursued within a 3D sequential integration scheme. The InGaAs FinFETs are part of a 3D stack, where the bottom layer consists of a Si CMOS functional substrate. The impact of the top-layer processing thermal budget on the lower tier is evaluated with electrical measurements. Finally, InGaAs FETs are demonstrated using a more exploratory integration approach, namely template-assisted selective epitaxy (TASE). Both RMG and gate-first (GF) device architectures are demonstrated and compared.

3.2 High-performance InGaAs FinFETs by Direct Wafer Bonding

3.2.1 Floating body effect in scaled III-V FETs

Ultra-thin-body (UTB) channels, silicon-on-insulator (SOI) technologies and 3D channel architectures represent the ultimate solutions to meet the target performance requirements, in terms of electrostatic control and current densities. SOI technology is particularly suitable for analogue and mixed signal applications, providing reduced junction capacitance [94]. However, the presence of a buried oxide (BOX) back-barrier in UTB MOSFETs (3.1) is responsible for the so-called floating body effect (FBE), the

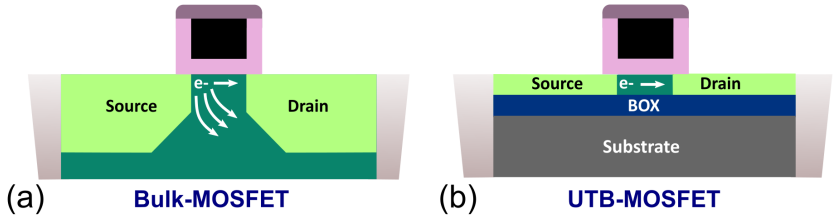


Figure 3.1 – Illustration schematic highlighting the differences between bulk-MOSFET and an ultra-thin body SOI technology. Due to the isolation from the substrate the latter can provide ideal conditions for analog and mixed signal applications, where low junction capacitances are necessary. On the down side, SOI-like technologies are more sensitive to floating body effects.

major parasitic effect in SOI MOSFETs. The floating body nature of these devices leads to the accumulation of positive charge – generated at the channel-drain interface – in the transistor body. FBE can cause device instability, high OFF-state leakage current and anomalies in the subthreshold slope. Moreover, carrier accumulation in the channel may trigger a positive feedback mechanism called parasitic bipolar effect (PBE): the source, body and drain of the MOS structure form the emitter, base and collector respectively of a bipolar junction transistor (BJT), as schematized in Fig. 3.2d. A strong electric field is present at the channel-drain interface and it is highly localized in proximity of the gate-to-drain overlap region, particularly at high drain bias. Impact ionization and band-to-band tunneling (BTBT) can likely occur and create electron-hole pairs that are injected into drain and channel respectively. The off-state injection of electrons in the drain is known as gate-induced drain leakage (GIDL), and it is pronounced in scaled architectures and/or low band gap channel materials. The resulting substrate current lowers the potential in the transistor body and contributes to the drain leakage current.

Due to the small energy band gap, scaled InGaAs MOSFETs are strongly affected by PBE [95, 96, 97]. In fact, although InAs-rich InGaAs is notably interesting due to its higher mobility, the enhanced sensitivity to leakage mechanisms needs to be carefully considered. An extensive 2D TCAD simulation analysis reported in Sant *et al.* [79] – based on our InGaAs MOSFETs experimental results – identifies three major leakage sources in scaled III-V FETs. As schematized in Fig. 3.2a, BTBT and source-to-drain-tunneling (STDT) occur across the transistor body and both contribute to electron injection in the drain. Furthermore, BTBT induces as well accumulation of holes in the channel that lower the potential in that region and activate the PBE (Fig. 3.2)c. Additional electron-hole pair generation occurs through trap-assisted-tunneling (TAT) at the InGaAs/gate-oxide interface (Fig. 3.2b). In the MOSFET off-state, the band bending at the gate-drain overlap region forms a triangular potential well and

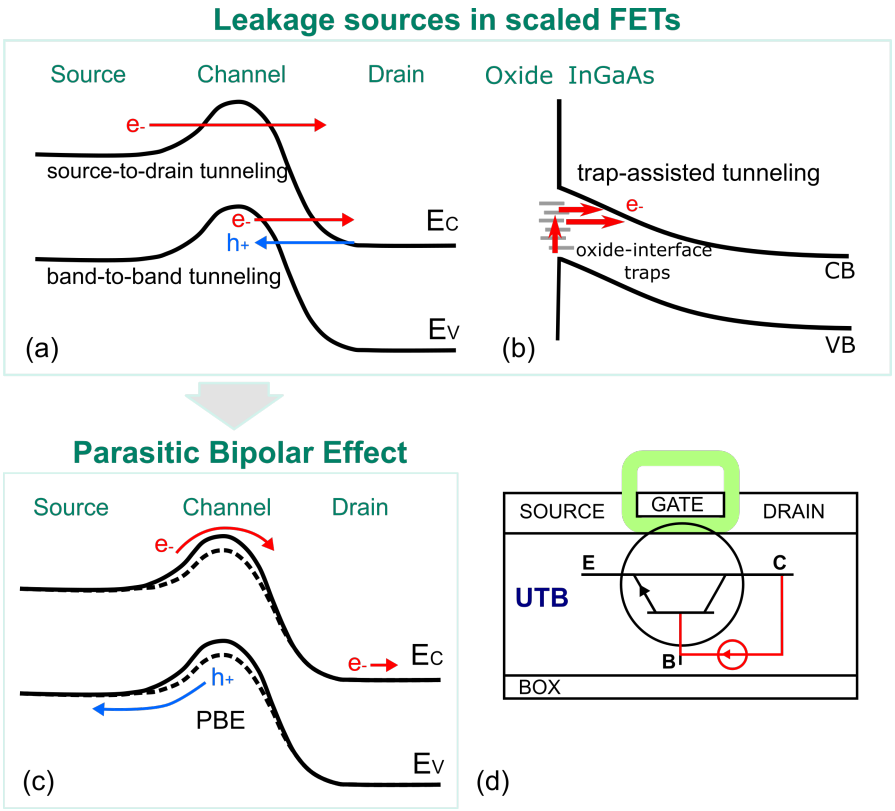


Figure 3.2 – Schematic band diagrams representing leakage sources in scaled MOSFETs. (a) Source-to-drain, band-to-band and (b) Trap-assisted tunneling contribute to the creation of a leakage off-state current. (c) The parasitic bipolar effect results from the accumulation of holes inside the channel that lower the body potential and contribute to the gain of a parasitic bipolar junction transistor (d).

electrons can be excited through multi-phonon excitation processes into traps located in the band gap and then reach the conduction band. To summarize, BTBT, STDT and TAT are all responsible for off-state conduction in scaled InGaAs FETs. Several countermeasures have been proposed to mitigate these effects. Source and drain band gap engineering through the use of dopant grading would enable lowering the peak of the electric field along the drain/channel interface and, therefore, reducing BTBT. TAT instead, can be partially suppressed by implementing thick oxide spacers between the gate oxide and the drain contact, as schematized in Fig. 3.3a. An estimated spacer thickness of 10 nm would prevent the formation of a triangular potential well and hence reduce the off-current (Fig. 3.3b). As counter effect, additional series resistance could negatively impact the on-current. Following these guidelines, spacers and doped extensions have been introduced in the scaled InGaAs FETs process flow presented in this work [80, 98]. While the technological details have been provided in the previous chapter, their impact on the electrical performance will be discussed in

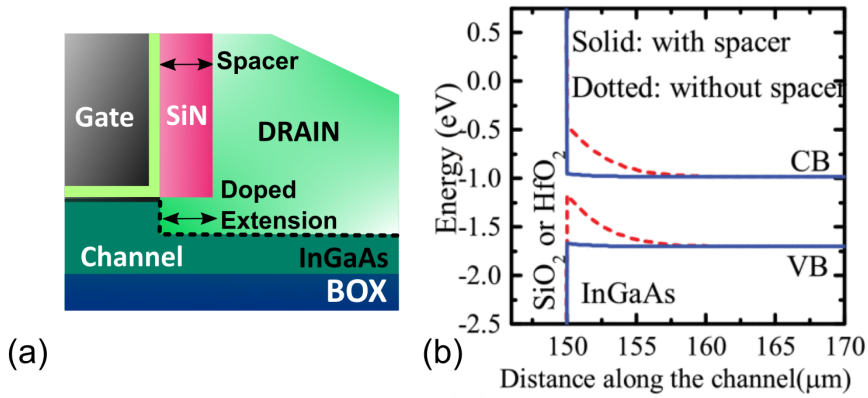


Figure 3.3 – (a) Schematic representing the drain side of a MOSFET with SiN spacers and doped extensions. (b) Band-edge diagram along the drain side showing the effect of spacers on the triangular potential well. Adapted from [79].

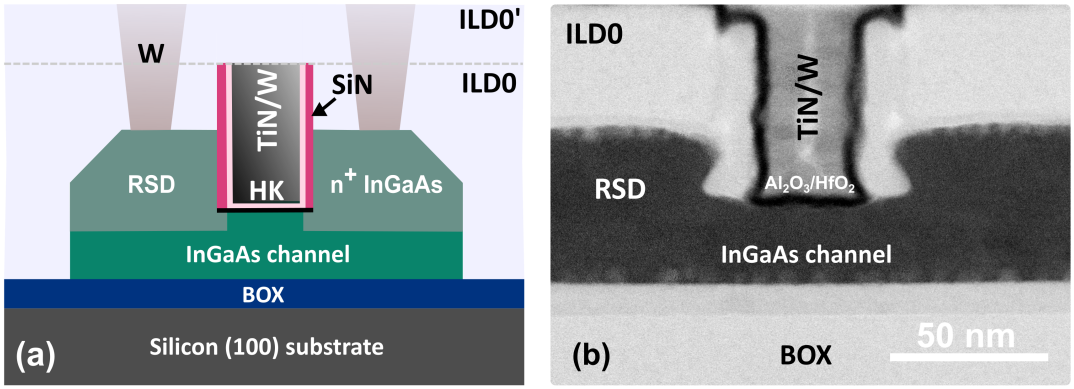


Figure 3.4 – (a) Schematic illustration of the fabricated InGaAs MOSFETs following the DWB integration scheme. (b) High-resolution STEM cross-section schematic of an InGaAs FinFET with gate length of 20 nm, 10 nm SiN spacers and doped extensions.

the following sections.

3.2.2 Bonded InGaAs FETs: device architecture overview

To fabricate the InGaAs MOSFET presented in this section, a 20 nm thin channel layer is transferred on a silicon (100) substrate using direct wafer bonding (DWB). The RMG device fabrication flow is described in Section 2.4. As illustrated in the structure schematic in Fig. 3.4a, the fabricated device features RSD, doped extensions, and source-drain spacers. Fig. 3.4b shows a high-resolution STEM cross-section image of a transistor with a gate length (L_G) of 20 nm, 10 nm source-drain spacers, and a scaled gate-oxide bi-layer composed of Al_2O_3/HfO_2 (EOT ~ 1 nm). The excellent crystal qual-

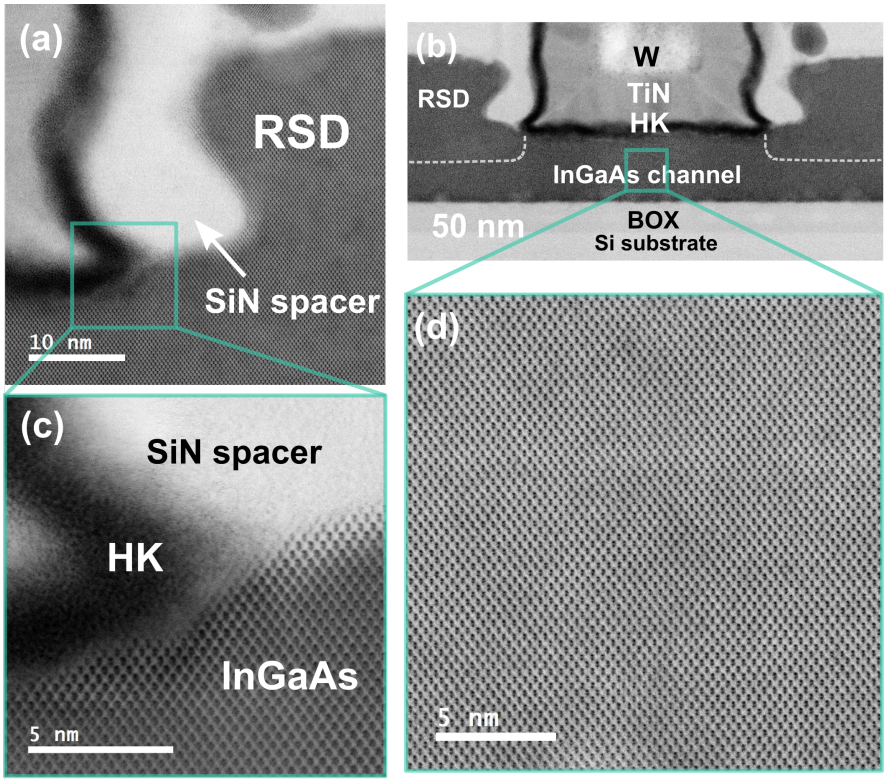


Figure 3.5 – STEM images of the InGaAs MOSFET (a) drain side and (b) HK/drain/channel corner. The atomic resolution assesses the excellent InGaAs material quality. A zoom-in inside the channel as shown in (c) is reported in (d).

ity inside the channel and at the contact regions is further assessed in Fig. 3.5. In this case, the junction between the channel and the RSD region cannot be distinguished in the TEM image. The high device yield provided by DWB method allows to study the impact of the geometrical parameters on the transistor performance. In the next sections, results from both planar and FinFET devices are reported, with nominal L_G ranging from 10 nm to 300 nm. Devices featuring fin widths (W_{FIN}) between 10 nm and 400 nm are also fabricated. All the shown measurement data are normalized by the gate periphery of the fins.

3.2.3 Impact of source-drain spacers on the off-state

As described in section 3.2.1, the use of gate sidewall SiN spacers is expected to mitigate TAT at the gate-oxide/channel interface and therefore decrease the I_{OFF}. A set of transistors featuring three different spacer thicknesses has been investigated (no spacers, 4 and 10 nm). All data shown in the following are normalized to the gated periphery of the fins. In Fig. 3.6a, the I_{OFF} – defined as the minimum drain current I_D – is plotted versus different L_G, for an InGaAs n-FET with W_{FIN}=25 nm. At L_G = 100 nm,

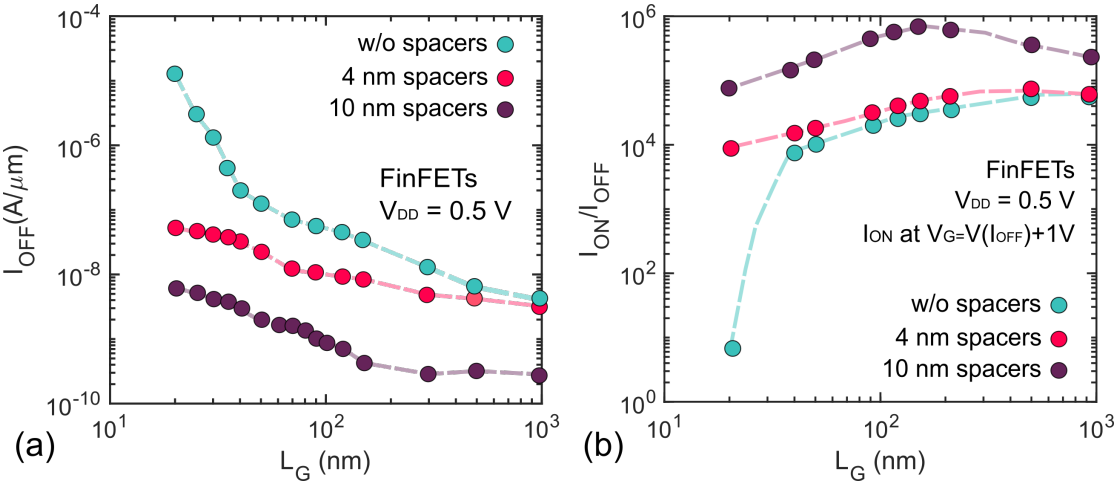


Figure 3.6 – (a) I_{OFF} and (b) I_{ON}/I_{OFF} versus L_G for devices with different spacers thickness. About three orders of magnitude improvement in I_{OFF} is achieved for scaled FinFETs with 10 nm spacers. The I_{OFF} generally increases at smaller L_G. A good on-off ratio is preserved due to the SS improvement near the I_{OFF} target. Adapted from [80].

an I_{OFF} one order of magnitude lower is achieved with 10 nm spacers compared to 4 nm and of two orders of magnitude with respect to the case without spacers. For the short-channel devices instead (e.g. L_G = 20 nm), the I_{OFF} improvement increases to three orders of magnitude. We can observe that in all cases the I_{OFF} increases at scaled L_G, in accordance with what has been reported in similar works [99]. To explain the higher I_{OFF} in short-channel devices, two aspects must be considered:

- The current gain of a bipolar junction transistor (BJT) increases with decreasing base length, in this case L_G, hence the described leakage mechanisms are further amplified at smaller dimensions.
- STDT is most dominant in short-channel devices due to the smaller tunneling barrier.
- In long-channel devices BTBT takes place mostly in the extrinsic drain region where PBE does not affect the field distribution. The coupling between BTBT and PBE is stronger in short-channel devices.

The use of sidewall spacers can negatively impact the I_{ON}, due to access resistance (R_{access}) increase. As discussed in Chapter 2, raised source-drain extensions have been implemented in our InGaAs FETs process to minimize the presence of ungated channel area. For the devices with 10 nm spacers, an R_{access} of 220 Ωμm is obtained. Similar values are achieved for the 4 nm spacer devices (210 Ωμm) and without spacers (200 Ωμm). These result indicate that the use of doped extensions effectively prevents any increase of R_{access}, although still allowing to enhance the off-state performance.

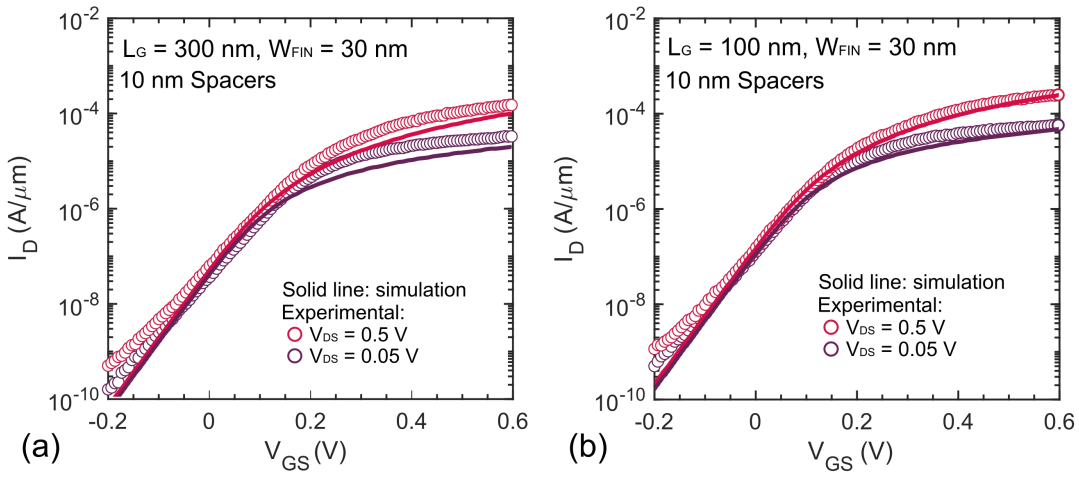


Figure 3.7 – Transfer characteristics of InGaAs FinFETs with (a) L_G = 300 nm and (b) L_G = 100 nm. Both devices feature 10 nm spacers. Solid lines show 2D TCAD simulations while symbols refer to experimental data. An excellent matching is achieved among the two. Adapted from [80].

In Fig. 3.6b, I_{ON}/I_{OFF} ratio for FinFETs with and without spacers is displayed versus L_G. In this case I_{ON} is defined as I_D at $V_{GS} = V_{GS}(I_{OFF})$+1 V and V_{DS} = 0.5 V. One order of magnitude improvement for the devices featuring 10 nm spacers is achieved compared to the case with no or thinner spacers, and for the shortest L_G the ratio further increases. Long-channel devices without spacers have higher I_{OFF} balanced by an increase in I_{ON}. Overall, thanks to the implementation of carefully designed source-drain spacers, combined with doped extensions, an optimized trade-off between on and off-state performance is demonstrated across several gate lengths.

2D TCAD simulations have been carried out in collaboration with ETH Zurich. InGaAs FinFETs are modeled as nanowire-FETs in 2D using Sentaurus-Device with cylindrical coordinates. A comprehensive description of the simulation set-up is available in [79]. Fig. 3.7a shows a transfer characteristic of a FinFET featuring L_G=300 nm and W_{FIN}=30 nm as well as 10 nm spacers. The gate metal work function has been adjusted to match the experimental data and it ranges from 4.65 to 5 eV. A very good match between experimental values (symbols) and simulated data (solid line) is achieved, both in the on- and off-state. A similar match is achieved for a device with L_G=100 nm (Fig. 3.7b). Fig. 3.8a shows transfer characteristics of a short L_G device (20 nm). Although also in this case a good match with simulated data is achieved, the presence of STDT mechanism at scaled dimensions (due to the narrower tunneling barrier) degrades the SS near the I_{OFF} target and slightly enhances the leakage current.

TAT is effectively suppressed by the use of sidewall spacers, and counter effects due to R_{access} are prevented through the implementation of doped extensions. Neverthe-

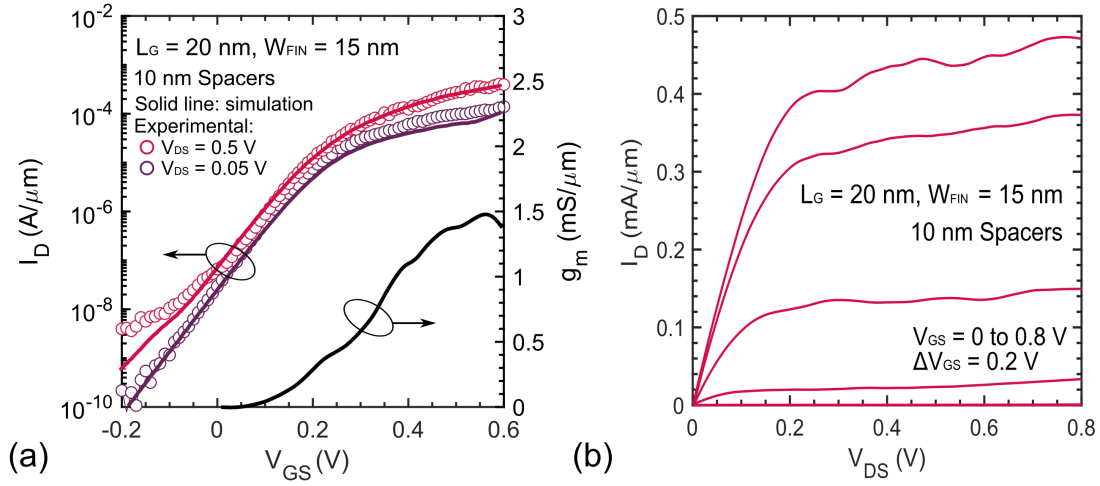


Figure 3.8 – (a) Transfer characteristics of InGaAs FinFETs with L_G = 300 nm and 10 nm spacers. This device exhibits record I_{ON} of 350 µA/µm at I_{OFF}=100 nA/µm and V_{DS}=0.5 V. g_m is plotted on the left axes featuring a peak value of 1.5 mS/µm. (b) Output characteristics for the same device showing low output conductance and R_{ON} of 300 Ω µm. Adapted from [80].

less, BTBT and STDT (the latter particularly in short-channel devices) are still present as a source of off-state leakage. Alternative technological solutions would be required to further suppress BTBT and STDT in scaled architectures. As suggested in [79], the use of dopant grading in source and drain is an example of how the peak of electric field at the channel/drain interface can be lowered, at the cost of I_{ON} reduction.

3.2.4 Bonded InGaAs FETs: logic performance

The DC electrical performance of the best fabricated devices is discussed and benchmarked in this section. The ambition of this work is to demonstrate that III-V-on-silicon FETs can outperform Si devices on the relevant metrics. In Fig. 3.8a, the transfer characteristic of a FinFET with L_G=20 nm and W_{FIN}=15 nm is reported. This device exhibits strong on-state performance with I_{ON}=350 µA/µm at I_{OFF}=100 nA/µm and V_{DS}=0.5 V. This value represents the highest reported on-current for CMOS-compatible III-V FinFET on silicon up to date. The same device shows drain-induced-barrier-lowering (DIBL) of 30 mV/V and inverse subthreshold slope (SS) in linear and saturation region of 74 mV/dec and 78 mV/dec respectively. Fig. 3.8b shows a well-behaved transistor output characteristic, featuring low output conductance and an on-resistance (R_{ON}) of 300 Ω µm. Moreover, the peak transconductance ($g_{m,peak}$) reaches 1.5 mS/µm, as shown in Fig. 3.8a. By further scaling down the gate length, excellent device performance is maintained. In Fig. 3.9a, transfer characteristic of an InGaAs FinFET with L_G=14 nm and W_{FIN}=25 nm is shown, the shortest gate length achieved. Here, an I_{ON}=300 µA/µm at I_{OFF}=100 nA/µm and V_{DS}=0.5 V is reported. A

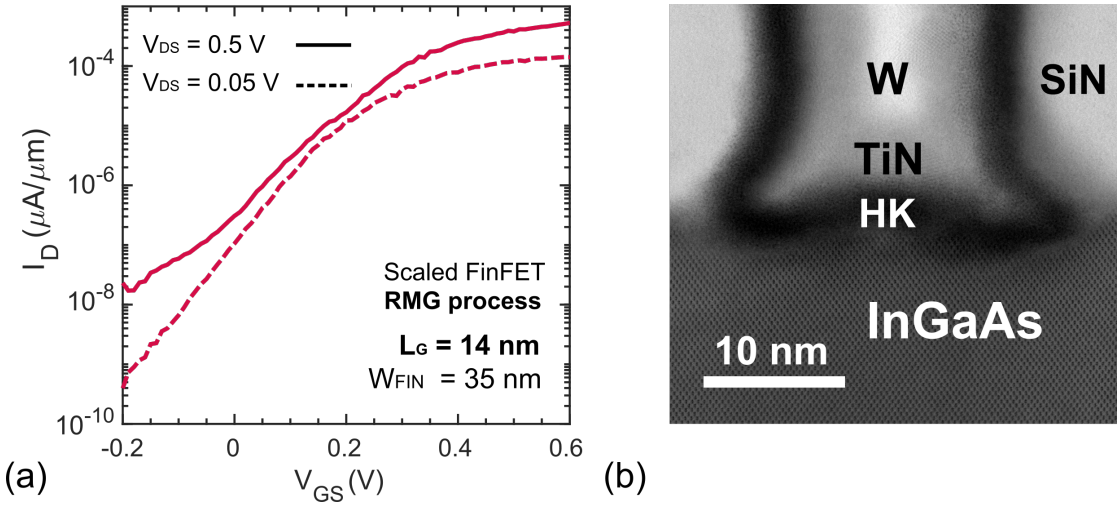


Figure 3.9 – (a) Transfer characteristic of scaled InGaAs FinFETs with L_G = 14 nm and 10 nm spacers. This is the shortest gate length demonstrated in this work. I_{ON}=300 µA/µm at I_{OFF}=100 nA/µm and V_{DS}=0.5 V is achieved. (b) STEM cross-section showing the ultra-scaled gate length.

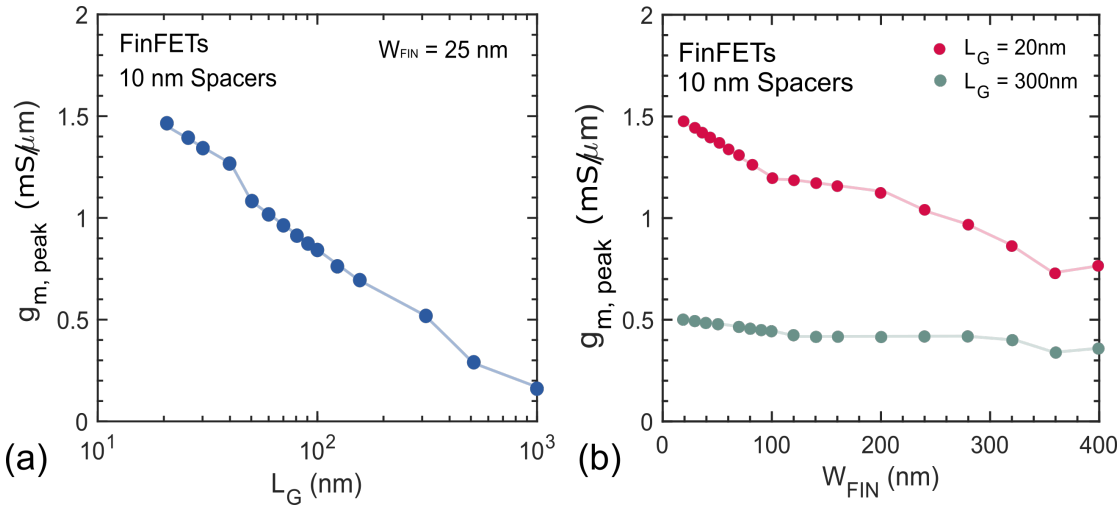


Figure 3.10 – (a) Peak g_m versus L_G and (b) W_{FIN} for InGaAs FinFETs featuring 10 nm spacers. Excellent scaling behavior is observed down to L_G = 20 nm. We can observe that for both long and short-channel devices g_m increases due to reduced g_d. Adapted from [80].

slightly higher I_{OFF} is obtained for the shortest L_G device, confirming the origin of the leakage mechanisms discussed in the previous section. Fig. 3.9b, shows a high-resolution STEM cross-section of the shortest gate length device. For these devices we estimate a field-effect mobility of about 500 cm^2/Vs, by approximating the gate capacitance. A summary of the best device performance is shown in table 3.1.

We now analyze the scaling behavior of the fabricated FinFETs and planar FETs. $g_{m,peak}$ is shown versus L_G and W_{FIN} in Fig. 3.10a,b. Both examples show excellent

Bonded InGaAs FinFETs	I_{ON}	SS_{LIN}
L_G = 14 nm, W_{FIN} = 15 nm	300 µA/µm	74 mV/dec
L_G = 20 nm, W_{FIN} = 15 nm	350 µA/µm	64 mV/dec
L_G = 100 nm, W_{FIN} = 30 nm	200 µA/µm	85 mV/dec

Table 3.1 – Summary of the best bonded InGaAs MOSFET devices. The on-current is calculated at I_{OFF}=100 nA/µm and V_{DS}=0.5 V

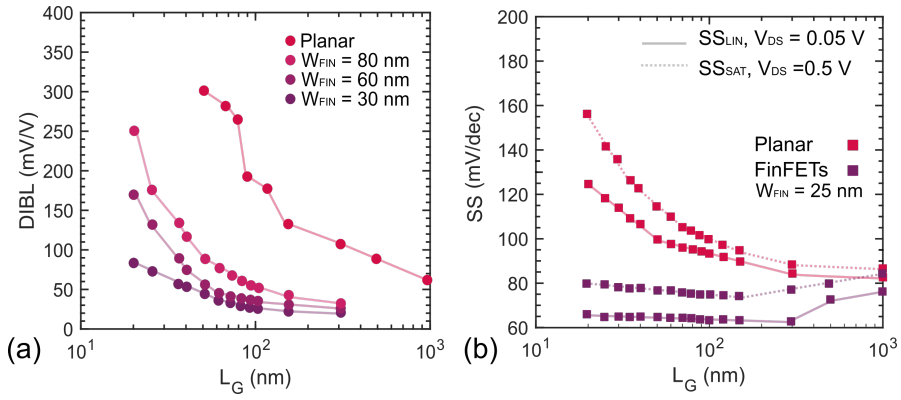


Figure 3.11 – (a) Drain-induced barrier lowering and (b) SS versus L_G comparing planar and FinFETs. A drastic improvement in electrostatic control is achieved for the FinFETs, less affected by short-channel effects. Adapted from [80].

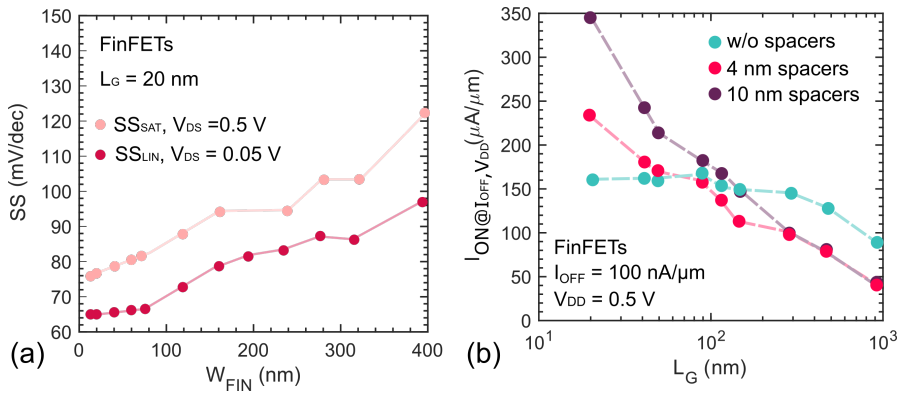


Figure 3.12 – (a) SS scaling versus W_{FIN} shows how device electrostatics would further benefit from fins scaling. (b) I_{ON} versus L_G featuring different spacer thicknesses.The use of spacers is beneficial as well for the on-state, allowing lower SS near the off-current target. Adapted from [80].

resilience against short-channel effects (SCE) down to the smallest dimensions. In Fig. 3.10b, the long-channel devices show a relatively flat $g_{m,peak}$, with a constant value of 0.5 mS/µm. Devices with L_G = 20 nm, instead, exhibit increased $g_{m,peak}$ for smaller fins. Although for scaled W_{FIN} it is expected that increased surface scattering would negatively impact the carrier mobility in the on-state, the observed increase in the

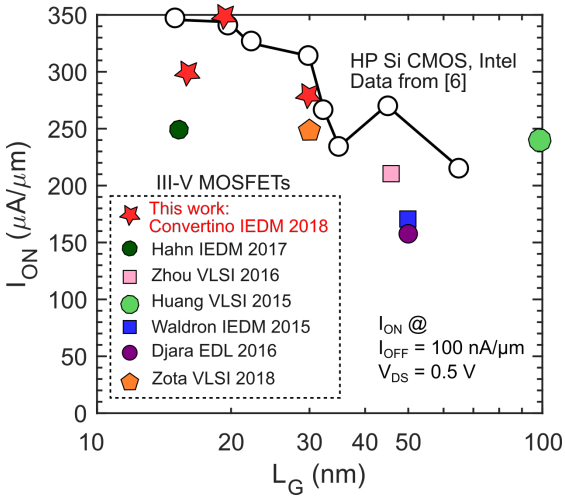


Figure 3.13 – Benchmarking plot comparing our InGaAs FinFET results to state-of-the-art competing III-V-on-Si technologies and to high-performance Si CMOS. We achieve record on-current values at three different gate lengths.

$g_{m,peak}$ can be explained with improved electrostatic control that results in decreased output conductance (g_D) and higher extrinsic g_m. $DIBL$ is plotted in Fig. 3.11a versus L_G for different W_{FIN} and for planar devices. The explained behavior is confirmed by the $DIBL$ improvement obtained with narrower fins. As a result, we can observe that L_G scalability is mostly limiting wider fin devices or planar FETs. Fig. 3.11b show SS in linear (SS_{lin}) and saturation (SS_{sat}) regions as function of L_G for different architectures. SS_{lin} reaches 65 mV/decade and SS_{sat} 78 mV/decade at the smallest gate length and fin width. While FinFETs demonstrate robustness against SCEs, planar devices show SS increase already below L_G=100 nm. Further W_{FIN} scaling would be beneficial to the subthreshold performance as can be seen from Fig. 3.12a. Finally, on-current scaling versus L_G is also considered, where I_{ON} is calculated at fixed I_{OFF}=100 nA/µm and V_{DS}=0.5 V (Fig. 3.12b). Here we again compare devices with and without spacers: The presence of gate sidewall spacers, as previously discussed, reduces the minimum I_{OFF} and improves the inverse subthreshold slope in proximity of the I_{OFF} target, enabling higher I_{ON} for the devices with 10 nm spacers. The results achieved in this work are compared and benchmarked in Fig. 3.13 against other III-V CMOS-compatible competing technologies [23, 25, 26, 29, 30, 100]. At the relevant high-performance technology nodes, namely the 28 and 14 nm our InGaAs FinFETs achieves an I_{ON} comparable with commercial Si CMOS devices [7].

In this section the DC performance of bonded InGaAs FinFETs has been discussed. Particularly we have achieved:

- 3 orders of magnitude **reduction of** I_{OFF} in the short-channel devices. This improvement can be partially attributed to the use of carefully designed source-

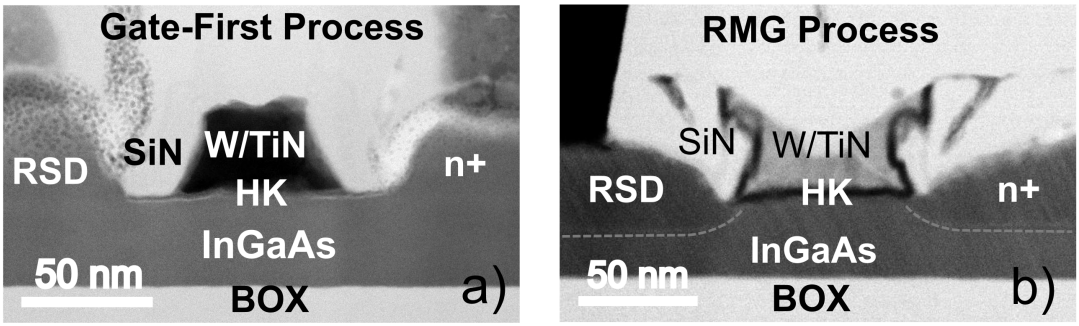


Figure 3.14 – STEM cross-section of InGaAs MOSFETs fabricated following a (a) gate-first (GF) and (b) replacement-metal gate (RMG) scheme. The latter features additionally doped extension regions. Both devices are obtained using TASE as integration scheme.

drain spacers that effectively reduce the electric field at the gate-drain interface;
- preserved **excellent on-off trade-off** due to the improved SS near the I_{OFF} target;
- **record on-current** performance for III-V MOSFET on silicon;
- the **smallest demonstrated InGaAs FinFET on silicon**, with L_G = 14 nm.

3.3 InGaAs FinFETs by Template-Assisted Selective Epitaxy

Selective epitaxy techniques are gaining increasing attention due to their ability to mitigate the formation of defects by confining the nucleation in smaller and predefined areas. Several examples of such techniques have been reviewed in the first part of the previous chapter (2.2.2). Although III-V on silicon integration is highly desired, cost and material quality remain major aspects that require consideration. Compared to DWB, local area growth methods eliminated the cost of expensive native substrates and limits the material growth volume to the quantity needed to fill the cavity. Moreover, several factors such as cavity shape and dimension, template oxide quality, seed cleaning etc. can drastically reduce the nucleation yield. Therefore, it is of extreme importance to carefully engineer these aspects. Although further efforts will be required to make these techniques suitable for industrial scale integration, we investigate in this work the suitability to advanced CMOS-compatible FinFET process. In this section we present the electrical characterization of InGaAs FinFETs fabricated with such technique, namely Template-Assisted Selective Epitaxy (TASE) [101].

3.3.1 TASE FinFETs: device architecture overview

The InGaAs MOSFETs are fabricated using TASE. A comprehensive description of the cavity fabrication is provided in 2.2.2. $In_{53}Ga_{47}As$ structures are grown by MOCVD, resulting in a channel thickness of 30 nm. To fabricate fins, there are two alternative approaches: directly patterning narrow cavities with a fin or nanowire shape or fabricating a micron-sized cavity and dry etching fins with the help of a hard mask. The former is the most desirable one since it does not expose the channel to any dry etching process that might induce crystal damage. However, it is also the most complicated due to the reduced cavity accessibility for the precursors at scaled dimensions. Although several demonstrations of directly grown nano-structures using TASE have been reported [27], further development would be required to reach a device yield compatible with the complex RMG process implemented in this work. Therefore, only results referring to dry-etched fins will be presented in the following section.

In Fig. 3.14, STEM cross-sections of the fabricated devices are shown. Both architectures feature source-drain sidewall spacers, RSD contact regrowth and high-k metal-gate (HKMG). In this experiment, two different CMOS-standard fabrication schemes are compared: replacement-metal gate (RMG) and gate-first (GF). GF used to be the most popular approach to build transistors, until a few technology nodes ago. Global Foundries, for instance, has been using GF process up to the 28 nm node and moving to RMG for further scaled technologies. What makes GF unsuitable for high-performance scaled nodes is essentially the HKMG exposure to high temperature steps, inducing several gate-stack long-term reliability issues. RMG on the other hand, uses a sacrificial dummy gate structure masking the channel during epitaxial contacts regrowth (as in the case of our process) or alternatively during source-drain doping implantation. The gate is deposited at the very end and replaces the sacrificial structure. This method enables higher flexibility in designing the device thermal budget as it will not affect the gate stack. RMG-like schemes come as well with some drawbacks. For instance, the metal deposited to fill-up the empty sacrificial gates needs to be planarized using chemical-mechanical polishing (CMP). The polishing can act differently on surfaces with dissimilar features, therefore, more restrictive design rules must be taken into account. In the next section, InGaAs GF and RMG FinFETs DC performance is discussed.

3.3.2 Replacement-metal-gate versus gate-first

The electrical performance of the fabricated TASE devices is investigated with DC measurements. Fig. 3.15a shows transfer characteristics of a GF InGaAs FinFET with L_G = 100 nm and W_{FIN} = 50 nm. This device features a $g_{m,peak}$ = 290 µS/µm and SS_{sat} = 190 mV/decade. The I_{OFF} current target of 100 nA/µm is hardly reached at high

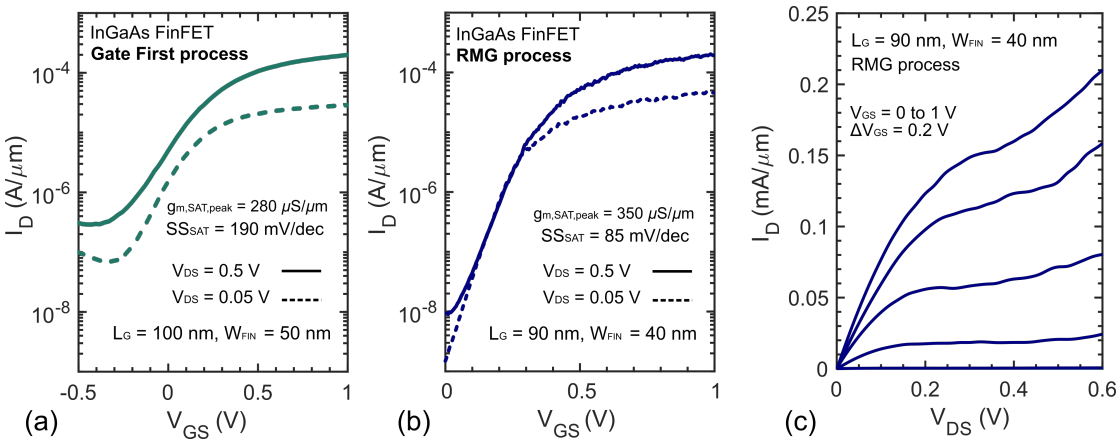


Figure 3.15 – Transfer characteristics of TASE-grown InGaAs FinFETs fabricated following a (a) gate-first (GF) and (b) replacement-gate (RMG) process. An overall improved performance is observed in the RMG device. A possible source of degradation in the GF process is the exposure of the high-k gate oxide to high temperature steps. (c) Output characteristic for the RMG FinFET. We extrapolate R_{ON} of 950 Ω μm.

TASE InGaAs FinFETs	I_{ON}	SS_{LIN}
L_G = 25 nm, W_{FIN} = 40 nm	70 μA/μm	95 mV/dec
L_G = 90 nm, W_{FIN} = 40 nm	100 μA/μm	85 mV/dec

Table 3.2 – Summary of the best TASE InGaAs MOSFET devices. The on-current is calculated at I_{OFF}=100 nA/μm and V_{DS}=0.5 V.

V_{DS}. This transistor clearly shows a weak off-state performance. The high SS and the higher gate leakage current level (not shown), can be attributed to the HKMG degradation occurring during the relatively high-temperature steps following the gate formation. Fig. 3.15b shows instead a device with comparable dimensions (L_G=90 nm and W_{FIN}=40 nm), fabricated using the RMG scheme. The FinFET shows $g_{m,peak}$ = 350 μS/μm, transconductance efficiency of 20 V^{-1} at 0.3 V and SS_{sat} = 85 mV/decade. As the device reaches the I_{OFF} target, we achieve an I_{ON} = 100 μA/μm. Although the device architecture is identical, the RMG transistor exhibits a stronger off-state performance, with a 50 % improvement in SS. The lack of exposure to thermally-induced HKMG damage results in less interface traps at the HKMG/channel interface. This impacts the on-state, as well as drastically improves the SS near the I_{OFF} target, resulting in higher I_{ON} and an I_{ON}/I_{OFF} ratio of 1×10^{-4}. Output characteristic for the same device is displayed in Fig. 3.15c. We measure an on-resistance (R_{ON}) of 950 Ω μm. The good off-state behavior of the RMG device can be partially attributed to the presence of doped extension regions, that are absent in the GF-FET. A summary of the best TASE InGaAs FinFET devices is available in Table 3.2.

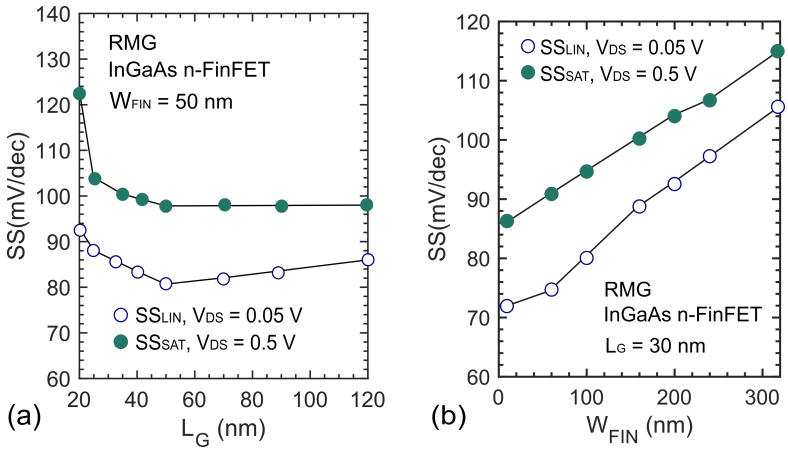


Figure 3.16 – *SS* scaling versus (a) L_G and (b) W_{FIN}, in saturation and linear region. Short-channel effects start revealing their presence below L_G = 30 nm whereas *SS* keeps improving with W_{FIN} scaling, a sign of enhanced electrostatic control.

3.3.3 TASE-grown InGaAs FETs scaling behavior

Average SS values versus L_G are shown in Fig. 3.16a, for RMG devices with W_{FIN} = 50 nm. Only for L_G smaller than 40 nm, SCEs start degrading both the linear and saturation *SS*. The same metric is plotted in Fig. 3.16b against W_{FIN}, for a set of devices featuring a gate length of 30 nm. Excellent fin dimension scaling is observed, meaning that there is a clear improvement in the channel electrostatic control and that further scaling should be explored. Fig. 3.17a,b show transfer characteristics of a short and a long-channel FinFET. The comparable *SS* assess the positive impact of scaling on the on-state performance, although a slightly higher I_{OFF} is obtained for the short-channel FinFET. The planar MOSFET characteristic displayed in Fig. 3.17c can be directly compared to the FinFET with the same gate length in Fig. 3.15b. Planar FETs feature a degraded SS due to the lower electrostatic control and also a lower I_{ON}.

Although the TASE-grown FinFETs show weaker performance than the devices fabricated by DWB and described in the previous section, the reported results still demonstrate a successful proof-of-concept of a complex CMOS-compatible, fully self-aligned process flow realized on III-V structures obtained with an exploratory technique such as selective area growth. Encouraging results following a similar approach have been also reported by Lee *et al.* [102]. As mentioned previously, the relatively low growth yield still represents a weak point of this method, limiting the statistical analysis that can be performed on the fabricated FETs. Nevertheless, this can be improved by further optimization specifically targeting the InGaAs material system.

In this section we have electrically characterized the InGaAs FinFETs fabricated using TASE, with the main achievements being:

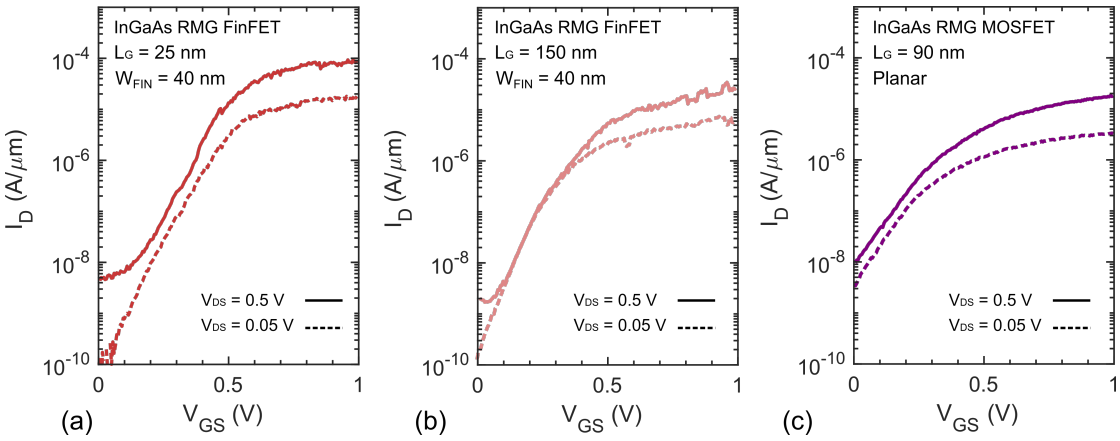


Figure 3.17 – (a,b) Transfer characteristics of short and long-channel TASE-grown InGaAs FinFETs. Higher on-current is achieved in the device with $L_G = 25$ nm. Subthreshold characteristic for a planar MOSFET is shown in (c).

- the successful implementation of the TASE integration technique and the complex RMG CMOS-compatible process;
- FinFETs featuring **excellent scaling behavior** and strong resistance to SCEs;
- demonstrated **performance gain** moving from a gate-first approach to **replacement-gate**.

3.4 3D Sequentially Integrated InGaAs FinFETs on Silicon CMOS

3D sequential integration (3DSI) is nowadays regarded as a key enabler to continue the CMOS scaling technology roadmap, as proven by the recent increasing industrial interest in the topic. Compared to packaged die stacking, processing multiple levels of devices on top of each other can enable up to two orders of magnitude increase in via density through the use of 3D vertical interconnects. More specifically, up to -50 % area gain and +25 % augmented performance is predicted [11].

Hybrid solutions using high-mobility III-V channels can leverage their relatively low thermal budget to bring new and complementary functionalities on silicon. Previous research conducted at IBM Research Zurich, demonstrated the co-integration of InGaAs and SiGe devices as well as InGaAs MOSFETs fabricated on top of SiGe p-FinFETs [103, 104]. Preliminary circuit demonstrators were also reported, including 3D CMOS inverters and III-V/Si SRAMs [105]. However, fabricating a III-V transistor above a pre-processed device layer is not equivalent to doing it on a blanket bulk substrate, due to more severe thermal budget constraints and increased process complexity. The InGaAs MOSFETs on Si CMOS demonstrated so far are approaching

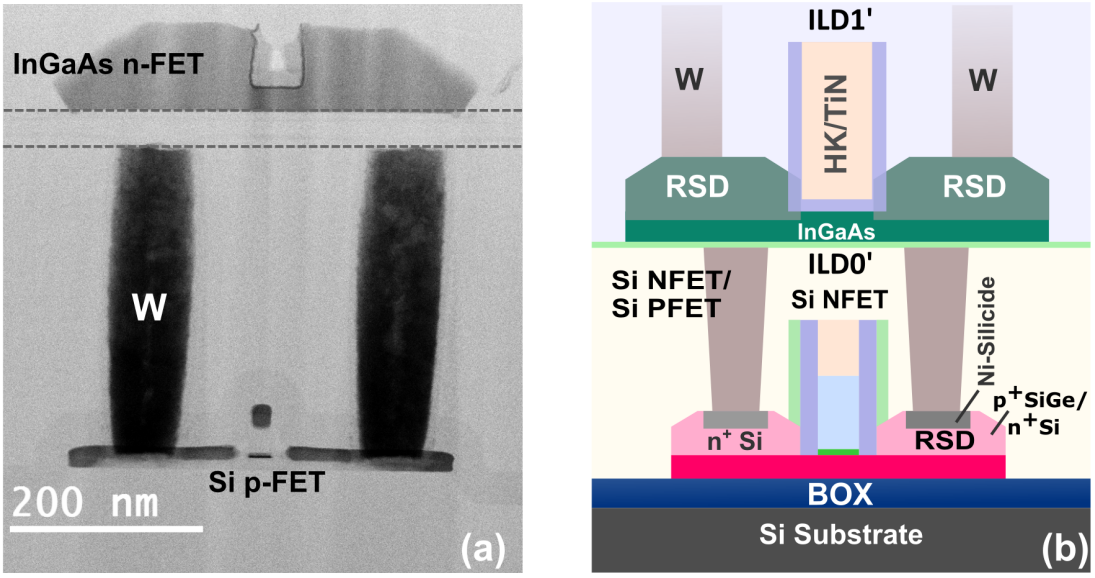


Figure 3.18 – (a) STEM cross-section image showing the fabricated InGaAs MOSFETs, 3D sequentially integrated on a Si-CMOS device layer. Sequential integration by direct wafer bonding allows for a very accurate alignment between the two tiers. A descriptive stack schematic is shown in (b). Adapted from [100].

but not yet matching state-of-the-art devices fabricated on silicon substrate [106]. The goal of this work is to narrow the existing performance gap between these two types of architectures.

3.4.1 3DSI InGaAs FETs: device architecture overview

Fig. 3.18a shows a high-resolution cross-section STEM of the fabricated InGaAs n-FET on top of a Si p-FET. The Si CMOS layer follows standard FDSOI fabrication flow with gate-first processing and Si/SiGe RSD epitaxy. The top InGaAs device layer is obtained by DWB, where both planar and FinFETs are processed following an RMG scheme. The fabrication flow description is available in section 2.5.2. A schematic cross-section of the implemented 3DS integration scheme is shown in Fig. 3.18b. Compared to the architecture reported in [105], two new modules are introduced: from the combination of gate sidewall spacers and doped extension regions, targeting off-state performance improvement, to modifications introduced in the wafer bonding techniques, aiming at a reduction of defects at the III-V bonding interface and, therefore, enhanced electron mobility [107]. Another important aspect of 3D integration is the alignment: the two fabricated transistor levels share the same design mask and alignment markers, enabling a very accurate positioning of the structures. This represents one of the major strength points of 3DS integration. DC electrical characterization have been

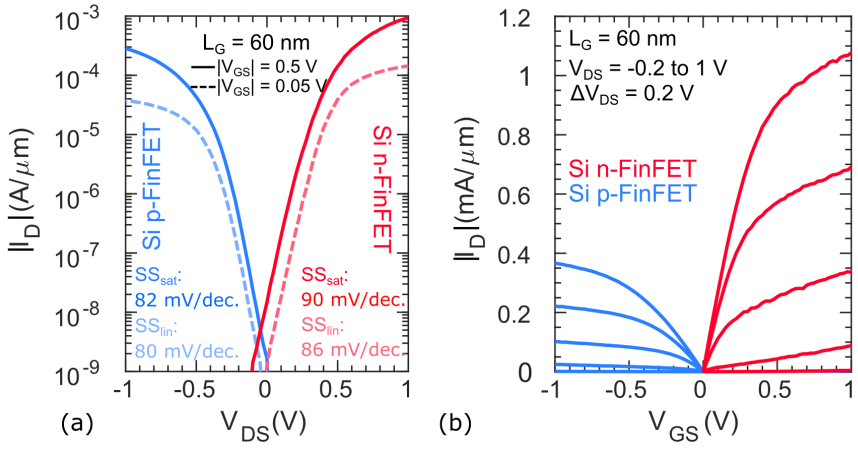


Figure 3.19 – (a) Subthreshold and (b) output characteristics of Si p-FinFET (blue) and n-FinFET (red). Bottom layer measurements are performed after completion of the top-layer processing. Adapted from [100].

carried out on both layers and will be discussed in the following sections.

3.4.2 Si CMOS: Impact of the III-V process

First of all, we evaluate the impact of the III-V layer fabrication flow on the bottom Si CMOS functionality. The most critical steps that might represent a possible source of performance degradation could be the bonding process or the RSD step. Fig. 3.19 shows transfer and output characteristics of Si p-FETs and n-FETs located in the first tier. The measurement has been carried out after the completion of the 3DS process. The devices, featuring L_G = 60 nm, show healthy transistor behavior and negligible effect on performance. This is more evident in Fig. 3.20, where the SS_{sat} trend versus L_G is displayed for both types of bottom-layer transistors before and after the 3DSI process. As can be noticed by the matching SS values, no significant effect on the lower tier layer performance is observed.

3.4.3 3D-integrated InGaAs FETs: DC performance

Planar and FinFET device performance is now compared. Fig. 3.21a shows threshold voltage (V_T) scaling with L_G. In the case of FinFETs, a V_T roll-off is observed only for L_G smaller than 50 nm whereas for planar FETs this value goes up to 500 nm. The same trend is confirmed in Fig. 3.21b, plotting $DIBL$ versus L_G. FinFETs start featuring $DIBL$ increase only below 30 nm gate length. By looking at both figures of merit, a drastic improvement in electrostatic control for FinFETs is registered. The inverse subthreshold slope in linear region is plotted in Fig. 3.21c versus L_G. As

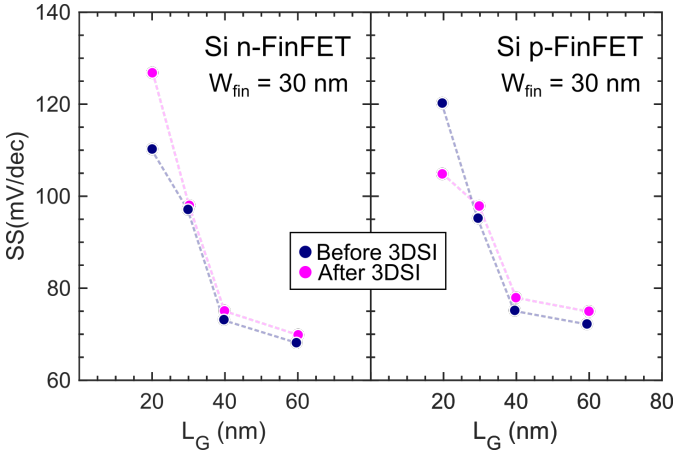


Figure 3.20 – Saturation SS scaling versus L_G for bottom-layer Si-CMOS devices, before (left) and after (right) top-layer processing. Negligible performance degradation is observed sign that the InGaAs thermal budget is compatible with the silicon devices. Adapted from [107].

already concluded from the V_T scaling, FinFETs with W_{FIN} = 50 nm feature SCEs for L_G smaller than 50 nm, when SS starts increasing due to lack of effective electrostatic control. Long-channel devices perform better with a planar geometry, since longer fins tend to be affected by distributed surface roughness. This explains the higher SS for FinFETs with L_G longer than 1 µm. On-current scaling with L_G is investigated in Fig. 3.21d. I_{ON} peaks at L_G = 50 nm for FinFET devices. At shorter gate length, the already discussed SS degradation due to SCEs lowers the on-state current level. Planar devices show limited gate length scalability as below L_G = 100 nm they no longer reach the off-current target at 0.5 V.

3.4.4 High-performance 3D-integrated InGaAs FinFETs

R_{ON} for FinFETs with different gate lengths L_G is shown in Fig. 3.21e and compares the devices fabricated in this work with similar architectures reported in [105]. The technological implementations previously discussed, enabled approximately a 50 % reduction in R_{ON}, for devices with L_G < 100 nm. We hypothesize that this improvement can be mainly attributed to increased channel mobility achieved by reducing the defect density at the bonded InGaAs/Al_2O_3 interface. Another factor that might positively impact the R_{ON} is the switching from a plasma process for the HKMG deposition to a thermal one, keeping the temperature unchanged. Moreover, we observe in both cases an R_{ON} saturation for shorter channels. One possible explanation could be the onset of SCEs, reducing the transconductance (g_m) due to higher output conductance (g_d). However, a non-homogeneous distribution of defects at the n+ contacts, particularly for scaled devices, could reduce the effective band gap and result in the observed behavior. FinFET scaling performance is investigated in Fig. 3.21f, displaying linear

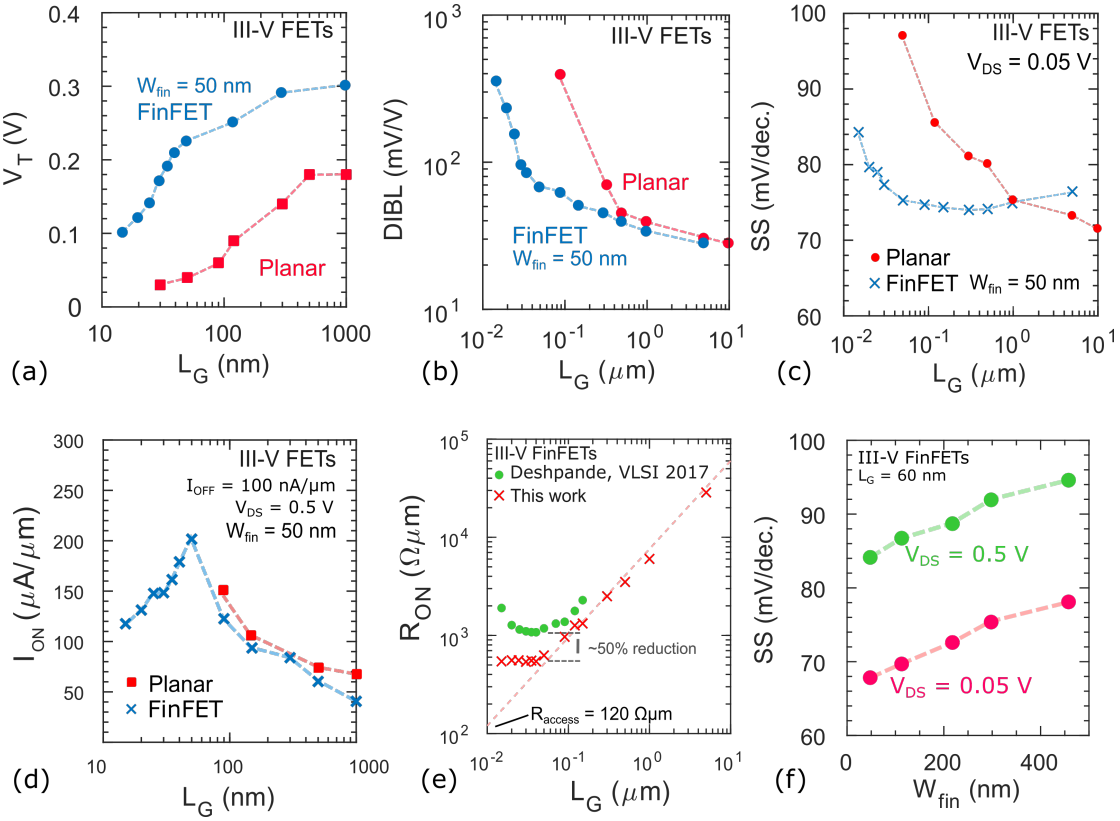


Figure 3.21 – (a) Threshold voltage (V_T) scaling with L_G. For FinFETs, V_T roll-off onset is observed only for $L_G < 50$ nm. (b) $DIBL$ and (c) SS versus L_G for planar and FinFETs. The latter show stronger resilience to SCEs. (d) I_{ON} scaling with L_G reveals the occurrence of SCEs for FinFETs with $L_G < 50$ nm. (e) R_{ON} benchmarking compared to previously demonstrated 3DSI InGaAs FETs [106]. The new process modules introduced enabled a 50 % reduction of access resistance. (f) SS scaling versus W_{FIN} showing enhanced electrostatic control. Adapted from [107].

and saturation SS versus W_{FIN}, for a device with $L_G = 60$ nm. An evident benefit from fin width scaling is observed – enhancing off-state performance and scalability – and no occurrence of SCEs down to $W_{FIN} = 15$ nm.

Fig. 3.22a shows subthreshold characteristics for a device with $L_G = 50$ nm and $W_{FIN} = 50$ nm. An I_{ON}=200 µA/µm, at I_{OFF}=100 nA/µm and V_{DS}=0.5 V and a transconductance peak of 1.1 mS/µm. The same device shows a $DIBL = 80$ mV/V and SS_{LIN} of 77 mV/decade. From the output characteristic displayed in Fig. 3.22b, an on-resistance (R_{ON}) of 500 Ω/µm is measured.

The 3DSI III-V FETs presented in this work are benchmarked in Fig. 3.23a against other 3D and non-3D InGaAs technologies [26, 30, 80, 106, 108]. The demonstrated on-current of 200 µA/µm (I_{OFF}=100 nA/µm, V_{DS}=0.5 V) is the highest reported until now for 3D sequentially integrated InGaAs FET on Si-CMOS. These results, while

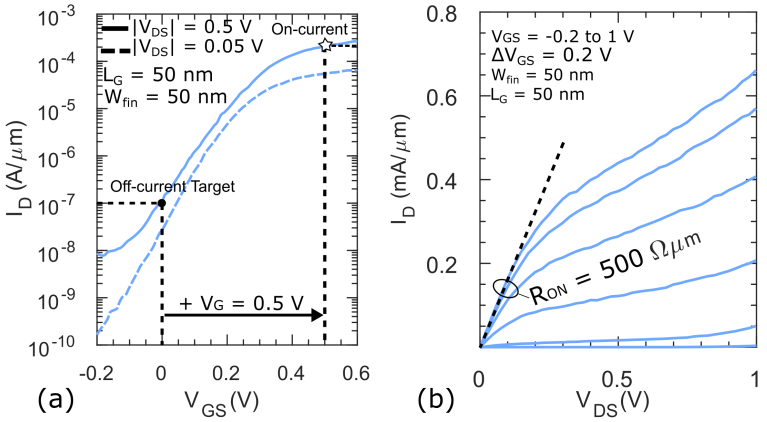


Figure 3.22 – (a) Transfer and (b) output characteristics for 3DSI InGaAs FinFET with L_G = 50 nm. We extrapolate an I_{ON}=200 µA/µm, at I_{OFF}=100 nA/µm and V_{DS}=0.5 V and a transconductance peak of 1.1 mS/µm. From the output characteristic we measure R_{ON} of 500 Ω µm. Adapted from [107].

outperforming state-of-the-art comparable architectures, also enable narrowing the gap with respect to non 3D-integrated technologies. Further work needs to be done to achieve comparable performance on more scaled devices. This shows that high-performance RMG III-V FETs can be integrated on processed substrates with negligible impact on the bottom device layer.

3.5 Conclusion and Outlook

In this chapter, electrical results of InGaAs MOSFETs fabricated with different techniques are reported. Fig. 3.23b summarizes the device performance for each category of transistors experimentally demonstrated in this thesis. The increasing technological complexity going from the more established DWB approach to the more exploratory TASE technique, justifies the existing performance discrepancy. In all cases, the transistors are processed following a CMOS-compatible replacement-gate scheme. InGaAs FETs integrated by DWB feature the strongest performance in this work. The reported on-current of 350 µA/µm is, to our best knowledge, the record value for III-V FET on silicon. Moreover, the achieved I_{ON} is matching high-performance Si CMOS at scaled L_G and V_{DD} = 0.5 V [7].

The devices fabricated with TASE show promising performance but do not yet match the one achievable with DWB. Further effort needs to be invested in increasing the device yield, sometimes compromised in the starting phase of the process by unsuccessful material nucleation inside the oxide cavities. Overall, the reported work shows that a complex, compatible with CMOS standards process such as RMG, can be successfully implemented on locally integrated III-V structures. Finally, DWB is

used to fabricate a 3D sequentially integrated layer stack made of Si CMOS logic and III-V logic (3D-DWB). Although the device processing is supposed to be equivalent to the non-3D DWB approach, the higher surface topography that characterizes a pre-processed substrate is unavoidably affecting the resulting bonded InGaAs layer quality. The higher technological complexity of TASE and 3D-DWB limits not only the maximum performance but also the minimum gate length that can be achieved. Addressing their major challenges will facilitate as well achieving performing devices at more scaled dimensions. The smallest InGaAs transistor on silicon ever reported has a gate length of 14 nm and has been fabricated with DWB.

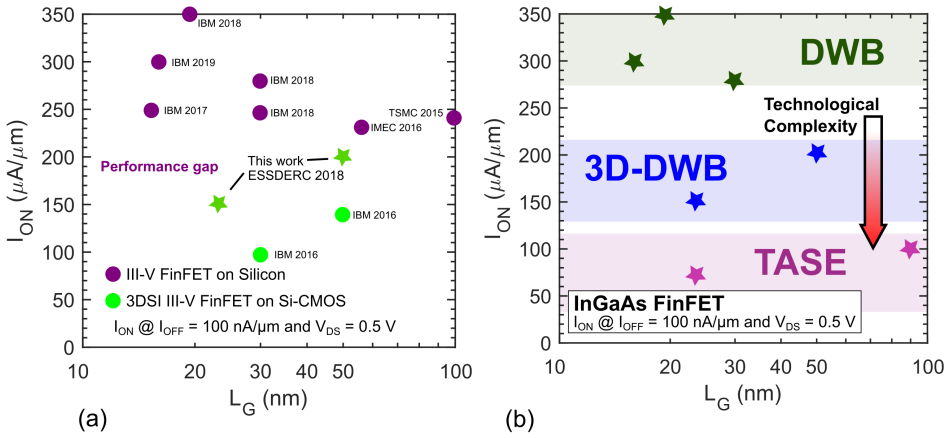


Figure 3.23 – (a) On-current benchmarking for different III-V technologies on silicon (purple) and 3D sequentially integrated (green).We have drastically outperformed previous 3D sequential demonstrations. (b) Benchmarking for the three integration approaches explored in this thesis. DWB refers to devices on a bulk Si wafer, 3D-DWB to devices bonded on a pre-processed Si-CMOS layer whereas the TASE transistors are fabricated by local integration of III-V. The last two categories show good performance but do not yet match the more established and least technologically complex DWB.

4 Heterostructure III-V Tunnel-FETs

4.1 InAs/GaSb Nanowire Tunnel Diodes

TFETs are promising devices that can outperform CMOS logic on several metrics. Two-terminal devices such as tunnel diodes can be useful to gain insights about the band-edge sharpness influencing the tunneling behavior. Measuring a TFET in a two-terminal configuration or monitoring a TFET process on equivalent structures lacking the gate contact can be an efficient method to decouple the junction transport properties from any gate-oxide contribution. In 2014, Agarwal *et al.* [109] have explored the concept of evaluating the joint density of state in an Esaki-backward diode by direct correlation with the diode negative differential resistance (NDR). In particular, they introduce a figure of merit called *semilog conductance swing*, the inverse of the semi logarithmic slope of the absolute conductance I/V. This quantity turns out to be proportional to a weighted average of the tunneling joint density of state over the Fermi function, as highlighted in Eq. (4.1):

$$S_{T\times D(E)} \equiv \left(\frac{dlog\langle T \times D_J(E)\rangle}{dV}\right)^{-1} \approx \left(\frac{dlog(I/V)}{dV}\right)^{-1} \tag{4.1}$$

Where $T \times D_J(E)$ is the tunneling joint density of state. Recently, Memisevic et al. [110], have proposed a similar model to evaluate the band-edge sharpness of a TFET, also based on conductance in the NDR and the *SS*. However, in their work they assert that diode measurements are only of limited use and a one-to-one correlation with TFETs can be misleading. The model can be applied instead to capture the role of band tails in the off-state and NDR region of a TFET. The main reason is that Esaki diodes require sharp p+/n+ doping profiles in contrast to the standard TFET body that is a gated p-i-n diode. This can result in radically different trap distribution and disorder-induced band tails. However, in the TFET characteristics reported until now, the NDR is not always visible. This can be attributed to several reasons such as low source doping levels or gate-metal work function shifting. Nonetheless, tunnel diodes may still provide a useful reference for comparing different TFET technologies, particularly

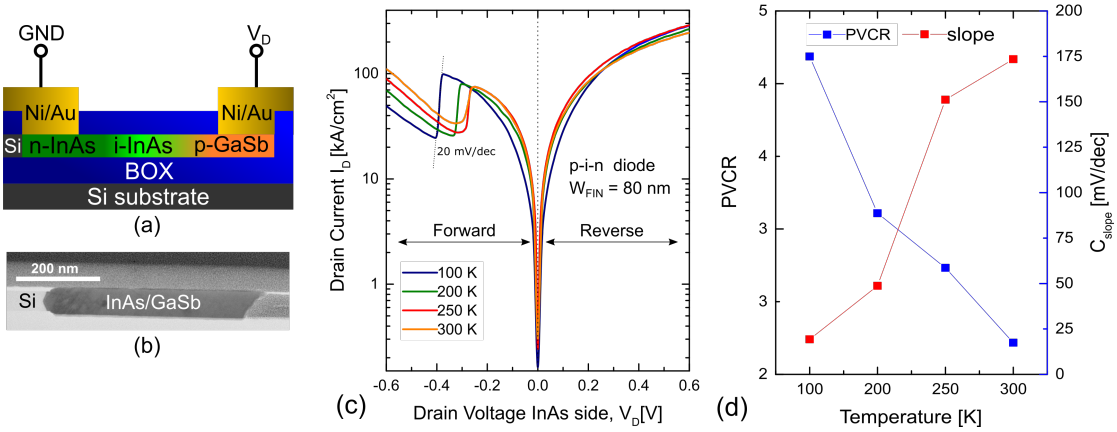


Figure 4.1 – (a) Illustration schematic of an InAs/GaSb tunnel diode fabricated using TASE and (b) TEM cross-section showing the Si seed and the surrounding oxide template. (c) Temperature-dependent I/V characteristics showing a conductance slope and $PVCR$ improvement with decreasing temperatures. $PVCR$ and C_{slope} trends are displayed in (d).

when the diode body is very similar to its TFET counterpart. In this work we explore the conductance slope method for InAs/GaSb p-i-n diodes, fabricated using TASE [111]. In this case, the only features that differentiate the considered structure from a TFET is the lack of a gate stack and gate contact. The diodes are fabricated on SOI substrates and Ni/Au metal-lift off is used to pattern the source-drain contacts. As described in section 2.2.2, the nanowires are protected with an oxide template and in this case the oxide is removed only in the contact regions (schematic in Fig. 4.1a). The shown III-V nanowires feature a rectangular cross-section of 80 nm × 30 nm. An STEM cross-section along the nanowire length is shown in Fig. 4.1b. Temperature-dependent $I-V$ measurement is reported in Fig. 4.1c, from room temperature down to 100 K. The NDR feature is visible at room temperature and becomes more pronounced when the device is cooled down. A conductance slope (C_{slope}) of 170 mV/decade and a peak-to-valley current-ratio ($PVCR$) of 2.2 is obtained. C_{slope} and $PVCR$ trends with temperature for the same device are shown in Fig. 4.1d. The symmetrical behavior in the voltage interval $V_D = \pm 200$ mV is due to the variation of the energy gap with temperature. For $V_D > \pm 300$ mV, a contribution of series resistance becomes evident, more dominant at 300 K. At the lowest temperature, 100 K, a slope of 20 mV/decade and a $PVCR$ of 4.2 is achieved. Ideally, only the diode excess current – being dominated by thermionic transport – and the energy gap are expected to be dependent on temperature and so the $PVCR$. The strong temperature dependence of C_{slope} can be attributed to a more dominant contribution of traps and defects located at the tunneling hetero-interface. Compared to previous results based on similar structures, we achieve a higher current density (74 kA/c^{2}m). We hypothesize that this improvement might be the results of an

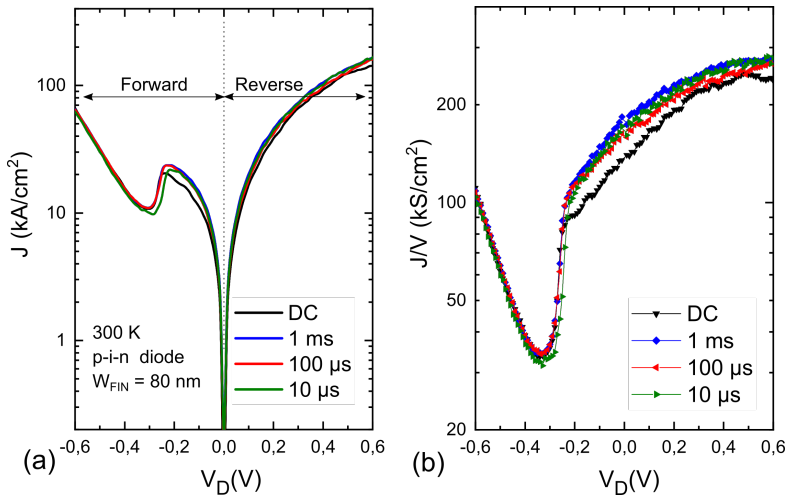


Figure 4.2 – (a) Pulsed I/V measurement of a p-i-n diode resembling the body structure of a TFET. (b) Absolute conductance in linear scale for the same device. The characteristics show a minor improvement in PVCR and independent slopes, probably due to the limited pulsing speed.

improved contact scheme.

Pulsed $I-V$ measurements can be carried out on tunnel diodes to analyze the dynamic response of traps and reduce the contribution of parasitic tunneling mechanisms. In this case we apply different pulse widths, from 1 MHz to 1 kHz with the use of a parameter analyzer (B1500A, *Agilent*) and remote-sense and switch units (RSU). For this measurement, the settling time depends on the measurement range. Therefore, an appropriate waiting time must be considered to achieve accurate results. An example measurement on the fabricated InAs/GaSb nanowire is shown in Fig. 4.2a and the absolute conductance is displayed in Fig. 4.2b. For different applied pulses, only minor changes in C_{slope} are observed, and no variation in the excess current, that is instead expected to decrease when reducing the impact of parasitic tunneling mechanisms. It is of importance to notice that the low absolute current of the single nanowire device limits the minimum available integration time hence the shortest pulse used might not be sufficient to capture the defect-mediated trapping mechanism.

Lateral n-TFETs sharing the same fabrication scheme and design as the presented tunnel diodes have been previously demonstrated from colleagues at IBM Research Zurich [54]. The platform, making use of TASE, represents an excellent example of co-integration of p-TFET and n-TFET using a scalable, industrial-compatible process. However, the reported n-TFET performance is not satisfactory and this is mainly attributed to a non-optimized gate stack combined with SCEs. Furthermore, as described in Chapter 2, Ga(As)Sb is extremely sensitive to process-induced damages, such the use of HF wet-etching to remove the TASE oxide template. Hence the con-

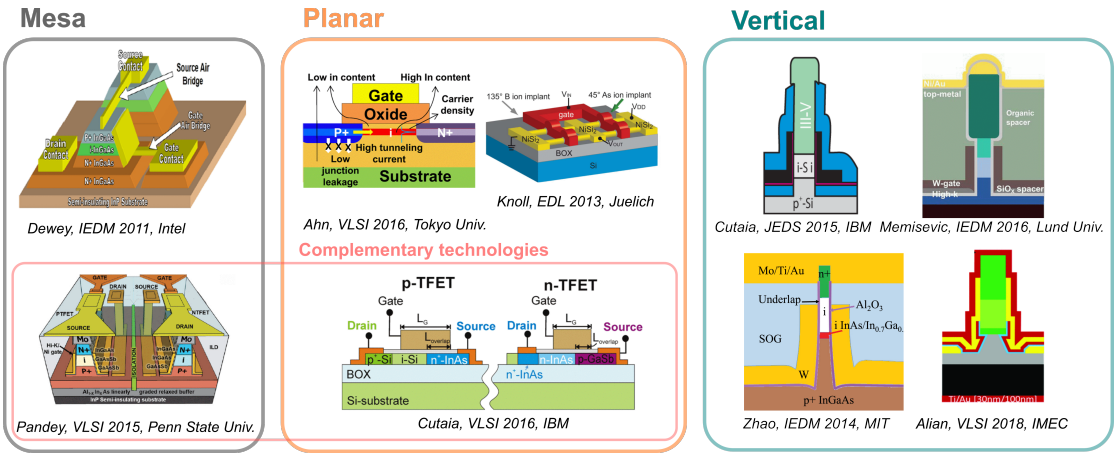


Figure 4.3 – Overview of different state-of-the-art TFET technologies. Both lateral and vertical implementations have been explored. Vertical TFETs have shown the best device performance due to the improved electrostatics. The In(Ga)As/Ga(As)Sb system is the optimum choice for complementary technology. Lateral designs include mesa structures but planar and nanowire geometries are the most promising for scalability and VLSI integration. Adapted from [49, 51, 53, 54, 54, 55, 56, 57, 112].

sidered process is not suitable for the realization of complex TFET devices and a new approach is essential. The new fabrication flow takes these weaknesses into account and includes a self-aligned scheme.

4.2 Tunnel-FETs

4.2.1 InGaAs/GaAsSb TFET: device architecture overview

The TFETs presented in this chapter, are fabricated following a self-aligned RMG process flow, compatible with CMOS standards [113] and they are co-integrated with InGaAs MOSFETs that are processed in parallel on the same silicon substrate. An overview of state-of-the-art TFET technologies is available in Fig. 4.3 [49, 51, 53, 54, 55, 56, 57, 58, 112]. Until now, the best device performance has been demonstrated in vertical implementations, that are however not the most ideal candidates for VLSI integration. Scalability is also a crucial aspect for TFETs and it is particularly challenging in mesa-like structures. Planar geometries give the best compromise in terms of scalability and suitability for large-scale integration. Although previous works have highlighted the challenges linked to aggressive L_G scaling for TFETs [114], here we demonstrate that our devices can be scaled without performance degradation. In our planar FinFET-like process, we have achieved a minimum gate length of 50 nm, the smallest ever reported for TFETs to our best knowledge.

The starting active device layer consists of 20 nm InP and 10 nm $In_{75}Ga_{25}As$ trans-

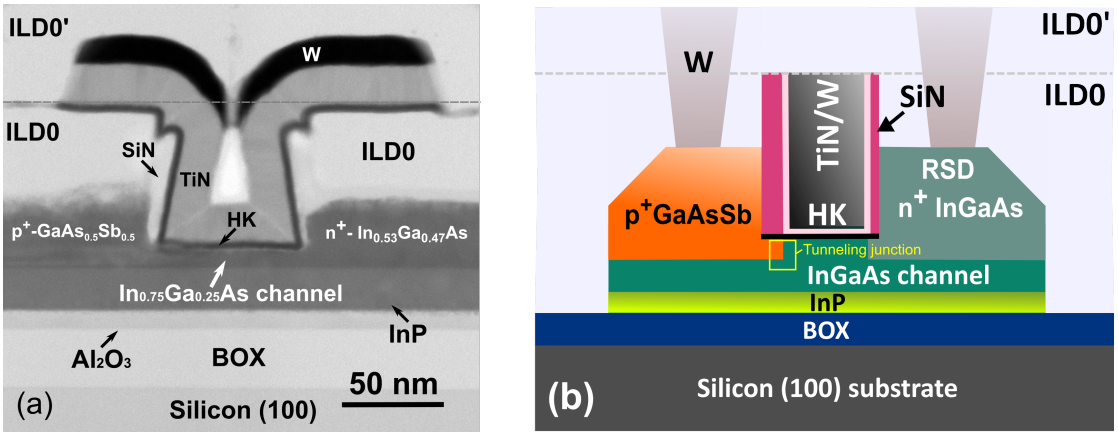


Figure 4.4 – (a) High-resolution STEM cross-section image of the fabricated InGaAs/GaAsSb TFET on silicon (100). Source and drain are grown in two independent steps. (b) Structure schematic overview. Thicker SiN spacers on one side are consequence of the double-masking process. The yellow rectangle highlights the position of the tunneling junction.

ferred on a 4" Si substrate using direct wafer bonding (DWB). A detailed description of the integration method and the device fabrication process is available in Chapter 2. Fig. 4.4a shows a high-resolution STEM cross-section image of a finalized device with L_G = 50 nm. The source/channel interface – i.e. the tunneling junction – is accurately self-aligned to the gate such that the gate-to-source overlap is controlled. The individual masking process necessary to grow the two different materials in separate growth steps induces a spacer of twice the thickness on the source side compared to the drain side, as highlighted in the device schematic in Fig.4.4b. Tunnel-FinFETs featuring L_G from 50 nm to 150 nm and W_{FIN} from 35 nm to 100 nm have been fabricated. One of the key advantage of the designed process, in addition to the self-alignment, is that it limits the number of steps performed on GaAsSb: this material, used for the source contact, is extremely sensitive to process-induced damage and shows poor selectivity in most of the common etching solutions. Moreover, the co-integration with MOSFETs is obtained without any additional fabrication step.

In the next sections, electrical DC measurement at room and low temperature down to 100 K are shown. The measurements have been performed in common-source configuration, hence by grounding the source p-type GaAsSb contact. Electrical data is acquired using an Agilent B1500 parameter analyzer and high resolution source monitor units (SMUs). Low temperature measurements are carried out using a cryogenic *Janis* vacuum probe station. Liquid nitrogen is used to cool down the system to a set-point temperature, monitored with a *Lake Shore* cryogenic temperature controller. The current normalization takes into account the gated perimeter of the fin as all the reported results refer to single-fin devices.

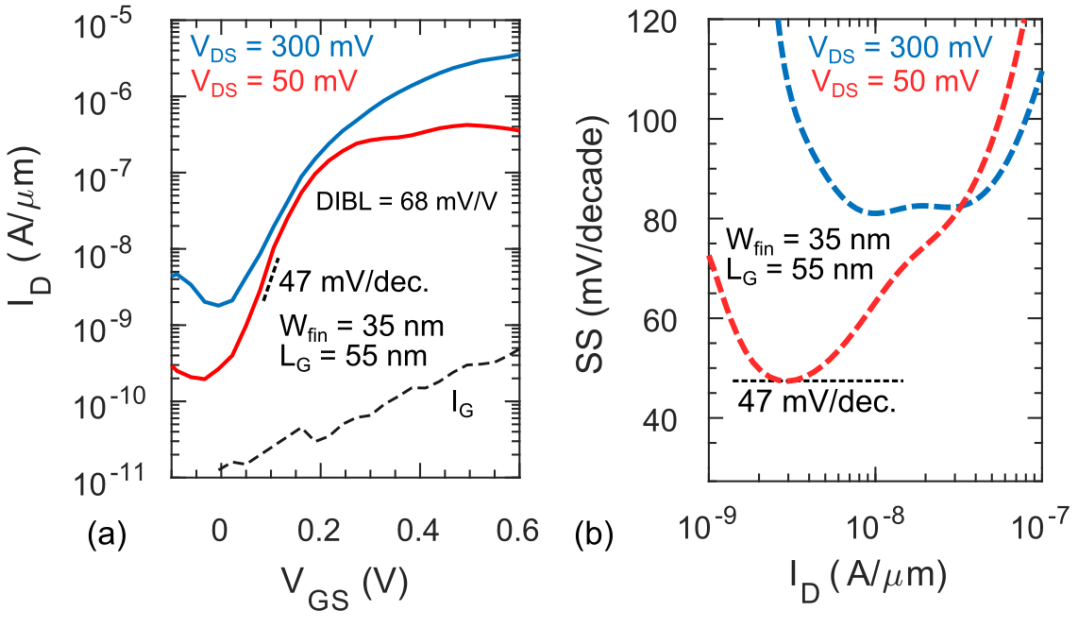


Figure 4.5 – (a) Subthreshold characteristic of InGaAs/GaAsSb Fin-TFET with L_G = 55 nm. A minimum SS of 47 mV/decade at 0.05 V is achieved in this device as shown in the SS versus current plot in (b).

4.2.2 Sub-thermionic InGaAs/GaAsSb TFETs

Fig. 4.5a shows the subthreshold characteristic of a TFET with L_G = 55 nm and W_{FIN} = 35 nm. The gate current (I_G), displayed on the same axis, is clearly negligible within the bias range under consideration. The device shows well-behaved tunneling transistor characteristic with a minimum drain-induced barrier lowering (DIBL) of 68 mV/V. A sub-thermionic slope of 47 mV/decade at V_{DS} = 50 mV is achieved. Fig. 4.5b reports the SS versus drain current (I_D): the transistor is sub-thermionic across one order of magnitude of current and an I_{60} – the highest drain current at which SS transitions from sub-60 to above 60 mV/decade – of 10 nA/µm is obtained. At higher drain bias (V_{DS} = 300 mV), the SS increases and the transistor is no longer sub-thermionic. This might be attributed to the influence of SCEs. Furthermore, the presence of an InP bottom layer in the channel – with the function of isolating the carriers from the defective bonding back-oxide interface – might be responsible for electrostatic control degradation, particularly at high drain bias. The output characteristic for the same device is shown in Fig. 4.6a, featuring a very low output conductance and good current saturation. The extrapolated on-resistance (R_{ON}) is here 10 kΩµm. A maximum drain current ($I_{D,max}$) of 3.4 µA/µm is achieved at V_{DS} = 0.5 V and V_{GS} = 0.45 V. The main observable feature is the typical NDR in forward bias direction, corresponding to negative V_{DS} values. The NDR, plotted in linear scale in Fig. 4.6b,

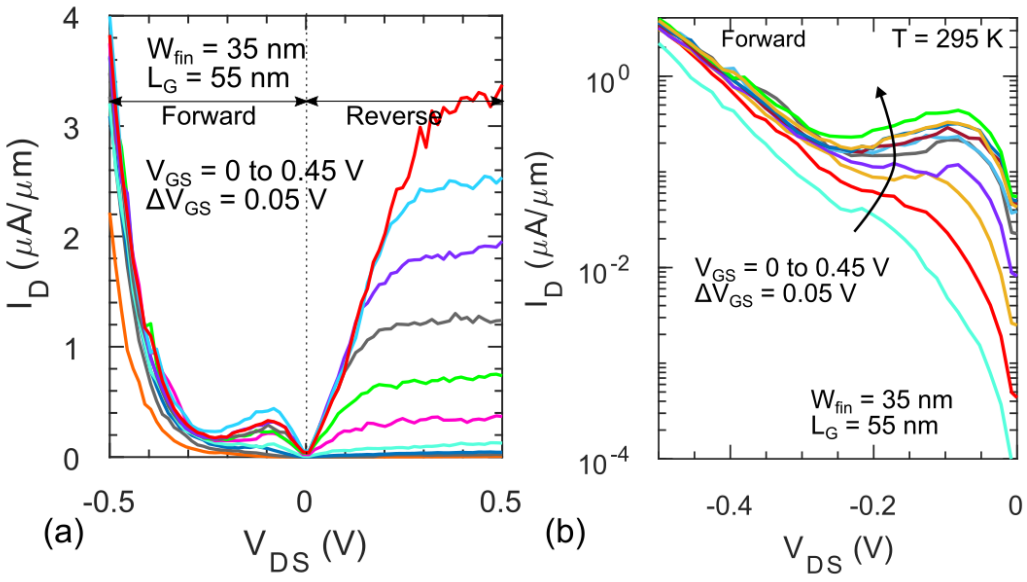


Figure 4.6 – (a) InGaAs/GaAsSb TFET output characteristic featuring the typical NDR in the diode forward bias region. From (b) we extrapolate a $PVCR$ of 2 and an I_{peak} of 440 nA/µm.

exhibits a $PVCR$ of 2 and an I_{peak} of 440 nA/µm. As discussed before, the observation of an NDR, particularly at room-temperature, validates the presence of a tunneling mechanism. Fig. 4.7a displays linear transfer characteristic and transconductance (g_m) behavior. The device under consideration achieves a $g_{m,peak}$ of 12 µS/µm and a transconductance efficiency (g_m/I_D) of 30 V^{-1}. g_m/I_D is inversely proportional to SS, hence for an ideal MOSFET the fundamental limit is 38 V^{-1} at room temperature. Investigating the low-temperature characteristic of a TFET can provide useful insights to distinguish its behavior from the one of a MOSFET. In a TFET, the on-current is directly dependent on the tunneling probability – as the main current mechanism is BTBT – influenced by effective tunneling band gap and carrier effective mass. Only a minor temperature dependence should be observed in the on-current of an ideal TFET, due to fluctuations in the band edges at the source/channel interface. MOSFETs I_{ON} instead, changes with carrier mobility and density of states, both depend on temperature. Fig. 4.7b shows SS trend versus temperature in the range of 130 K-300 K for a Fin-TFET with L_G = 55 nm and W_{FIN} = 40 nm. SS is reduced from 55 mV/decade to 33 mV/decade at the lowest temperature measured. The typical MOS SS dependence due to thermionic emission is drawn in the same figure: the considered TFET exhibits weaker but non-negligible temperature dependence. This effect indicates that parasitic tunneling mechanisms such as trap-assisted tunneling (TAT) – through trap states at the oxide interface or at the source/channel hetero-junction itself – might be present, increasing the SS compared to the ideal value. Further gate-oxide

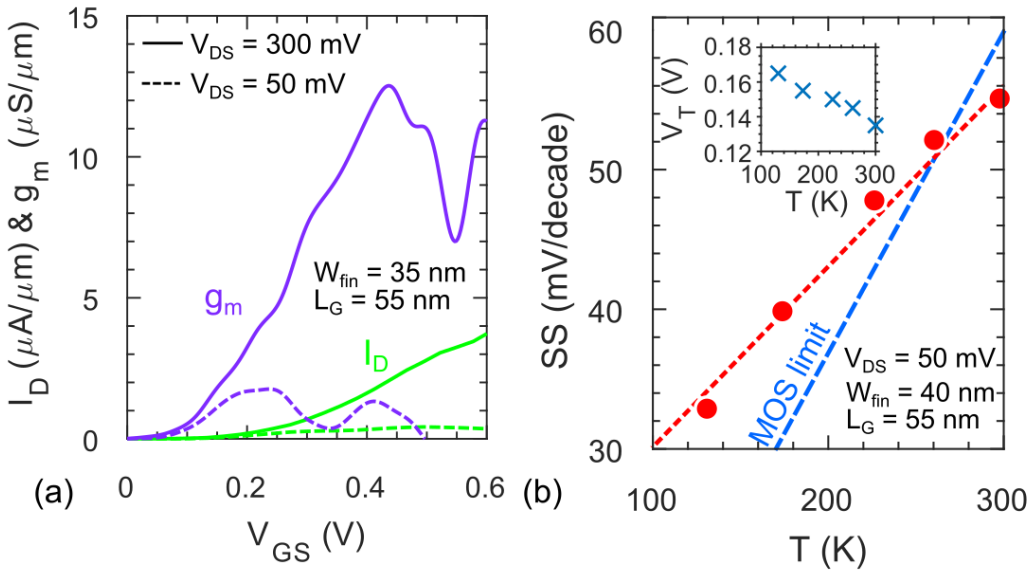


Figure 4.7 – (a) Transfer characteristic and transconductance for a TFET with L_G = 50 nm and W_{FIN} = 35 nm. A peak g_m = 12 µS/µm is measured. (b) Minimum SS versus temperature showing a weaker dependence compared to the MOS limit (blue line). V_T temperature dependence is shown in the inset.

optimization and hetero-interface defect reduction would be beneficial. The inset in Fig. 4.7b shows threshold voltage (V_T) versus temperature characteristic. In this case only a minor dependence is observed. The subthreshold characteristic for a TFET with larger W_{FIN} is available in Fig. 4.8a. This device (L_G = 55 nm and W_{FIN} = 80 nm) achieves an excellent I_{ON} of 1.5 µA/µm at fixed I_{OFF}=1 nA/µm and V_{DS}=0.3 V. A still sub-thermionic but higher minimum SS is obtained (Fig. 4.8b) compared to the device with smaller W_{FIN} shown in Fig. 4.5a. This result shows that poorer electrostatic control has an important impact on the TFET performance and further fin scaling should be pursued. These findings are confirmed by the trend displayed in Fig. 4.9a, that shows minimum SS versus W_{FIN} for different devices. Only TFETs with W_{FIN} smaller than 50 nm exhibit sub-thermionic behavior and a clear scaling trend is observed, in good agreement with what has been previously reported by Memisevic *et al.* [115]. At fixed W_{FIN} of 35 nm, devices with different gate lengths show comparable SS (Fig. 4.9a) and in this case no relevant scaling trend is recorded. Due to the scaled fin dimension, L_G variations have negligible impact on the SS. In fig. 4.10 the scaling behavior of MOSFET and TFET I_{ON} is analyzed. I_{ON} is extrapolated at fixed I_{OFF} of 100 nA/µm for MOSFETs and 10 nA/µm for TFETs. In this case we are mostly interested in the relative trend rather than in the absolute values. Therefore, each distribution is normalized by its maximum. While the MOSFETs show, as expected, a clear dependence on L_G scaling, the behavior is more scattered for the TFETs and no

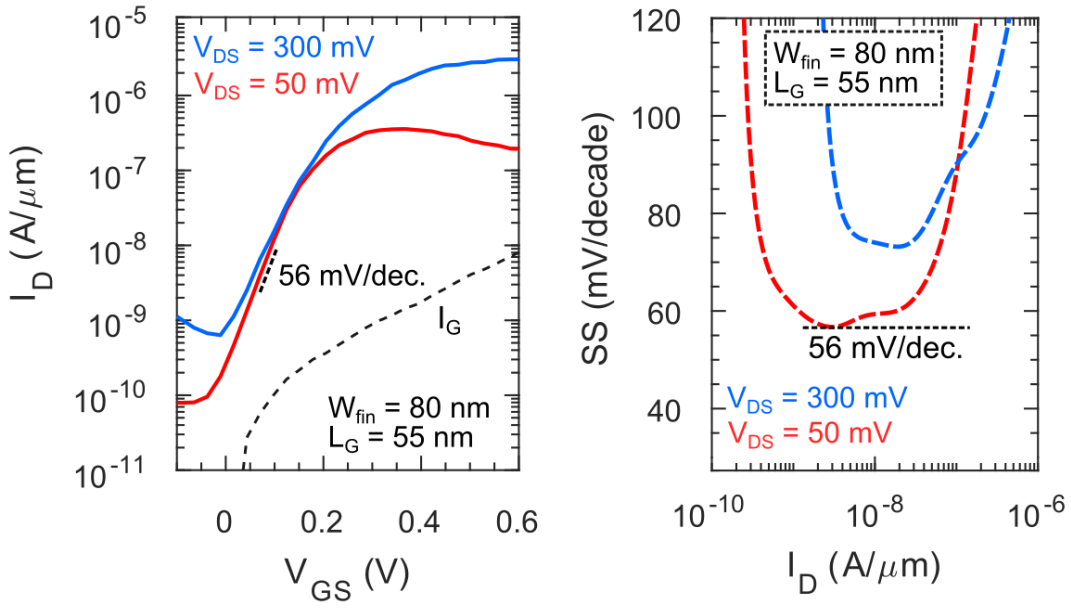


Figure 4.8 – (a) Subthreshold characteristic of InGaAs/GaAsSb Fin-TFET with L_G = 35 nm. A minimum SS of 56 mV/decade at 0.05 V is achieved in this device as shown in the SS versus current plot in (b).

clear correlation is observed. The lack of dependence of I_{ON} on TFET L_G have been experimentally confirmed also by Sandow *et al.* [116].

4.2.3 Benchmarking

In this section, the demonstrated InGaAs/GaAsSb TFETs are benchmarked against state-of-the-art competing technologies [49, 52, 53, 54, 55, 56, 57]. Among all, what differentiates this work from the other available III-V TFETs, is the suitability of the implemented process for VLSI integration. Sub-thermionic TFETs are here demon-

III-V TFETs	Junction	Substrate	SS_{MIN} (mV/dec)	L_G (nm)
Alian, VLSI 18	Vertical	III-V	47	100
Zhao, EDL 17	Vertical	III-V	53	> 100
Noguchi, IEDM 13	Lateral	III-V	64	> 100
Ahn, VLSI 16	Lateral	III-V	57	> 100
Dewey, IEDM 11	Vertical	III-V	58	150
Memisevic, IEDM 16	Vertical	Si (111)	48	260
Cutaia, VLSI 16	Lateral	SOI	70	900
This work	**Lateral**	**Si (100)**	**47**	**55**

Table 4.1 – III-V TFET technologies benchmarking.

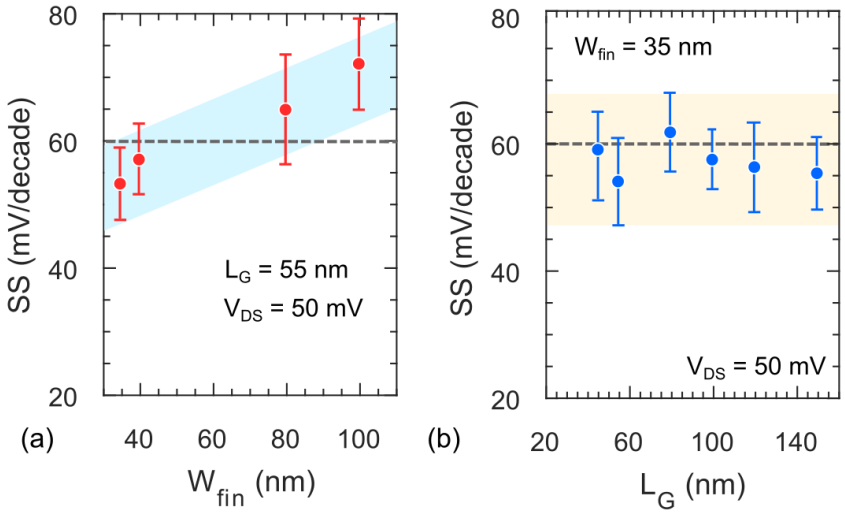


Figure 4.9 – Minimum SS versus (a) L_G and (b) W_{FIN} for several acquired TFET measurements. Due to the scaled fin dimension, L_G scaling does not impact SS significantly whereas a clear scaling trend is observed for smaller W_{FIN}, demonstrating the importance of electrostatic control in TFET devices.

strated for the first time using a scalable, CMOS-compatible RMG process on silicon (100) and the entire process, performed on 4" substrates, can be easily reproduced on larger wafers. As highlighted in Tab. 4.1, we have also demonstrated the TFET with the shortest gate length, and the only one with comparable size to scaled CMOS nodes. I_{60} versus gate length are benchmarked in Fig. 4.11a. Here, all the points are extrapolated at 50 mV unless otherwise stated. The I_{60} reported in our work, with a value of 10 nA/µm is well positioned with respect to the other sub-thermionic demonstrations, featuring a minimum SS of 47 mV/decade. SS versus I_D is shown in Fig. 4.11b, highlighting that our devices achieve the highest drain current while having sub-thermionic behavior.

4.3 Conclusion and Outlook

In this chapter, experimental electrical data of both tunnel diodes and tunnel FETs have been presented. First, InAs/GaSb tunnel devices integrated on SOI substrate using TASE are analyzed through temperature-dependence and conductance slope measurements.

We have introduced a new TFET process that enabled achieving the first sub-thermionic III-V TFET on silicon, with a scalable and CMOS-compatible flow. TFETs and MOSFETs are processed in parallel and co-integrated on the same substrate. Direct wafer bonding is used to transfer the InGaAs layer on Si and a standard RMG process is performed. The designed fabrication steps fulfill three major requirements

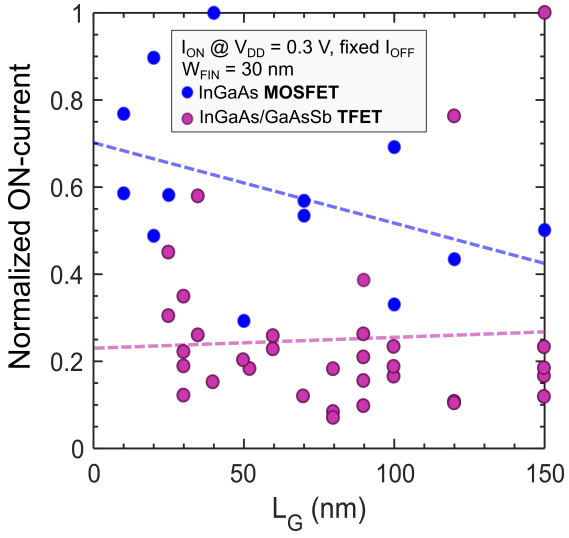


Figure 4.10 – I_{ON} versus L_G for MOSFETs and TFETs co-integrated on the same substrate. The dashed lines correspond to the linear fit to the experimental values. As expected the I_{ON} for MOSFETs increases at shorter L_G while TFETs do not seem to have a net correlation with L_G scaling. An order of magnitude difference exists between the two slopes. The I_{OFF} target is set to 100 nA/µm for MOSFETs and 10 nA/µm for TFETs. Each distribution is normalized by its maximum value as in this case we are interested in the trend rather than the absolute values.

for high-performance TFETs: near-zero overlap between gate and source, channel scaling down to 25 nm of gate length and reduced exposure to process-damages for the Sb-based material. Electrical results show that the fabricated TFETs achieve sub-thermionic performance and represent the first demonstration on Si (100). TFET operation is confirmed by temperature-dependent measurement and from the observation of the NDR feature at room temperature. The best demonstrated device achieves a minimum SS of 47 mV/decade (V_{DS}=50 mV), an I_{ON} of 1.5 µA/µm (at I_{OFF}=1 nA/µm and V_{DS}=0.3 V) and I_{60} of 10 µA/µm. The selected material combination, InGaAs/-GaAsSb, is also suitable for complementary TFET technology, as demonstrated in [51].

Further improvement of the demonstrated devices should focus on exploring the formation of a highly-doped pocket in the source – that would be straightforward to implement in the described process –, compare TFET performances with different junction doping levels and further scaling of the device size. Alternatively, a type II (broken-gap) band configuration can be explored by replacing the III-V heterostructure with InAs/GaSb.

The implemented TFET process makes use of direct wafer bonding to transfer the III-V on the Si substrate. This integration technique is more established and allowed focused effort on the actual device process optimization, starting from a high-quality InGaAs layer. However, the same approach can be applied to devices locally grown on

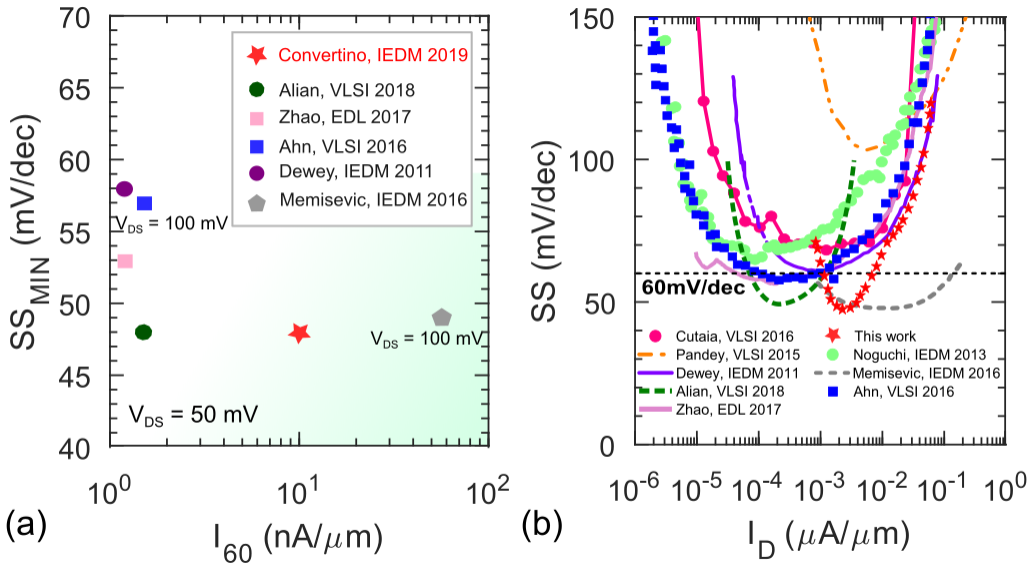


Figure 4.11 – (a) Minimum SS versus I_{60} for different III-V TFETs. Our work, the only sub-thermionic TFET demonstration on silicon (100), is very well-positioned with an I_{60} of 10 nA/µm. (b) SS versus I_D benchmarking. Values are extrapolated from pdf files hence minor deviations from actual data might be present.

Si, for instance by using template-assisted selective epitaxy.

5 Conclusion

The main driver of this work has been the high demand for less power-constrained integrated circuits combined with the request for compact, portable and high-performing devices. A key requirement is to reduce the operating voltage and simultaneously minimize the off-state leakage, although the two aspects are strongly correlated in conventional silicon CMOS technology. The use of strained-Si as channel material for n-MOSFETs have certainly postponed by a few years the farewell to Moore's law, but a switch to more disruptive architectures may be an opportunity to other material systems.

In this thesis I have experimentally demonstrated the use of III-V semiconductors such as InGaAs and GaAsSb for the realization of high-performance digital devices. Processes and materials have been thoroughly designed to match some of the integration density requirements of advanced CMOS nodes, although the concrete technology readiness of III-V logic to high-volume manufacturing remains still an open question. The presented III-V platform is the common thread linking high-mobility channel MOSFETs, 3D-integration and a *beyond-CMOS* category of devices, the Tunnel-FETs. We have identified opportunities and challenges for each technology and designed optimized process modules targeting specific performance improvements.

- **InGaAs n-FinFETs with reduced off-current and record on-current.**

  Previous research has largely assessed the superiority of InGaAs n-MOSFETs against strained-Si devices, in terms of on-current, static leakages and speed [21]. Although these results are very encouraging and match the performance expectations that the III-V community has built in the last years, challenges relating to scalability of these devices and high manufacturing costs remain unaddressed. Silicon wafer processing is cheap, well-established and reliable. This means that foundries will accept a transition to InGaAs n-MOSFET logic technology only within a framework of co-integration with existing Si modules. In Chapter 2, we have provided an overview on different methods to integrate

III-V compounds on Si wafers. Direct wafer bonding (DWB) and template-assisted-selective epitaxy (TASE) are the ones experimentally explored in this work. Advantages and disadvantages of each approach can be optimally delivered for target applications. DWB, for instance, allows for high-quality large-area III-V layer integration (up to 300 mm) but requires expensive native III-V substrates and it is constrained to sequential layer processing. TASE, on the other hand, enables local integration of nanostructures, does not involve the use of native substrates, but requires template pre-processing.

For all the fabricated devices we have pursued a replacement-metal-gate (RMG) MOSFET process, featuring high compatibility with industry standard modules. The InGaAs n-MOSFETs fabricated by DWB are characterized by exceptional device yield and therefore have been considered for an extensive study on off-current reduction. Low energy band gap materials such as InGaAs are notably affected by several leakage mechanisms such as the parasitic bipolar effect. We have addressed this problem by following design guidelines obtained through device simulations. It turned out that the use of lateral oxide spacers on the gate sidewalls has enabled a three orders of magnitude off-current reduction in scaled FinFET devices. This result has been achieved without any compromise on the on-state: the additional implementation of doped extension regions prevented the undesired access resistance increase, often associated with the presence of un-gated channel regions. Record I_{ON}=350 µA/µm at I_{OFF}=100 nA/µm and V_{DS}=0.5 V have been demonstrated, as *the highest value reported for CMOS-compatible InGaAs FinFET to our best knowledge. We have additionally demonstrated InGaAs MOSFETs using TASE and for the first time we have combined this powerful integration method with a CMOS-compatible RMG transistor process.* Excellent device performance has been achieved although further work is required to improve device variability and yield. Both demonstrations open-up possibilities for the actual co-integration of Si and high-performance III-V FETs within an industry-viable and cost-effective framework.

- **3D sequentially integrated InGaAs MOSFETs on Si-CMOS.**

The advantages of wafer bonding have been leveraged to exploit the third dimension and achieve higher integration densities. 3D sequential integration (3DSI) is a rising trend, currently included in the semiconductor roadmap as a potential solution to excessive IC power dissipation and as possibility to relax some aggressive scaling requirements. In Chapter 2 we have described the minor modifications that can be applied to DWB when the host silicon substrate

is replaced by a pre-processed wafer. In Chapter 3 we show electrical data of InGaAs MOSFETs sequentially integrated on top of a Si CMOS device layer. *A major achievement is that the bottom layer functionality is entirely preserved*, as assessed by electrical measurements acquired after the top layer processing is completed. The relatively low fabrication thermal budget of III-Vs makes them the perfect candidates for such sequential integration schemes and provides an additional reason for the co-integration of Si and InGaAs. Obviously, 3D fabrication flows are more complex and expensive and the demonstrated results are not yet matching the ones achieved in the 2D case. Nevertheless in this work we have demonstrated that key technological boosters can bring the two technologies closer in performance.

- **First sub-thermionic InGaAs/GaAsSb Tunnel-FETs on Si (100).**

  The results presented in this thesis, from the first to the last chapter, feature increasing fabrication complexity and success risk. Chapter 4 is indeed focused on the experimental demonstration of a more exploratory device concept, the Tunnel-FET (TFET). This device is predicted to overcome fundamental limitations of standard MOSFET technology by exploiting a more energy-efficient switching mechanism based on quantum mechanical tunneling. This efficiency is measured by the inverse subthreshold slope (SS), that in a TFET can be smaller than the thermal limit of 60 mV/decade at room temperature. Despite the theoretical predictions, only a few experimental demonstrations feature *sub-thermionic* behavior. Several existing technological challenges make these devices extremely hard to fabricate. *The major requirements can be summarized in low defect densities,* – particularity at the tunneling junction and at the interface with the gate oxide – *extremely accurate gate-to-source alignment and channel dimension scaling.*

  To address each of these issues we have designed a new fabrication flow, starting from the existing InGaAs platform and making use of the extensive knowledge developed during the fabrication of CMOS-compatible InGaAs MOSFETs. Hence we have demonstrated InGaAs/GaAsSb heterostructure TFETs with minimum SS of 47 mV/decade, an I_{ON} of 1.5 µA/µm (at I_{OFF}=1 nA/µm and V_{DS}=0.3 V) and I_{60} of 10 µA/µm. *This is the first demonstration of sub-thermionic TFET integrated on Si (100) substrate following industry standard CMOS process steps.* An accurate positioning of the tunneling junction – with respect to the gate – has been enabled by the creation of doped extension regions and by the consequent re-growth of lattice-matched GaAsSb as source material. Sb-based compounds

are extremely sensitive to process-induced damage but the design flow has been designed to avoid any material degradation.

The designed process enabled the co-integration of TFETs and InGaAs MOSFETs on the same silicon substrate. Several studies have shown the advantages of combining the two types of devices in a TFET-MOSFET mixed circuit design. Examples are level shifters for voltage-up conversions [117] or hybrid SRAM cells [118].

The demonstrated results, although encouraging, are a preliminary proof-of-concept showing the potential of this technology. Ideally, a sub-60 SS across several orders of magnitude of current, higher I_{ON} and negligible I_{OFF} would be desirable. The still existing gap between theoretical predictions and state-of-the-art experimental demonstrations shows that several technological challenges remain unsolved.

5.1 Future Directions

This study demonstrates the strengths and limitations of III-V technologies for logic applications. Beyond the documented achievements, there are several potential improvements that could be implemented, and would benefit both TFET and MOSFET devices:

- Reducing the fin width to dimensions smaller than 20 nm would benefit the off-state performance, as demonstrated from the scaling trends shown in this thesis. Although W_{FIN} of 10 nm can potentially be achieved with the described process, their yield is affected by structural stability and excessive roughness. Alternative resists could be explored to address this problem as well as reducing the fin length.

- A reduced fin edge roughness could be achieved by introducing a crystal re-flow annealing step right after the fins dry etching or by completely replacing the dry etching process with alternative solutions such as direct fin growth or wet etching. Moreover, the fins roughness can be improved by performing some digital etching cycles (that would also enable width scaling).

- Improving the specific contact resistance (ρ_C) to the source/drain region would enable higher transconductance (g_m). Moreover, a lower ρ_C allows for contact area scaling, that is nowadays limited to about 30 nm for InGaAs, due to the maximum achievable doping concentration of about 1.4×10^{19} cm^{-3}.

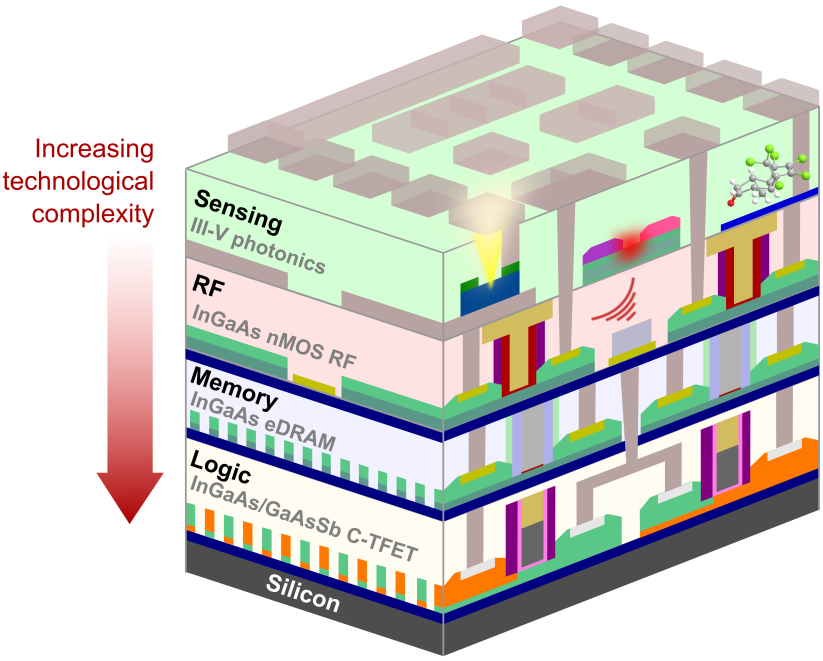


Figure 5.1 – Schematic illustration of an envisioned low-power 3D platform. III-V materials can be advantageous to each layer of this multi-functional stack. Complementary TFET-FinFET technology for the logic in the bottom layer, InGaAs-based capacitor-less embedded DRAM cells for the memory layer, NFET InGaAs planar technology for the RF module and upper sensing layer.

- An enhanced electrostatic control could be achieved by changing the channel geometry from tri-gate to gate-all-around. Obviously this would increase the process complexity. Therefore, a balance between performance and technology would be required.
- Scattering at the backside bonding interface can be reduced by engineering a layer stack that separates the channel layer from the actual bonding oxide.
- Improving the material quality, in particular reducing the interface defect density (D_{it}) between the channel and the gate oxide by optimizing the ALD process.
- Gate length scaling for TFET would represent an encouraging path towards the integration of these complex devices with ultra-scaled technology nodes. Moreover, reducing L_G would further increase the MOSFET on-current.

Further research should focus on improving the gate-stack reliability and gain a deeper understanding of long-term sources of device instabilities. But digital circuits

require complementary technologies and InGaAs does not offer the same mobility advantage for holes as for electrons. The identification of suitable material combinations for hybrid complementary technologies and the design of compatible process steps should hence be prioritized. Antimonide-based compound semiconductors show higher hole mobility, but cannot compete with germanium. Moreover, they suffer from fast non-self limiting oxidation and poor thermal stability. Hence, a full III-V CMOS logic platform seems rather unfeasible. On the other hand, the InGaAs/-GaAsSb system would be suitable for complementary TFET logic. The heterogeneous integration of different materials is therefore essential, creating unique opportunities for cost-effective techniques such as TASE. Although new device concepts and novel computing paradigms are being continuously explored, their go-to-market success rate will always be conditioned by the proven compatibility with existing silicon technologies. In this work we have tried to show how this can be achieved through careful process design, without compromising on device performance.

Although this thesis has focused on logic III-V transistors, the same technology has been shown to outperform Si devices also in terms of RF performance [119]. Moreover we have recently reported the smallest 1T capacitor-less InGaAs DRAM cell, a promising concept towards scaled embedded DRAM technologies [120]. More details about the development of this technology are available in Appendix B. Hence on-chip logic, high-frequency and optoelectronic functionalities can be foreseen, for instance pursuing a 3D sequential integration approach, where each component shares the same fabrication scheme. The illustrative example of an envisioned low-power platform, mostly based on the III-V technology shown in this work, is reported in fig. 5.1. From the top, a sensing layer can be obtained by co-integrating lasers, detectors and sensors while planar InGaAs HEMT-like transistors would be used in the RF modules for the off-chip communication. The technological complexity increases toward the bottom levels, where both e-DRAM cells and complementary TFET technology require ultra-scaled dimensions and non-planar channel geometries. Although the described overall system might sound unrealistic, the majority of its single components have already been demonstrated and they may share the same fabrication scheme, such as the one proposed in this thesis. Both RF and logic InGaAs transistors, in different measures, have now entered a phase of fine performance tuning, and whether they are ready to be turned into an industrial product is mostly a matter of economical incentives.

However, the semiconductor industry is not the only one showing interest in III-V materials. The emerging field of quantum computing is, in fact, opening up new possibilities and research directions: a quantum computing system requires cryogenic electronics to be integrated close to the qubits. III-V semiconductors show unique cryogenic properties that can be leveraged towards custom low-temperature

technologies and novel devices with new functionalities.

A Appendix A

A.1 MOSFET inverse subthreshold slope analytical derivation

In the source and drain of a MOSFET, the probability that the energy state E at given temperature T is occupied by an electron is given by the Fermi-Dirac function:

$$f_{S,D}(E) = \left(\frac{1}{1 + \frac{E - E_{F_{S,D}}}{k_B T}} \right) \tag{A.1}$$

where we identify the Boltzmann constant k_B, the elementary charge q and the energy Fermi level E_F in the source or in the drain. In a quasi-ballistic transport description, the drain current can be written as:

$$I_D \propto \int_{-\infty}^{+\infty} T(E)(f_S(E) - f_D(E))dE \tag{A.2}$$

At equilibrium, the E_F levels in the source and the drain are equal hence only in the presence of an external bias a current can flow. T is the transmission probability for the carriers to cross the potential barrier separating source and drain. In a simplified thermionic emission picture, $T(E)$ can be approximated by a step function being equal to 1 for energies above the channel conduction band maximum E^* and zero below. By replacing the current expression into the definition of inverse subthreshold slope one obtains:

$$SS \equiv \left(\frac{dlog(I_D)}{dV_{GS}} \right)^{-1} \tag{A.3}$$

$$SS = \left(\frac{ln(10)\frac{k_B T}{q} \left(1 + exp\frac{-qV_{GS}}{k_B T}\right) ln\left(1 + exp\frac{-qV_{GS}}{k_B T}\right)}{exp\frac{-qV_{GS}}{k_B T}} \right). \tag{A.4}$$

This expression is valid under the assumption that the surface potential changes proportionally with V_{GS}, hence in the subthreshold region. This expression is minimized for V_G tending to ∞ therefore, at room temperature, we can rewrite:

$$SS = \lim_{V_{GS}\to\infty} \left(\frac{ln(10)\frac{k_B T}{q}\left(1+exp\frac{-qV_{GS}}{k_B T}\right) ln\left(1+exp\frac{-qV_{GS}}{k_B T}\right)}{exp\frac{-qV_{GS}}{k_B T}} \right) = ln(10)\frac{k_B T}{q} \approx 60mV \tag{A.5}$$

This calculation, although obtained through several simple assumptions, demonstrates how MOSFET SS is fundamentally limited by the high (and low) energy tail of the Fermi-Dirac distribution and that this limitation does not depend on any material or geometrical parameter.

A.2 Transistor Body factor

The transistor body factor m describes the fraction of the total gate voltage effectively controlling the amount of electrons injected across the channel hence it is defined as $\frac{dV_{GS}}{d\Psi_S}$. Its expression can be derived by applying the simple equivalent capacitor divider model to the MOSFET, as schematized in Fig. A.1. C_{ox} is the gate oxide capacitance, C_S is the semiconductor depletion capacitance and C_{it} is particularly relevant in presences of a significant interface trap density D_{it}. Due to conservation of charge, we can write the following relation:

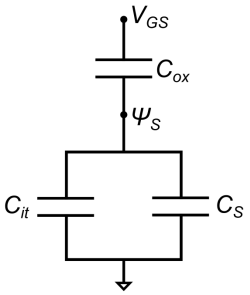


Figure A.1 – Voltage capacitor divider representation of a MOSFET.

$$Q = V_{GS}C_T = \Psi_S(C_S + C_{it}). \tag{A.6}$$

Ψ_S being the surface potential. The total capacitance C_T can be calculated as:

$$C_T = \frac{(C_S + C_{it})C_{ox}}{C_S + C_{it} + C_{ox}}. \tag{A.7}$$

Hence replacing the total capacitance in eq.A.6 we obtain:

$$\frac{dV_{GS}}{d\Psi_S} = \frac{C_S + C_{it}}{C_T} = 1 + \frac{C_S + C_{it}}{C_{ox}} \equiv m \tag{A.8}$$

A.3 Description of TFET inverse subthreshold slope

In a TFET, carriers are injected from the source into the channel through band-to-band tunneling (BTBT). As in the case of MOSFETs, carriers in the source are energetically

distributed following Fermi-Dirac statistic but only the ones with energy within a window $\Delta\Phi$ are qualified to contribute to the tunneling current (see Fig. 1.5). For instance, in the case of a pTFET, $\Delta\Phi$ correspond to the overlap between the channel valence band (E_V^{ch}) and the source conduction band (E_C^s). Hence the tunneling current can be written as [36]:

$$I_D = \frac{2q}{h} W \int_{E_V^{ch}}^{E_C^s} T(E)(f_S(E) - f_D(E))dE. \tag{A.9}$$

In this case, $T(E)$ is the BTBT transmission probability. Ideally $T(E)$ should be close to 1 in the on-state and the spatial extent of the tunneling regions (λ) must be minimized. The barrier can be reasonably approximated with a triangular potential well, using a WKB approximation [13]:

$$T_{WKB} \approx exp\left(-\frac{4\lambda\sqrt{2m^*}\sqrt{E_g^{\frac{3}{2}}}}{3q\hbar(E_g + \Delta\Phi)}\right). \tag{A.10}$$

We can hence rewrite the inverse subthreshold slope (SS) expression as function of T_{WKB}. Recalling the definition of SS

$$SS = \left(\frac{\delta log(I_D)}{\delta V_{GS}}\right)^{-1} = ln(10)\left(\frac{\delta I_D}{\delta V_{GS}}\frac{1}{I_D}\right)^{-1}, \tag{A.11}$$

we can then focus on the term expressing the change of current with the applied gate voltage:

$$\frac{\delta I_D}{\delta V_{GS}} = q\frac{\delta I_D}{\delta E_V^{ch}} = \frac{2q^2}{h}\left(\frac{\delta T_{WKB}}{\delta E_V^{ch}}F(E_V^{ch}) + T_{WKB}\frac{\delta F(E_V^{ch})}{\delta E_V^{ch}}\right) \tag{A.12}$$

where $F(E_V^{ch})$ is the integral of the Fermi distributions evaluated in the energy window $\Delta\Phi$. The two terms in Eq. A.12 identify two distinct mechanism to achieve SS below than the thermal limit. The first term dominates if the tunneling probability is small but changes rapidly with V_{GS}. In this case the SS can be approximated with the following expression:

$$SS \approx \frac{ln(10)}{q}\frac{3q\hbar(E_g + \Delta\Phi)^2}{4\lambda\sqrt{2m^*}E_g^{\frac{3}{2}}}. \tag{A.13}$$

In this case an SS below the thermal limit can be achieved only in small voltage ranges, due to the quadratic dependence of SS on $\Delta\Phi$. The other term dominates instead if T_{WKB} is close to 1, such that SS only depends on the function $F(E_V^{ch})$. By

using WKB approximation and expanding the $F(E_V^{ch})$ function for small $\Delta\Phi$ we obtain the following SS expression:

$$SS \approx \frac{ln(10)}{q}\Delta\Phi. \tag{A.14}$$

This time the SS exhibits a linear dependence on $\Delta\Phi$ therefore it ca be smaller than the thermal limit over a broader gate voltage range. This term captures the band pass filtering feature of the TFET, as the high and low tails of the Fermi function are effectively cut off by the small energy window $\Delta\Phi$. Moreover, both terms show that in presence of ideal BTBT, the SS does not have any temperature dependence.

The TFET inverse subthreshold slope is an extremely complex quantity, influenced by several material and geometrical parameters and does not have an analytical closed form. However, by simple approximations it is possible to gain deeper understanding of the major requirement to achieve a subthermionic behavior, in a relevant voltage range. More details on this derivation can be found in [36].

B Appendix B

B.1 III-V-on-Si 1T-DRAM Cells

Following the same fabrication scheme described in this thesis, we have demonstrated the smallest InGaAs-based capacitor-less DRAM memory cell [120]. The working principle of these devices is radically different from the logic transistors described until now, therefore we have chosen to not to include this topic in the main body of the thesis. Nevertheless, we will here summarize the major features of this project, that was carried on within a collaboration between IBM and University of Granada, under the European project "REMINDER".

1T memory cells make use of the floating body effect (FBE) to allow local charge storage inside the channel of a transistor. This way we can eliminate the need for an external capacitor [6] and reduce the fabrication complexity. III-V materials in a 1T DRAM cell can bring advantages in terms of band gap engineering, i.e. narrow band gap for efficient hole injection, and flexibility to heterostructure design.

The working principle of a III-V 1T DRAM cell is schematically drawn in Fig. B.1a. FBE and electrostatic coupling between the front and back-gate interfaces are the two major phenomena at stake. In write '1' operation, a negative front gate voltage (V_{FG}) induces band-to-band-tunneling on the drain side resulting in increased stored hole density in the front channel. The stored holes reduce the back-channel potential by inter-gate coupling (charge screening) causing a high current during read '1' operation. During write '0' instead, a positive V_{FG} reduces the stored hole density and a low read '0' current is measured. We have demonstrated both InGaAs cells as well as quantum-well-based InP/InGaAs implementations. It turned out that the latter design enhances the carrier retention time by separating the stored charges from recombination centers in the oxide interfaces, allowing for the lowest reported refresh power at the smallest demonstrated L_G = 14 nm for 1T-DRAM. In Fig. B.1b we report transient memory operation, using a W0, 5×R, W1, 5×R sequence with corresponding applied biases V_{FG} and V_{DS}. This result demonstrates successful memory functionality. The transient memory behavior is instead reported in Fig. B.1c. The currents evolve towards a

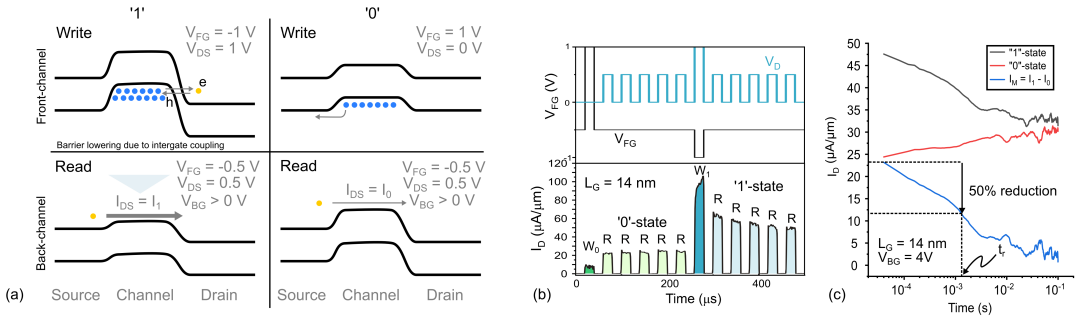


Figure B.1 – (a) Schematic illustration of 1T DRAM memory cell working principle. In write '1' operation, a negative V_{FG} induces hole population increase due to BTBT. The stored holes reduce the back-channel potential by inter-gate coupling and a high-current is measured during read '1' operation. During write '0' instead, a positive V_{FG} empties the stored holes and a lower read '0' current is measured. (b) Drain and front-gate applied bias pattern and transient drain current readout. (c) Reading current transient showing the margin between "1" and "0" state (blue) and demonstrating memory operation.

steady-state condition due to the mechanisms described above. More details about this work can be found in [120].

This work shows the promise of III-V 1T DRAMs for embedded memory applications in III-V high-frequency and future logic node technologies.

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C. Zota, **C. Convertino**, M. Sousa, D. Caimi, and L. Czornomaz, "First Demonstration of InGaAs FinFETs on Si for RF Applications," in *Compound Semiconductor Week*, 2018.

C. Zota, **C. Convertino**, D. Caimi, and L. Czornomaz, "Suppression of Band-to-Band Tunneling in III-V MOSFETs on Silicon Using Source and Drain Spacers," in *International Conference on Solid State Devices and Materials (SSDM)*, 2018.

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M. Rupakula, **C. Convertino**, H. Schmid, K. Moselund, and A. Ionescu, "High Aspect Ratio InAs-on-Insulator fins in Silicon Substrate Towards Logic Applications," in *IEEE Silicon Nanoelectronics Workshop*, 2018.

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M. Rupakula, J. Zhang, F. Bellando, F. Wildhaber, C. Convertino, H. Schmid, K. Moselund, A. M. Ionescu, "Monolithically integrated catalyst-free High Aspect Ratio InAs-On-Insulator FinFETs for pH sensing," in *2019 49th European Solid-State Device Research Conference (ESSDERC)*, 2019.

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C. Zota, T. Morf, P. Mueller, **C. Convertino**, S. Filipp, W. Riess, L. Czornomaz, "III-V-on-CMOS Devices and Circuits: Opportunities in Quantum Infrastructure," in *International Electron Devices Meeting (IEDM)*, 2019.

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Clarissa Convertino

I am a researcher in the field of ultra low-power hardware based on high-mobility compound semiconductors and 3D integration. My main research interests are nanotechnology, materials integration, microelectronics, quantum devices and solid-state physics. I am constantly seeking for new opportunities and challenges.

- PROFILE -

- PhD Candidate in Microelectronics (IBM-EPFL)
- Expert in micro-nano fabrication technology
- Broad background (electrical engineering and physics)

- ACADEMIC EDUCATION -

Sep 2016 – Present

- **PhD in Microelectronics at EPFL & IBM Zurich Research Laboratory**
  - Thesis: Advanced MOSFETs and TFETs based on high-mobility compound semiconductors for digital and high-frequency applications.
  - Involved in several EU projects (writing porposals and deliverables, preparing reviews).
  - Supervision of master student (Luca Vergano, EPFL).
  - 7 oral presentations at international conferences.

Sep 2014 – Aug 2016

- **M.Sc. Double Degree Program at Polytechnic of Turin and Paris Diderot University**
  - Main topics: physics of electron devices, quantum mechanics, and optoelectronics.
  - Highly selective program, acceptance rate of 10%.
  - Master thesis project at IBM Research (Zurich) on tunnelling devices.
  - Final grade: 110/110 with Honours.

Sep 2011 – Aug 2014

- **B.Sc. at Polytechnic of Turin**
  - Internship semester project at I.N.RI.M (Italy) on superconductivity.

- PATENTS AND PUBLICATIONS -

- 3 patent applications submitted (tunnel field-effect transistors and memory devices).
- 30+ peer-reviewed publications, 10 as first author.
- H index of 4, 40+ citations.

- RECOGNITIONS -

- Best Young Scientist Paper Award, ESSCIRC/ESSDERC 2018
- Compound Semiconductor Magazine feature, “Combining logic and wireless”, 2019
- Semiconductor Today news article, March 2019 and August 2019
- Selected as “highlight paper” at Symposia on VLSI Technology and Circuits, 2018
- EDISU Scholarship based on academic grade, obtained consecutively for 4 years, 2015
- Featuring in the Italian Register for Excellence, high school diploma with Honors, 2011

- SELECTED PUBLICATIONS -

- **C. Convertino et al.,** "InGaAs-on-Insulator FinFETs with Reduced Off-Current and Record Performance," in 2018 IEEE International Electron Devices Meeting (IEDM), p. 39.2.1-4, 2018
  - Experimental study of the influence of parasitic bipolar effect and floating body effect on the electrical performance of ultra-scaled III-V FinFETs. Highest on-current reported for III-V transistors integrated on silicon.
  - 4 citations.
- **C. Convertino et al.,** "InGaAs FinFETs Directly Integrated on Silicon by Selective Growth in Oxide Cavities," Materials., vol. 12, no. 1, p. 87, 2019.
  - Demonstration of high-performance InGaAs FinFETs on silicon by using a novel integration technique (Template-Assisted Selective Epitaxy).
  - 1 citation.
  - Invited contribution.
- **C. Convertino, et al.,** "InGaAs FinFETs 3D Sequentially Integrated on FDSOI Si CMOS with Record Perfomance," in 48th European Solid-State Device Research Conference (ESSDERC), pp. 162–165, 2018
  - Demonstration of 3D sequential stacking of III-V FETs on top of a Si CMOS pre-processed layer without affecting bottom tier functionality.
  - Selected as Best Young Scientist Paper Award
  - 4 citations.
- C. B. Zota, **C. Convertino** et al., "InGaAs-on-Insulator MOSFETs Featuring Scaled Logic Devices and Record RF Performance," in 2018 IEEE Symposium on VLSI Technology, pp. 165–166, 2018.
  - Demonstration of record f_t and f_{max} (400 and 100 GHz respectively), the highest reported for a III-V MOSFET on silicon.
  - 8 citations.
- **C. Convertino, et al.,** "III–V heterostructure tunnel field-effect transistor," Journal of Physics: Condensed Matter 30 (26), 264005, 2018.
  - Comprehensive review article describing the state-of-the-art development in the field of III-V TFET devices.
  - 9 citations.
  - Invited contribution.

SKILLS

- **IT-Skills**
  - Reactive Ion Etching, Rapid Thermal Annealing, Atomic Force Microscopy, Scanning Electron Microscopy, Ellipsometry, Metal-Organic Chemical Vapor Deposition and several CVD tools.
  - Electrical characterization: DC, pulsed, cryogenic measurements.
- **IT-Skills**
  - LateX, C++, Matlab, Phyton, Origin, LTspice, LabView, Inkscape.
- **Memberships**
  - Member of Electron Devices Society (EDS)
  - Member of EDS Young Professionals and Women in Engineering.
  - IEEE Student Member.
  - President of the PhD Students community at the IBM Research Laboratory (2017).

LANGUAGES

- Italian: mother tongue
- English: full professional proficiency
- French: B2 level
- German: A2 level