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Phosphorous-Doped Silicon Carbide as Front-Side Full-Area Passivating Contact for Double-Side Contacted c-Si Solar Cells

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Abstract*—We present an electron selective passivating contact based on a tunneling SiO_x capped with a phosphorous doped silicon carbide and prepared with a high-temperature thermal anneal. We investigate in detail the effects of the preparation conditions of the SiC_x(n) (i.e., gas flow precursor and annealing temperature) on the interface recombination rate, dopant in-diffusion, and optical properties using test structures and solar cells. On test structures, our investigation reveals that the samples annealed at temperatures of 800–850 °C exhibit an increased surface passivation toward higher gas flow ratio ($r = CH_4/(SiH_4 + CH_4)$). On textured and planar samples, we obtained best implied open-circuit voltages (i-V_{OC}) of 737 and 746 mV, respectively, with corresponding dark saturation current densities (J_0) of ∼8 and ∼4 fA/cm^2. The SiC_x(n) layers with different r values were applied on the textured front side of p-type c-Si solar cells in combination with a boron-doped SiC_x(p) as rear hole selective passivating contact. Our cell results show a tradeoff between V_{OC} and short-circuit current density (J_{SC}) dictated by the C-content in the front-side SiC_x(n). On p-type wafers, best V_{OC} = 706 mV, FF = 80.2%, and J_{SC} = 38.0 mA/cm^2 with a final conversion efficiency of 21.5% are demonstrated for 2 × 2 cm^2 screen-printed cells, with a simple and patterning-free process based on plasma depositions and one annealing step 800 °C < T < 850 °C for the formation of both passivating contacts.

***Index Terms*—Chemical oxide, passivating contact, phosphorus diffusion, refractive index, silicon, silicon carbide, silicon solar cells.**

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I. Introduction

RECOMBINATION losses occurring at the direct metal/silicon contact interfaces are the main efficiency limiting factor for industrial and laboratory scale c-Si solar cells as manifested by their suboptimal open-circuit voltages (V_{OC}) [1]–[3]. Passivating contacts provide a close to ideal scenario to obtain excellent carrier collecting and selective junctions, even when metallized. Passivating contacts consisting of doped polycrystalline silicon (poly-Si) layers that are deposited on a SiO_x layers (also known as TOPCon, POLO or poly-Si), were originally researched in the 1980s [4] and have experienced a recent revival. Variations of the concept also include the incorporation of C [5]–[7] or O atoms [8], [9] to the doped Si-based layer. The excellent passivation quality of these junctions is highlighted by the dark saturation current density (J_0), values in the range of 1–10 fA/cm^2 for electron-selective [8]–[15] and 5–15 fA/cm^2 for hole-selective junctions [5], [6], [11], [15]. Such high junction quality has enabled conversion efficiency above >25.7% [16], [17]. Poly-Si-based passivating contacts benefit from a thermal treatment at temperatures above 800 °C to obtain the required material properties and to form a shallow doped region at the wafer surface. This thermal treatment can also be used to promote crystallization of the deposited layer(s), which eventually renders them sufficiently transparent for front-side applications [18]. Moreover, the higher effective doping and larger mobility of crystalline layers [19]–[22] enable to relax constrains on the lateral conductivity of the transparent conductive oxide.

As the tunneling SiO_x does not necessarily provide sufficient surface passivation after annealing, a hydrogenation step is commonly applied to reduce the interfacial defect density. The high-temperature process required by this technology offers the opportunity to utilize existing industrial processes for material improvements, such as gettering of impurities [23]–[27] and deactivation of thermal donors [28], more difficult to implement in low-temperature passivating contacts such as the well-known silicon heterojunction [29]–[31]. An attractive approach for a lean integration of passivating contacts in solar cells consists of applying them over the *full* front and rear-side areas. This would

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enable to quench solar cell contacts recombination by means of a simple and patterning-free processing sequence. Such approach was already demonstrated on planar *n*-type wafers [32]. More recently, *p*-type front-side textured solar cells with front and rear passivating contacts with efficiencies up to 22.3% have been shown [33]. For this cell architecture, the ∼30 nm-thick phosphorous implanted front-side poly-Si resulted in limiting the J_{SC} [34]. Possible solutions to reduce parasitic absorption in the front side were explored in [8] and [9] by incorporating O atoms in the poly-Si-based layer.

In this paper, we explore partially crystallized silicon carbide layers with *in situ* phosphorous doping (SiC_x(n)) as front-side electron-selective passivating contacts. Si-C alloys offer the advantages of a tunable optical bandgap [35], [36], and high stability to wet chemistry used for cell fabrication [5], [37] motivating their application on the front side. We used parallel plate plasma-enhanced chemical vapor deposition (PECVD) as it enables a high degree of versatility for tuning of the electrical, micro-structural, and compositional properties of the deposited layer, combined with the advantage of single side processing. We report on the effect of the C-content in the front SiC_x(n) on the surface passivation, charge carrier transport, and optical transparency on test structures and solar cells. To simplify the solar cell processing sequence, the developed front-side SiC_x(n) was deposited over the full front-side textured area of p-type wafers and co-annealed with a SiC_x(p) layer, that will be presented elsewhere [38], as full area rear hole selective passivating contact.

II. Experimental

A. Test Structures

Boron-doped float zone (FZ) 4-inch shiny etched silicon wafers, <100> oriented, with a thickness of 200 μm and a resistivity of ∼2 Ω·cm were used for test structure fabrication. After KOH texturing and wet chemical cleaning, a thin SiO_x layer (∼1.3 nm) was grown by wet chemical oxidation in hot nitric acid (69% w.t at 80 °C). Afterward, a ∼12 nm thick a-SiC_x(n) layer was deposited via PECVD, at a temperature of 200 °C and a plasma frequency of 40.6 MHz on both sides of the wafer. The compositional properties of the SiC_x(n) were modified through variation of the normalized flow ratio ($r = CH_4/(SiH_4+CH_4)$). When varying *r,* the deposition time was adjusted accordingly in order to obtain the same film thickness. Subsequently, these precursors were annealed at temperatures of 800, 850, or 900 °C in a nitrogen (N_2) atmosphere for a dwell time of 8 min. Then, a hydrogenation process was applied by depositing a SiN_x:H layer as hydrogen donor and subsequently annealing it at 450 °C for 30 min (more details in [5]). After hydrogenation, this SiN_x:H layer was etched away in diluted hydrofluoric acid. Minority carrier lifetime for the symmetrical samples was measured with a Sinton WCT-100 instrument. Dark saturation current densities (J_0) were extracted by using the method of Kane and Swanson [39]. The electrically active phosphorus doping profiles were measured on planar substrates, by electrochemical-capacitance-voltage (ECV) measurements using 0.1 molar ammonium hydrogen difluoride (NH_4HF_2) solution. For the determination of their thickness and optical properties, the deposited layers were characterized using variable angle spectroscopic ellipsometry (HORIBA Jobin Yvon, UVISEL). Complex refractive indexes were extracted from fits to ellipsometry measurements with a Cody–Lorentz model of the respective layer. The external quantum efficiency (EQE) and reflectance (*R*), including metal shading losses, were measured using the Loana (pv-tools) tool, and the internal quantum efficiency (IQE) was calculated according to IQE = EQE/(1 − *R*). Raman measurements were performed by using the Mono-Vista confocal Raman system. Excitation wavelength of 266 nm (deep UV) together with textured samples were used to ensure that most of the exciting beam is absorbed in the deposited film, giving only a small contribution from the wafer. The deconvolution of the Raman spectrum gives three independent Gaussian peaks: a transverse optical (TO) mode of the nc-Si component near 520 cm^{-1}, an intermediate fraction near 510 cm^{-1}, and a TO-like a-SiC_x phase near 480 cm^{-1}. The crystalline fraction (χ) was estimated according to the following equation:

$$\chi = \frac{A_{510} + A_{520}}{A_{510} + A_{520} + A_{480}} \quad (1)$$

where A_i is the area under the Gaussian peak at wavenumber *i*.

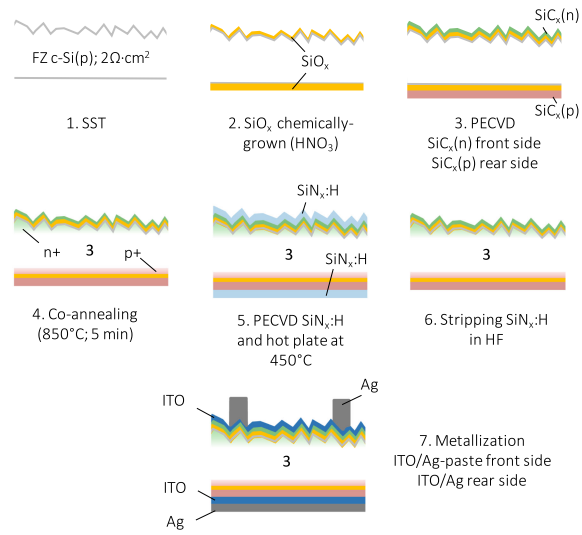

Fig. 1. Processing sequence of the solar cell employing full-area front and rear passivating contacts.

B. Solar Cells

Co-annealed solar cells (2 × 2 cm^2) employing the SiC_x(n) on the textured front side and the SiC_x(p) on the planar rear side were fabricated on the 200 μm thick, ∼2 Ω·cm p-type 4" FZ-Si, according to the processing sequence depicted in Fig. 1. After standard cleaning, surface texturing on solely the front side was performed in a KOH solution by using a protective SiN_x:H layer on the rear side of the wafer (see *step 1* in Fig. 1). This SiN_x:H layer was subsequently stripped in HF and wafers were cleaned and a chemical oxide was grown (see *step 2* in Fig. 1). PECVD deposition of the a-SiC_x(n):H and a-SiC_x(p):H were respectively applied on the entire front and rear surfaces,

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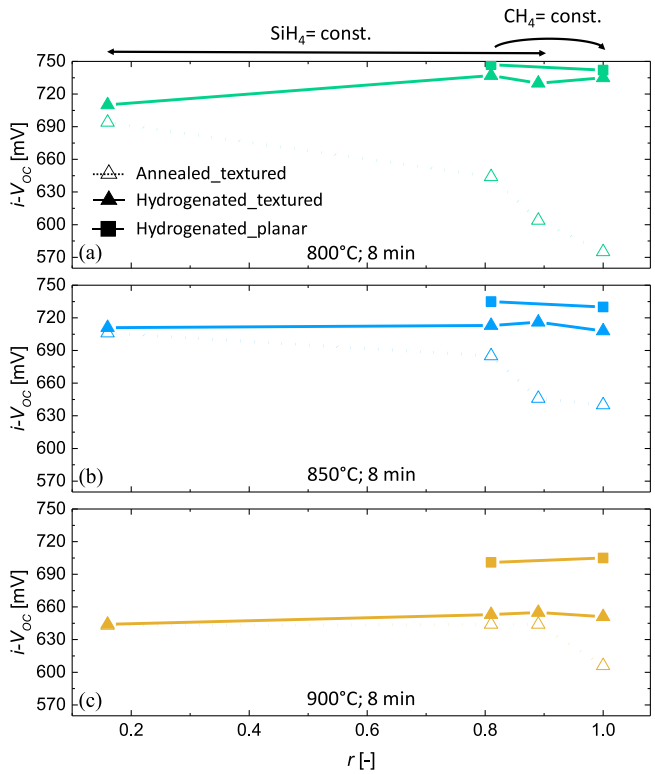

Fig. 2. i-V_{OC} as function of r for symmetrically processes samples annealed at temperatures (a) 800, (b) 850, and (c) 900 °C for dwell time of 8 min. Open triangles represent the i-V_{OC} values before hydrogenation for the textured samples. Closed triangles and squares the values after hydrogenation and stripping of the SiN_x:H for textured and planar samples, respectively. The lines are guides for the eye.

followed by a co-annealing and hydrogenation (as for the symmetrical samples), as sketched in *steps 3–6* of Fig. 1. A transparent conducting indium-tin-oxide (ITO) was sputtered on both sides of the cell precursors through aligned hard metal masks defining the cell area of 2×2 cm^2. Finally, a full area Ag layer of 0.5 μm thickness was sputtered on the rear side, while Ag metal fingers were screen printed on the front side followed by curing at 200 °C for 30 min (see *step 7* in Fig. 1). The front-side metal grid design had a coverage of ~3% excluding the busbars that were placed outside the active cell area. Current voltage (*I–V*) characteristics of the solar cells were measured at 25 °C with a source meter (Keithley, 2601A), using an AAA solar simulator (Wacom) calibrated to 100 mW cm^{-2} (1 sun) with a c-Si reference cell that has been calibrated by Fraunhofer ISE CalLab. A black hard mask covering the full wafer with a 2×2 cm^2 opening was used to define the cell area for the *I–V* measurements. Suns-V_{OC} measurements were carried out on the individual cells at 25 °C using the Suns-V_{OC} unit of a WCT-100 photoconductance tool by Sinton Consulting Inc.

III. Results

A. Surface Passivation of Symmetrical Test Structures

Fig. 2(a)–(c) depict the i-V_{OC} of the SiC_x(n)-based passivating contact as a function of r and three annealing temperatures of 800, 850, or 900 °C with a constant dwell time of 8 min, respectively. For the SiC_x(n) processed with $0.16 \leq r \leq 0.81$, the SiH_4 flow was kept constant while the CH_4 flow was increased. For the sample with $r = 1.00$, the same CH_4 flow as for the sample with $r = 0.81$, but a lower SiH_4 flow was used. Right after annealing at 800 °C, Fig. 2(a) clearly indicates a decrease in i-V_{OC}, when r is increased (open green triangles). However, after hydrogenation and stripping of the SiN_x:H (filled green triangles), the samples with $r \geq 0.81$ showed higher i-V_{OC} with respect to that of the sample with $r = 0.16$ reversing the trend observed after annealing. A very similar behavior of the i-V_{OC} as a function of r was observed for the same set of samples annealed at 850 °C, as reported in Fig. 2(b). Comparing the trends in Fig. 2(a) and (b), one can notice that before hydrogenation all samples annealed at 850 °C deliver higher i-V_{OC} than those annealed at 800 °C. Moreover, the i-V_{OC} of the samples annealed at 850 °C differ less from those after hydrogenation when compared with the same evolution at 800 °C. At 900 °C thermal annealing, regardless of r, surface passivation remains poor, with i-V_{OC} in the range of 640–660 mV even after hydrogenation.

To fully assess the surface passivation potential of our SiC_x(n) layers, we tested them also on planar p-type wafers [filled squares in Fig. 2(a)–(c)] and compared with the respective textured samples. For sake of clarity of the figure, the results are reported only after hydrogenation. The films with $r = 0.16$ applied to planar substrates are not reported as they blistered-off during the annealing. As Fig. 2(a) indicates, for both r values of the SiC_x(n), annealing at 800 °C resulted in small losses in surface passivation on textured surfaces compared with the planar ones (i-$V_{OCplanar}$ - i-$V_{OCtextured}$ $\leq$ 10 mV). Increasing of the annealing temperature to 850 °C [see Fig. 2(b)] resulted in a moderate degradation of the passivation quality between textured and planar substrates (i-$V_{OCplanar}$ - i-$V_{OCtextured}$ >15 mV). Finally, when annealed at 900 °C [see Fig. 2(c)], a significant drop in surface passivation on textured compared with planar surfaces was revealed (i-$V_{OCplanar}$ - i-$V_{OCtextured}$ > 30 mV). In summary, best i-V_{OC} of 737 and 746 mV corresponding to J_0 of ~7 and ~4 fA/cm^2 were respectively achieved on textured and planar substrates for the SiC_x(n) layer with $r = 0.81$ that was annealed at 800 °C for 8 min and hydrogenated.

B. Electrochemical Capacitance Voltage Measurements (ECV)

Electrically active P-profiles for the SiC_x(n) layers with $r = 0.81$ and 1.00 deposited on planar substrates and annealed at three temperatures (800, 850, and 900 °C) were measured by means of ECV and are reported in Fig. 3. For the SiC_x(n) with $r = 0.16$, ECVs are not reported as considered not trustworthy because of blistering. For any of the r conditions studied here, the doping profiles resulting from annealing at 800 °C could not be detected by our setup (possibly because very shallow and/or with surface concertation below the sensitivity of our system).

Comparing the profiles of the electrically active P-diffused atoms into the wafer, see Fig. 3, it appears clear that annealing at 850 °C of the samples with $r = 0.81$ and 1.00 results in similar junction depth of ~30 nm with a slightly higher surface doping concentration obtained for the film with $r = 1.00$. The figure also shows that the samples with same set of r values

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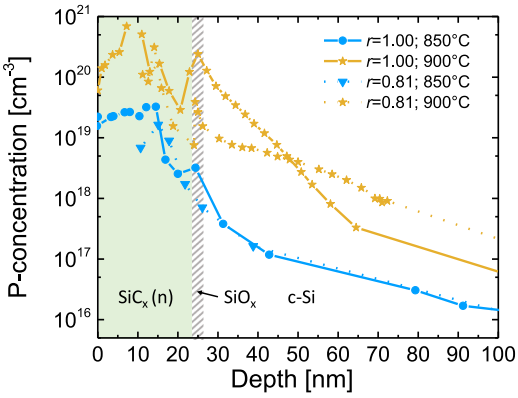

Fig. 3. ECV P-doping profiles after annealing of the SiC$_x$(n) layers with $r = 0.81$ and $r = 1.00$ at temperatures of 850 and 900 °C. The vertical shaded gray area in the plot defines the edges of the c-Si/SiO$_x$ interface.

but annealed at 900 °C have P-diffused profiles with depth of ∼50 nm, and again with a higher surface doping concentration for the SiC$_x$(n) with $r = 1.00$.

C. Raman Characterization

The microstructural analysis of the SiC$_x$(n) as a function of r and the annealing temperature was performed by means of Raman measurements on textured samples. The crystalline fraction (χ) was calculated according to (1). As depicted in Fig. 4(a), the SiC$_x$(n) with $r = 0.16$ partially crystalize already at 800 °C annealing temperature as indicated by the χ of 80% and the weak TO mode ∼480 cm^{-1}. The figure also shows that increasing of the annealing temperature does not significantly affect the Raman spectra. On the contrary, Fig. 4(b) indicates that the SiC$_x$(n) prepared with an $r = 0.81$ remains partially amorphous when annealed at 800 °C. In addition, its film crystallinity increases from 17% to 77%, when the annealing temperature is raised from 800 to 900 °C. Finally, the SiC$_x$(n) with $r = 1.00$ presented low χ (<50%) independently of the annealing temperature, see Fig. 4(c).

D. Ellipsometry Measurements

Fig. 5(a) and (b) illustrate the refractive index n and extinction coefficient k, respectively. The data are relative to ∼12 nm thick SiC$_x$(n) layers with $r = 0.81$ and $r = 1.00$ deposited on planar wafers (the results for $r = 0.16$ are not reported due to layer blistering) that have been annealed at 800, 850, or 900 °C. The figures show a significant decrease of n and a slight decrease of k for wavelengths above 300 nm when r is increased. This is a clear indication that the layer with $r = 1.00$ has a higher C-content compared with the one with $r = 0.81$. Additionally, for a given r, increasing of the annealing temperature also slightly reduces the n and k values. This effect appears to be more prominent for the samples with $r = 0.81$.

E. Measured Solar Cell J–V Parameters

Solar cells employing the electron selective SiC$_x$(n) on the front textured side, co-annealed with the hole selective SiC$_x$(p)

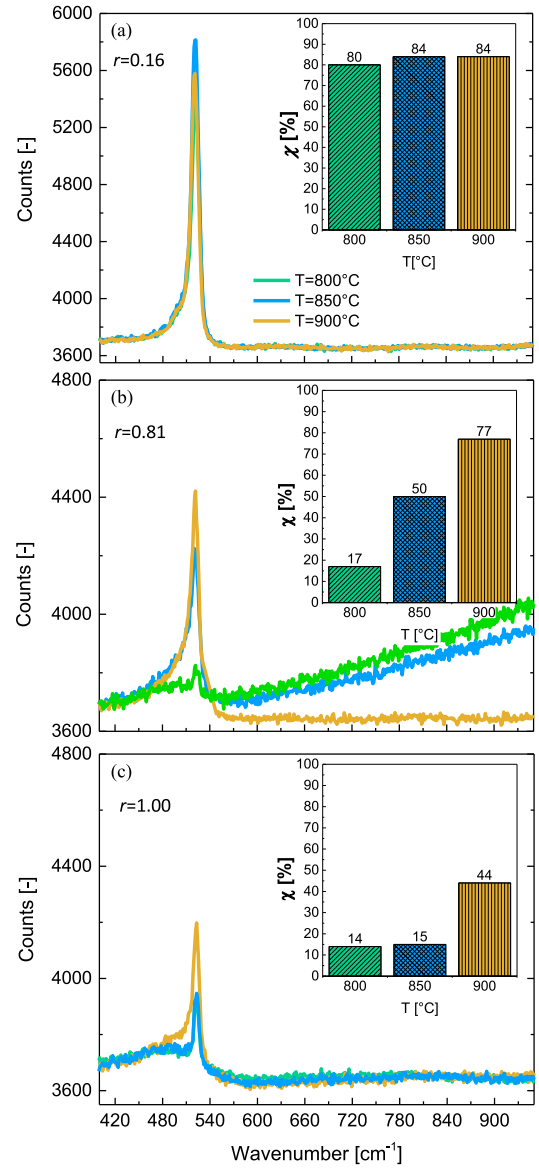

Fig. 4. Raman spectra for the SiC$_x$(n) annealed at 800, 850, and 900 °C with (a) $r = 0.16$, (b) $r = 0.81$, and (c) $r = 1.00$. The inset represents the calculated crystallinity fraction (χ) at 800 °C green with oblique pattern, 850 °C blue with crossed pattern, and 900 °C dark-yellow with vertical pattern.

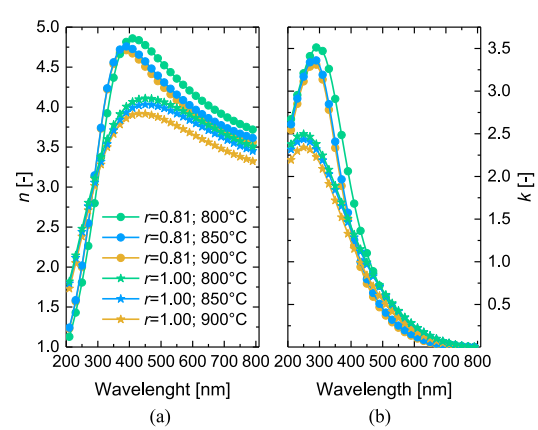

Fig. 5. (a) Refractive index n and (b) extinction coefficient k, of ∼12 nm thick SiC$_x$(n) layers with $r = 0.81$ and $r = 1.00$ annealed at 800, 850, and 900 °C.

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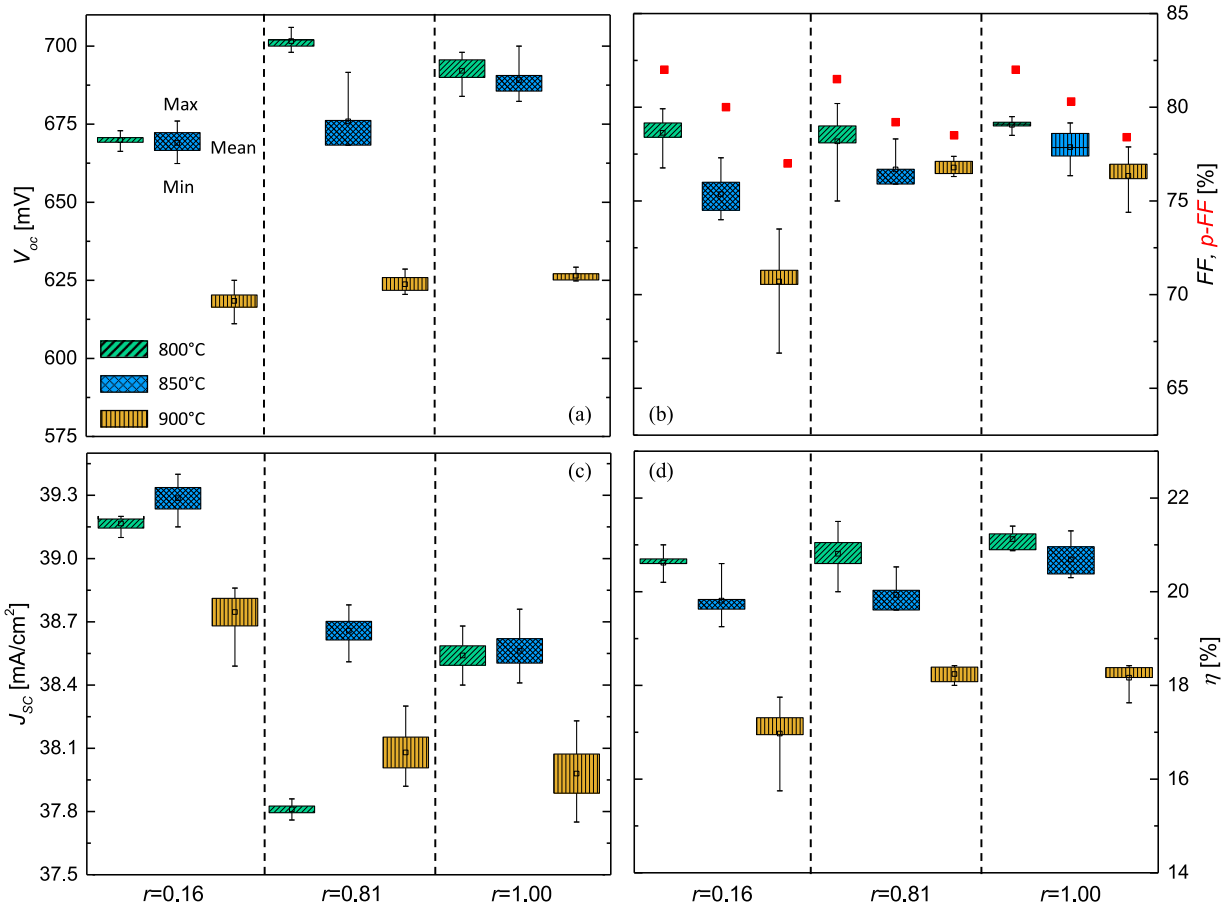

Fig. 6. Box plot of measured *J*–*V* parameters of solar cells with co-annealed carrier selective SiC_x-based junctions on both wafer sides. (a) V_{OC}, (b) FF and *i*-FF, (c) J_{SC}, and (d) η as function of *r* and annealing temperatures of 800 °C (green with oblique pattern), 850 °C (blue with crossed pattern), and 900 °C (dark-yellow with vertical patter). Red squares in (b) indicate the pseudo FF (*p*-FF) as extracted from SunsV_{oc} measurements. In the box plots, the square defines the mean value and the horizontal tick marks the maximum and minimum value of the respective distribution.

on the planar rear side were fabricated. Three values of *r* for the front SiC_x(n) (0.16, 0.81, 1.00) and three annealing temperatures (800, 850, and 900 °C) with a constant dwell time of 8 min were considered. For the rear side SiC_x(p) J_0 of 6, 12, and 20 fA/cm^2 were obtained on symmetrical test samples after annealing at 800, 850, and 900 °C for 8 min and hydrogenation, respectively. Fig. 6(a) shows that for the solar cells annealed at 800 °C the mean V_{OC} peaks for the SiC_x(n) with $r = 0.81$ reaching the best value of 706 mV. When annealing at 850 °C, the mean V_{OC} value increases toward higher *r* with highest V_{OC} of 700 mV obtained for the SiC_x(n) with $r = 1.00$. As expected from the lifetime samples, the cells annealed at 900 °C delivered low V_{OC} values regardless of *r*. Overall, the measured V_{OC} values followed the *i*-V_{OC} trends as a function of *r* and annealing temperature as reported in Fig. 2(a)–(c). In Fig. 6(b), we report the FF and *p*-FF trends for the fabricated set of solar cells. The figure indicates that the cells annealed at 800 °C have similar mean values of the FF for all three *r* values. Best FF = 80.2% was obtained for the SiC_x(n) with $r = 0.81$. Interestingly, even for more C-rich layers ($r = 1.00$), FF values above 79.5% were obtained. The cells annealed at 850 or 900 °C showed an increase of the FF toward higher *r* values but were overall on a lower level compared with that annealed at 800 °C. This effect seemed to be linked to the lower *p*-FF [red squares in Fig. 6(b)] obtained when annealing at higher temperature, suggesting that FF degradation is rather recombination than series resistance driven.

The J_{SC} values, including the optical shading losses of the metal grid (∼3%), of the fabricated solar cells as function of *r* and the annealing temperature are reported in Fig. 6(c). The figure indicates that the mean value of J_{SC} for the cells annealed at 800 °C has a maximum of 39.2 mA/cm^2 at $r = 0.16$ and a minimum of 37.8 mA/cm^2 at $r = 0.81$. Increasing of the annealing temperature to 850 °C only slightly increases the mean J_{SC} of the cells with $r = 0.16$ and $r = 1.00$. Whereas, a significant boost in J_{SC} (> 1 mA/cm^2) was observed for the cells with $r = 0.81$. Fig. 6(c) also shows that for a given *r* value the lowest J_{SC} values are measured for annealing temperature of 900 °C.

The η trends as a function of *r* and annealing temperature are presented in Fig. 6(d). The devices annealed at 800 °C show a slight increase in the mean η toward higher *r* values with the highest value of 21.5% achieved at $r = 0.81$. The cells annealed at 850 °C show a similar trend of the mean η, but with lower

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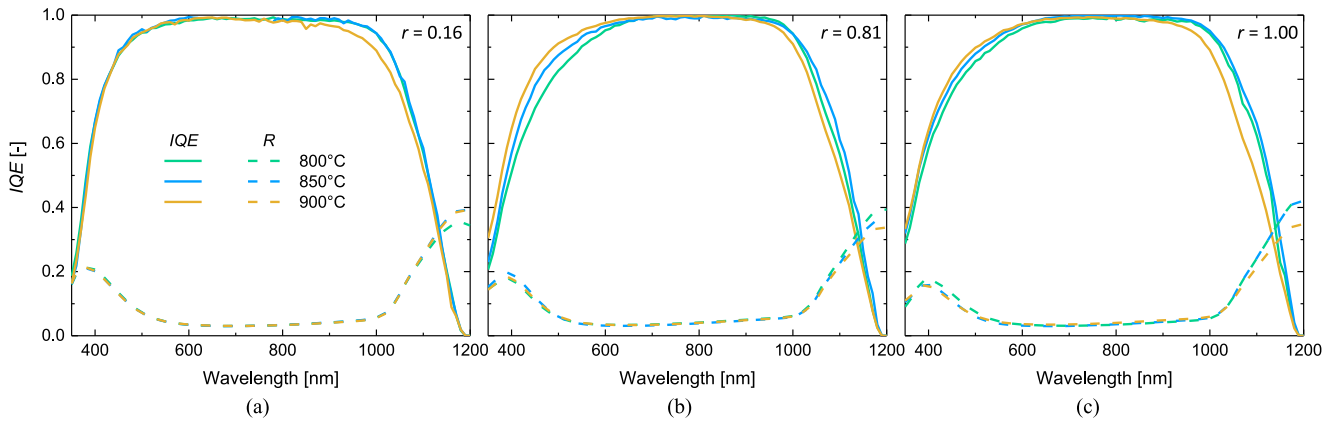

Fig. 7. Measured IQE and R for both sides SiC_x-based solar cells co-annealed at 800, 850, and 900 °C. Front-side SiC_x(n) with $r = 0.16$ in (a), $r = 0.81$ in (b), and $r = 1$ in (c).

TABLE I
SUMMARY OF THE BEST SOLAR CELL PARAMETERS AS FUNCTION OF r AND AFTER ANNEALING AND HYDROGENATION

r [-]	T_{ann} [°C]	V_{OC} [mV]	FF [%]	J_{SC} [mA/cm^2]	η [%]
0.16	800	670	79.9	39.3	21.0
0.81	800	706	80.2	38.0	21.5
1.00	800	698	79.0	38.5	21.4

The cells are screen-printed with a metallization fraction of ~3% and have an area of 2 × 2 cm^2.

absolute values compared with those annealed at 800 °C. In this case, a best efficiency of 21.0% was obtained at $r = 0.16$. As expected, at 900 °C, low conversion efficiencies are obtained regardless of r. Table I summarizes the solar cells parameters of the best cells annealed at 800 °C.

F. Internal Quantum Efficiency (IQE) and Reflectance (R)

R and IQE measurements of the cells employing the front SiC_x(n) grown with three r values (0.16, 0.81, and 1.00) and annealed at 800, 850, and 900 °C are reported in Fig. 7(a)–(c). As the figures show the IQE response at short wavelengths of the cells with SiC_x(n) with $r = 0.16$ is almost independent on the annealing temperature, whereas for those with $r = 0.81$, a clear increase toward higher annealing temperature is observed. Finally, for the solar cells with SiC_x(n) with $r = 1.00$, a weak dependence of the blue IQE response as function of the annealing temperature was observed. It is worth noticing that for a given r value all devices processed at 900 °C exhibit a decrease of IQEs in the infrared-region, which can be explained with a degradation of the passivation quality of the rear SiC_x(p).

IV. DISCUSSIONS

A. Surface Passivation and ECV Doping Profiles

The decrease in i-V_{OC} toward higher r values for the as-annealed samples [open symbols in (a)–(c)] can be explained with several effects such as higher defect density and lower crystallinity fraction (see Raman in Fig. 4) typical for C-rich layers [35], [40] with the latter also influencing P-diffusivity into the wafer [41]. In particular, as for Si-rich layers ($r = 0.16$), crystallization occurs during annealing [see Raman in Fig. 4(a)], the grain boundaries act as high diffusivity channels for a rapid supply of dopants into the substrate. Therefore, deeper and stronger doped in-diffused regions (in the c-Si wafer surface) can be expected compared with C-rich SiC_x(n) layers. Based on this, we speculate that for Si-rich SiC_x(n) layers minority carriers are better shielded by the in-diffused region from the electronic defects at SiO_x/c-Si interface explaining the i-V_{OC} of ~700 mV obtained even without hydrogenation. Moreover, in the as-annealed state (for temperatures between 800 and 850 °C), the samples with $r = 1.00$ exhibit lower i-V_{OC} with respect to the ones with $r = 0.81$ despite their slightly larger surface concentration (see Fig. 3). A possible explanation for this is given by the fact that the beneficial electrical shielding of the c-Si/SiO_x interface (because of the higher surface concentration) is overcompensated by the larger defect density typical of C-rich SiC_x(n) [35], [40]. The expected stronger in-diffused regions for the SiC_x(n) with $r = 0.16$ might also be responsible for the little improvements in i-V_{OC} after hydrogenation as they may set an upper limit to the overall junction recombination rate. On the contrary, the i-V_{OC} of SiC_x(n) with $r \geq 0.81$ and annealed between 800 and 850 °C is strongly boosted by the hydrogenation process, suggesting that the overall surface passivation is driven by the chemical passivation mechanism. As for the low i-V_{OC}, measured for the samples annealed at 900 °C, even after hydrogenation, we believe that partial or total disruption of the interfacial SiO_x has occurred, leading to a permanent degradation of its passivation properties of c-Si surfaces. The explanation for larger difference between the i-V_{OC} values between planar and textured samples with increasing of the annealing temperatures [see (a)–(c)] is not clear yet and requires further investigation.

As the flow ratio and the annealing temperature of the SiC_x(n) affects the film microstructure with the latter also influencing the sputtering rate during the ECV, we only discuss the P-diffused doping profiles into the wafer. For both annealing temperatures of 850 and 900 °C, Fig. 3 shows a higher P-concentration at wafer surface for the sample with $r = 1.00$ compared with $r = 0.81$. This could be associated to a more efficient doping

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incorporation as the SiH_4 flow is reduced. The origin for the crossover of the doping profiles occurring at a depth of >35 nm for the samples annealed at 900 °C is unclear and requires a deeper investigation.

B. Influence of C-Content on Layer Crystallinity and its Relation to Solar Cell Performance

The Raman analysis reported in Fig. 4 allowed us to conclude that the originally purely amorphous Si-rich layers with $r = 0.16$ are partially crystallized already by the 800 °C annealing treatment, whereas the layer with the highest C-content ($r = 1.00$) remains to a large extent amorphous even when annealed at 900 °C. Those results confirm the trend observed before, that C-addition to amorphous Si layers hinders crystallization [42]. Furthermore, the absence of the Raman peak between 750 and 950 cm^{-1} associated with the formation of crystalline silicon carbide (c-SiC) phase [43] indicates that our nc-SiC_x(n) films consists of nc-Si grains embedded in a-SiC_x matrix. As result, the positive effect of a wider bandgap due to C-incorporation is overcompensated by the higher absorption coefficient due to the amorphous lattice. Fig. 6(a) and (c) clearly indicate a tradeoff between V_{OC} and J_{SC} due to C-addition to the Si network. In particular, for a given annealing temperature, best J_{SC} is obtained for the more crystalline SiC_x(n) processed with $r = 0.16$.

On the contrary, incomplete layer crystallization due to C-addition has a positive effect on the cell V_{OC}. Among with preventing crystallization, C-incorporation in a-SiC_x:H is also known to shift the valence band edge to higher energy while leaves the energetic position of the conduction band virtually unaffected [44], [45]. Therefore, we argue that electron transport through the SiC_x(n) is largely unaffected by the carbon content [see Fig. 6(b)]. On the contrary, according to the Boltzmann distribution, the density of holes reaching the SiO_x interface decreases exponentially with the band bending [46]. After that, carriers have to overcome the barrier associated to the potential drop across the interfacial oxide and an additional barrier associated to the valence band offset before they can tunnel into available states in the valence band of the doped SiC_x(n) layer and recombine at metal contact. Based on this, we expect a decrease of the recombination rate of holes with increasing of the valence band offset dictated by C-incorporation.

In summary, we speculate that C-incorporation fosters V_{OC} but increases parasitic absorption losses, both effects being mediated by the hindered layer crystallization.

C. Optical Simulations

The evaluation of the optical losses in our front-side SiC_x(n) was performed by means of optical simulations with OPAL2 [47]. The simulated optical system was formed of a 72 nm thick ITO and ~12 nm thick SiC_x(n) described by the *n and k* data reported in Fig. 5(a) and (b). A good fit between measured and simulated IQEs was observed, as shown in Fig. 8(a). Measured and simulated *R* were also in good agreement, but are omitted from Fig. 8(a) for the sake of clarity. Since *n* and *k* data were not measureable for the layer with $r = 0.16$, due to layer blistering,

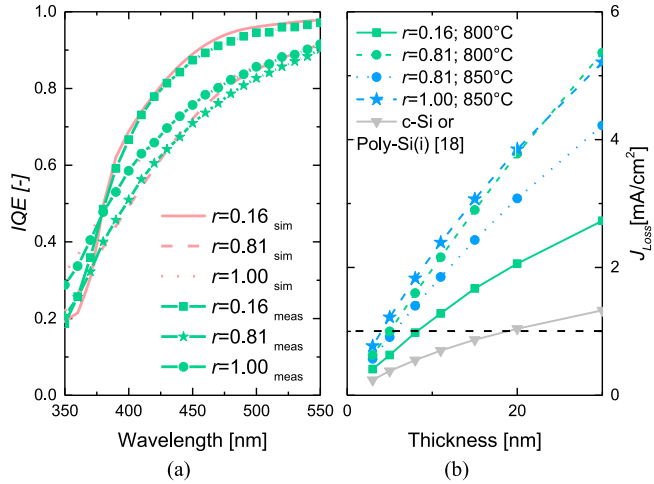

Fig. 8. (a) Measured and simulated IQE as function of *r* for the solar cells annealed at 800 °C. (b) Optical simulations of current density losses (J_{Loss}) as a function of the SiC_x(n) layer thickness, *r* value and annealing temperature. The horizontal dashed black line in (b) indicates the J_{Loss} target of 1 mA/cm^2.

because partially crystalline it was modeled as a stack of layers composed of c-Si and a-Si. The thicknesses of those layers were used as free parameters. A good fit between the simulated and measured characteristics was achieved when using 6.5 nm of c-Si and 2.5 nm of a-Si. Confident that our *n* and *k* data are trustworthy, we have performed optical simulations to identify the maximum layer thickness ensuring that short-circuit current density losses (J_{Loss}) induced by the front SiC_x(n) layer remain below 1 mA/cm^2. This study was performed for the layers annealed at temperatures of 800 and 850 °C as those were the most promising in terms of surface passivation. As lower limit for the parasitic absorption, we considered the case in which the front-side layer has the same complex refractive index as c-Si. In the best scenario, this is the case for intrinsic poly-Si (poly-Si(i)) [18]. Structural defects and grain boundaries in the poly-Si can result in higher parasitic absorption [48]. As Fig. 8(b) indicates, the thickness of the SiC_x(n) layer with $r = 0.16$ has to be reduced down to 10 nm to meet the target of $J_{Loss} < 1$ mA/cm^2, whereas thicker layer up to 20 nm can be afforded for the reference poly-Si case, thanks to its higher optical transparency. For the layers with higher *r* values, it needs to be further thinned down to ~6 nm.

V. Conclusion

In this paper, we have demonstrated phosphorous-doped SiC_x(n) layers as front-side passivating electron-selective junction. We show that increasing of *r* of the SiC_x(n) resulted in an increase of the surface passivation quality. On test structures, *i*-V_{OC} values up to 737 mV on textured surfaces and up to 746 mV on planar surfaces were achieved. Annealing at a temperature of 850–900 °C resulted in significantly lower passivation quality for textured compared with planar surfaces. The developed SiC_x(n) layers were integrated on the textured front side of p-type c-Si solar cells and co-annealed with a passivating SiC_x(p) rear contact. Our results suggest that widening of the band gap due to C-incorporation is not sufficient to compensate the

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negative effect of a higher absorption coefficient due to incomplete layer crystallization. Conversely, we speculate that surface passivation quality of C-rich SiC_x(n) benefits from another degree of passivation provided by the valence band offset linked to incomplete layer crystallization. For Si-rich SiC_x(n) layers, J_{SC} up to 39.4 mA/cm^2 was obtained, which is the highest value reported so far for this kind of solar cell architecture with a full front-side high-temperature passivating contact. Charge carrier transport was not substantially affected by the C-content in the layer as FF values up to 80.2% were reached also for more C-rich layers. With this simple solar cell architecture based on full-area processes and only one high-temperature thermal treatment, we demonstrated conversion efficiencies up to 21.5%. Finally, our optical simulations indicate that reducing front-side parasitic absorption related J_{SC} losses below 1 mA/cm^2 could be achieved for 10 and 6 nm thick SiC_x(n) layers that are Si-rich ($r = 0.16$) and C-rich ($r = 1.00$), respectively.

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