EPFL
Advanced NEMS Group

2D Material-Metal contact resistance measurement

Ti-Graphene contact with different cleaning methods

Author : **Frédéric Junod**

Supervisor : **Tom Larsen**

Professor: **Guillermo Villanueva**

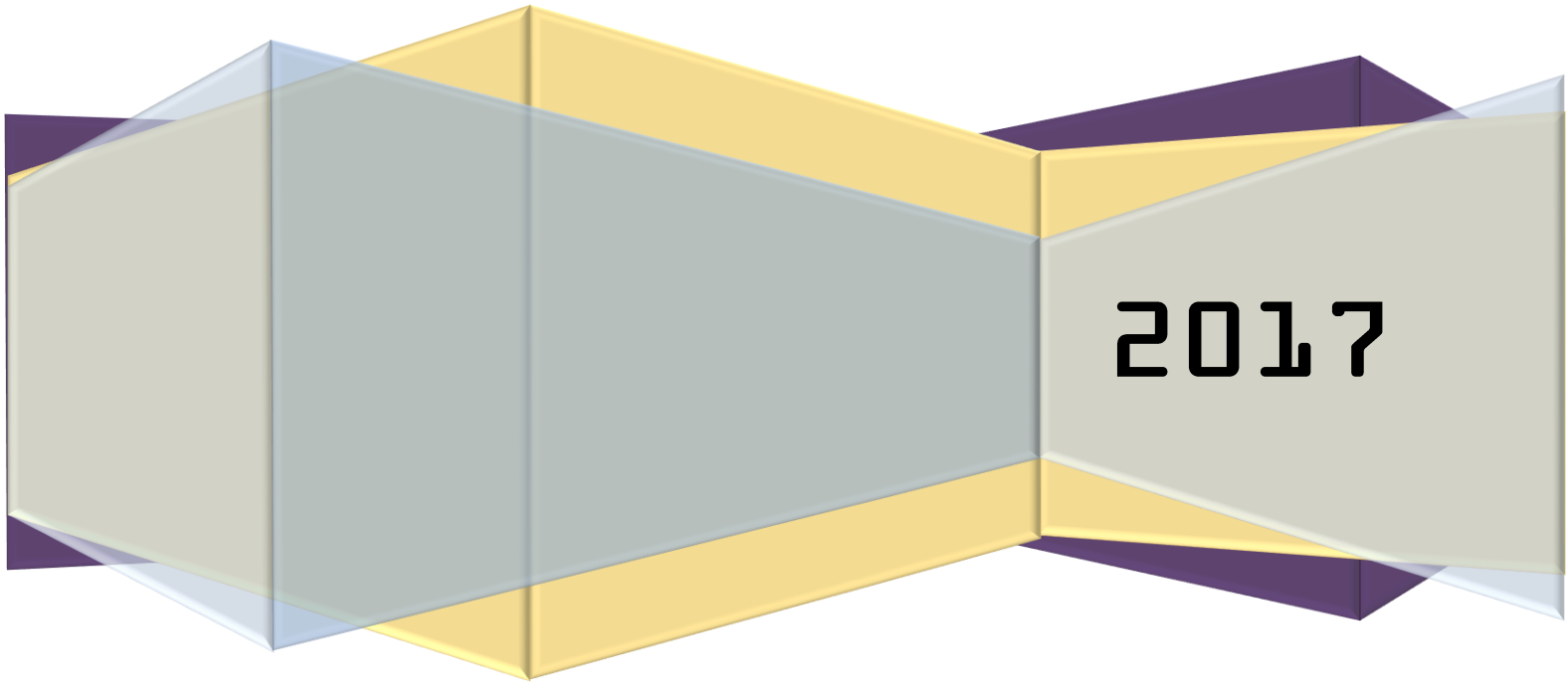


Table of Contents

1. ABSTRACT 2

2. INTRODUCTION 3

3. PRINCIPLES 5

3.1. STATE OF THE ART 5
3.2. DESIGN 8

4. FABRICATION 12

4.1. PROCESS FLOW 12
4.2. MASKS DESIGN 14
4.3. ISSUES ENCOUNTERED 16
4.4. RESULTS 20

1. MEASUREMENTS AND ANALYSIS 23

1.1. MEASUREMENTS 23
1.2. ISSUES ENCOUNTERED 24
1.3. RESULTS 25

1. PERSPECTIVES 28

2. CONCLUSION 29

3. REFERENCES 30

4. APPENDICES 31

4.1. PROJECT SPECIFICATIONS 31
4.2. PROCESS FLOW 33
4.3. DESIGNS AND CHIPS DISTRIBUTION 36
4.4. MEASUREMENTS TABLES, GRAPHS AND RAW RESULTS 37

1. Abstract

Metal/graphene contact resistance is becoming a major limiting factor in the creation of graphene devices. In this report, we will study and refine the whole process flow towards the creation of graphene devices meant for contact resistance measurements.

We first defined a new modified structure called "**Modified Transmission line model**" combining two different kinds of resistance measurements in order to get more reliable results.

We then create different chips with different methods and tests such as dose tests in order to redefine a given process flow. We mainly improve the graphene sheet etching as well as the resist stripping in the graphene patterning process. We expose the choice of Acetone as the resist stripper instead of 1165 remover as **we get more than twice as many suitable results with Acetone than 1165 remover**. But we see that the main defect factor of defects in the graphene sheet is the deposition step.

Finally we expose the results of contact resistivity measurements on differently created "modified TLM" devices and obtain values starting at 80 x 10^{-6} $\boldsymbol{\Omega\, cm^2}$, higher than collected literature values, due to too few usable chips.

2. Introduction

Graphene is a hexagonally-organized form of carbon. Its special structure allows it to be used in layers down to one atom thick and makes it an incredible 2D material with exceptional electrical, optical, mechanical and thermal properties. But although Graphene presents a bright future for electronic devices, there is an obstacle on the way, Metal-graphene contact resistance. Reducing that contact resistance is of great importance for any applications of graphene sheet structures.

In this project, we aim to optimize the contact resistivity between 2D materials (graphene) and metal. In order to do that, we will test different designs to measure the contact resistivity for different deposition methods and cleaning and etching methods. Original specifications of the project are to be found in Appendix1.
This project presents the particularity of studying metal-graphene device with graphene deposited on top of metal contacts, unlike any measurements in the literature.

We first chose a special design in order to have the best possible resistivity measurements and we took 4 declinations of this design. The design is inspired by the Transmission Line Measurement Model (TLM) that we modified for the purpose of better results.

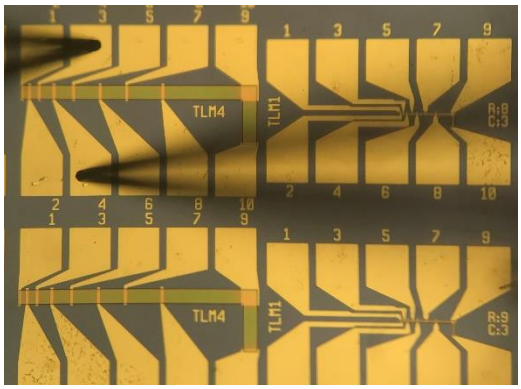
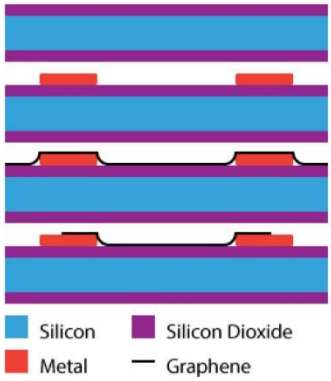


Figure 1 Close-up of one of the fabricated chips

We started from a pre-designed process flow that we modified partly to get better results and finally came up with a well-designed process flow for graphene circuit creation.



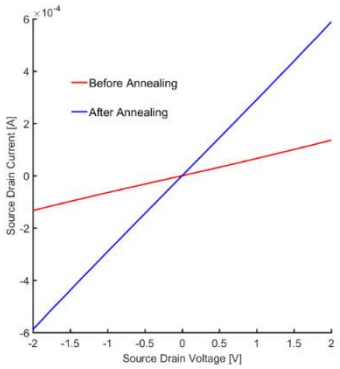


Figure 2

Appendix1:

(left) Fabrication of test structures. Metal electrodes is defined via lift-off on a silicon wafer silicon dioxide. Graphene is transfer onto of the wafer and patterned by oxygen plasma using photoresist as an etch mask.

(right) IV curves of graphene contacted with gold electrodes before and after annealing. Annealing was performed at 400°C for 8 hours in a hydrogen and argon atmosphere.

Unfortunately some of the original specifications and objectives couldn't be met within the time of this project. We will see that some changes and problems occurred in the process flow and lead to longer steps and loss of time in the process.

3. Principles

3.1. State of the art

The great intrinsic performance of graphene transistors is masked by the high contact resistance that is currently the greatest electric current limiting factor (up to 2 orders of magnitude larger than graphene sheet resistance).

The research on the contact resistance has already been explored by some people in different papers, and this project aims to compare any measured result with the known contact resistance literature values. This way we can also test the quality of the process and specifically of the graphene on top of metal contacts (all gathered literature values used contacts on top).

There are different ways to perform the contact resistivity measurement. In this paper we will focus on the Transmission Line Measurement model (TLM) (See figure below).

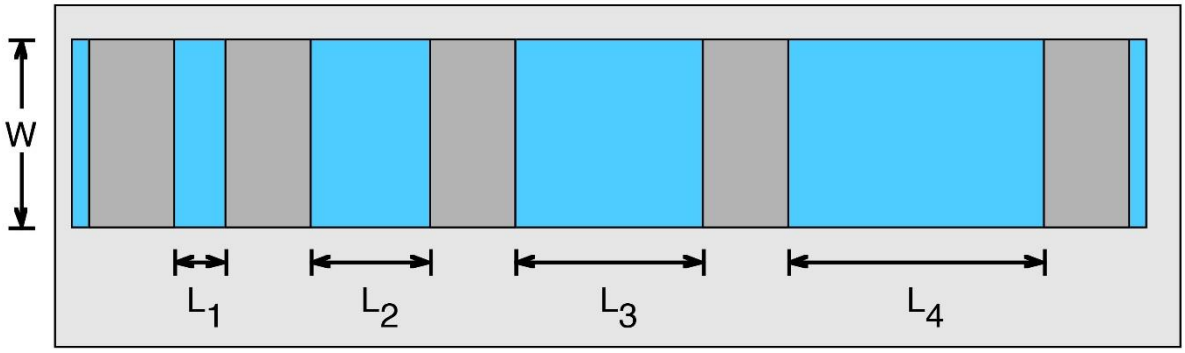


Figure 3 Transmission Line Measurement model (TLM) Grey: metal contacts, Blue: graphene sheet. ref. [3]

In order to have a reliable measurement of the contact resistance, we will have a design with different distances between the metal contacts. We will then measure the resistance of each of these lengths, plot them on a graph and from there we will be able to determine the Contact resistance.

The resistance between 2 contacts can be represented as follows (figure below):

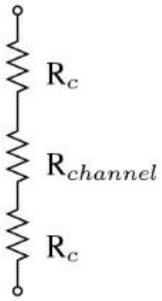


Figure 4 Resistance representation of a graphene channel between two metal contacts. ref. [13]

And we can deduce for the total resistance:

$$R_T = R_{graph} + 2R_C \quad (1)$$

Having the total resistance [1], and the graphene sheet resistance (R_{sh}), we can deduce the contact resistance ($2R_C$). To do that, we plot the measured resistance for every different length of a design (same width W), make a linear regression on the values and we obtain $2R_C$ at $L = 0$. (See figure below)

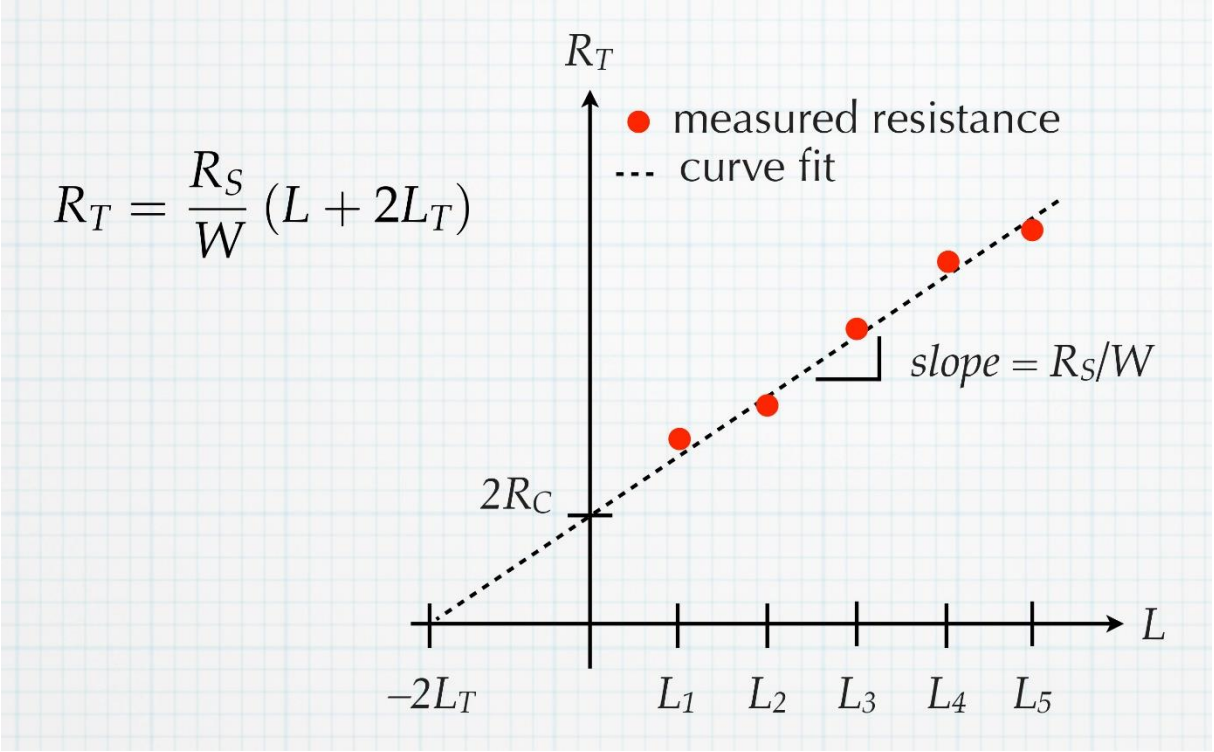


Figure 5 Contact resistance and TLM measurements, plot of total R. ref. [3]

From these measurements, and as it appears on this graph, we can also obtain the transfer length (L_T) which is the average distance that an electron travels in the graphene over the contact before it flows into the contact. This value can lead us to the contact resistivity by the relation [2].

$$L_T = \sqrt{\frac{\rho_C}{R_S}} \quad (2)$$

From relations [2] and R_T equation, we can deduce

$$\rho_C = R_C L_T W \quad (3)$$

In order to perform our measurements and to be able to analyze them correctly, we gathered different values from previous measurements done by different teams and published in different papers with different conditions and designs.

The gathered values for contact resistance in the referenced literature are listed in table 1.

Metal/Graphene	$\boldsymbol{\rho_C}$	*References*
Pd	~230 Ω µm²	[5]
Ni	500 Ω µm²	[13]
Ti	> 1000 Ω µm²	[13]
Ti	< 250 Ω µm² (liquid helium temp.)	[10]

Table 1 Collected litterature values for contact resistivities at room temperature

We can see out of this table that the result can vary widely. This is due to many different things. First the temperature has shown to be a great changer in the different resistances

Voltage range, graphene deposition quality, graphene sheet size and quality, annealing as well as cleaning methods could vary and are of significant impact on the contact resistance of the different designs. Even between 2 devices with the exact same design we can see significant differences as we can see in the following figure.

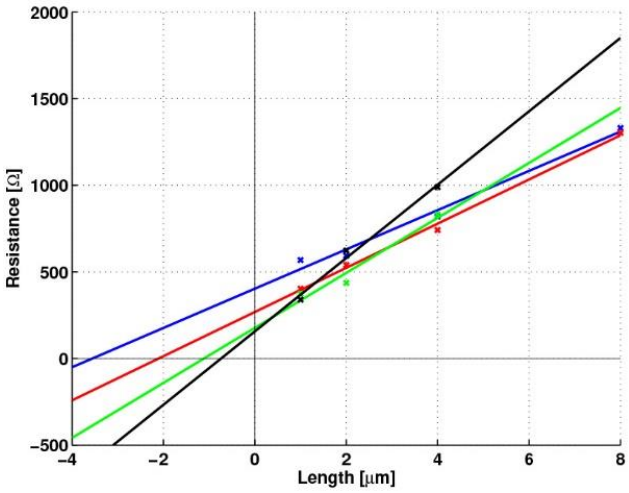


Figure 6 Resistance measurements results on different TLM structures for the different length (same Width). Ref. [13]

3.2. Design

One of the crucial part in order to start any measurement campaign is to have a well-defined design. In the literature, we can find plenty of different designs used for contact resistance measurements, such as traditional TLM, probably the most common but also four probe structure.

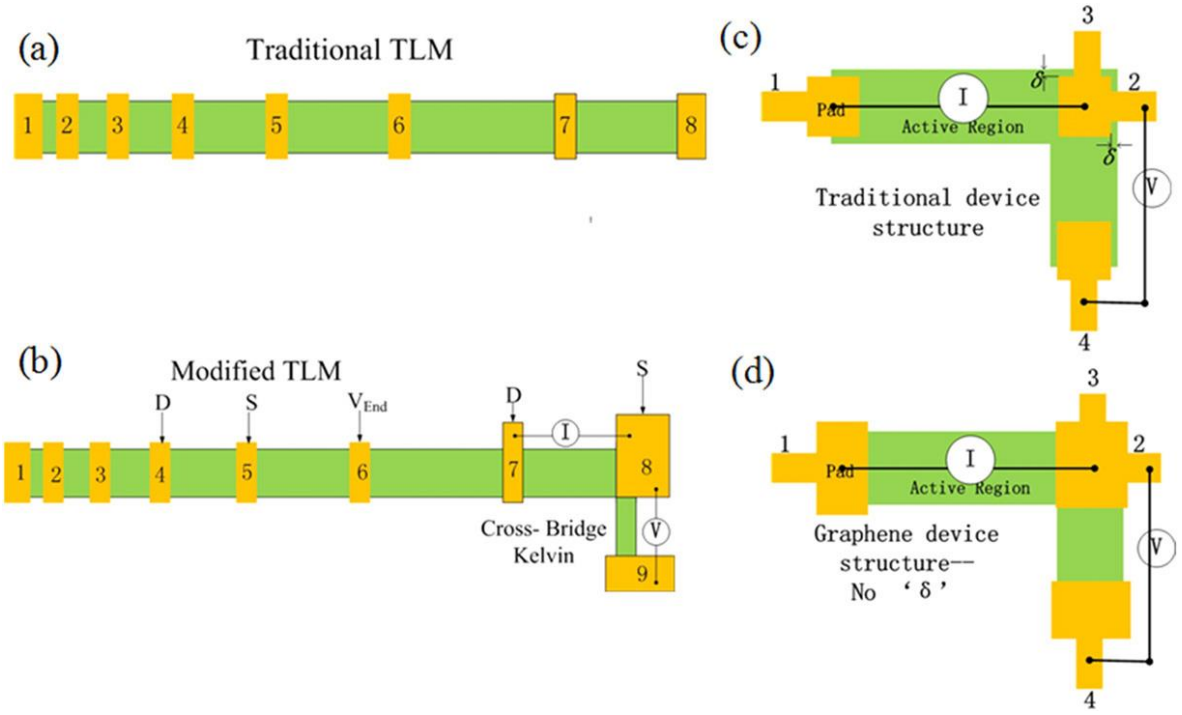


Figure 7(a) The traditional TLM structure, (b) the modified TLM structure, (c) the traditional four-terminal Kelvin test structure and (d) the four-terminal Kelvin test structure of graphene devices. ref. [2]

They all have pros and cons but based on the work of the institute of Microelectronics at the Chinese academy of science (ref [2]), we decided to incline for a new design that could be called “modified TLM”. To make this design, we started from a classic TLM structure to the right end of which we added a cross-bridge structure. According to ref [2], this modified TLM has proved to give more reliable values and to grant access to contact-related parameters such as transfer length and graphene sheet resistance over and outside the contact metal at the same time. Table 2 gives literature values obtained with 2 modified TLM designs (they will be just called TLM in this report).

T (K)	R_{CE} (Ω)	R_{Kelvin} (Ω)	L_T (μm)	ρ_c ($\Omega \cdot \mu m^2$)	R_{SK} ($\Omega \cdot \mu m^2$)
290	5.21	15.42	1.72	298.83	101.50
180	3.93	10.15	1.87	210.27	62.93
140	3.65	9.95	1.81	200.77	61.50
100	3.31	9.67	1.73	188.67	59.98
60	3.21	9.02	1.77	179.11	57.15

Table 2The contact resistances and other parameters at different temperatures. ref. [2]

In our case, we created 4 different designs with different widths (W) and different lengths (L). The figure below gives an example of our chosen design. Table 3 gives all dimensions for our four different TLM designs. The dimensions were chosen very small for TLM1 and 2, limited by the resolution of the photoresist LASER writer (MLA 150), but also very close to the designs used in ref [2] to have a comparison point for the measurements. And larger for TLM3 and 4 (up to 6 times larger) to reduce measurement problems due to potential poor quality of the graphene layer or by any photolithography error.

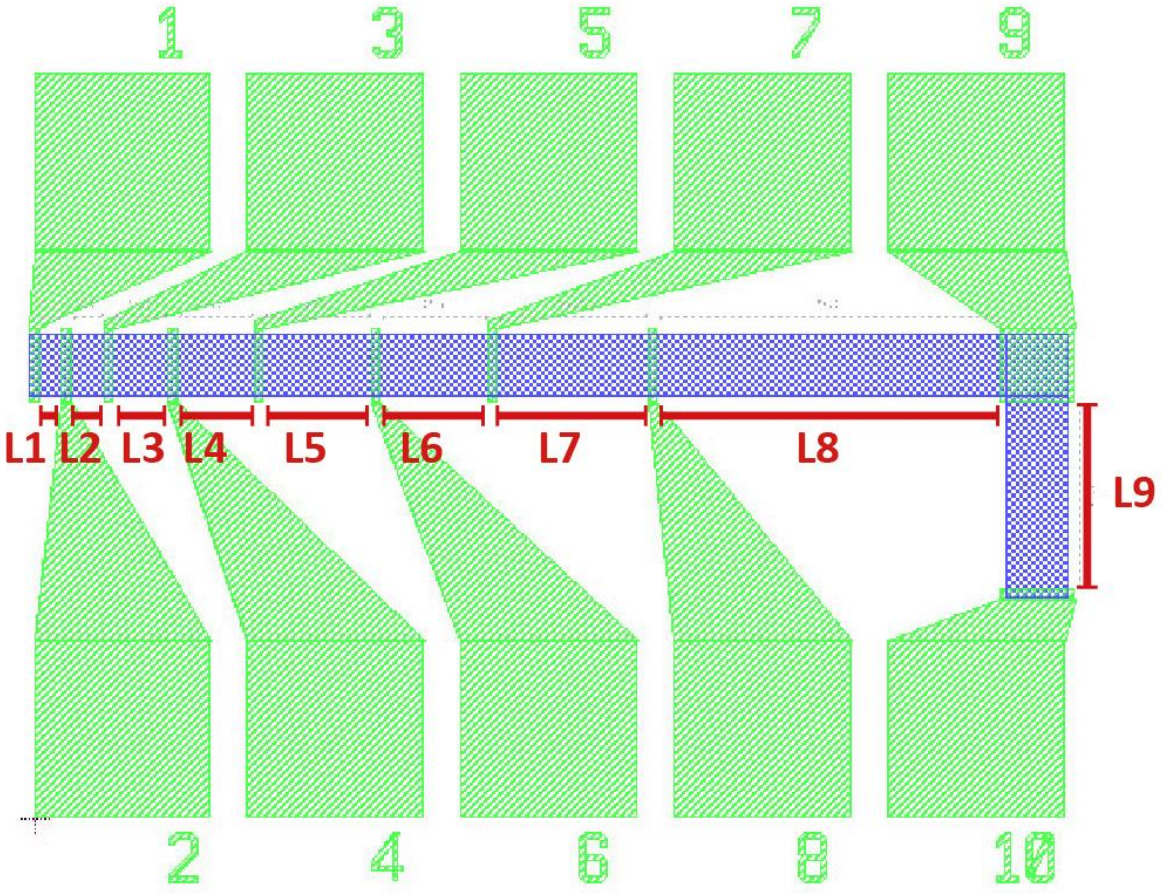


Figure 8 Example of a TLM design mask

	TLM1	*TLM2*	*TLM3*	*TLM4*
W	7	12	24	36
L1	2	4	8	12
L2	4	6	12	18
L3	6	10	20	30
L4	10	14	28	42
L5	10	20	40	60
L6	18	20	40	60
L7	22	28	56	84
L8	35	64	128	192
L9	28	35	70	105
Contact width	2	2	4	6

Table 3 Designs dimensions

In addition to the four TLM designs, we also added a traditional four probes structure on some extra chips for the purpose of measurements comparison. (See figure below)

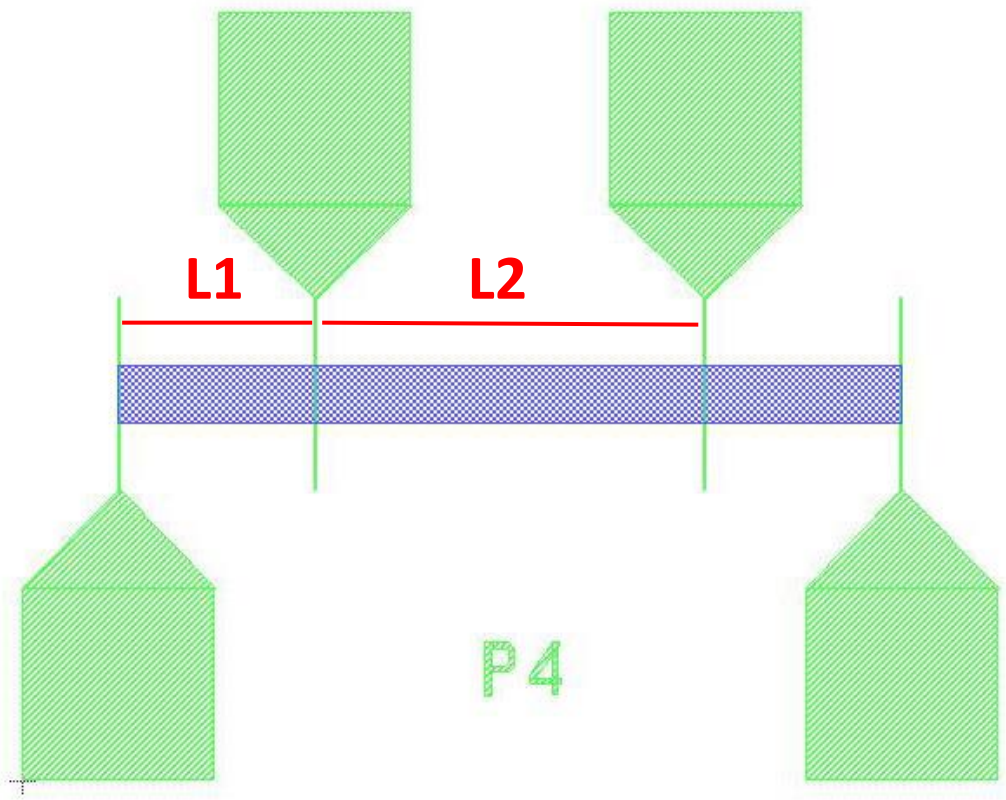


Figure 9 Four probes structure, L1=100um, L2=200um, W=30um, contact width: 2um

Finally, the contacts were chose to be made of three layers. A first layer of Chromium (Cr, 10nm) in order to add a second layer of Platinum (Pt, 100nm) and a third layer of Titanium (Ti, 20nm). The choice of Titanium was made despite its larger resistivity literature results in order to last through the different steps of

graphene deposition, such as annealing. However, its greater literature values could prove useful when interpreting differences between cleaning methods or other design dissimilarities. The lower layers (Cr and Pt) will serve some other experience but only the last layer (Ti) will be useful for the measurements of this project.

As a matter of time, one additional reason that lead the choice was the metal availability of CMi available machines.

4. Fabrication

In this section, we will summarize the chosen process flow leading to the creation of the different chips on which the measurements were done providing explanation to the key steps and issues and ending with a short analysis of the resulting chips. A detail of every step and recipe of the process flow is given in Appendix 2.

4.1. Process flow

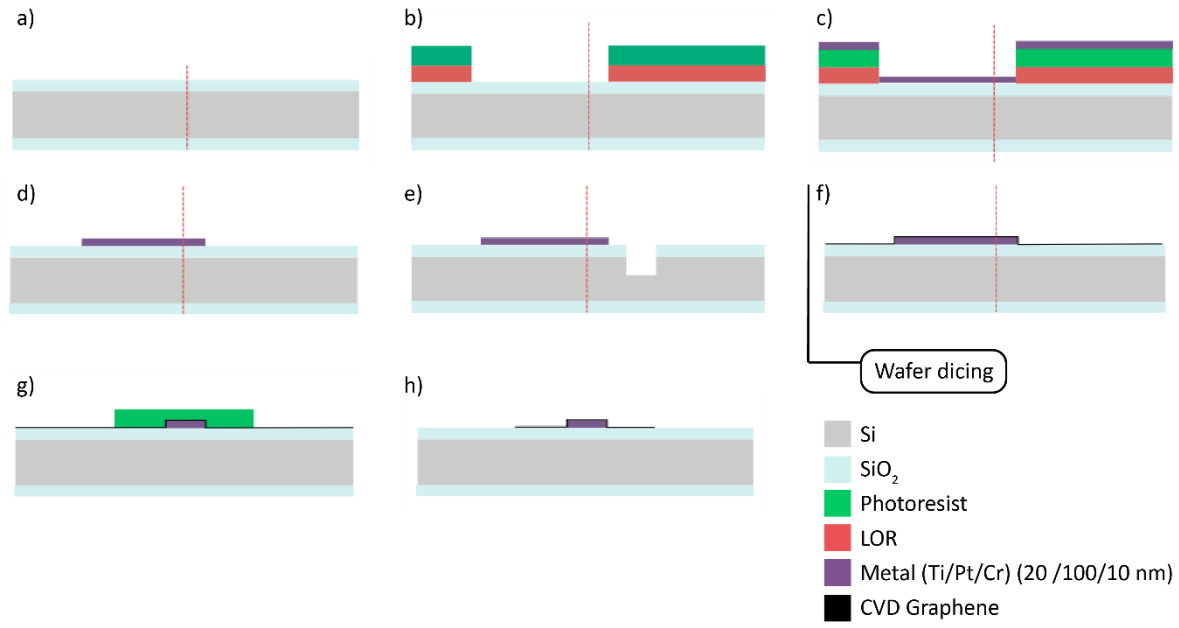


Figure 10 : The first six figures are split into two in order to be able to explain at the same time the steps concerning only some chips. On the left-hand side the schematic representation of chip TLM and chip 4P, while chip "Tom Larsen" is represented on the right hand side. (a) The starting point is a silicon wafer with dry silicon dioxide on both sides. (b) The wafer is coated with photoresist (AZ1512 on LOR). (c) A layer of Chromium/Platinum/Titanium is evaporated on one side. (d) The metal is patterned with a lithography step and lift-off. (e) (Chips "Tom Larsen") SiO_2 etching and Si dry etching. (f) Graphene transfer. As of this step no further mention of chips "Tom Larsen" will be made. (g) The graphene is patterned through a lithography step and oxygen plasma etching. (h) Resist is stripped (UFT wet bench or ACETONE still bath).

As Illustrated in figure 10, the fabrication started from 2 525um thick Silicon wafers single side polished, with dry thermal oxidation (290nm). These wafers were joined by two double side polished other wafers. The four wafers were spin coated with 0.48um AZ1512 on LOR (ACS 200) and exposed on MLA150 following the metal design of the masks. The masks are made of two different chips: Chip 1, containing the 4 TLM designs, and Chip "Tom Larsen", containing a separate design that we won't use for this project (the steps concerning chips "Tom Larsen" will still be briefly exposed as they were entirely part of the fabrication). The four wafers were separated in two different designs in order to add chips

containing a four probes measurement structure on two of them. After a descum in the TeplaGIGABatch, the metal deposition was made in the EVA 760. The metal contacts are constituted with (from bottom to top) a first 10nm layer of Chromium over which was deposited a 100nm layer of Platinum and on top of this was added a 20nm layer of Titanium. The LOR, AZ1512 resist as well as the surplus of metal are the removed in the lift-off wet bench leaving the expected metal contacts design. After these, we did a second photolithography (ACS 200 coating and development ECI 3007 and MLA150 for exposure) followed by a 290nm etching of the oxide and a >20um etching of Si (step concerning only the chips “Tom Larsen”).

After these steps, the wafer were cleaned, 30s low strip in TeplaGIGABacth followed by a UFT wet bench resist striping consisting on two remover 1165 baths (5minutes at 70°), a first moved DI water rinse bath (~5min), a second stiller bath (~5min) and a spin dryer program to finish. Finally, two wafers (1 of each type) are coated with resist (5um ECI top EC) and sent to dicing.

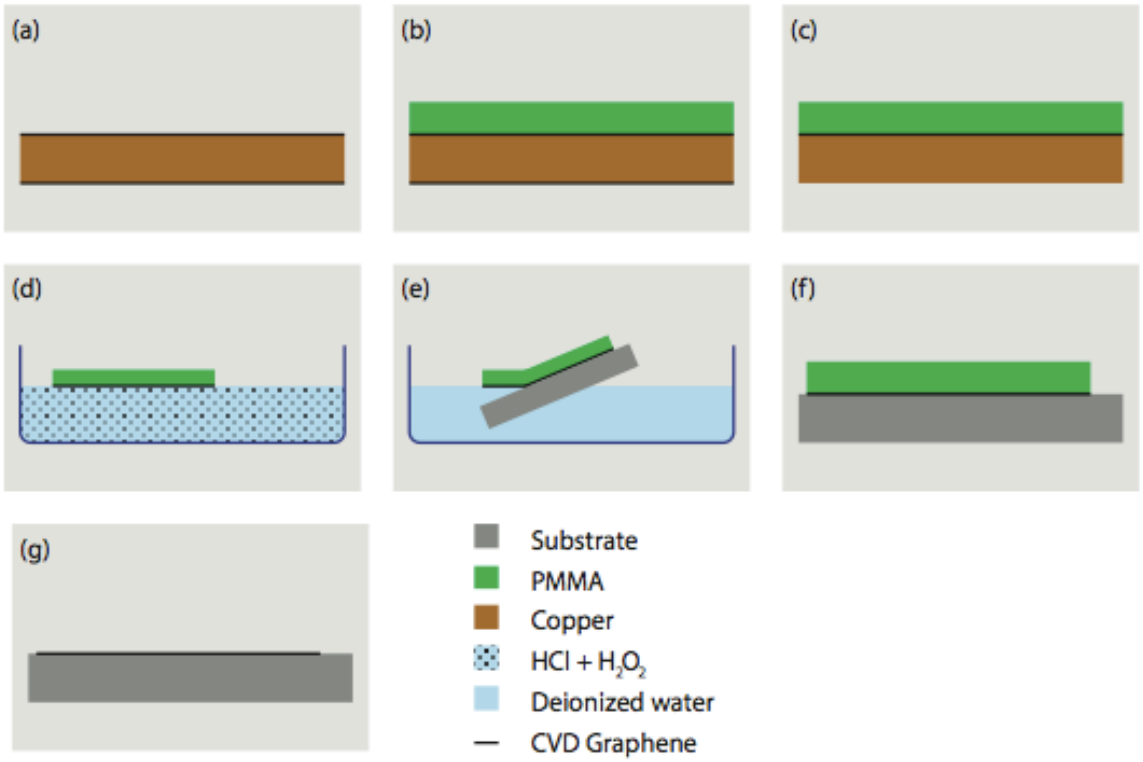


Figure 11: Wet graphene transfer on a substrate. (a) The starting point is a copper thin film with CVD graphene on both sides. (b) A PMMA layer is spin-coated on top of the foil. (c) Graphene on one side of the copper foils is etched by oxygen plasma. (d) Copper is etched in an HCl+H2O2 solution. (e) The PMMA and graphene foil are transferred to the substrate using the fishing method. (f) The graphene is attached to the substrate prevalently by van der Waals bounds. (g) The PMMA is dissolved in acetone. Ref. [14]

After dicing, the chips are inspected with microscope and some of them are selected for the graphene deposition. The graphene deposition was made outside the cleanroom and is detailed in figure 11.

After the graphene deposition, and after a first week of measurements on the un-patterned graphene chips, the graphene was patterned in the cleanroom.

First, every chip was separately coated in SSE SB20 manual coater with ECI 3007, and exposed with MLA 150. Development was made manually as well, 1min in AZ 726 MIF remover and 1min in DI water, and the chips are the left to dry on a clean surface at room temperature. After that, the etching of the surplus graphene was made in the TeplaGIGABatch (1min strip high). Some chips were already extracted from the cleanroom at this point to make a few measurements without striping the resist off the graphene. For the resist stripping, we separated the chips into two different methods:

- Standard UFT (2x 1165 bath) with 2x rinse in the cascade batch
- ACETONE 1H followed by IPA and drying at room temperature, lying on a clean surface

After these, the chips were extracted from the cleanroom and ready for measurements.

The results of the fabrication are briefly presented in the result section of this chapter.

4.2. Masks design

In this section, we present the different and significant parts of the wafers designs.

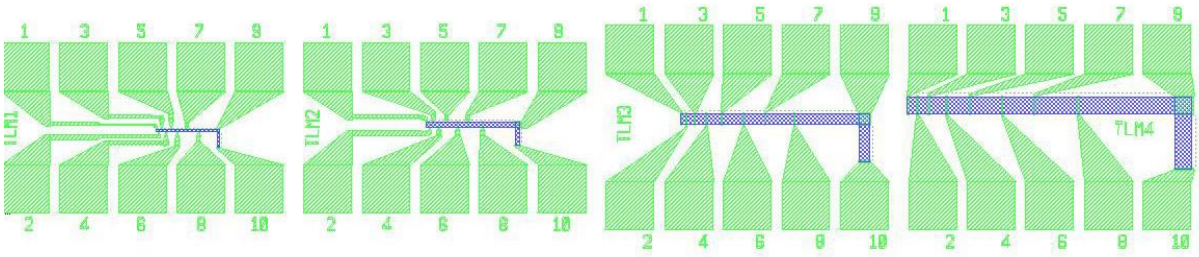


Figure 12 Design block with all 4 different TLM designs

In figure 12 we see the block containing all four TLM designs. This block is patterned in 3 columns and 17 rows (51) per chip (10x10mm).

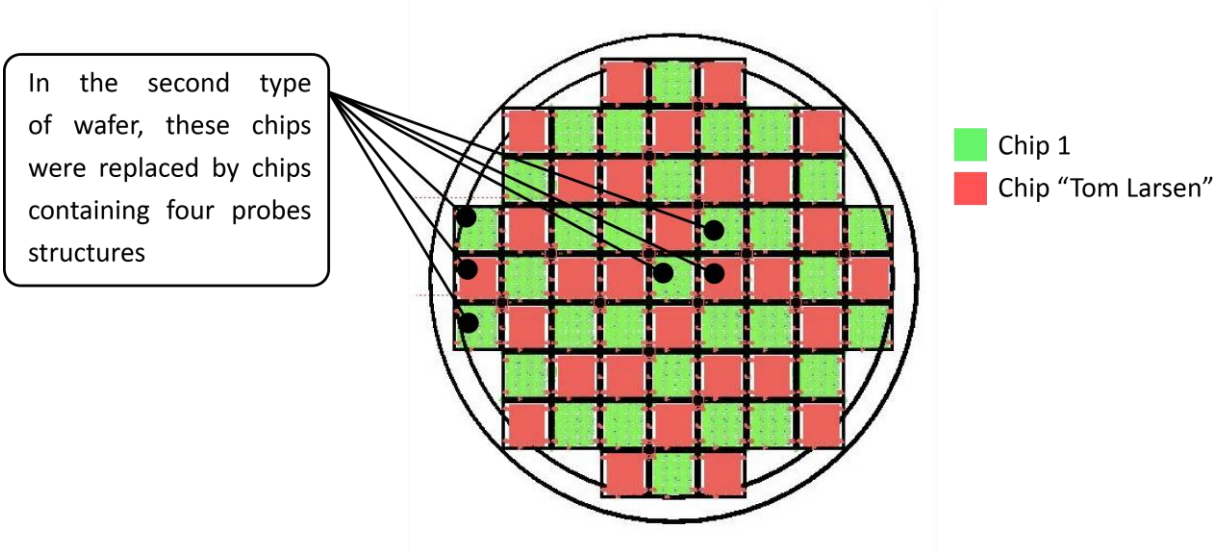


Figure 13 Wafer composition

In figure 13 we can see an example of a chip of type F1. There are two types of wafers:

- F1, with TLM chips (chip 1) and chips “Tom Larsen”.
- F2, in this type, we add some four probes structures (chip 3)

In figure 14, we can see a close up of the chips on a wafer of type F2.

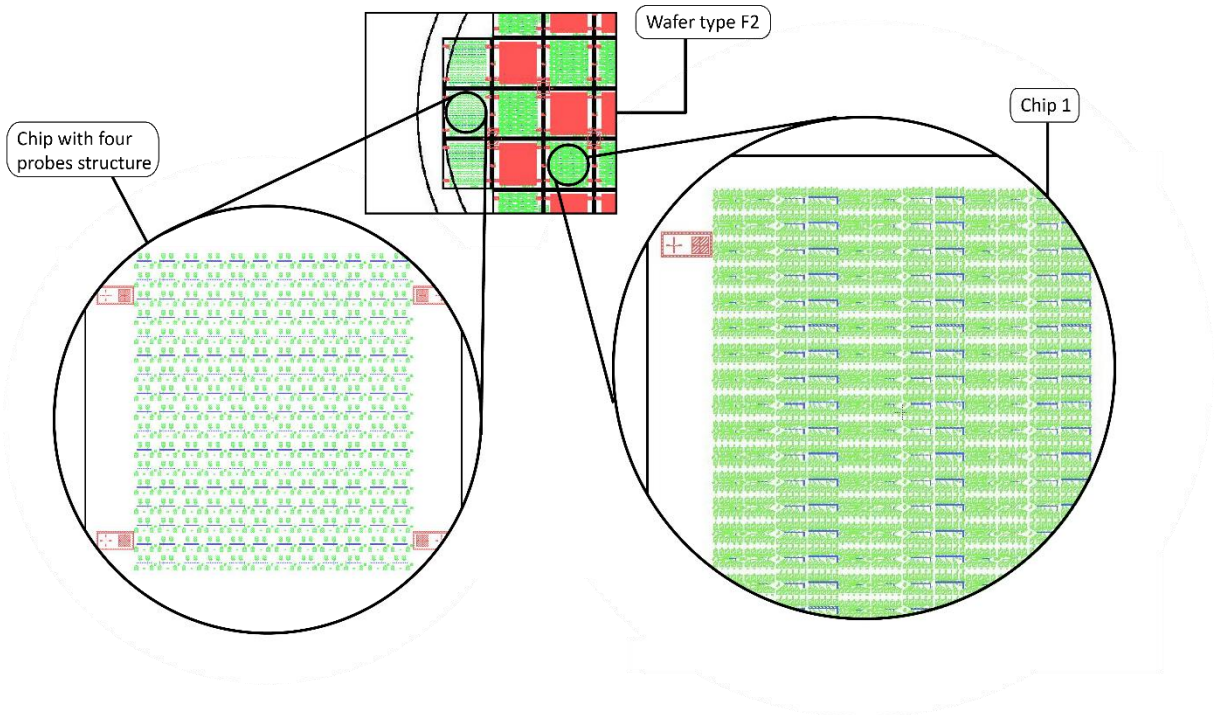


Figure 14 Close up on a wafers chips

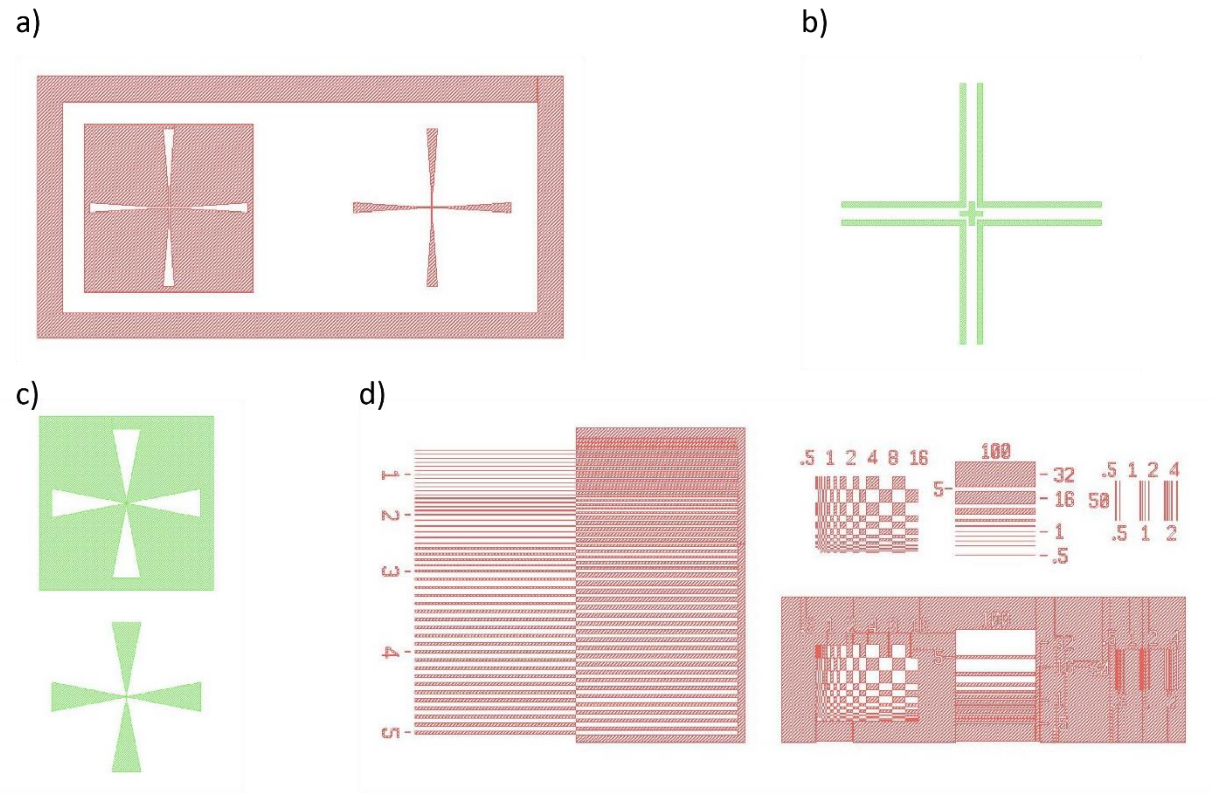


Figure 15 Important marks to find on a wafer. a) Chip alignment marks. b) Dicing marks. c) Wafer alignment marks. d) Exposure grids

Figure 15 shows the different useful marks in the process. We can see in c) the wafer alignment marks that were used for the second exposition on the wafers. c) Shows the chips alignment marks used for all the exposures after the dicing done following the appropriate marks on b). Finally, on d), the exposure grids are used to check the exposure quality (overexposed vs underexposed).

4.3. Issues encountered

4.3.1. Exposure and Dose

One of the important part of the fabrication was the MLA exposures and in order to have the as good as possible, some exposure test were needed.

For the first exposure (on AZ1512 on LOR) started from a 70mJ/cm^2 recommended in ref. [14]. That we augmented a little due to substrate difference first but also to get to a point with a slight over-exposure that would allow total removal of resist where it shouldn't be after development.

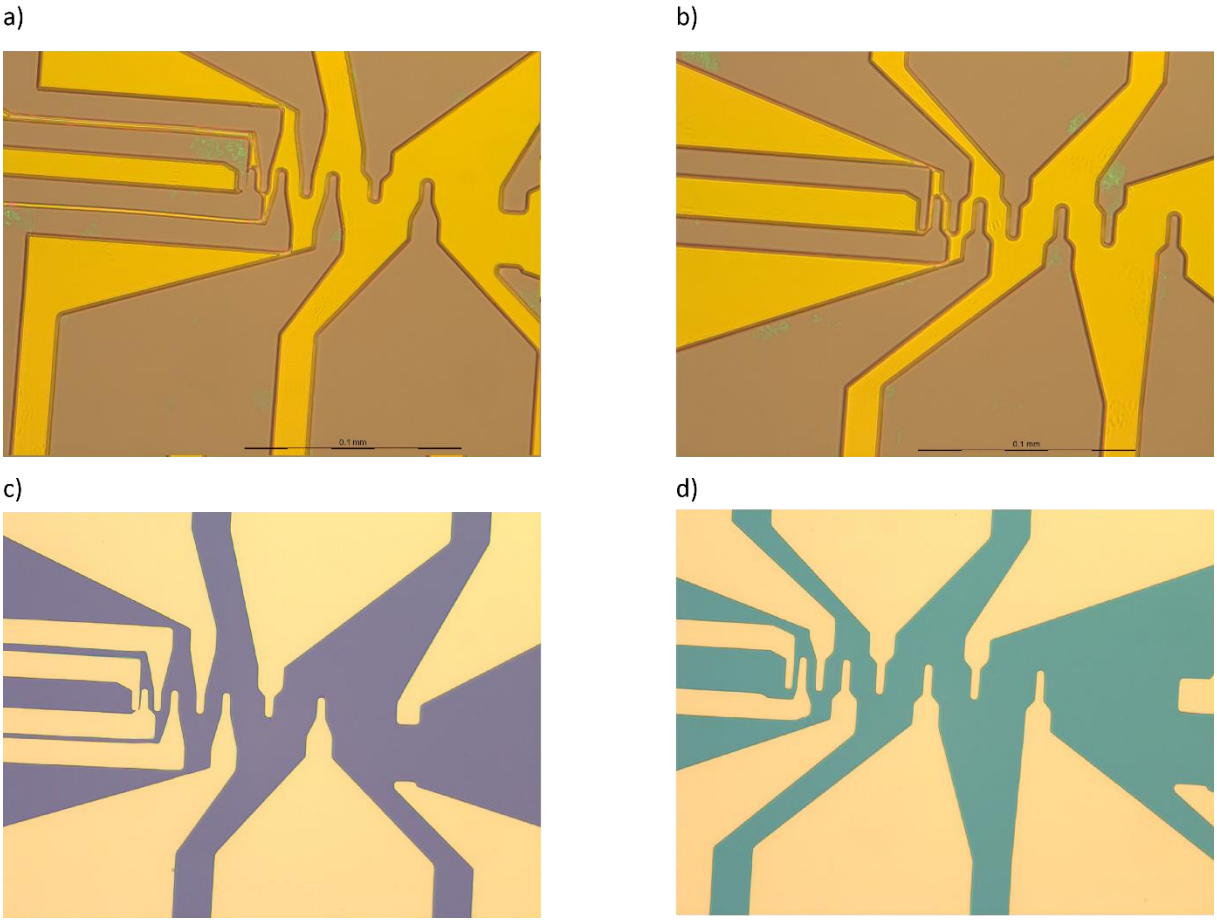


Figure 16 a) TLM1 after first exposure and before metal deposition. b)TLM2 same conditions. c) TLM1 after design modifications and metal deposition. d) TLM2 same conditions

As it can be seen on figure 16, the overexposure, along with the MLA resolution, give a bad result and so the design has been changed avoiding short cuts between contacts.

For the second exposure, we had to run dose tests on our exposure grids in order to be able to define the right dose and defocus for our exposures on ECI 3007.

As shown in figure 17, we decided to incline for a 160mJ/cm^2 with a -1 defocus.

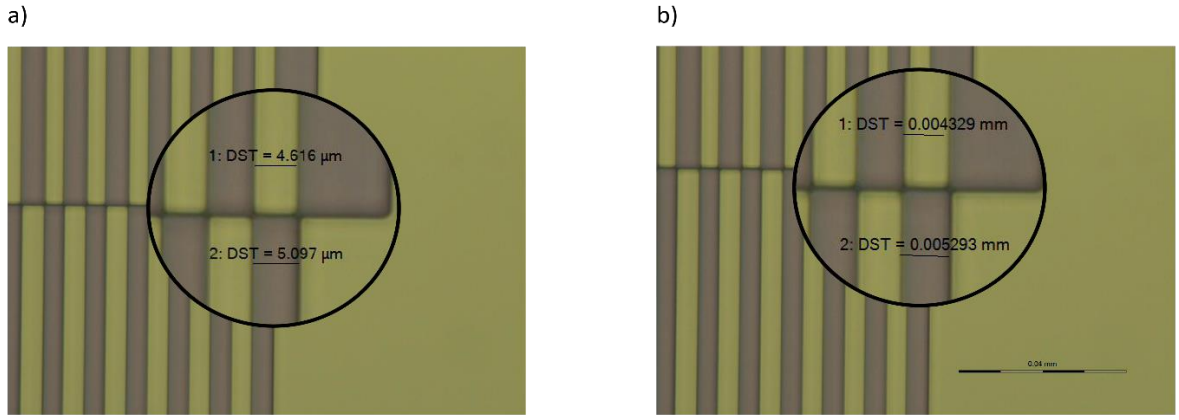


Figure 17: Dose tests for second exposure: a) 160mJ/cm^2. b) 180mJ/cm^2.

As of for the third exposure, we followed the CMi recommendations (130mJ/cm^2, Defocus=0)

4.3.2. Graphene deposition

The graphene deposition is probably the most critical part of this fabrication process. It is also the part that caused the most problems towards any resistance measurements. Figure 18 shows how the graphene deposition looks like before any patterning. We can see that the graphene, due to its 2D structure and extremely low thickness, cracks very easily on a chip.

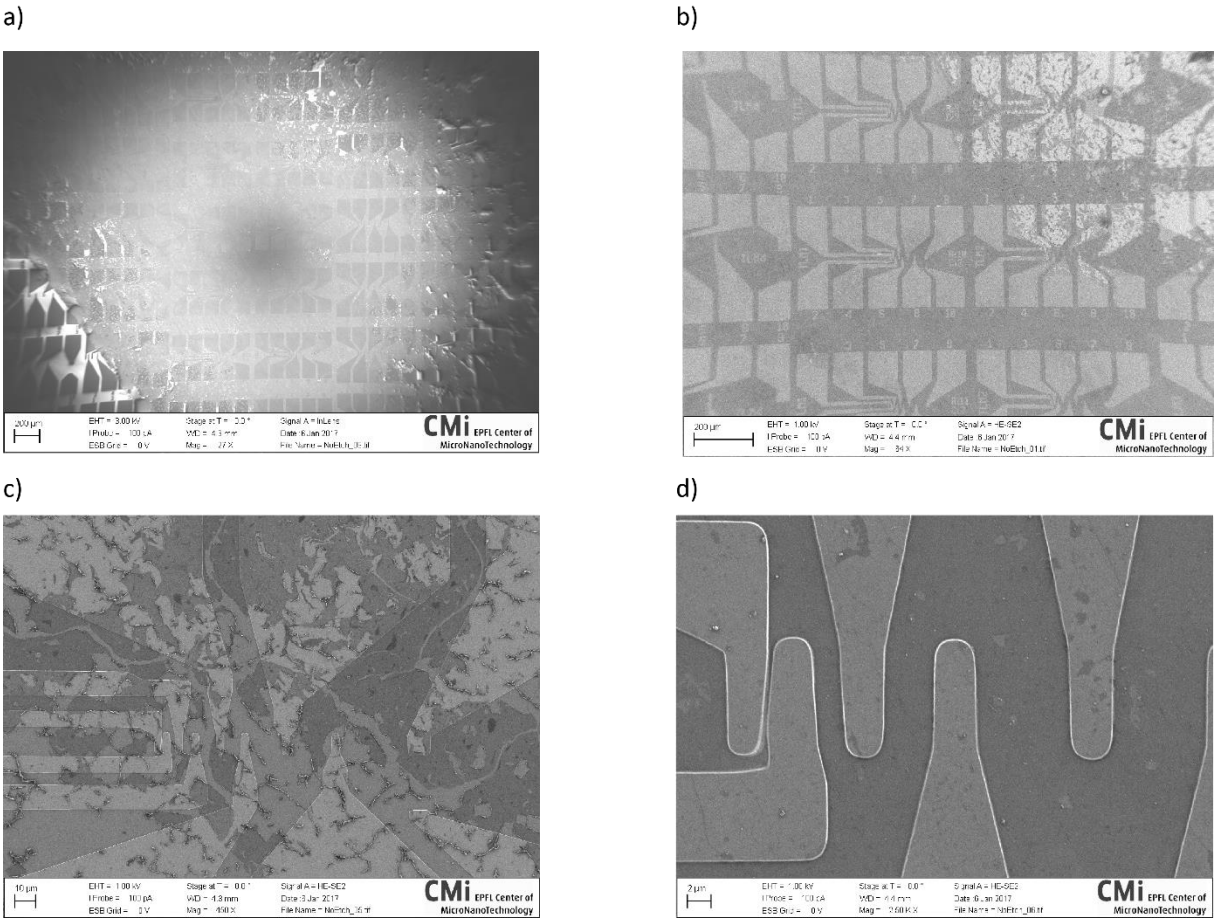


Figure 18 Graphene deposition: a) Graphene sheet on a chip. b) Graphene sheet with many cracks. c) Graphene on TLM1, bad deposition (no channel). d) small graphene marks on a very good part of deposition.

We can see (figure 19) that the cracks will significantly change the width W of a graphene channel, and that defects are of quite big importance regarding the dimensions of a TLM structure. This could cause significant errors in the resistance measure.

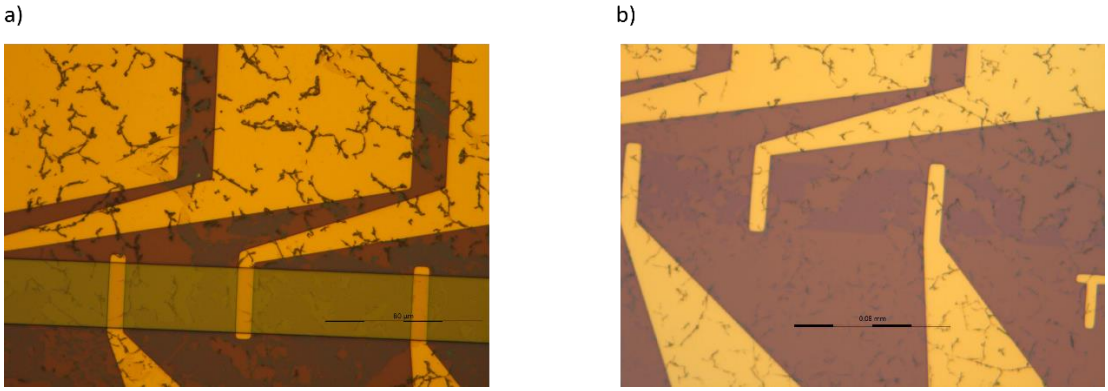


Figure 19 Graphene channel with (a) and without resist (b). Resist removed by 1165

Finding a good structure on a chip then gets tricky as we have an average of about 10 well deposited structures (no cracks or other defects) per chip (about 2.5%).

4.3.3. Etching the graphene

The step of etching the graphene represented quite a challenge as there wasn't a really good definition of the recipes to follow to be able to completely strip the graphene sheet around the resist defined TLM channels.

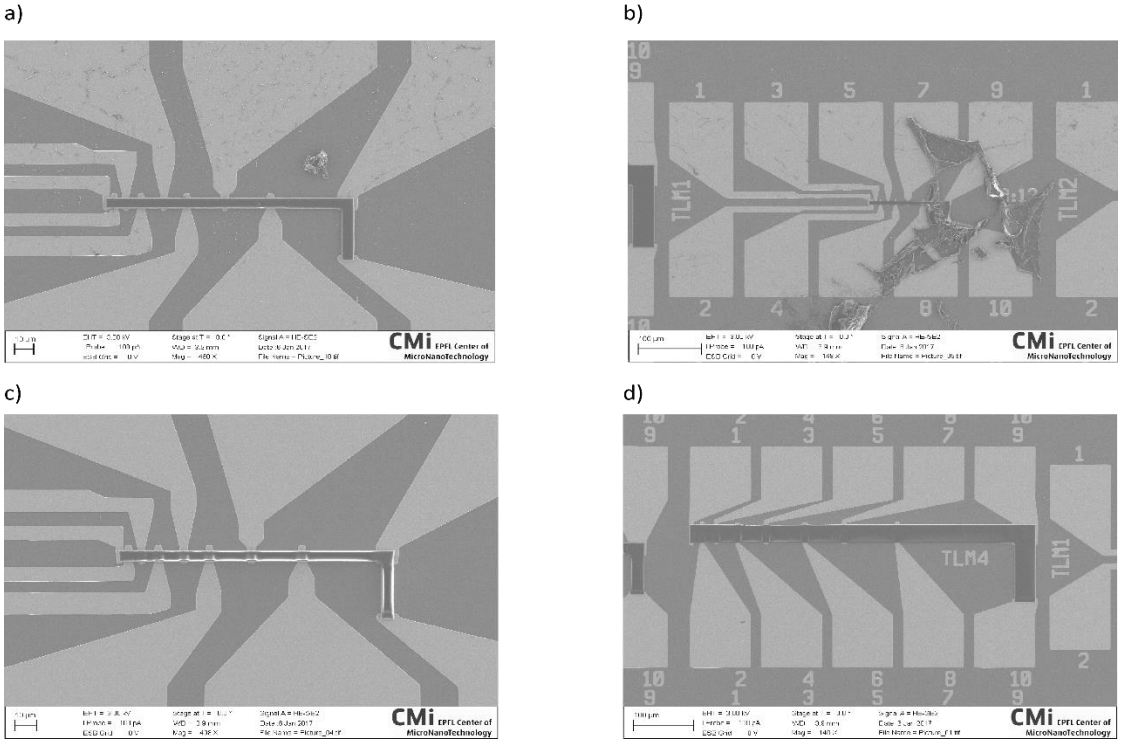


Figure 20 Etching graphene: a) (TLM1) and b) graphene leftovers after 1min strip high. c) (TLM1) and d) some chips give better results under the same conditions.

The original recipe was an oxygen plasma etching on the TeplaGIGABatch, strip_Low_30s. After iterative microscope inspections, we had to repeat it until having a strip_High_1min and even 1.5 min for some chips.

4.3.4. Resist strip

Finally, getting to strip the resist, two different methods were implemented with different results. Three chips we striped in standard UFT wet bench with 1165 remover and three others were prepared in a still beaker of Acetone, followed by a 20 min IPA rinse bath and were left drying on a clean surface at room temperature.

a) b)

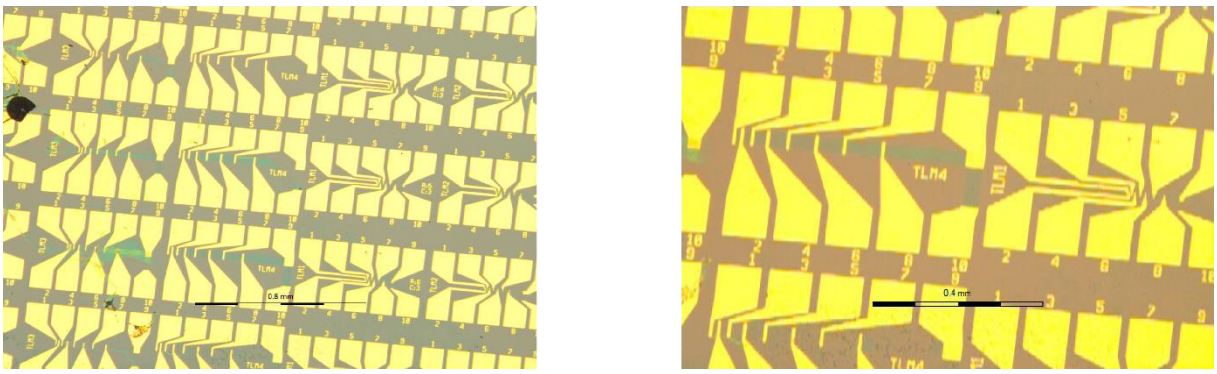


Figure 21 some results after Acetone resist strip

As shown in Figure 21, Acetone gave better results and the rest of the chips were done following this method.

4.4. Results

4.4.1. Resist measurement

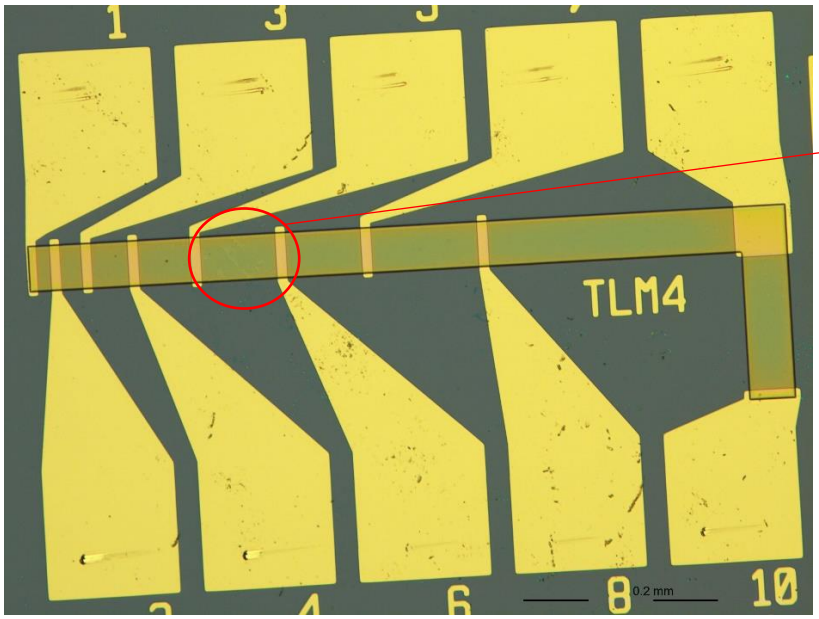


Figure 22 TLM4 good quality resistance measurement with resist on graphene channel.

After etching the graphene but before striping any resist off the TLM graphene channels, some measurements were done. Figure 19 and 22 shows the TLM structures with resist recovering the graphene channel. It was very difficult though to have a good estimation of the channel uniformity under the resist before doing the measurements, that leading to many open circuit measurement rounds.

4.4.2. Resist stripping

The figure below (figure 23) shows the differences between 1165 remover and Acetone to strip the resist. We see very well that in the case of remover 1165 (left) there are many chips with no graphene left at all and in the cases we have only part of the expected structures. The good / bad structures rate were calculated on chip 11 (Acetone) and chips 17 and 19 (1165 remover) and are about the following:

- **<5%** if stripped with 1165 remover: CHIP 17&19 (counting for goods the semi-suitable structures)
- **~10%** if stripped with Acetone: CHIP 11

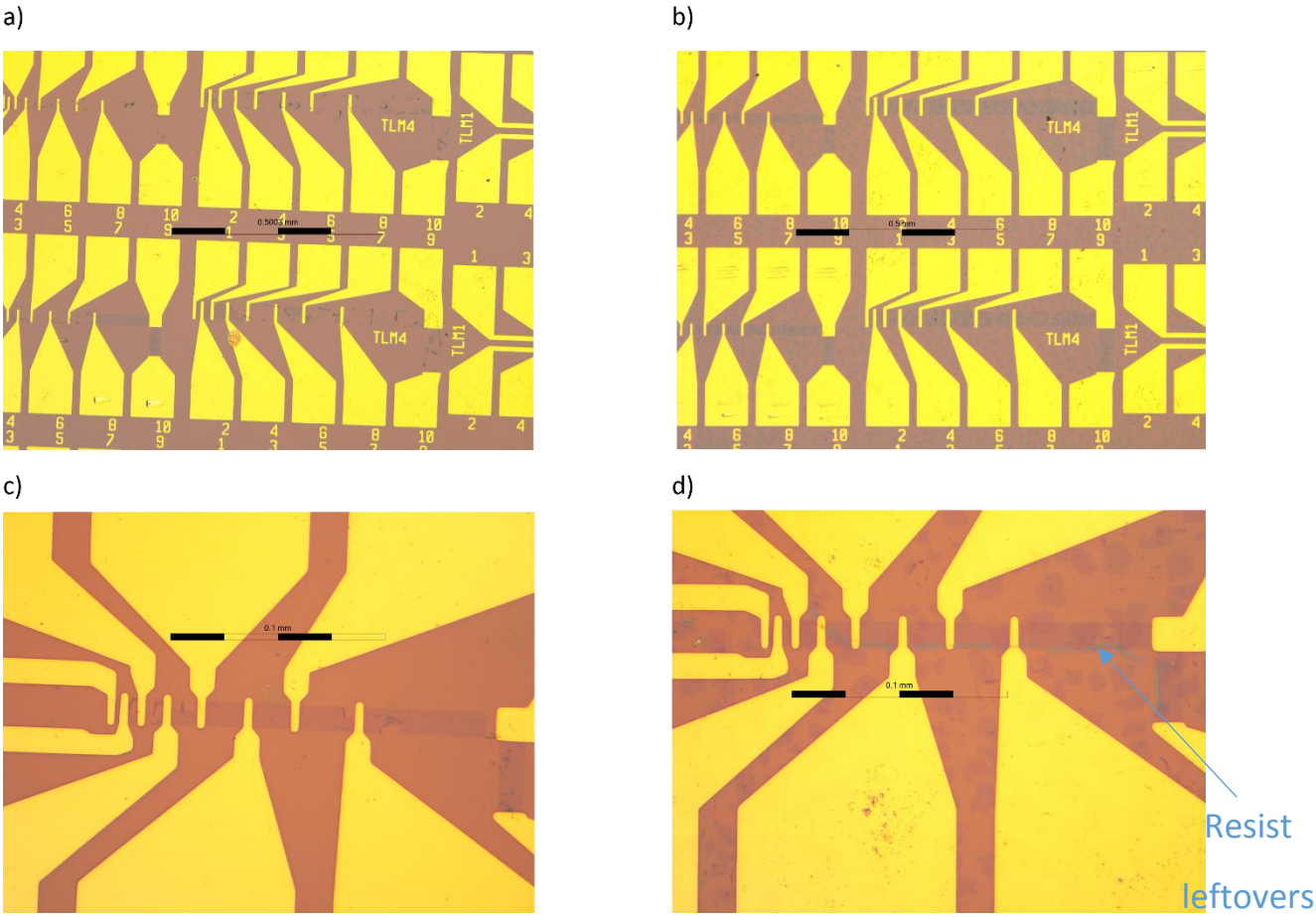


Figure 23 Differences between 1165 remover resist strip (a) & (c) and Acetone resist strip (b) & (d)

However, we can also see on figure 23 that Acetone removal leaves some resist marks on the chips. We can also see in figure 21 some of the best structures obtained after etching and striping the resist in Acetone.

The last figure (24) of this section shows the results of chips “Tom Larsen”. We can see the conditions are met due to the good dose test. We can also see the silicon dry etching on the bottom of the W of the chip number label.

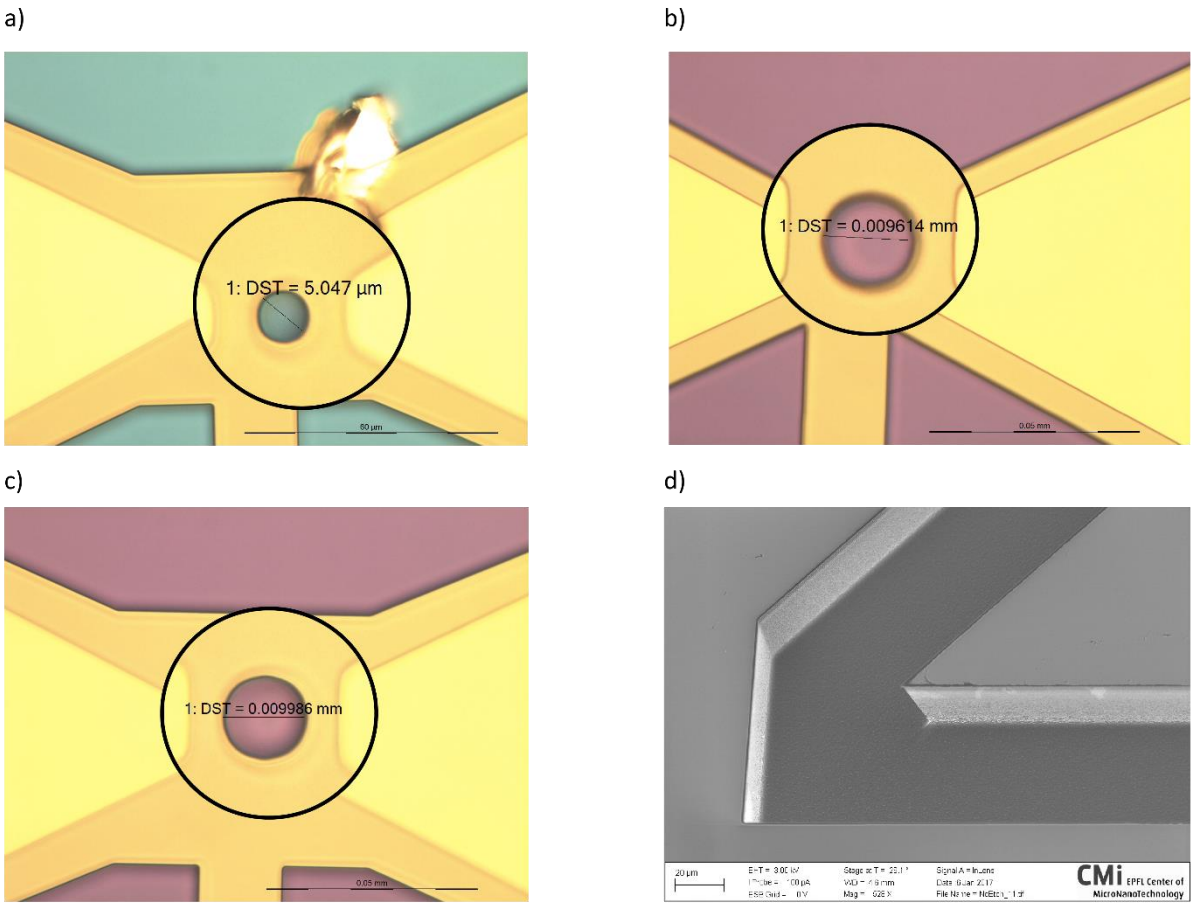


Figure 24 Good exposure results on "Tom Larsen" chips. Designed values a) 5um. b) &c) 10um. d) Silicone etching.

1. Measurements and analysis

In this section, we will summarize the measurement rounds, how and why they were done, what were the issues encountered and what the results are. Due to time constraints we were unfortunately unable to do any four probes measurements.

1.1. Measurements

The measurements towards contact resistance as seen in chapter 3 of this report, we will apply voltage and measure current on different designs with different lengths and widths. See figures 1 and 25.

From each measurement (on a specific length of a chosen design) an average resistance that we will use to extract the contact resistance.

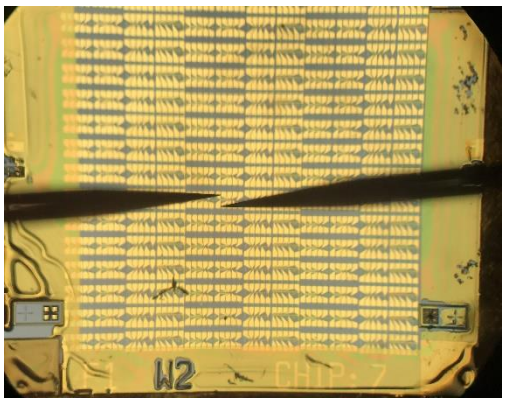


Figure 25 Microscope view of the measurement probes over chip 7 (type chip 1)

The resistance measurement were made on a voltage range from -10 to 10 [V] with steps of 0.5 [V]. Figure 26 show an example of the IV curve of the voltage application between 2 points of a TLM design.

We can see that the curve is quite linear (as expected). Any nonlinear curve was not taken into consideration for contact resistance measurement.

A first measurement campaign was made before patterning graphene to try out the measurement tool. But all result are extracted from the second measurement campaign for the calculation of contact resistance and contact resistivity. This concerns the following chips:

- Chips with resist: CHIP 7 and CHIP 15
- Chips stripped with 1165 remover: CHIP 9, CHIP 17 and CHIP19
- Chips stripped with Acetone: CHIP 3, CHIP 11 and CHIP 21

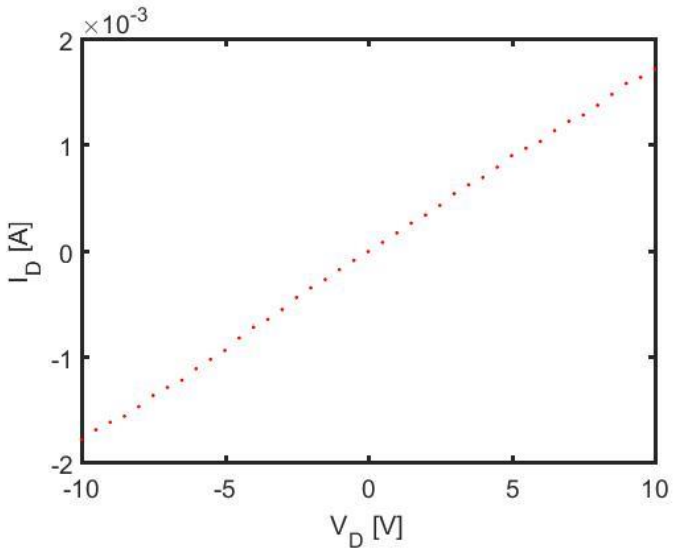


Figure 26 IV curve for a measurement round on chip 11 TLM1 design between contacts 9 and 10

1.2. Issues encountered

The main issue encountered in the measurement campaign is the great difficulty of finding well deposited graphene on a chip.

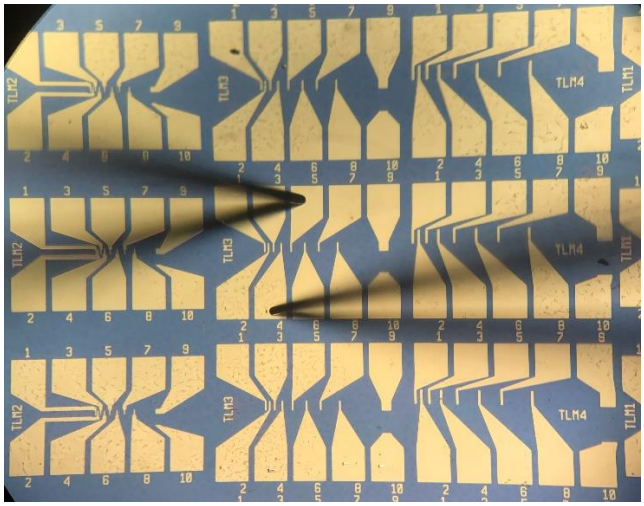


Figure 27 Microscope view of the measurements probes on CHIP 3 (1165 stripped) no graphene left anywhere

We can see in figure 27 (and other figures above) that most of a chip after resist stripping are unsuitable for any measurement (no graphene channel at all). Only a few would actually have a well deposited graphene channel (about 10% with Acetone, <5% with 1165) and most of the time we couldn't even make measurement on the whole deigned structure.

For chips with resist, (figure 22) it is particularly difficult to see through resist to analyze the state of the graphene sheet.

1.3. Results

The results are separated in 3 parts: with resist, 1165 and Acetone. All measurements values, tables and graphs are to find in a raw form in appendix 4.

The measurements are separated in different stripping methods, different chips and different designs.

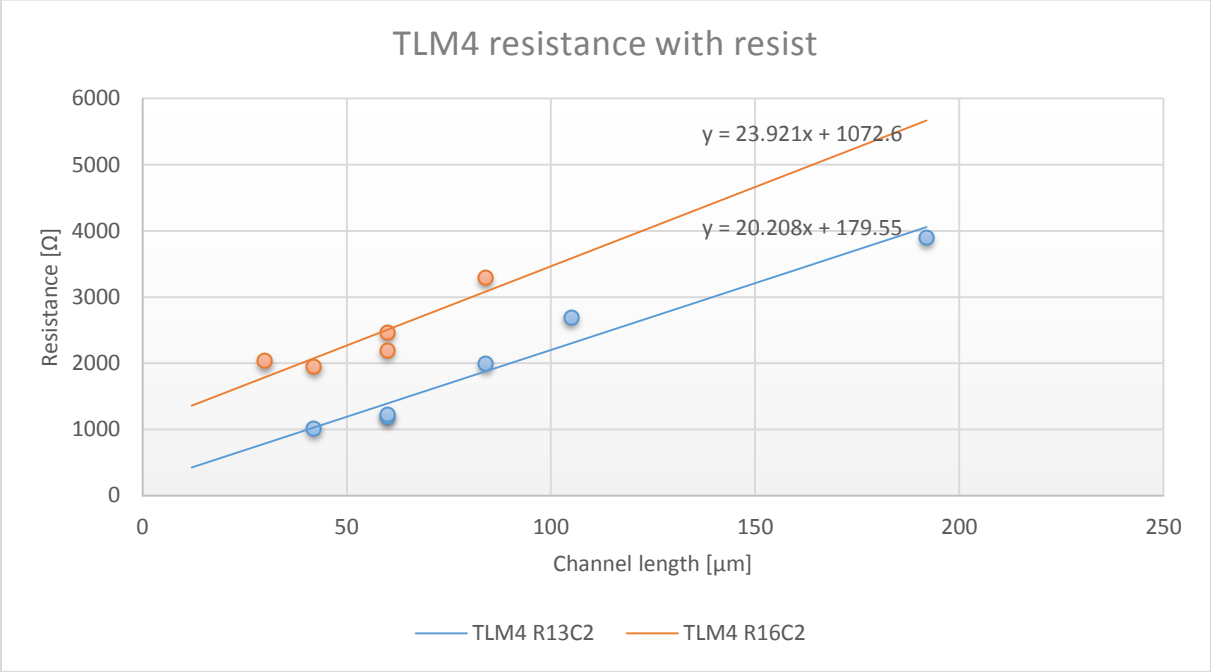


Figure 28 Measured resistances for two TLM4 structures of CHIP 7 with resist on the graphene channel

This first graph shows resistances of two TLM4 structures with the same fabrication conditions (on the same chip) with resist. TLM4 structures were chosen here because they are the widest TLM structures tested and thus are less affected by grains or cracks of the graphene channel. We can see that even though these structures have the same dimensions and have been put through the same fabrication conditions, we can see differences about one order of magnitude in the calculated resistances. Their contact resistance are respectively **90[Ω] (Row13 Column2) and 536[Ω] (R16C2).**

Such differences are due mainly to the poor repeatability of the graphene sheet quality. The thickness is not always uniform (darker parts of figure 24) as well as the width that can easily vary between the fabrication steps justifying slope differences. As for the cracks, grains, dirt and other defects, they can be the changing factors for the measured resistance.

For the rest of the results we always took the smallest measured R_C per design.

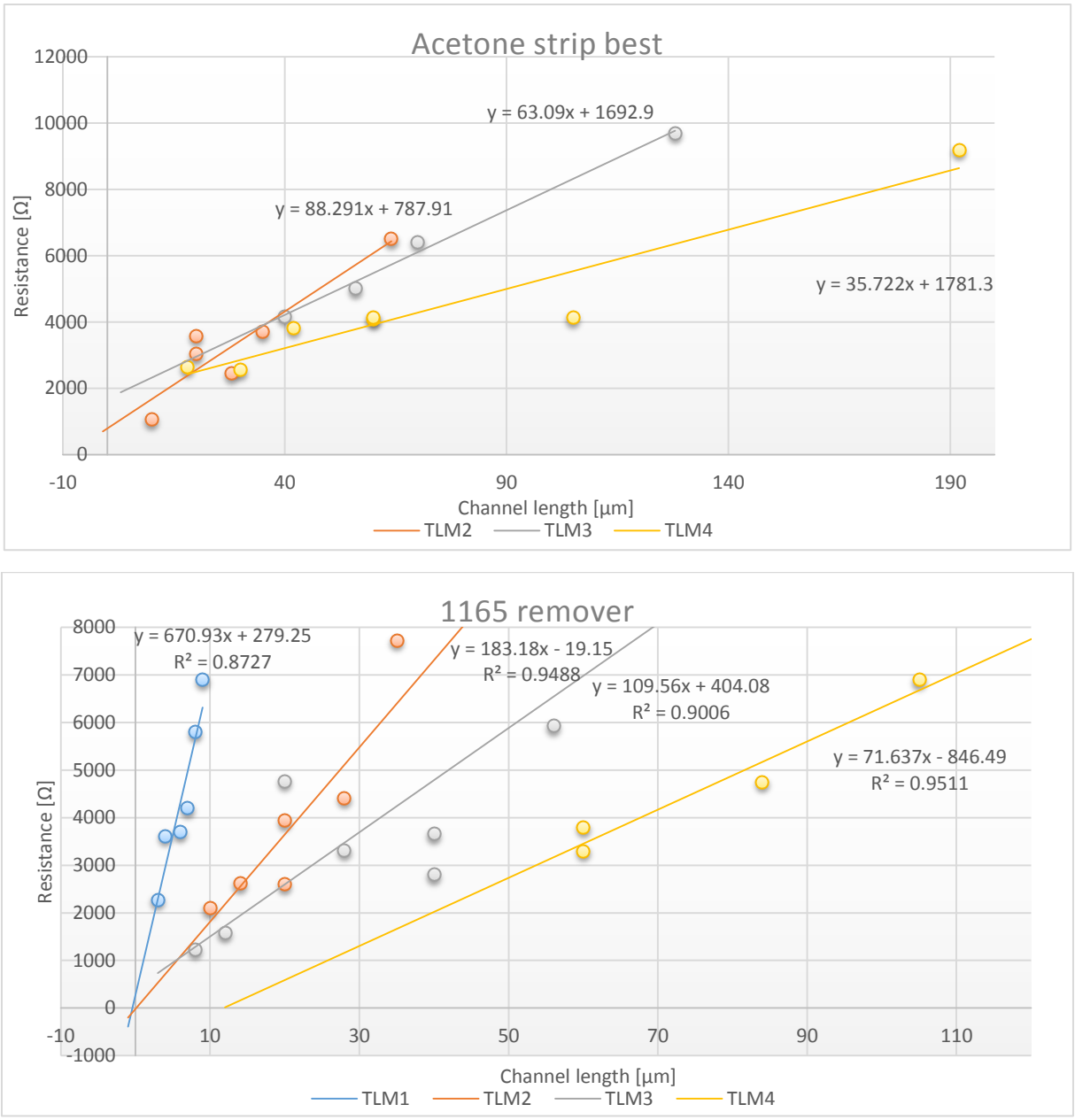


Figure 29 Plots of measured resistances for different TLM structures:

(up) Acetone resist strip. (down) Remover 1165 resist strip

Figures 29 and 30 show the plots of the measured resistance for chips stripped with respectively with remover 1165 and Acetone. As we can see from the R^2, it is difficult to extract much tendencies from these very variable graphs. We can see that the linear regression is quite a poor fit in some cases when we know that resistance should vary linearly. Again this is due to changes of the channel and contacts between the different pads of a same structure.

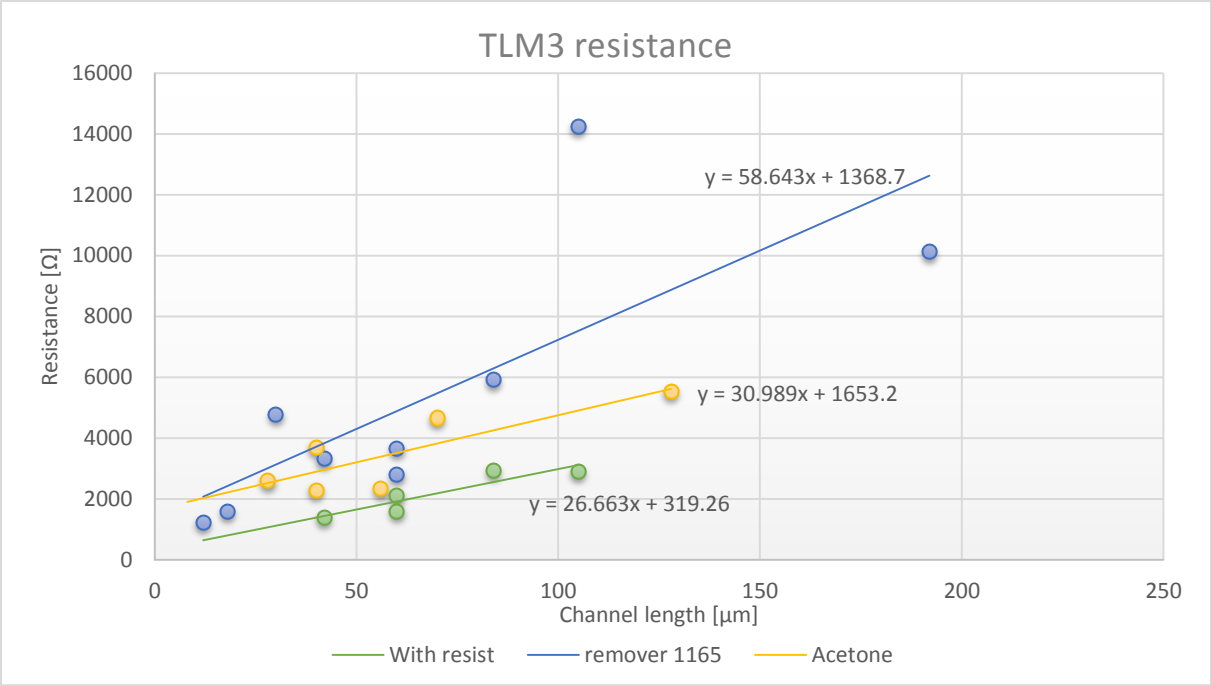


Figure 30 Comparison of TLM3 resistance plots for different TLM structures

This last graph is a representation of TLM3 structures resistances with different fabrications. Out of this graph and according to the trend lines, we could say that the resist stripping with Acetone only rises the value of R_C and doesn't change the graphene channel properties (same slope). The Acetone stripping seems to be less aggressive on the graphene.

The remover 1165 removal gives a greater slope implying that after stripping, the graphene sheet resistance increases. This could be explained by the reaction of graphene to the contact of the photoresist, giving better sheet resistance and contact resistance but larger transition length.

The table below summarizes the best measured and calculated values of the TLM structures. Results in this table are about 10 times bigger than the state of the art.

Design Type		W [µm]	R_C [Ω]	L_T [µm]	ρ_C [Ω µm^2]
With resist	TLM3	24	319.26	-7.98	15286.17
	TLM4	36	179.55	-8.885	14357.72
Acetone	TLM2	12	787.9	-8.92	21084.2
	TLM3	24	1383	-27.7	229854.6
	TLM4	36	2276.6	-71.8	1471139
1165 remover	TLM2	12	707.95	-3.766	7998.419
	TLM3	24	861.91	-7.91	40906.25

Table 4 Measured and calculated values of TLM structures

1. Perspectives

This project constitutes a first step of maybe further researches, fabrications and measurements. This section proposes further objectives and methods to continue on this project's goals.

Unfortunately, due to time constraints, no comparisons between different graphene deposition methods were done. Though as exposed in this report, the graphene deposition quality is an important and very limiting factor for the measurement quality and of course, for the final design quality as well.

- The first thing that should be done continuing this student's work is following up on the treatment of all fabricated chips towards comparison of different pre-deposition treatments and deposition methods.
- Secondly, the modified TLM designs made in this project combine both traditional TLM structures and Kelvin test structure. This feature hasn't been exploited fully yet and further measurement campaigns should include 4 probes measurements for more reliable results (the single four probes design is also available).
- In addition to that, this project gives a detailed fabrication process and more fabrication rounds should be in order to refine the process flow and graphene patterning.

This work was made towards improving the graphene deposition, and creating chips suitable for reliable contact resistance measurements. Any further work should be done accordingly.

2. Conclusion

In this paper, we analyze and refine the process flow of designs meant for contact resistance measurements for graphene-metal devices.

We first analyze the state of the art concerning contact resistivity measurement designs and define a new kind of design here called “Modified TLM” that combines both traditional transmission line structure and four probes Kelvin test structure. This modified structure is meant to allow more reliable calculations of contact resistivity $\boldsymbol{\rho_C}$ as well as contact resistance and contact transmission length. Unfortunately we weren’t able to fully test that new model but the model should be used for further analyses on contact resistance measurements.

This project also constitutes an analysis of the fabrication process of contact of such devices. We followed, analyzed and refined a given process flow towards the idea of improving graphene deposition and patterning. The paper shows how the etching of a graphene sheet should be done in order to obtain better results in patterning. The main result about the graphene patterning though is the fact that Acetone resist stripping gives better results than remover 1165 giving more than twice as many suitable results.

But the main problem towards reliable graphene devices patterning resides in the graphene sheet deposition. Most of the cracks and other defects in the graphene sheet result from deposition and not from the patterning process.

Finally this paper gives the results of some TLM measurements made on differently treated chips, the best resistivity results of which are around 80 x 10^{-6} $\boldsymbol{\Omega\, cm^2}$. These values are about 10 times higher than collected literature results.

In addition to these, this project was for me the opportunity to start discovering the secrets of graphene and the secrets of a very promising material in the field of microelectronics. I am more oriented in robotics and production techniques and it was a great opportunity for me to discover more about cleanroom environment, manipulations and micro and nano devices fabrication process and associated constraints.

I would like to address special thanks to Dr. Tom Larsen who was of great advice and support throughout this semester project as well as Mr. Marco Di Gisi who took of his time to help me on some manipulations.

3. References

[1] Yang Xu, Cheng Cheng, Sichao Du, Jianyi Yang, Bin Yu, Jack Luo, Wenyan Yin, Erping Li, Shurong Dong, Peide Ye, and Xiangfeng Duan, *"Contacts between Two- and Three-Dimensional Materials: Ohmic, Schottky, and p–n Heterojunctions", ACS NANO 2016.*

[2] Shaoqing Wang, Dacheng Mao, Zhi Jin, Songang Peng, Dayong Zhang, Jingyuan Shi and Xuanyun Wang, *"A more reliable measurement method for metal/graphene contact resistance", Nanotechnology 26 (2015) 405706 (7pp).*

[3] Unknown author*, "Contact resistance and TLM measurements"*, [ONLINE]. Available: https://www.google.ch/url?sa=t&rct=j&q=&esrc=s&source=web&cd=1&cad=rja&uact=8&ved=0ahUKEwj6g56DjLjRAhUCxxQKHVifCckQFgghMAA&url=https%3A%2F%2Fwww.researchgate.net%2Ffile.PostFileLoader.html%3Fid%3D582435245b4952aeab0f1a34%26assetKey%3DAS%253A426797692133376%25401478767908011&usg=AFQjCNEnpXa6p5ZHXi_QuTXE-JRT31AaCg&sig2=lw-zFhVYKf7qMMi3k4ly9A.

[4] N. Stavitski, Student Member, IEEE, J.H. Klootwijk, Member, IEEE, H.W. van Zeijl, B.K. Boksteen, A.Y. Kovalgin and R.A.M. Wolters, *"Cross-Bridge Kelvin Resistor (CBKR) Structures for Measurement of Low Contact Resistances", NXP Research.*

[5] Fengnian Xia, Vasili Perebeinos, Yu-ming Lin, Yanqing Wu and Phaedon Avouris, *"The origins and limits of metal–graphene junction resistance", nature nanotechnologies, 6 FEBRUARY 2011 | DOI: 10.1038/NNANO.2011.6.*

[6] Van der Pauw, L. J. *"A Method of Measuring Specific Resistivity and Hall Effect of Discs of Arbitrary Shape." Philips Research Reports 12.1 (1958): 1-9. Print.*

[7] K. Nagashio, T. Nishimura, K. Kita and A. Toriumi, *"Contact resistivity and current flow path at metal/graphene contact", Department of Materials Engineering, The University of Tokyo.*

[8] Chen Liang, Yuelin Wang, Tie Li, *"Studies on contact resistance in graphene based devices", Microsyst Technol (2016)DOI 10.1007/s00542-015-2616-2.*

[9] Hyung-Youl Park , Woo-Shik Jung , Dong-Ho Kang , Jaeho Jeon , Gwangwe Yoo , Yongkook Park , Jinhee Lee , Yun Hee Jang , Jaeho Lee , Seongjun Park, Hyun-Yong Yu , Byungha Shin , Sungjoo Lee , and Jin-Hong Park, *" Extremely Low Contact Resistance on Graphene through n-Type Doping and Edge Contact Design", wileyonlinelibrary.com, 2015 WILEY-VCH Verlag GmbH & Co.*

[10] S. Russo, M.F.Craciun, M.Yamamoto, A.F.Morpurgo, S.Tarucha , *"Contact resistance in graphene-based devices", 2009 ElsevierB.V.*

[11] A. Gahoi, V. Passi, S. Kataria, S. Wagner, A. Bablich and M. C. Lemme, *" Systematic Comparison of Metal Contacts on CVD Graphene", 2015 IEEE.*

[12] Kazuyuki Ito, Takamasa Ogata, Tadashi Sakai, and Yuji Awano, *"Ultralow contact resistivity in annealed titanium edge contacts for multilayered graphene", Applied Physics Express 8, 025101 (2015).*

[13] Johanna Anteroinen, Wonjae Kim, Kari Stadius, Juha Riikonen, Harri Lipsanen, Jussi Ryynänen, *"Extraction of Graphene-Titanium Contact Resistances using Transfer Length Measurement and a Curve-Fit Method", International Journal of Chemical, Molecular, Nuclear, Materials and Metallurgical Engineering Vol:6, No:8, 2012*

[14] Marco Di Gisi, *" 2D Material-Based Bolometer", Master Thesis, EPFL 2016*

4. Appendices

4.1. Project specifications

4.2. Process flow

Projet : Graphene Electrical Resistance						
Operator : Frederic Junod						
Created : 2016.11.10						
Substrates : silicon <100>, 100mm, 525um, single side, p type, 0.1-0.5 Ohmcm and fused silca						
Step N°	**Description**	**Equipement**	**Program / Parameters**	**Target**	**Actual**	**Remarks**
1	**DRY OXIDATION**					
2	300 nm oxide	-	-	300 nm		CMi staff
3	Oxide thickness	Nanospec		300 nm		With Tom
4	Rinsing of wafers					With Tom
	PHOTOLITHOGRAPHY - First litho					
5	Spincoating	ACS	Recipe: 171_CMi.AZ1512onLOR.0um48			
6	Exposure	MLA150	defocus -3, dose 70 mJ/cm2			
7	Developing	ACS	Recipe: 171_CMi.AZ1512onLOE.0um48_2um (TWICE)			
8	Inspection	Microscope	Chech exposure grids			
	METAL deposition					
9	Descum	TeplaGIGA	Strip_Low_30s			
10	METAL deposition	EVA760	Plate distance 450 mm	Cr/Pt/Ti 10/100/20 nm		
	Liftoff					
11	Dissolve resist	Plade Solvent	2h30min in static 1165 remover bath			Try first one wafer and see how it goes
12	Dissolve resist	Plade Solvent	10min in ultrasound 1165 remover bath			
13	Dissolve resist	Plade Solvent	10min in static 1165 remover bath			
14	IPA rinse	Plade Solvent	1h			
15	Spin Rinser Dryer	Semitool SRD	prog 1 10min			wash and dry
	Added a round		10 min remover / 10min us remover / 5 min remover / 30 min IPA / Spin prog1			useless
16	Inspection	Microscope				
	PHOTOLITHOGRAPHY - Second litho					
17	Spincoating	ACS	AZ ECI 2 um - with EBR			
18	Exposure	MLA150	Second mask, Dose 160 defoc-1			We need to test this

19	Developing	ACS	926 Cmi.Dev 3027 ECI 2um0			
20	Inspection	Microscope	Chech exposure grids			
	Silicon oxide and silicon etching					
21	Oxide Etching	Z2/ALCATEL 601 E	Process: SiO2, Rate 340 nm/min, Etch time: 1.5 min	290nm		
22	Inspection	Nanospec				
23	Silicon Dry Etch	Z2/ALCATEL 601 E	Process: Si_ambient1, Rate 6-9 um/min, Etch time: 3 min	>20 um		
24	Inspection	Z2/uScope				
25	Inspection	Bruker Dektak XT		>20um		
	CLEANING					
26	O2 plasma	TeplaGIGA	Strip_low_30sec			
27	Remover 1165	UFT resist	Bath 1 : main remover	5min, 70°C		
28	Remover 1165	UFT resist	Bain 2 : clean remover	5min, 70°C		
29	Fast fill rinse	UFT resist	DI Rinse			
30	Trickle tank	UFT resist	DI Rinse			
31	Spin Rinser Dryer	UFT resist	prog 1			
32	Inspection	Z6/uScope				
	DICING					
33	Spincoate	ACS200	5um ECI top EC			
34	Dicing	-	-	-	-	CMi staff
35	Resist strip	UFT Resist	Standard			
	Graphene deposition					
36	Graphene Deposition	Chnemical Lab				
37	Annealing	Chemical Lab				
38	Cleaning	Chemical Lab				
	CLEANING					
39	Remover 1165	UFT resist	Standard			
40	Inspection	Microscope				
	Graphene patterning					
	PHOTOLITHOGRAPHY - Second litho					
41	Spincoating	SSE SB20	ECI 3007 STD-2000rpm			
42	Exposure	MLA150	Third mask, Dose 130 defoc0			cross 3950/3250
43	Developing	Wetbench	Manual development (Beaker) AZ 726 MIF			

44	Inspection	Microscope	Chech exposure grids			
	Graphene etching					
45	O2 plasma	TeplaGIGA	Strip_High_1min			all chips
46	O2 plasma	TeplaGIGA	Strip_High_30sec			3/41
47	Inspection	Microscope				1.5 too much
	Resist stripping					
48	Fast fill rinse	UFT resist	Bath 1 : main remover	5min, 70°C		
49	Remover 1165	UFT resist	Bain 2 : clean remover	5min, 70°C		
50	Cascade Tank	UFT resist	DI Rinse 2x			
51	Inspection	Microscope				
	Resist stripping					
48	ACETONE	Solvent Z13	1H			
49	IPA rinse	Solvent Z13	20min			
50	Air drying	Clean surface				
51	Inspection	Microscope				

4.3. Designs and chips distribution

Here are tables of how the designs are distributed on a chip

Chip 1: TLM structures

Chip_1	C1				C2				C3			
R1	TLM1	TLM2	TLM3	TLM4	TLM1	TLM2	TLM3	TLM4	TLM1	TLM2	TLM3	TLM4
R2	TLM1	TLM2	TLM3	TLM4	TLM1	TLM2	TLM3	TLM4	TLM1	TLM2	TLM3	TLM4
R3	TLM1	TLM2	TLM3	TLM4	TLM1	TLM2	TLM3	TLM4	TLM1	TLM2	TLM3	TLM4
R4	TLM1	TLM2	TLM3	TLM4	TLM1	TLM2	TLM3	TLM4	TLM1	TLM2	TLM3	TLM4
R5	TLM1	TLM2	TLM3	TLM4	TLM1	TLM2	TLM3	TLM4	TLM1	TLM2	TLM3	TLM4
R6	TLM1	TLM2	TLM3	TLM4	TLM1	TLM2	TLM3	TLM4	TLM1	TLM2	TLM3	TLM4
R7	TLM1	TLM2	TLM3	TLM4	TLM1	TLM2	TLM3	TLM4	TLM1	TLM2	TLM3	TLM4
R8	TLM1	TLM2	TLM3	TLM4	TLM1	TLM2	TLM3	TLM4	TLM1	TLM2	TLM3	TLM4
R9	TLM1	TLM2	TLM3	TLM4	TLM1	TLM2	TLM3	TLM4	TLM1	TLM2	TLM3	TLM4
R10	TLM1	TLM2	TLM3	TLM4	TLM1	TLM2	TLM3	TLM4	TLM1	TLM2	TLM3	TLM4
R11	TLM1	TLM2	TLM3	TLM4	TLM1	TLM2	TLM3	TLM4	TLM1	TLM2	TLM3	TLM4
R12	TLM1	TLM2	TLM3	TLM4	TLM1	TLM2	TLM3	TLM4	TLM1	TLM2	TLM3	TLM4
R13	TLM1	TLM2	TLM3	TLM4	TLM1	TLM2	TLM3	TLM4	TLM1	TLM2	TLM3	TLM4
R14	TLM1	TLM2	TLM3	TLM4	TLM1	TLM2	TLM3	TLM4	TLM1	TLM2	TLM3	TLM4
R15	TLM1	TLM2	TLM3	TLM4	TLM1	TLM2	TLM3	TLM4	TLM1	TLM2	TLM3	TLM4
R16	TLM1	TLM2	TLM3	TLM4	TLM1	TLM2	TLM3	TLM4	TLM1	TLM2	TLM3	TLM4
R17	TLM1	TLM2	TLM3	TLM4	TLM1	TLM2	TLM3	TLM4	TLM1	TLM2	TLM3	TLM4

Chip 3: Four probes structures

Chip_3 4 probes	1	2	3	4	5	6	7	8	9	10	11	12
1	4P	4P	4P	4P	4P	4P	4P	4P	4P	4P	4P	4P
2	4P	4P	4P	4P	4P	4P	4P	4P	4P	4P	4P	4P
3	4P	4P	4P	4P	4P	4P	4P	4P	4P	4P	4P	4P
4	4P	4P	4P	4P	4P	4P	4P	4P	4P	4P	4P	4P
5	4P	4P	4P	4P	4P	4P	4P	4P	4P	4P	4P	4P
6	4P	4P	4P	4P	4P	4P	4P	4P	4P	4P	4P	4P
7	4P	4P	4P	4P	4P	4P	4P	4P	4P	4P	4P	4P
8	4P	4P	4P	4P	4P	4P	4P	4P	4P	4P	4P	4P
9	4P	4P	4P	4P	4P	4P	4P	4P	4P	4P	4P	4P
10	4P	4P	4P	4P	4P	4P	4P	4P	4P	4P	4P	4P
11	4P	4P	4P	4P	4P	4P	4P	4P	4P	4P	4P	4P
12	4P	4P	4P	4P	4P	4P	4P	4P	4P	4P	4P	4P
13	4P	4P	4P	4P	4P	4P	4P	4P	4P	4P	4P	4P
14	4P	4P	4P	4P	4P	4P	4P	4P	4P	4P	4P	4P
15	4P	4P	4P	4P	4P	4P	4P	4P	4P	4P	4P	4P
16	4P	4P	4P	4P	4P	4P	4P	4P	4P	4P	4P	4P
17	4P	4P	4P	4P	4P	4P	4P	4P	4P	4P	4P	4P
18	4P	4P	4P	4P	4P	4P	4P	4P	4P	4P	4P	4P

4.4. Measurements tables, graphs and raw results