Design optimization for low light CMOS image sensors readout chain

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***Abstract*—For a CIS readout chain based on 4T pixel, column amplification and CDS, we confirm that thermal noise can be reduced to be neglected compared to $1/f$ noise using parameters independent of the pixel design, namely column level gain, bandwidth control or correlated multiple sampling (CMS). Based on analytic noise calculation and simulation results using $180nm$ process, we show that CMS has no advantage over CDS for thermal noise reduction but offers slightly more $1/f$ noise reduction (about 18% less $1/f$ noise if high number of samples is used). $1/f$ and RTS noise originating from the in-pixel source follower transistor are reported to be the dominant noise sources in CIS readout chain. Based on analytic noise calculation, we demonstrate that, for a given CMOS process, the input referred $1/f$ noise is minimal for a unique pair of gate dimensions of the in-pixel source follower and we give its expression as a function of technological parameters.**

I. Introduction

In state of the art low light CIS readout chains, circuit techniques reduce effectively the reset noise, pixel offset and thermal noise. However, even with a CDS, $1/f$ noise and random telegraph signal originating from in-pixel amplifier dominates the read noise [1]. To address this problem, in-pixel amplifiers, with relatively low in-pixel $1/f$ noise, like pMOS [2] transistor or buried channel nMOS [3] can be used. The $1/f$ noise optimization through transistor dimensions is important to be discussed. In fact, both the pixel conversion gain and the $1/f$ noise power spectral density (PSD) depend on the gate area of the in-pixel amplifying transistor, thus, for a given technology and design constraints, the optimal gate dimensions have to be found.

In this paper we present circuit techniques reducing thermal and $1/f$ noise. Section 2 presents the analog readout chain. Based on analytic noise calculation and transient noise simulations, we analyze, in section 3 the impact of multiple sampling (CDS and CMS), bandwidth control and column gain, which are independent of the pixel design, on thermal and $1/f$ noise. In section 4 we give a mathematical demonstration, using analytic $1/f$ noise expression, leading to the optimal gate dimensions of the in-pixel amplifying transistor, for a given CMOS process. We confirm the analytic results with transient noise simulations using a $180nm$ process.

II. Low light CIS readout chain

Classic low light CIS readout chains are based on 4T pixels with pinned photodiode, column level amplification with

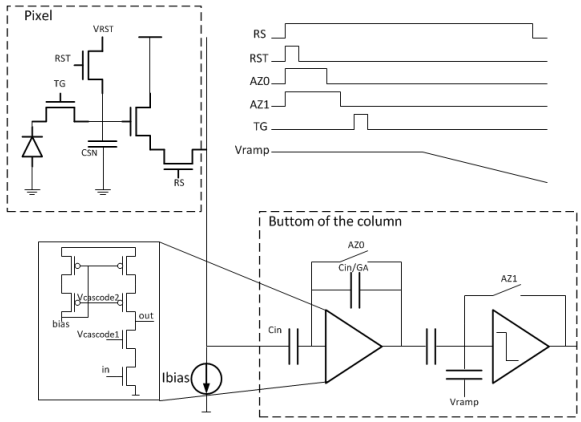

Fig. 1. 4T readout chain with in-pixel source follower, column amplification and CDS

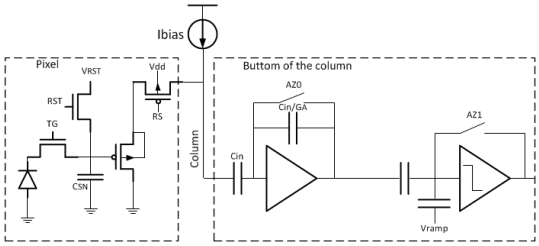

Fig. 2. 4T readout chain with in-pixel pMOS source follower, column amplification and CDS

bandwidth control and correlated double sampling (CDS) or multiple sampling (CMS). Figure 1 presents the readout chain used for noise calculation and transient noise simulations. The conversion gain (CG) of the 4T pixel is given by [4]

$$CG = \frac{qG_{SF}}{C_{SN} + C_{GD} + (1 - G_{SF})C_{GS}} \tag{1}$$

Where G_{SF} is the gain of the source follower stage, C_{SN} is the sense node capacitance defined by parasitic capacitances of the reset transistor, the transfer gate, the n+ junction and wiring. It is decorrelated from the amplifying transistor parasitic capacitances contribution. C_{GD} and C_{GS} are gate drain and gate source capacitances of the in-pixel amplifying transistor, and q the charge of one electron.

The source follower voltage gain is approximately given by $\frac{g_{m,SF}}{g_{ms,SF}} = \frac{1}{n}$, where $g_{m,SF}$ and $g_{ms,SF}$ are the amplifying

transistor gate and source transconductance and n is the slope factor whose values ranges from 1.2 to 1.6 [5]. If a pMOS in-pixel amplifying transistor is used, the bulk can be connected to the source leading to a more efficient source follower stage where the gain is approximately equal to unity (0.99 in simulation). In fact $g_{m,SF} = g_{ms,SF}$ for a bulk source connected transistor. In this case the conversion gain increases, it is approximately given by

$$CG = \frac{q}{C_{SN} + C_{GD}} \tag{2}$$

Column amplification is commonly used in sensitive CMOS image sensors to reduce thermal noise by controlling the bandwidth and minimizing the noise contribution of ADC stage [6] [7] [3] . As depicted in figure 1, column amplifier is implemented using a single stage complete cascode amplifier associated with two capacitors whose ratio determines the gain of the stage. CDS is operated by means of AZ0 and AZ1. Auto-zeroing at the column amplifier and ADC level reduces offsets of the source follower and column level amplifiers. For noise calculation, we consider the noisy model of a MOS transistor in saturation where the source drain noise current PSD including thermal and $1/f$ noise is given by [5]

$$I_n^2(f) = 4kT\gamma g_m + \frac{K}{C_{ox}^{\alpha} WL}\frac{g_m^2}{f} \tag{3}$$

Where k is the Boltzmann constant, T the absolute temperature, g_m the transconductance of the transistor, γ the excess noise factor given by, in case the transistor is in strong inversion, $\frac{2n}{3}$ where n is the slope factor [5], K is a process dependent parameter referred to as the Flicker noise constant, C_{ox} is the gate oxide capacitance area density for a given technology process and α is a process parameter whose value ranges between 1 and 2. For noise calculation in next sections, we consider $\alpha = 1$.

III. Correlated sampling after column amplification and bandwidth control

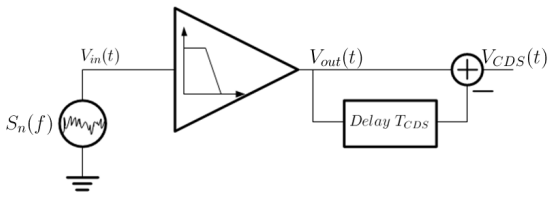

Fig. 3. CDS model

The correlated multiple sampling is a general case of CDS. CMS results in the average value of M samples obtained after successive correlated double sampling separated by T_{CMS} (average of the signal after CDS). The CMS is implemented after amplification and bandwidth control in column level circuitry. Figure 3 shows a simplified model of a CDS circuit. The signal is low-pass filtered before sampling. The output voltage after CMS can be expressed by

$$V_{CMS}(t) = \frac{1}{M}\sum_{k=0}^{M-1} V_{CDS}(t - kT_{CMS}) \tag{4}$$

Considering a first order low pass filtering with a cut-off frequency f_c, the transfer function of the CMS is given by

$$H_{CMS}(f) = \frac{1}{M^2}\frac{4sin^2(\pi T_{CDS} f)sin^2(\pi M T_{CMS} f)}{sin^2(\pi T_{CMS} f)} \tag{5}$$

Consider a noise source at the input of CMS circuit with a power spectral density $S(f)$ given by

$$S_n(f) = N_{th} + \frac{N_{1/f}}{f} \tag{6}$$

Where N_{th} is the white noise PSD and $N_{1/f}$ represents a $1/f$ noise constant. The output noise PSD is given by

$$S_{n,CMS}(f) = S_n(f) \times H_{CMS}(f) \tag{7}$$

For simplification we consider $T_{CDS} = MT_{CMS}$. Based on numerical evaluation, Figure 4 and 5 show the thermal noise variance normalized with $\frac{N_{th}\pi f_c}{M}$ and $1/f$ noise variance normalized with $N_{1/f}$ as a function of $2\pi f_c T_{CMS}$. Note that $2\pi f_c T_{CMS}$ should be at least equal to 5 for sufficient settling of the signal between two samples, thus, thermal noise variance is given by

$$\overline{V_{n,th,CMS}^2} \simeq \frac{\pi f_c N_{th}}{M} \simeq \frac{2\overline{V_{n,th,out}^2}}{M} \tag{8}$$

Thermal noise variance is then multiplied by $\frac{2}{M}$. and 1/f noise variance can be given by

$$\overline{V_{n,1/f,CMS}^2} \simeq \alpha_{CMS} N_{1/f} \tag{9}$$

Where α_{CMS} is ploted in figure 5, for different values of M, as a function of $2\pi f_c T_{CMS}$. The small signal analysis of the

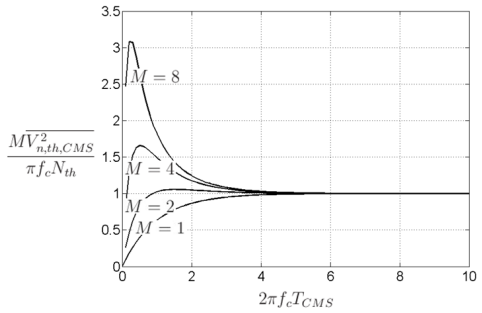

Fig. 4. Impact of CMS on a first order low pass filtered white noise

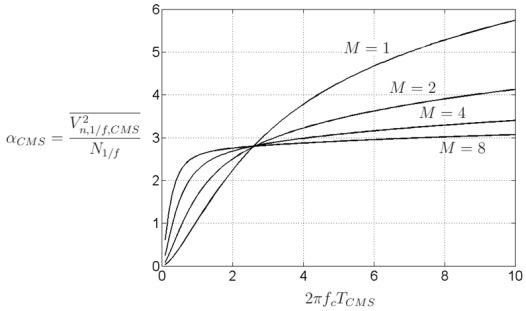

Fig. 5. Impact of CMS on a first order low pass filtered $1/f$ noise

pixel level and column level circuits detailed in [8] combined

with equation 8 leads to the expression of the variance of the input referred thermal noise

$$\overline{Q_{n,th}^2} = 2\frac{kT(C_{SN}+C_{GD})^2}{MG_AC}\left(\frac{g_{m,A}}{g_{m,SF}}\gamma_{SF}\beta+\gamma_A\right) \quad (10)$$

$C = C_L + \frac{C_{in}}{G_A+1}$ and $\beta = \left(\frac{C_{SN}+C_{GS}+C_{GD}}{C_{SN}+C_{GD}}\right)^2$ Where C_{in} is the integrating capacitor of the column amplifier,C_L the load capacitance, C_{GS} and C_{GD} are gate source and gate drain capacitances of the in-pixel source follower transistor, G_A the column level gain, γ_{SF} and γ_A are respectively the noise excess factors of the in-pixel amplifying transistor and column amplifying transistor.

The design parameters, independent of the pixel design, that reduce thermal noise are the number of CMS samples M, the column gain G_A and the frame rate inversely proportional to C. But since increasing M for a given readout chain decreases proportionally the frame rate, using M samples has the same effect of reducing M times the bandwidth (using MC instead of C). Thus CMS shows no advantage for thermal noise reduction. Figures 6 and 7 show transient noise simulation results (using ELDO) that confirm analytic noise calculation. The results of figure 6 have been obtained with $C_L = 150fF$. Figures show that increasing M is equivalent to increasing C_L. Based on [8] and equation 9, The variance of the input

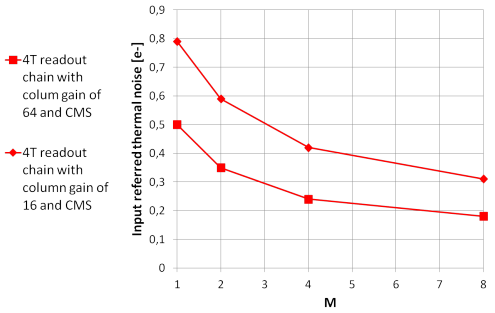

Fig. 6. Transient noise simulation results showing the impact of multiple sampling and column gain on thermal noise for the redout chain of figure 1

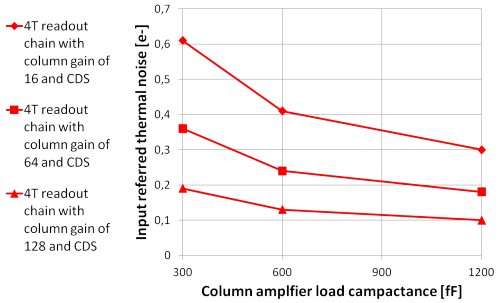

Fig. 7. Transient noise simulation results showing the impact of bandwidth control and column gain on thermal noise for the redout chain of figure 1

referred $1/f$ noise is given by

$$\overline{Q_{n,1/f}^2} = \alpha_{CMS}\frac{K}{C_{ox}^{\alpha}WL}(C_{SN}+c_{GS}WL+c_{GD}W)^2 \quad (11)$$

Where c_{GS} is the gate source capacitance per unit area and c_{GD} is the gate drain capacitance per unit length of the in-pixel amplifying transistor. For $1/f$ noise, analytic noise calculation shows that multiple sampling offers a slight advantage compared to CDS as shown in figure 5 (about 18% less noise for $M = 8$). This result is confirmed with transient noise simulations shown in figure 8.

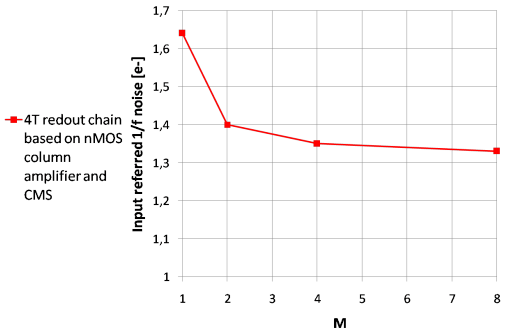

Fig. 8. Transient noise simulation results showing the impact of multple sampling on $1/f$ noise for the redout chain of figure 2 with column gain of 16

IV. In-pixel transistor gate dimensions optimization

Thermal noise originating from the pixel source follower and the column amplifier can be reduced by means of the column level gain G_A and by increasing proportionally the readout time and C_L. Transient noise simulations results shown in figures 6, 7 and 8 show that using these techniques, thermal noise can be reduced to make $1/f$ and RTS noise originating from the in-pixel source follower dominant.

Based on equation 11, the $1/f$ noise can be optimized by choosing the source follower dimensions that minimize F(W,L) defined by :

$$F(W,L) = \frac{1}{WL}(C_{SN}+c_{GS}WL+c_{GD}W)^2 \quad (12)$$

The minimum of $F(W,L)$ corresponds to the optimal W and L. It becomes a mathematical problem to solve in the set $[W_{min},+\infty]\times[L_{min},+\infty]$, where W_{min} and L_{min} are the minimum gate dimensions allowed by technology. The local and global extrema correspond to the points that nullify the gradient. Otherwise they exist in the border of the set. After calculation of the gradient, one can find :

$$\overrightarrow{\nabla}F(W,L) = 0 \Leftrightarrow L = -\left(\frac{C_{SN}}{Wc_{GS}}+\frac{c_{GD}}{c_{GS}}\right)$$

Since L is positive as all the parameters of F, $F(W,L)$ has no extrema except on the square defined by the border of $[W_{min},W_{max}]\times[L_{min},L_{max}]$. The problem is then simplified and only the functions $F(W_{min},L)$ and $F(W,L_{min})$ have to be studied. We find for $F(W_{min},L)$

$$\begin{cases} \frac{\partial}{\partial L}F(W_{min},L) = 0 \Leftrightarrow L = \frac{c_{GD}}{c_{GS}}+\frac{C_{SN}}{c_{GS}W_{min}} \\ \lim_{L\to 0}\frac{\partial}{\partial L}F(W_{min},L) = -\infty \\ \lim_{L\to+\infty}\frac{\partial}{\partial L}F(W_{min},L) = +\infty \end{cases}$$

and for $F(W,L_{min})$:

$$\begin{cases} \frac{\partial}{\partial W}F(W,L_{min}) = 0 \Leftrightarrow W = \frac{C_{SN}}{c_{GS}L_{min}+c_{GD}} \\ \lim_{W\to 0}\frac{\partial}{\partial W}F(W,L_{min}) = -\infty \\ \lim_{W\to+\infty}\frac{\partial}{\partial W}F(W,L_{min}) > 0 \end{cases}$$

We conclude that $F(W,L)$ only admits two minimums in the border of $[W_{min},+\infty[\times[L_{min},+\infty[$ and the optimal (W,L) is either :

$$(W,L)_{opt,W_{min}} = (W_{min}, \frac{c_{GD}}{c_{GS}} + \frac{C_{SN}}{c_{GS}W_{min}}) \quad (13)$$

or :

$$(W,L)_{opt,L_{min}} = (\frac{C_{SN}}{c_{GS}L_{min}+c_{GD}}, L_{min}) \quad (14)$$

By calculating the difference between values of $F(W,L)$ in optimal points defined in equations (13) and (14). One can find that it is proportional to $c_{GS}W_{min}L_{min} - C_{SN}$. Thus, if $C_{SN} > c_{GS}W_{min}L_{min}$ the optimal point is defined by equation (13), and if $C_{SN} < c_{GS}W_{min}L_{min}$ the optimal point is defined by equation (14). This result is interesting since it gives the optimal (W,L) for a given technology depending on C_{SN}. In case a minimum point (W_{min},L) or (W,L_{min}) is out of the possible range, the closest possible point is to be used instead. Based on this analysis, it is simple to find the optimal in-pixel source follower gate dimensions. This transistor can be biased depending on the obtained W/L ratio.
To give an example, we plot, in figures 3, the calculated input referred noise, of a $180nm$ process where the minimum gate width is given by $0.22\mu m$ and the minimum gate length is given by $0.3\mu m$, $C_{ox} = 5.10fF/\mu m^2$, $c_{GS} = 3.4fF/\mu m^2$ and $c_{GD} = 0.4fF/\mu m$ and $C_{SN} = 0.8fF$. Analytic noise calculation shows that, for the $180n$ we used, $1/f$ noise is minimal for in-pixel amplifying transistor with the minimum width and large length ($\frac{c_{GD}}{c_{GS}} + \frac{C_{SN}}{c_{GS}W_{min}} = 1.18\mu m$) we confirm this result with transient noise simulation results shown in figure 10.

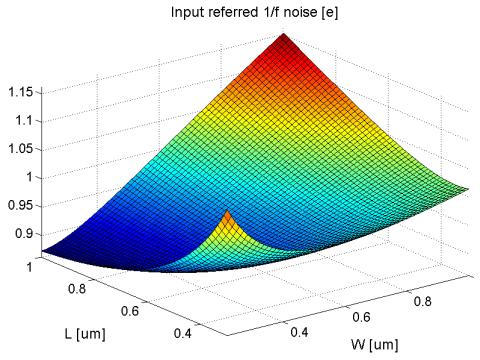

Fig. 9. Calculated input referred $1/f$ noise of the readout chain of figure 1 as a function of the width W and length L of the in-pixel amplifying transistor for a $180nm$ process

V. Conclusion

Based on analytical noise calculation confirmed with transient noise simuations using a $180nm$ process, we find the following results

- Thermal noise can be reduced independently from the in-pixel source follower design by means of column level gain, bandwidth control or multiple sampling.
- CMS shows no advantage over CDS for thermal noise reduction and offers slightly more $1/f$ noise reduction (about 18% less $1/f$ noise if high number of samples is used).
- $1/f$ noise dominates then the read noise. For a given CMOS process, and a given C_{SN}, the optimal gate dimensions W and L for the minimum $1/f$ noise can be obtained analytically. This transistor can be biased depending on the obtained W/L ratio.
- For a given CMOS process and a given C_{SN}, if $C_{SN} > c_{GS}W_{min}L_{min}$ the optimal point is defined by $(W,L)_{opt,W_{min}} = (W_{min}, \frac{c_{GS}}{c_{GS}} + \frac{C_{SN}}{c_{GS}W_{min}})$. It is defined by $(\frac{C_{SN}}{c_{GS}L_{min}+c_{GD}}, L_{min})$ if $C_{SN} < c_{GS}W_{min}L_{min}$.

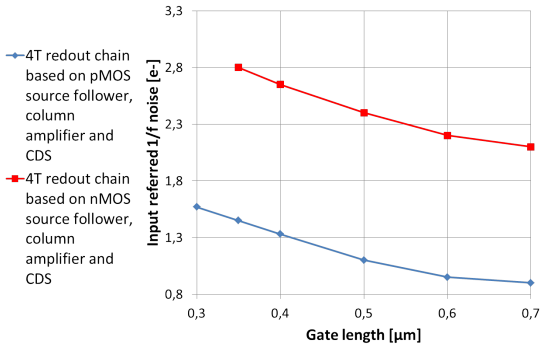

Fig. 10. Transient noise simulation results showing the impact of in-pixel amplifying transistor gate dimensions optimization on input referred noise of the readout chains of figures 1 and 2

Acknowledgment

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