The Impact of Body Biasing on the Gain-Cell Memories: A Silicon Proof

P. Meinerzhagen, A. Teman, A. Fish, and A. Burg

Gain-Cell based embedded DRAMs are a high density potential alternative to mainstream SRAM. However, the limited data retention time of these storage bits result in the need for power consuming periodic refresh cycles. This study examines the spatial retention time of gain-cells, spread out across an entire memory block, and measures the impact of body biasing as a control factor to improve the retention time. The concept is demonstrated through silicon measurements of a test chip manufactured in a logic compatible 0.18 µm CMOS node. While there is a large retention time spread across the measured 2 kb gain-cell array, the minimum, average, and maximum retention times are improved by up to 2 orders of magnitude when sweeping the body voltage over a range of 375 mV.

Introduction: Embedded memories are a crucial building block of virtually all modern system-on-chip (SoC) designs, and account for an increasingly dominant area and power share [2]. Gain-cell based embedded DRAM (eDRAM) has recently gained significant popularity as a potential successor of the conventional mainstream SRAM solution, primarily due to its higher integration density, decoupled read and write ports for improved robustness, logic compatibility, and inherent two-port functionality [1]. The application field of gain-cell based eDRAM is broad, ranging from high-speed caches in microprocessors [2] to ultra-low power systems [3]. The main drawback of gain-cell memories is the need for periodic refresh cycles, which results in a considerable amount of power consumption and limits the read/write availability of the memory array. Therefore, to improve the competitiveness of gain-cell eDRAM in terms of power consumption and array availability, it is crucial to extend the data retention time.

Data levels in eDRAM are stored as charge upon an in-cell, storage node (SN) capacitance, and therefore, data retention is limited by the time it takes for this charge to leak away. Accordingly, several simple measures can be taken to extend the retention time, such as: 1) increasing the storage node capacitance (C_{SN}) through layout techniques [4, 3]; 2) minimizing the subthreshold conduction through the write access transistor (MW) by using low-leakage MOS transistors [5, 3]; and 3) employing write bitline (WBL) control schemes to minimize charge loss through MW [6]. An additional technique that has not yet been applied to gain-cells is V_{T} adjustment through body biasing. Whereas the application of a reverse body bias (RBB) raises the threshold voltage (V_{T}, and therefore, reduces the charge loss through subthreshold leakage, this means of control can also improve the array availability by applying a forward body bias (FBB) during refresh cycles to reduce access time [7]. In this letter, for the first time, silicon measurements show the precise retention times of all bitcells in a 2 kb gain-cell macrocell, and display the impact of body biasing on these retention times.

Bitcell Design: Fig. 1(a) shows the schematic and the basic operation of the two-transistor (2T) all-PMOS gain-cell used in this study to demonstrate the dependence of retention time on body bias. MW is the write-access transistor, used to transfer the data driven onto the WBL to the storage node capacitance (C_{SN}). MR is the read-access transistor, used to read out the data level stored in the bitcell. A write access is initiated by applying an underdrive voltage ($-V_{\mathrm{NWL}}$) to the write wordline (WWL) in order to properly transfer a logic '0' level (V_{SS}) from WBL to SN in a short time. A read access is initiated by pre-discharging the read bitline (RBL) and subsequently raising the read wordline (RWL). If a logic '0' is stored on C_{SN}, MR will charge RBL past a detectable threshold, whereas if a logic '1' (V_{DD}) has been written to the SN, RBL will remain discharged. The basic in-cell capacitance is increased by building up side-wall capacitors between SN and a constant potential (V_{DD}) atop the bitcell footprint, using all 6 available metal layers [3].

The dominant leakage mechanism that causes the deterioration of the stored data levels is clearly the subthreshold conduction through MW. This is especially true for mature CMOS nodes, such as the 0.18 µm process used in this study, but has been shown to hold for deeply scaled CMOS nodes, as well [3]. In order to achieve the highest possible retention time, an I/O PMOS transistor was used to implement MW, as this device features the lowest subthreshold conduction among all devices offered in the chosen 0.18 µm CMOS technology [4]. By implementing MR with a PMOS device, as well, the entire array resides in an equi-potential n-well, enabling simple control over the body voltage of the bitcells. Reverse biasing the n-well at a voltage, V_{B}, above V_{DD}, increases the V_{T} of the transistors, thereby further suppressing the subthreshold conduction of MW and improving the retention time. Likewise, forward biasing V_{B} below V_{DD} lowers the V_{T} of the transistors, resulting in faster access times for both read and write. The variable ΔV_{B} is used to express the amount of body biasing, according to (1):

$$V_{\mathrm{B}} = V_{\mathrm{DD}} + \Delta V_{\mathrm{B}}, \tag{1}$$

where a positive value of ΔV_{B} coincides with an applied RBB and a negative value represents an applied FBB. In this study, we will consider a biasing range of -250 mV$< \Delta V_{\mathrm{B}} <$125 mV, corresponding to a V_{T} range of $-770\,\mathrm{mV} < V_{\mathrm{T}} < -625\,\mathrm{mV}$ for a PMOS I/O device under nominal conditions with V_{DD}=750 mV.

Macrocell Architecture and Test Chip Design: Fig. 1(b) shows the layout of a 2 kb gain-cell macrocell manufactured in 0.18 µm CMOS technology. The core bitcell array consists of 64×32 gain-cells, all sharing the same n-well and V_{B}. N-well contacts are provided every 16 rows, and at the top and the bottom of the array. In addition to the bitcell array, the macrocell comprises the following peripheral circuits: 1) A write address pre- and post-decoder that drives V_{DD} or $-V_{\mathrm{NWL}}$ onto WWL; A read address pre- and post-decoder that drives V_{DD} or V_{SS} onto RWL; level-shifters; WBL drivers; readout sense buffers; and timing control units.

Fig. 1(c) shows a microphotograph of the manufactured, bonded test chip. In addition to the 2 kb gain-cell macrocell in the lower-left corner, the chip contains a Built-in Self Test (BIST) unit. The main features of the BIST can be summarized as follows: 1) address sequence generation (increasing, decreasing, pseudo-random); 2) data pattern generation (checkerboard, pseudo-random, all-'1', all-'0'); 3) programmable refresh period of the memory under test (MUT); 4) pass/fail decision during readout of the MUT; 5) embedded SRAM for storing bit maps of MUT retention time, read failures, or write failures; and 6) support for two-port operation of MUT.

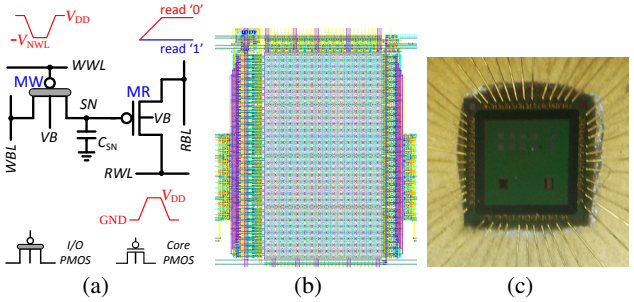

Fig. 1 *(a) 2T gain-cell design and basic operation, (b) layout of 2kb gain-cell memory macro, (c) microphotograph of test chip.*

Silicon Measurement Results: The packaged test chips were mounted on a test board in a generic socket and connected to an Agilent XXXX and XXXX for digital pattern generation and logic analysis. The main supply of the memory macrocell was supplied with a 750 mV supply voltage, and the body voltage was swept from 500 to 875 mV to analyze the impact of body biasing. A separate negative voltage of −1.5 V was supplied to the macrocell for WWL underdrive. The BIST and other digital control units were supplied with the technology's nominal voltage of 1.8 V that is down-shifted to the memory supply inside the macrocell. Both the write and read access times were set to 1 µs for robust write and read operations, even at the low V_{DD}. This ensured that the measured failures were due to retention time, and not caused by incomplete writes or erroneous reads due to insufficient access time. Table 1 summarizes the primary specifications of the measurement setup.

Measurements indicate that the 2-PMOS gain-cell retains logic '1' levels for extensive periods (>1 s), even when the WBL is held at 0 V (which maximizes the subthreshold conduction of MW). This coincides with previous reports that logic '1' levels decay very slowly due to the increasing reverse gate overdrive and body effect of MW as the SN voltage drops [4]. Therefore, the gain-cell's retention time is almost exclusively

Table 1: Measurement Setup.

V_{DD}	750 mV
ΔV_B	−250 to 125 mV
Write access time	1 µs
Read access time	1 µs
Write-'1' disturb activity	25%
Temperature	Room temperature (uncontrolled)

limited by its ability to hold a logic '0' level. The decay of a cell's logic '0' level is heavily dependent on the state of the WBL. When WBL is low, subthreshold conduction discharges the SN, reinforcing a stored logic '0' level. On the other hand, when WBL is high, a worst-case condition occurs, as leakage through MW causes accelerated decay of a stored logic '0' level. Our measurement setup assumes a 50% write duty cycle (i.e., there is a write access during 50% of the time) and that the probability of writing a '1' (which requires pulling WBL up to V_{DD}) is 50% as well. Overall, this leads to a write-'1' disturb activity factor ($\alpha_{disturb}$) of 25%.

Using the measurement setup described above, retention time was measured for the entire 2 kb array under standard biasing conditions (i.e., $V_B = V_{DD} = 750$ mV) at room temperature (temperature is not controlled). The results of this measurement are shown in Fig. 2(a). The minimum and maximum retention times (t_{ret}) of 2,048 measured gain-cells were found to be 23 and 569 ms, respectively. The majority of the cells exhibited retention times in the range of 20 to 200 ms (dark and light blue color), whereas a small number of cells exhibited considerably higher retention times (yellow, orange, and red colors). In order to better visualize the differences among the lower retention times (20–2000 ms), Fig. 2(a) plots t_{ret} on a logarithmic scale. There is no systematic pattern, indicating that the retention time variability arises from local (within-die), random process parameter variations.

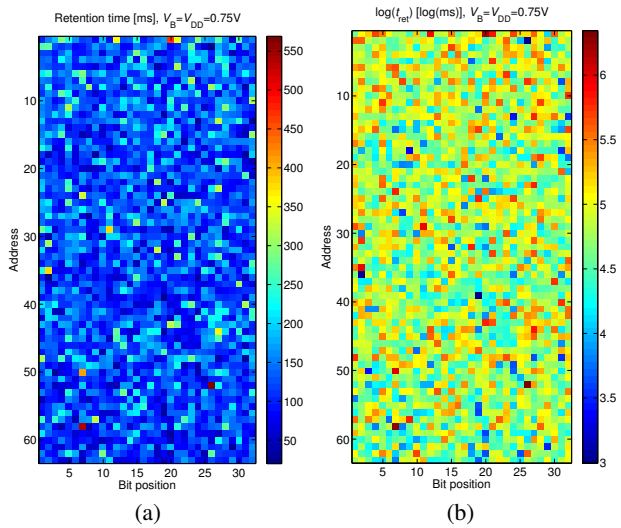

Fig. 2 *(a) Retention time (t_{ret}) map of 2 kb 2T gain-cell array with zero body bias and $\alpha_{disturb}$=25% at room temperature. (b) Map of* $\log(t_{ret})$.

The impact of body biasing on the measured retention times was evaluated by sweeping V_B from 500 mV to 875 mV (-250 mV< ΔV_B <125 mV). The minimum and maximum measured retention times across the entire array are plotted in Fig. 3. This figure clearly shows that the minimum and maximum retention times change by up to 2 orders of magnitude over this 375 mV V_B range. As expected, the best cells with the highest retention time remain at the same location under varying V_B (not shown in figure).

Finally, Fig. 4 shows the distributions of the retention time across the 2k measured cells, for three biasing conditions: 100 mV FBB, zero body biasing (i.e., $V_B = V_{DD}$), and 100 mV RBB. The minimum retention time for each biasing condition is annotated. The spread of retention time across the array is large; however, there is a clear improvement in the minimum, as well as in the average retention times with each 100 mV increase in the body bias, illustrating the effectiveness of the proposed technique.

Conclusions: This study measured the impact of body bias on the retention time of an all-PMOS 2T gain-cell topology in a mature 0.18µm CMOS

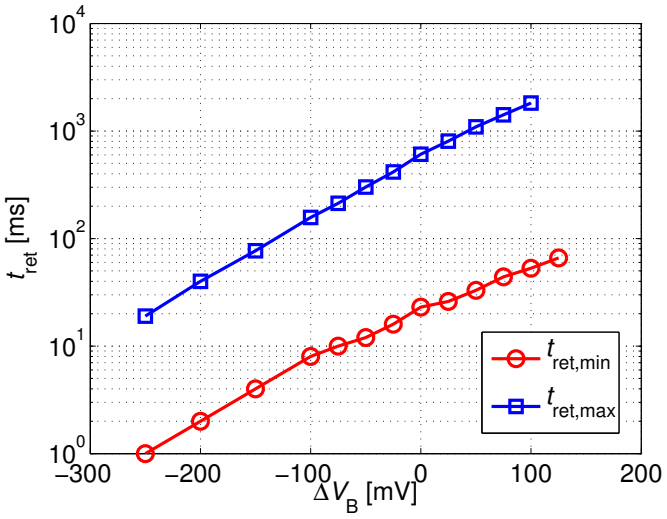

Fig. 3 *Minimum ($t_{ret,min}$) and maximum ($t_{ret,max}$) retention times across the entire 2 kb array, as a function of ΔV_B, for $V_{DD} = 750$ mV with $\alpha_{disturb}$=25% at room temperature.*

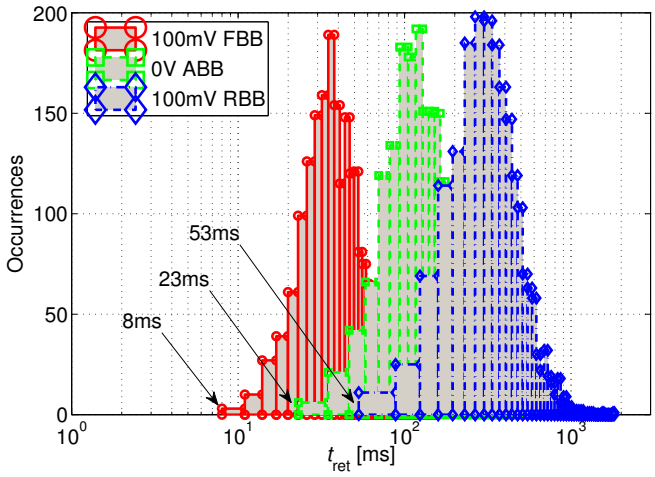

Fig. 4 *Retention time distributions of 2,048 measured gain-cells for 100 mV FBB, zero body biasing, and 100 mV RBB with $V_{DD} = 750$ mV and $\alpha_{disturb}$=25% at room temperature.*

technology. The measured retention time of a 2 kb memory macrocell is improved by 2.3× (from 23 to 53 ms) with a reverse body bias of only 100 mV. The cell-to-cell retention time variability is high, ranging from 23 to 569 ms; however, the absence of a systematic pattern in the measured retention time maps suggests that the high variability is due to local parametric variations, which are particularly high in memory array due to the use of minimum-sized devices. Moreover, the process parameters of I/O devices may be less carefully controlled those of core transistors. Nevertheless, reverse body biasing is an attractive technique to improve the minimum (as well as the average) retention time. At the same time, the retention time penalty for forward body biasing (used for fast memory access) is high, exhibiting a 2.9× reduction for a 100 mV FBB. However, a possible control scheme could dynamically apply an RBB during retention and periodically applying an FBB during refresh cycles to maximize array availability. Overall, sweeping the body voltage over a range of 375 mV provides an interesting trade-off between access and retention time, with the retention time range spanning almost 2 orders of magnitude.

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References

1 A. Teman, P. Meinerzhagen, A. Burg, and A. Fish, "Review and classification of gain cell eDRAM implementations," in *Proc. IEEE IEEEI*, 2012.

2 K. C. Chun *et al.*, "A 667 MHz logic-compatible embedded DRAM featuring an asymmetric 2T gain cell for high speed on-die caches," *IEEE JSSC*, 2012.

3 P. Meinerzhagen, A. Teman, R. Giterman, A. Burg, and A. Fish, "Exploration of sub-VT and near-VT 2T gain-cell memories for ultra-low power applications under technology scaling," *J. Low Power Electronics and Applications (JLPEA), under review*, 2013.

4 P. Meinerzhagen, A. Teman, A. Mordakhay, A. Burg, and A. Fish, "A sub-VT 2T gain-cell memory for biomedical applications," in *Proc. IEEE Subthreshold Microelectronics Conference*, 2012.

5 Y. Lee *et al.*, "A 5.4nW/kB retention power logic-compatible embedded DRAM with 2T dual-Vt gain cell for low power sensing applicaions," in *Proc. IEEE A-SSCC*, 2010.

6 R. Iqbal *et al.*, "Two-port low-power gain-cell storage array: voltage scaling and retention time," in *Proc. IEEE ISCAS*, 2012.

7 A. Teman, O. Yadid-Pecht, and A. Fish, "Leakage reduction in advanced image sensors using an improved AB2C scheme," *IEEE Sensors Journal*, vol. 12, no. 4, pp. 773 –784, April 2012.