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MoS_2 Transistors Operating at Gigahertz Frequencies

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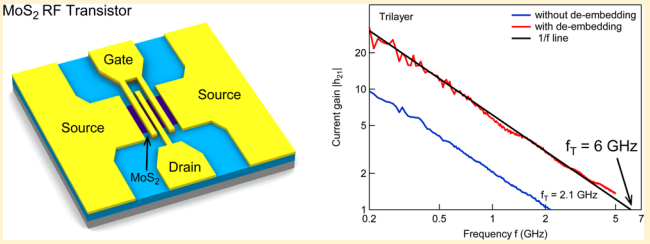
Supporting Information

ABSTRACT: The presence of a direct band gap[1−4] and an ultrathin form factor[5] has caused a considerable interest in two-dimensional (2D) semiconductors from the transition metal dichalcogenides (TMD) family with molybdenum disulfide (MoS_2) being the most studied representative of this family of materials. While diverse electronic elements,[6,7] logic circuits,[8,9] and optoelectronic devices[12,13] have been demonstrated using ultrathin MoS_2, very little is known about their performance at high frequencies where commercial devices are expected to function. Here, we report on top-gated MoS_2 transistors operating in the gigahertz range of frequencies. Our devices show cutoff frequencies reaching 6 GHz. The presence of a band gap also gives rise to current saturation,[10] allowing power and voltage gain, all in the gigahertz range. This shows that MoS_2 could be an interesting material for realizing high-speed amplifiers and logic circuits with device scaling expected to result in further improvement of performance. Our work represents the first step in the realization of high-frequency analog and digital circuits based on 2D semiconductors.



KEYWORDS: *MoS_2, 2D semiconductors, radio frequency, current gain, voltage gain, power gain*

The operating frequency of semiconductor devices has increased remarkably since the invention of the first transistor. By reducing the transistor's critical dimensions, we can at the same time reduce the electron transit time and the gate capacitance that boosts the performance of transistors in the high-frequency range. The next challenging step is to reduce the device dimensions in the vertical direction to their ultimate limit. For this purpose, nanoscale materials such as carbon nanotubes (CNTs)[11,12] and graphene[13−15] have been suggested. Theory predicts that CNTs operating in the ballistic regime could provide a gain in the terahertz range.[16] However, their small size carries disadvantages, such as the large contact resistance resulting in high device impedance, making it difficult to measure and integrate CNT-based devices with a standard radio frequency (RF) setup.

Another candidate for future high-frequency devices is graphene. Graphene shows large carrier mobility[17] and saturation velocity.[18] Graphene field-effect transistors (GFETs) have lower impedance compared to CNT-FETs, making impedance matching a less sensitive issue in GFETs than in CNT-FETs. The other important advantage of graphene compared to CNTs lies in its two-dimensional (2D) nature and high mobility that results in large transconductance g_m and intrinsic cutoff frequency f_T,[13,19,20] the frequency at which current gain becomes unity.

Power and voltage amplification are also important transistor applications in electronic circuits. The maximum frequency of oscillation f_{max} is the frequency at which the power gain equals unity. In high-performance voltage and power amplifiers, f_{max} should be as high as possible. In the case of RF-GFETs, f_{max} still remains lower than the current gain cutoff frequency f_T[19,20] because it is relatively difficult to achieve saturation in graphene FETs due to the absence of a band gap. In devices that lack saturation in drain current, this results in high values of drain conductance g_{ds} and limited voltage gain $A_v = g_m/g_{ds}$.

Other 2D materials such as for example molybdenum disulfide (MoS_2) could be interesting for applications in RF electronics, especially in high-frequency digital electronics where voltage gain higher than 1 is desired. MoS_2 is a semiconductor from the family of transition-metal dichalcogenide (TMD) materials with the common formula MX_2, where M represents a transition metal (M = Mo,W, Nb, Ta, Ti, or Re) and X stands for either Se, S, or Te. MoS_2 has a bandgap and unique valley[21,22] and spin properties as well as remarkable properties for new electronic and optoelectronic applications.[23] In contrast to graphene, which is a semimetal, MoS_2 is a 2D semiconductor with an electronic structure dependent on its thickness.[1−4] First, locally gated FETs based on monolayers of MoS_2[24] were shown to have room-temperature current on/off ratio higher than 10^8. Monolayer MoS_2 also shows voltage gain[25] larger than 10, due to its natural band gap, high intrinsic transconductance and drain-source current saturation.[10] The combination of all these properties makes MoS_2 attractive for high-frequency applications. Self-consistent ballistic quantum transport simulations, independent of mobility values, show that cutoff frequencies well above 100 GHz could be possible for MoS_2 transistors with channel lengths of $L_g \sim 15$ nm, operating in the ballistic limit.[26] In addition, large-area MoS_2 can be prepared using either liquid-phase exfoliation[27] or CVD growth.[28−30]

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Here, we characterize top-gated MoS_2 FETs in the high-frequency range. The current gain of MoS_2 FETs decreases with increasing frequency and shows the typical $1/f$ dependence for different thicknesses of 2D MoS_2 crystals. We realized MoS_2 FETs with a maximum transconductance $g_m = 54\ \mu S/\mu m$, the highest transconductance in MoS_2 transistors reported up to date,[10] and showing current saturation. The highest intrinsic cutoff frequency f_T derived from the measured scattering parameters is 6 GHz and presents a strong dependence on the bias voltage, gate voltage, and material thickness. MoS_2 RF transistors also show a voltage gain higher than 1 and a maximum frequency of oscillation comparable to the cutoff frequency, reaching $f_{max} = 8.2$ GHz, which makes MoS_2 interesting for high-frequency logic circuits and amplifiers.

Our MoS_2 FETs are fabricated from MoS_2 exfoliated onto a highly resistive intrinsic Si substrate covered with 270 nm thick SiO_2.[31] Figure 1 shows the device layout of a MoS_2 FET with probe pads in the ground−signal−ground configuration (GSG) designed for high-frequency measurements. We have fabricated RF transistors based on 1L-MoS_2, 2L-MoS_2, 3L-MoS_2, and multilayer (5 nm thick) MoS_2 crystals shown in Figure 1b. Electrical contacts were patterned using electron-beam lithography and by depositing 90 nm thick gold electrodes. This was followed by an annealing step at 200 °C in order to remove resist residue and decrease the contact resistance. Atomic layer deposition (ALD) was used to deposit a 30 nm thick layer of high-κ dielectric HfO_2. Local top gates for controlling the current in the two branches were fabricated using another e-beam lithography step followed by evaporation of 10 nm/50 nm of Cr/Au. All of our devices had a gate length $L_g = 240$ nm with the underlap region 50 nm long on both sides of the gate electrode. Channel widths are in the 9−21.5 μm range due to the stochastic nature of the MoS_2 exfoliation process.

Transfer and output characteristics of 1L-MoS_2 and 3L-MoS_2 FETs are shown in Figure 2. All our devices show transconductance typical of n-type semiconductors with on-state current reaching ~300 $\mu A/\mu m$ for $V_{ds} = 2$ V and gate voltage $V_{tg} = 10$ V in the case of monolayer MoS_2. The dielectric constant of 30 nm HfO_2 deposited at 200 °C is 14, probably due to surface impurities trapped between the HfO_2 and MoS_2 layer. From the $I_{ds}-V_{tg}$ characteristic of our devices, we extract estimates for the field effect mobility and contact resistance $\mu_{FE} = 85\ cm^2/(V\ s)$ and $R_c = 2.0\ k\Omega\cdot\mu m$ for the case of the monolayer device and $\mu_{FE} = 51\ cm^2/(V\ s)$ and $R_c = 3.1\ k\Omega\cdot\mu m$ for the trilayer device (Figure S1 in Supporting Information).

One of the most important parameters affecting the high-frequency performance of transistors is the transconductance $g_m = dI_{ds}/dV_{tg}$, shown in the insets of Figure 2a,b. The magnitude of g_m drastically rises when increasing V_{ds} in the range from 100 mV to 1.5 V for 1L-MoS_2 and from 100 mV to 2 V for 3L-MoS_2, reaching a maximum of ~44 $\mu S/\mu m$ for the single-layer and ~54 $\mu S/\mu m$ for the trilayer device. These values are comparable to those reported for the first graphene RF devices[13] and are desirable for achieving high-frequency operation. Our devices can also easily achieve saturation. Figure 2c,d show the I_{ds}-V_{ds} characteristics of two MoS_2 devices with a different number of layers. We measure very low values for the channel conductance g_{ds}, reaching values as low as ~3 $\mu S/\mu m$ in the trilayer device at $V_{ds} = 3$ V and $V_{tg} = 4$ V.

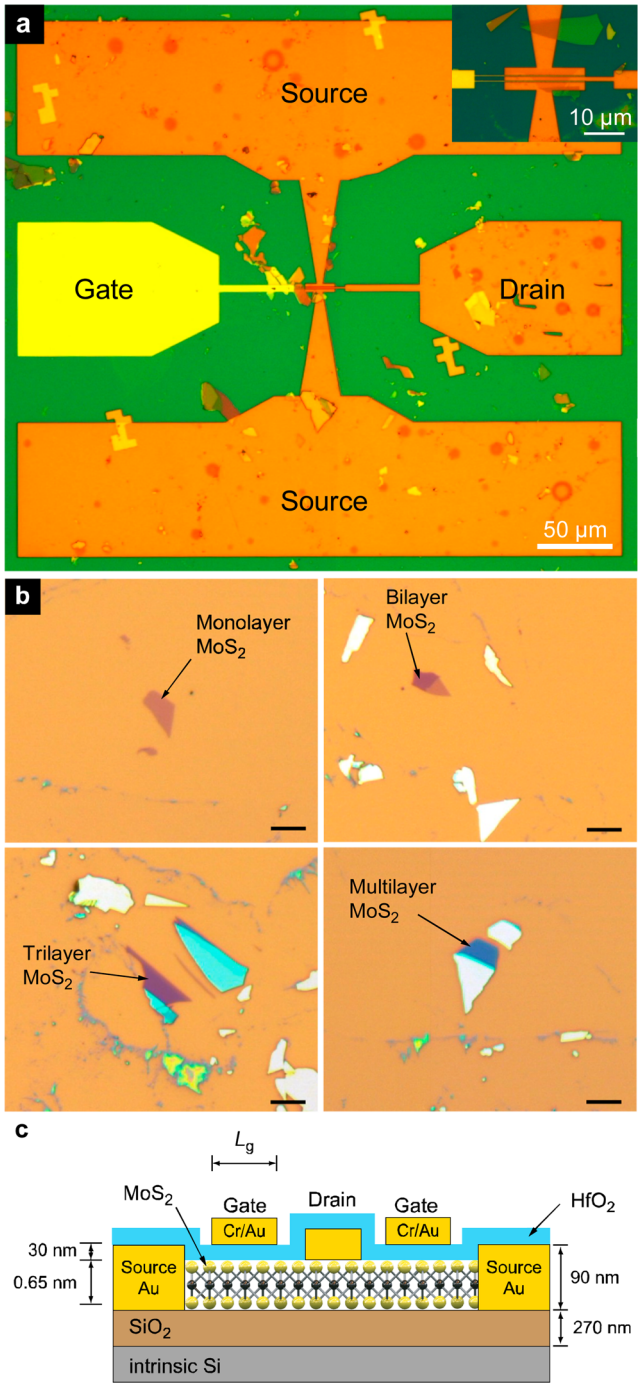

Figure 1. MoS_2-based high-frequency transistors. (a) Optical image of the device layout with ground−signal−ground pads for the drain and the gate on intrinsic Si substrate covered with a 270 nm thick SiO_2 layer. The inset shows the magnified optical image of the coplanar waveguide with the gate length $L_g = 240$ nm. The total channel length is 340 nm. Underlap regions are 50 nm long. (b) Optical images of 1L-MoS_2, 2L-MoS_2, 3L-MoS_2, and multilayer (5 nm thick) MoS_2. Transistors are fabricated on top of regions with uniform crystal thickness. Scale bar is 10 μm long. (c) Schematic cross-sectional view of the RF-MoS_2 transistor.

One of the main figures of merit to estimate the performance of radio frequency devices is the cutoff frequency f_T, the frequency at which the current gain becomes unity[32]

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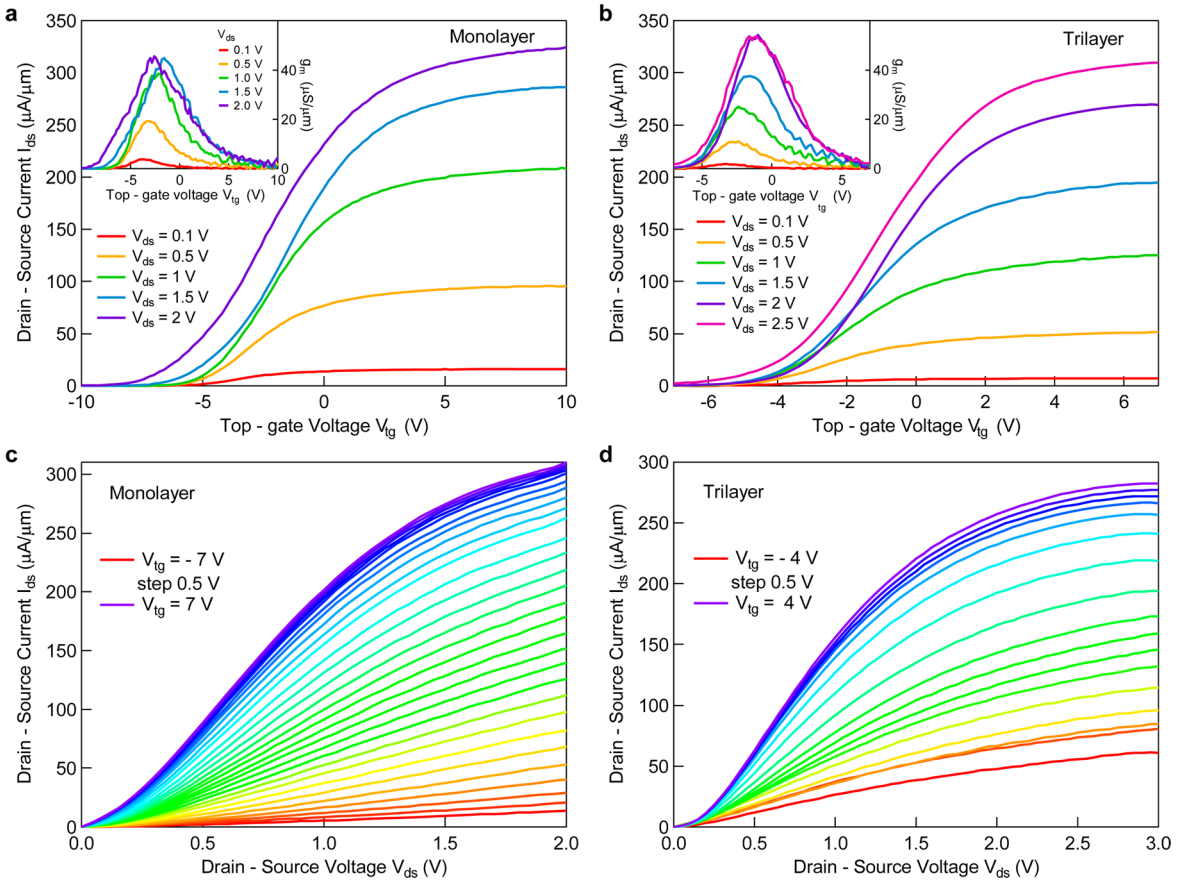

Figure 2. DC output characteristics of MoS_2 RF transistors. (a) Transfer characteristic for 1L-MoS_2 FET under the applied drain voltage in the range from V_{ds} = 0.1−2 V with a step of 0.5 V. (b) Transfer characteristic for 3L-MoS_2 FET under the applied drain voltage in the range from V_{ds} = 0.1−2.5 V with a step of 0.5 V. Insets in panels a and b show the transconductance of 1L-MoS_2 and 3L-MoS_2 derived from I_{ds}−V_{tg} characteristics. (c) The drain current I_{ds} as a function of bias voltage V_{ds} measured for different top−gate voltages in the case of a device based on single-layer MoS_2. The top-gate voltage varies from −7 to 7 V with a step of 0.5 V. (d) The drain current I_{ds} as a function of bias voltage V_{ds} for the 3L-MoS_2 device, measured for different top−gate voltages. The gate voltage varies from −4 to 4 V with a step of 0.5 V.

$$f_T = \frac{g_m}{2\pi} \times \frac{1}{(C_{gs} + C_{gd})[1 + g_{ds}(R_s + R_d)] + C_{gd}g_m(R_s + R_d)}$$

where g_m is the intrinsic transconductance, C_{gs} is the gate-source capacitance, C_{gd} is the gate-drain capacitance, g_{ds} is the drain conductance, and R_s and R_d are the source and drain series resistances, respectively.

To probe the intrinsic performance of MoS_2 FETs in the RF range of operation, we measure the scattering S-parameters describing our devices using a vector network analyzer and perform standard calibration using dummy OPEN and SHORT structures[33] with the purpose of de-embedding the influence of the parasitic gate capacitance and resistance due to contact pads and device connections. These structures were fabricated with the same layout as the MoS_2 FETs and produced in the same fabrication run on intrinsic Si substrates, Supporting Information Figure S3. The intrinsic cutoff frequency obtained in this way is related to the carrier transit time between the source and drain terminals. We analyzed FETs based on 1L-MoS_2, 2L-MoS_2, and 3L-MoS_2 as well as multilayer MoS_2 stacks with thicknesses of ∼5 nm. All the devices have a 240 nm gate length, total channel length of 340 nm, and a 30 nm thick layer of HfO_2 acting as the gate dielectric.

Figure 3 shows the short-circuit current gain (the ratio of small-signal drain and gate currents) h_{21} as a function of frequency for different thicknesses of exfoliated MoS_2, before and after de-embedding. We operated our devices under bias and gate voltages V_{ds} and V_{tg} where they showed the highest intrinsic transconductance. We attribute the significant noise in the low-frequency characteristics to the large impedance mismatch between our devices and the test setup. The current gain H_{21} decreases with increasing frequency. All our devices showed f_T higher than 1 GHz after de-embedding. For 1L-MoS_2, we obtain a cutoff frequency f_T = 2 GHz for V_{ds} = 2 V and V_{tg} = −3 V. We record the highest cutoff frequency for trilayer MoS_2 with f_T = 6 GHz for V_{ds} = 2.5 V and V_{tg} = −1.5 V. To estimate the value of f_T independently, we also used the Gummel's method[34,35] with results shown on Supporting Information Figure S2. The cutoff frequencies obtained from intercept of the $1/f$ dependence and Gummel's method are closely matched.

Figure 4 represents the behavior of the cutoff frequency as a function of the number of layers of MoS_2 FETs. We see a rise of the cutoff frequency with increasing number of layers from 1L-MoS_2 to 3L-MoS_2, while the 5 nm thick multilayer MoS_2 devices shows no improvement in performance over the trilayer device. Possible reasons for this could include a lower contact resistance in the case of the trilayer device and longer collision-free paths for the trilayer device as indicated by the more

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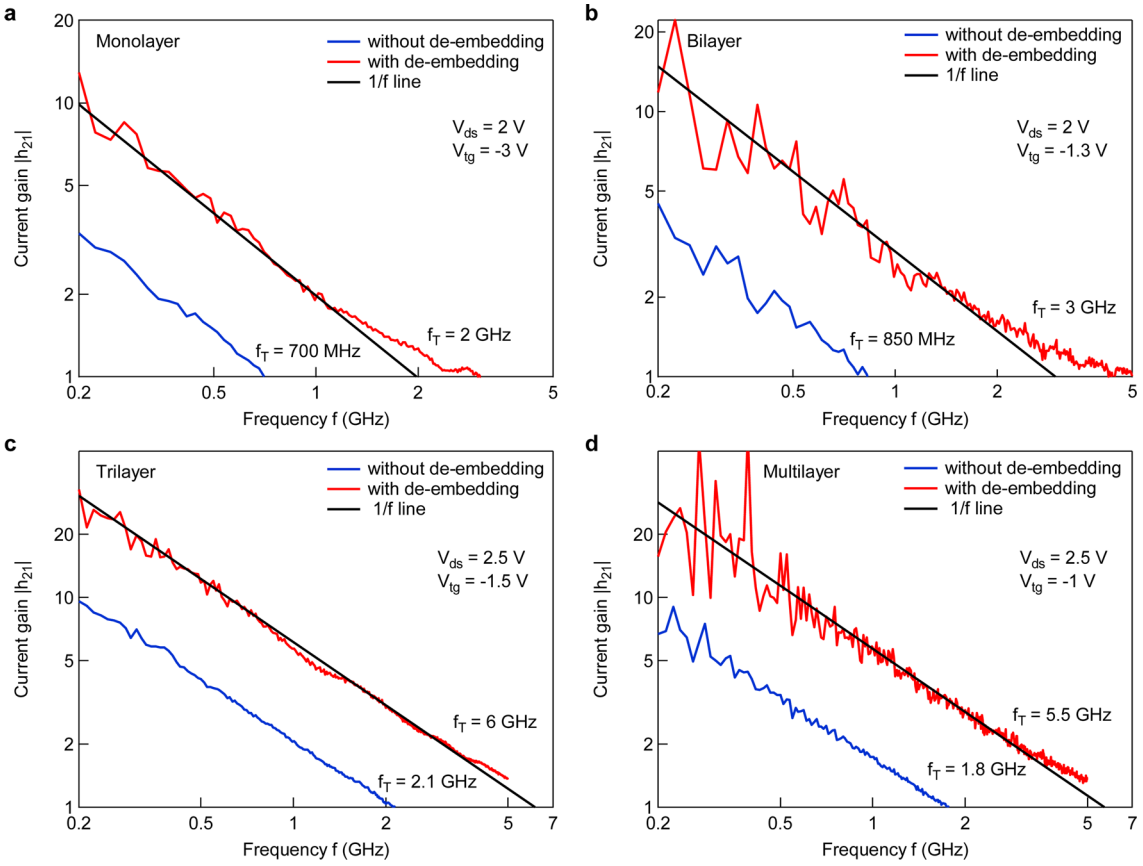

Figure 3. RF performance analysis for devices based on exfoliated MoS_2. Small-signal current gain h_{21} as a function of frequency for devices based on 2D MoS_2 crystals with different thicknesses with and without deembedding. (a) Single-layer MoS_2 with the cutoff frequency f_T = 2 GHz (b), bilayer MoS_2 with f_T = 3 GHz at applied V_{ds} = 2 V and V_{tg} = −1.3 V. (c) Trilayer MoS_2 with f_T = 6 GHz and (d) multilayer MoS_2 with f_T = 5.5 GHz at applied V_{ds} = 2.5 V and V_{tg} = −1 V. The current gain h_{21} decreases with increasing frequency, following the −20 dB/dec slope expected for conventional FETs.

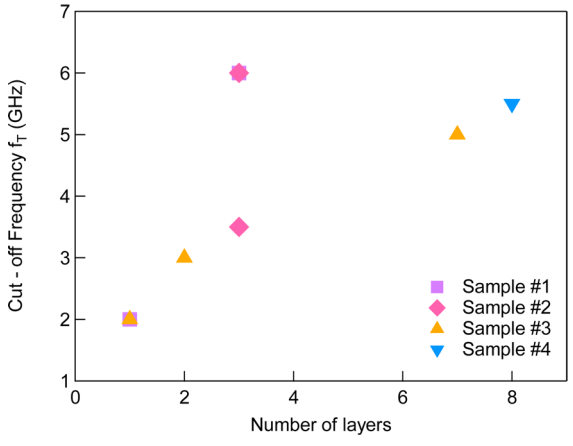

Figure 4. Summary of the RF performance of MoS_2 devices. (a) Intrinsic cutoff frequency f_T as a function of the number of layers of MoS_2 transistors for four different samples with L_g = 200 nm. Highest cutoff frequency is observed for the trilayer transistor.

pronounced saturation behavior in the trilayer device when compared to the monolayer device.

Because the intrinsic cutoff frequency is mostly determined by the minimum time required for charge carriers to travel across the channel, decreasing the length of the semiconducting channel and the gate length are expected to result in increased cutoff frequency of FETs as reported for RF GFET devices.[13,35−37] Because the cutoff frequency f_T is proportional to transconductance g_m, which in turn is proportional to the field-effect mobility μ_{FE}, improving the mobility of the material by removing the adsorbates,[38] removing intrinsic defects and reducing the temperature should result in further improvements to the cutoff frequency.

In addition to current gain, transistors for high-frequency logic circuits and amplifiers should also show voltage and power gains characterized by the maximum frequency of oscillation f_{max}. This is the frequency at which the power gain is equal to 1. Just as f_T, f_{max} can be expressed by following the equation for field-effect transistors[39]

$$f_{max} = \frac{f_T}{2\sqrt{g_{ds}(R_g + R_S) + 2\pi f_T C_g R_g}}$$

where g_{ds} is the drain differential conductance, R_s is the source resistance, C_{gd} is the gate to drain capacitance, and R_g is the gate resistance, which mainly depends on the gate thickness and area.

In Figure 5, we plot Mason's unilateral power gain U as a function of frequency for two MoS_2 devices. This figure of merit is useful for describing the quality of three-terminal devices and is the highest possible gain obtained by unilateralizing the two-port network with lossless feedback. For active devices, the quantity U is higher than 1 and f_{max} corresponds to the frequency at which U = 1 (U = 0 dB). As

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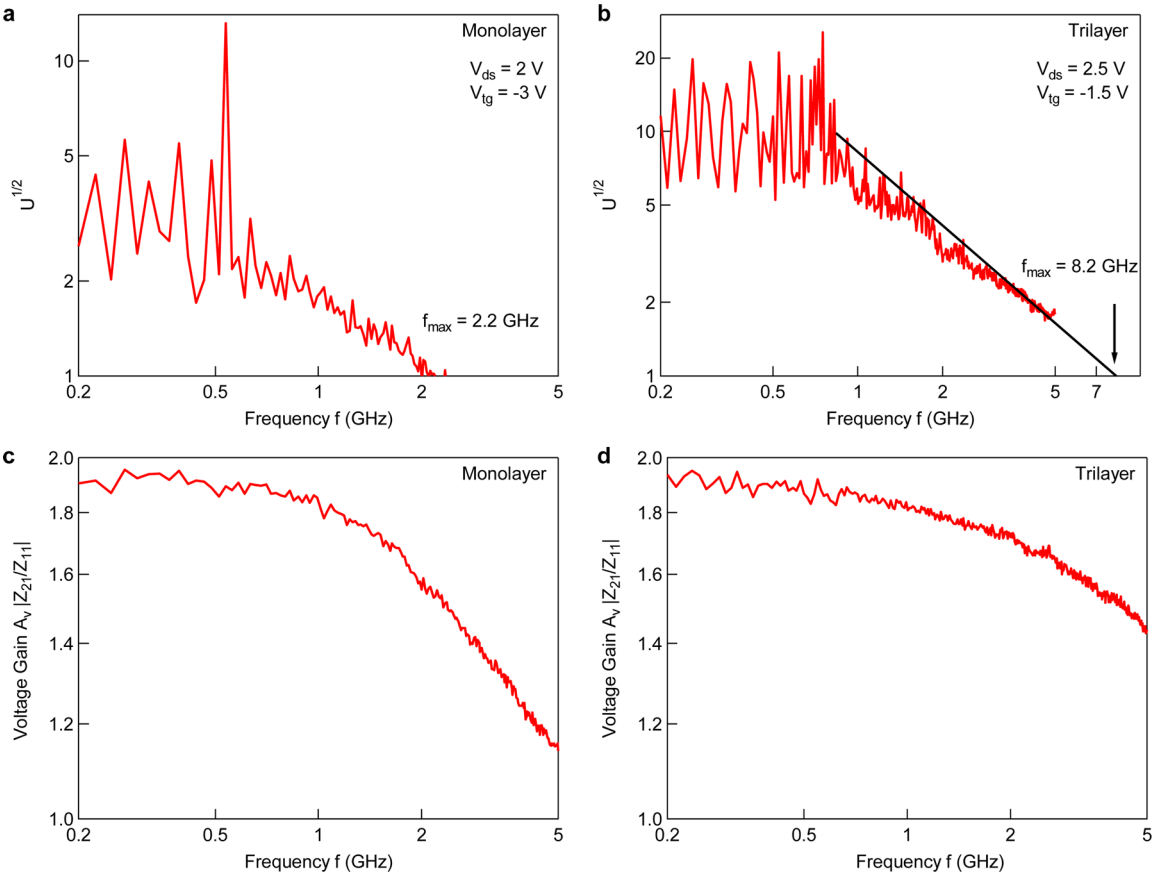

Figure 5. Power and voltage gain analysis for devices based on exfoliated MoS_2. (a) Mason's unilateral gain U as a function of frequency for the monolayer MoS_2 device. Maximum frequency of oscillation f_{max} = 2.2 GHz is extracted at the point where power gain reaches unity. (b) Same as in part a but for a trilayer device, resulting in f_{max} = 8.2 GHz. (c) Voltage gain $|Z_{21}/Z_{11}|$ as a function of frequency for the monolayer MoS_2 device showing gain higher than 1 up to 5 GHz. (d) Dependence of the voltage gain on frequency for the trilayer device.

shown in Figure 5a, we obtain f_{max} = 2.2 GHz for single-layer MoS_2 with 240 nm gate length. For trilayer MoS_2, we obtained f_{max} = 8.2 GHz, Figure 5b, similar to high-end RF FETs based on epitaxial graphene.[15] This result shows that MoS_2 could be interesting for high-frequency amplifiers. We also extract the intrinsic voltage gain $A_v = g_m/g_{ds}$ for the same set of devices by converting the scattering S-parameters to impedance Z-parameters where $A_v = Z_{21}/Z_{11}$.[39] The results are presented in Figure 5c,d for our MoS_2 FETs. At 200 MHz, A_v is equal to 1.9 (5.5 dB) and is twice as high as in state-of-the-art RF-GFETs with equivalent gate oxide thickness and similar gate lengths.[37] Further device scaling is expected to improve all the operating parameters described here. Improvements in the voltage gain can be expected from decreasing the oxide thickness, resulting in better electrostatic control over the semiconducting channel. Reducing the gate length and improving the semiconducting channel mobility is expected to result in increased cutoff frequency f_T, while the maximum frequency of oscillation f_{max} can be increased by reducing the parasitic effects due to the layout, capacitance, gate, and contact resistance.

In conclusion, we have characterized the high-frequency operation of top-gated MoS_2 transistors with a 240 nm gate length. Our MoS_2 RF-FETs show an intrinsic transconductance higher than 50 μS/μm, saturation of drain-source current, and a voltage gain higher than 1. These features allow the operation of MoS_2 transistors in the gigahertz range of frequencies. Our devices show cutoff frequencies as high as 6 GHz and are able to not only amplify current in this frequency range but also power and voltage with the maximum frequency of oscillation f_{max} = 8.2 GHz. These features show that MoS_2 and other 2D TMD semiconductors can be used to fabricate transistors that operate at gigahertz frequencies. Further improvements in device geometry and material processing are possible and will help realize the full potential of 2D semiconductors for low-cost and flexible high-frequency analog current and voltage amplifiers as well as high-frequency logic circuits.

Materials and Methods. Device characterization is performed at room temperature in an RF probe station (Cascade Microtech). Direct current (dc) and alternating current (ac) voltages are applied using bias tees connected to each probe head. The dc currents are measured using an Agilent B2912A parameter analyzer. The ac excitations and subsequent S-parameter measurements are performed using an Agilent N5224A vector-network analyzer (VNA). High-frequency S-parameter characterization was carried out in the 0.2−5 GHz frequency range. The two VNA ports are connected to the sample's source and drain electrode via the bias-tees and probe heads. The probe system was calibrated before the measurements of the device under test (DUT) in order to take into account any spurious contribution of connectors, cables, and the electrical environment of the DUT and to subtract it from the measured signal. This is done first by means of a calibration pad and in the second step using a set of dummy structures. The system was calibrated using the line−reflect−reflect−match method for the required frequency range

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and at low input power (typically −27 dBm) using a standard CSR-8 substrate. On-chip OPEN and SHORT structures with exact design layout of the devices were used to de-embed the parasitic effects such as pad capacitance and interconnection resistance with the purpose to obtain the intrinsic RF performance. OPEN dummy structures are used to cancel the influence of the capacitive coupling between the electrodes. SHORT dummy structures are used to cancel the series resistance from the leads and contact resistance between probe tips and landing pads.

■ ASSOCIATED CONTENT

Supporting Information

Supplementary figures and discussion related to device fabrication, field-effect mobility and contact resistance extraction, cutoff frequency extraction using the Gummel's method, and layout of structures used for parameter de-embedding. This material is available free of charge via the Internet at http://pubs.acs.org.

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Notes

The authors declare no competing financial interest.

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Supplementary Information

for

MoS_2 Transistors Operating at Gigahertz Frequencies

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1. Device fabrication

Top-gated MoS_2 transistors were fabricated starting with the adhesive-tape based micromechanical cleavage of commercially available, naturally occurring crystals of molybdenite using the method previously developed for graphene fabrication.[1] The adhesive tape with ultrathin crystals is pressed against the surface of a substrate composed of intrinsic Si with 270 nm of SiO_2. The substrate is imaged using an optical microscope (Olympus BX51M) equipped with a color camera. We have previously established the correlation between the optical contrast and thickness as measured by AFM for a number of dichalcogenide materials, including MoS_2.[2] We investigate the RF operation of MoS_2 in the GHz range for different thicknesses of the material.

2. Field-effect effective mobility and contact resistance

The particular contact geometry dictated by the need to interface RF transistors with the network analyzer and RF probes prohibits the fabrication of four or six contact devices, necessary to accurately measure the contact resistance and field-effect mobility in our devices. The presence of an underlap region is also expected to result in a relatively high value of the contact resistance which would dramatically underestimate the mobility extracted using the conventional two-contact field-effect mobility expression.

We can however, give an estimate of these quantities, based on a simple model where the source-drain current I_{ds} in a field-effect transistor is given by the following expression:

$$I_{ds} = \mu_{FE} C_{ox} \frac{W}{L_g} \left(V_{tg} - V_T\right)\left(V_{ds} - 2I_{ds}R_c\right) \quad (1)$$

Where of μ_{FE} is the field-effect effective mobility, C_{ox} the gate capacitance, W the channel width, L_g the gate length, V_{tg} the top-gate voltage and V_T the threshold voltage. V_{ds} is the drain-source bias voltage while $-2I_{ds}R_c$ is its reduction due to voltage drop on the contact resistance R_c. In this picture, the contact resistance corresponds to the in-series resistance of a single metal/MoS_2 junction and the ungated region of the MoS_2

channel next to it. Because of the absence of a back-gate, we can neglect the variation of R_c with the gate voltage. We also neglect the variation of μ_{FE} with the gate voltage.

We can rewrite equation (1) as:

$$I_{ds} = \frac{V_{ds}}{\frac{L_g}{\mu_{FE} C_{ox} W \left(V_{tg} - V_T\right)} + 2R_c} \tag{2}$$

and fit the I_{ds} - V_{tg} curves as shown on Figure S1. We restrict the fit to regions of V_{tg} where the curve shows a substantial deviation from a linear behavior, indicating a significant influence of the contact resistance. Previous measurements have shown that at these doping levels, the mobility of MoS_2 is not dependent on charge density.[3]

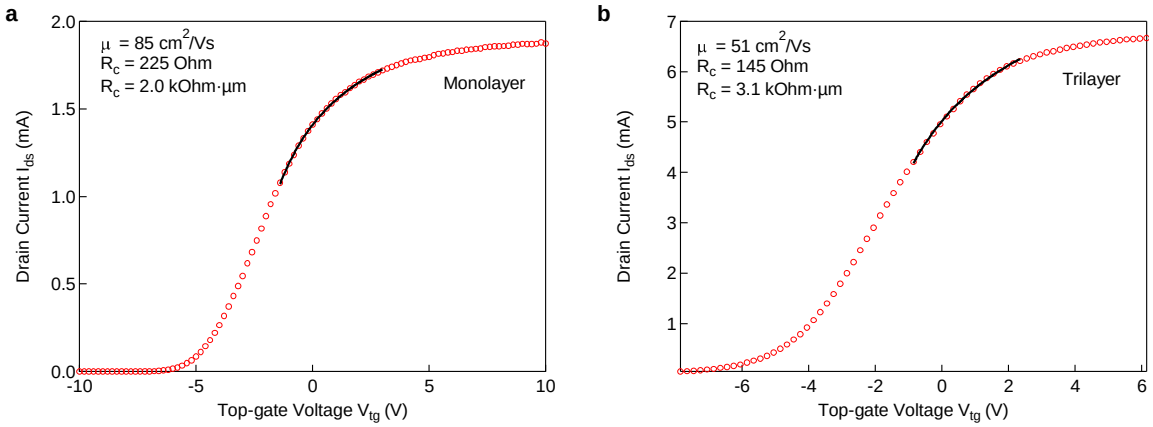

Fig. S1. Mobility and contact resistance extraction from the transfer characteristics of (a) monolayer and (b) trilayer MoS_2 field-effect transistors. For both cases, V_{ds} = 0.1V, κ = 14, dielectric thickness is 30 nm and channel length L_g = 240 nm. Channel width is W = 9 μm for the monolayer and W = 21.5 μm for the trilayer device.

Using this model, we extract estimates for the field effect mobility and contact resistance μ_{FE} = 85 cm^2/Vs and R_c = 2.0 kΩ·μm for the case of the monolayer device and μ_{FE} = 51 cm^2/Vs and R_c = 3.1 kΩ·μm for the trilayer device.

3. Cut-off frequency extraction using the Gummel's method

Gummel's method of extracting the cut-off frequency f_T offers a very useful verification of f_T values since it relies on lower frequency measurements.[4] The method is based on the common-emitter current gain transfer function and the quasi-static definition for f_T:

$$h_{21}(f) = \frac{h_{21}(f=0)}{1 + j h_{21}(f=0)\frac{f}{f_T}} \tag{3}$$

Together with the realization that the best line-fit through $Im[1/h_{21}(f)]$ for low values of f yields a slope equal to $1/f_T$. Figure S2 shows the results for our devices, resulting in f_T values in agreement with those presented in the main manuscript.

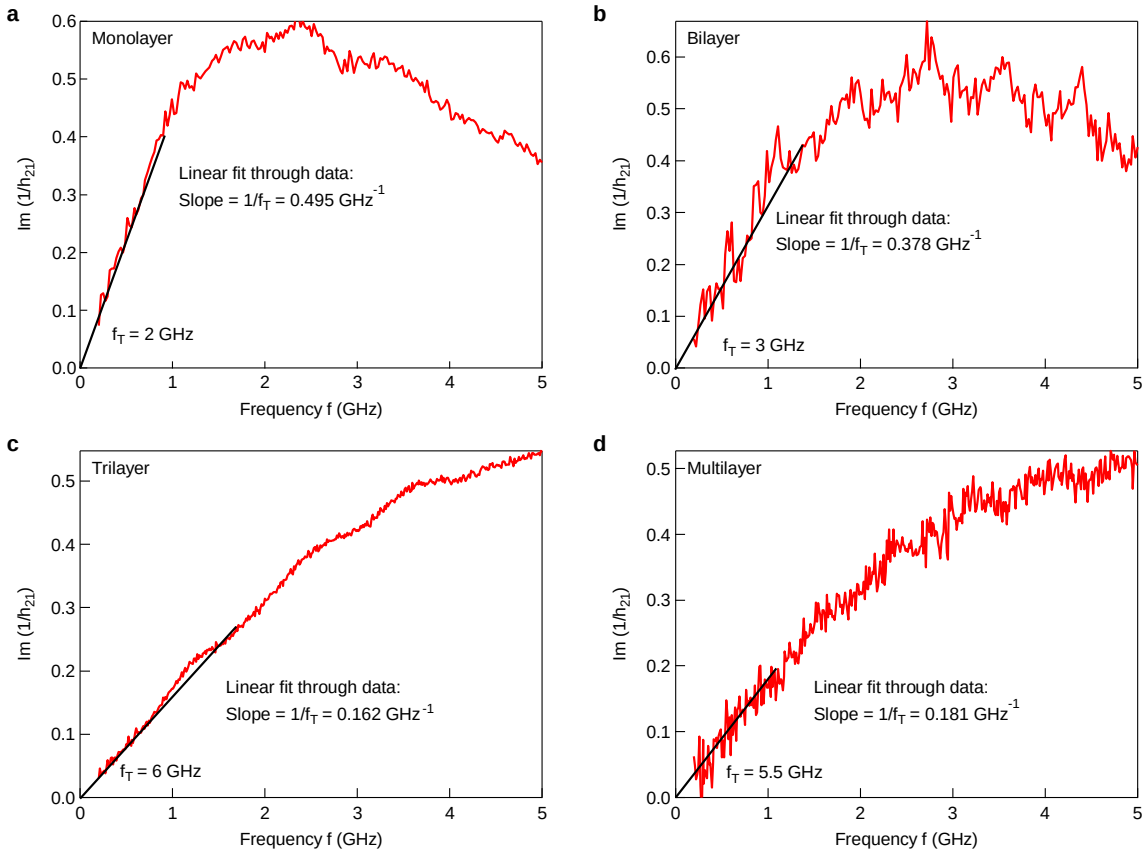

Fig. S2. Gummel's method. (a) The cut-off frequency for the monolayer MoS_2 FET extracted using the Gummel's method is 2 GHz. (b) Gummel's method results in f_T = 3GHz for the bilayer device. (c) The cut-off frequency for trilayer MoS_2 FET obtained using the Gummel's method is 6 GHz. (d) The cut-off frequency for multilayer MoS_2 FET extracted with Gummel's method is 5.5 GHz.

4. Structures used for parameter de-embedding

In our work, we performed an OPEN/SHORT de-embedding procedure to remove the influence of gate capacitance and resistance due to contact pads and device connections. Figure S3 presents the OPEN and SHORT structures used for de-embedding. They were fabricated together with the device under test (DUT) with the same geometry.

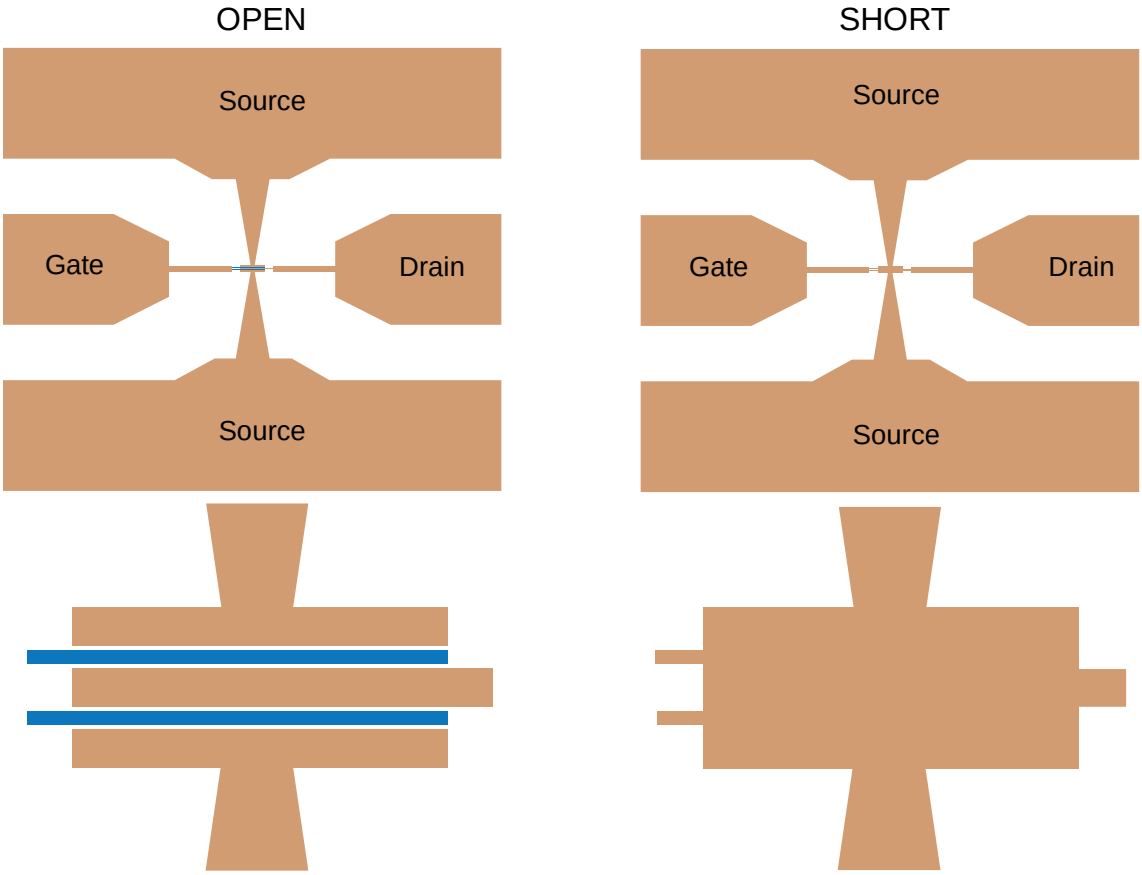

Fig. S3. Schematic images of OPEN and SHORT structures used for the de-embedding procedure. Lower panels: magnified view of the middle portion of the device. The de-embedding procedure subtracts the effect of the pads and reveals the intrinsic behavior of the device in the active area.

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