3D Integrated Architectures for Microelectronic Two-Phase Flow Cooling Applications

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And about my newborn daughter Lara, what can I say... Lara I love you, and I hope someday you might flip through these pages to see what your old man was up to when he was young.

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Abstract

Higher computational performance demands microchips with more and more cores and cache memory that communicate via long wires, consuming a lot of energy and generating a lot of heat. As a solution, three-dimensional (3D) stacking of integrated-circuit (IC) dies by vertical integration increases system density and package functionality. Area-array Through-Silicon-Vias (TSVs) reduce global interconnects lengths and signal delay times, resulting in a better performance and reduced energy consumption. Ongoing miniaturization of ICs increases chip-level power densities and together with vertical integration renders cooling a major challenge. Thus, the development of new chip cooling concepts is very important and therefore scalable interlayer cooling solutions for chip stacks need to be investigated. This thesis aims to show the feasibility of such a prototype for two-phase flow cooling applications. It starts by presenting a new concept for the integration of intra chip stack fluidic cooling structures, using a newly developed patterned thin-layer eutectic solder bonding technique for the stack assembly which is compatible with the fabrication constraints caused by the implementation of interlayer cooling. 5-layer chip stacks with embedded microchannels and high aspect ratio TSVs were successfully fabricated. Optical inspections demonstrated the proper bond line formation and electrical tests indicated the successful combination of TSVs with thin-layer solder interconnects. Mechanical shear tests showed the strength of the patterned thin-layer solder bond and an added solder ring-pad component to seal the electrically active pad from any conductive liquid coolant was experimentally implemented, resulting in strict design rules to avoid solder reflow instabilities. Secondly, this thesis proposes an innovative approach for electrical chip to substrate and chip to chip interconnects using solder balls and rails on a single chip for higher solder area fill factor that supports power delivery and heat removal for high-performance flip-chip-on-board as well as 3D stack applications. After establishing design and fabrication rules for these novel structures to avoid solder reflow instabilities, numerical results were obtained via surface energy minimization to predict solder shape after reflow with a deviation of less than 9%.

To optimize heat spreading and fluid flow using interlayer two-phase evaporative cooling within a multi-microchannel evaporator chip stack, a new thermal model and simulation method are presented to enable the study of ideal local heat load placement. The design used to test the model mimicked the actually built 3D chip stacks. This new model simultaneously solves heat and two-phase flow spreading effects, the latter due to the pressure drop's sensitivity to heat flux/vapor quality. Several heat load patterns were implemented and compared. Simulation results showed a strong effect of thermal spreading between the dies, since these have a small thermal resistance compared to the convective heat transfer coefficient in the channels, which is effective in flattening thermal gradients from non-uniform heating within the chip stack.

Flow boiling of refrigerants 236fa and 1234ze (R236fa & R1234ze) were experimentally investigated within two different test sections. First-of-a-kind high pressure fluidic tests were successfully achieved within a 3D chip stack with interlayer cooling capabilities and high aspect ratio TSVs. However, fabrication defects and a scarce amount of TSV wafers rendered the heat transfer study within the chip stack impossible. Finally, pressure drop measurements and local junction temperatures were measured on a 2D silicon pin fin test section as a potential candidate for future 3D modules. A good cooling performance was demonstrated, with a junction temperature response of 40°C for a base heat flux of 66.6 W/cm^2. The observed high pressure drops were a result of the very small flow cross-sectional area.

Keywords

Electronic packaging, thermal management, 3D integration, chip stacking, solder bonding, microscale flow boiling, refrigerants.

Résumé

L’empilement tri-dimensionnel de circuits intégrés de manière verticale permet d’augmenter la densité d’un système ainsi que la fonctionalité d’un paquet électronique. L’intégration verticale de puces à l’aide de Voies Traversant le Silicium (VTS) réduit la longueur des connections globales et par conséquent le délai du signal. D’un autre côté, la miniaturisation continue des puces a pour conséquence l’augmentation croissante de leur densité de puissance. Le développement de nouvelles techniques de refroidissement devient ainis crucial. Par conséquent, des techniques à échelle modifiable comme le refroidissement inter-couches doivent être étudiées. Cette thèse présente un nouveau concept pour l’intégration de refroidissement fluidique à l’intérieur même d’un empilement tri-dimensionnel de puces par l’intermédiaire de microcanaux usinés directement à l’arrière des puces, pour le management thermique à travers écoulements mono- ou biphasiques, en utilisant une technique de fine micro-soudure pour l’assemblage vertical des puces. Les résultats ont montré la fabrication fructueuse d’un empilement à 5 couches avec microcanaux fluidiques intégrés et VTS à rapport hauteur/largeur élevé. Des inspections optiques ont demontré la bonne formation du lien de soudure entre les puces et des analyses électriques ont indiqué la combinaison fructueuse de VTS avec la technique de fine micro-soudure. Des tests de cisaillement méchaniques ont aussi démontré la force et durabilité de la fine couche de micro-soudure (16MPa). De plus, le design d’un anneau de soudure additionnel a été recherché dans le but d’isoler le plot de soudure principal, actif électriquement, d’un potentiel liquide de refroidissement conducteur. Des tests de refusion sur ces anneaux ont montré l’apparition d’accumulations locales de soudure. Il a été découvert que ces accumulations disparaissaient quand le rapport hauteur/ largeur de l’anneau (hauteur de la quantité de soudure déposée/ largeur de l’anneau) était maintenu en-dessous de 0.65, valeur critique observée expérimentalement. Additionnellement, cette thèse propose une approche innovative pour l’interconnection électrique entre 2 puces de silicium ainsi qu’entre une puce de silicium et un substrat en polymer. La potentielle co-existence de boules ainsi que de rails de soudure sur une seule et même puce, permettant la livraison de puissance et évacuation de chaleur pour paquets électroniques de haute performance à travers un taux de remplissage surfacique de soudure plus élevé, est discutée dans le travail qui suit. Après refusion, les géométries en rails peuvent parfois résulter d’une largeur maximale bien supérieure à leurs plots de soudure de base respectifs. De plus, il a été observé qu’un design imparfait du rail pouvait engendrer deux types d’instabilités : formation locale d’une boule de soudure et accumulation asymétrique de soudure le long du rail. Les expériences de refusion sur ces nouvelles géométries ont été complétées par des résultats numériques obtenus via une technique de minimisation de surface d’énergie. Une qualité de prédiction avec déviations inférieures à 9% a été identifiée, indicant ainsi l'applicabilité de cette technique au design de futures geométries de soudure. Au final, les résistances thermiques d'interfaces boules et rails ont été mesurées et comparées et il s'est avéré que l'interface rail, avec un taux de remplissage surfacique de soudure de 57%, possède une résistance thermique d'interface 7 fois plus petite.

Cette thèse introduit aussi un nouveau modèle thermique et une méthode de simulation permettant l'étude en profondeur du placement idéal de charges calorifiques à l'intérieur d'un module à puces empilées avec système de refroidissement intégré (microcanaux), afin d'optimiser la diffusion de chaleur et le passage du fluide tout en utilisant une technique de refroidissement biphasique par évaporation, à l'intérieur d'un design identique à celui de l'empilement de puces fabriqué et mentionné plus haut. Ce nouveau modèle inclus la résolution simultanée de la diffusion calorifique et fluidique, cette dernière étant due à la sensibilité de la perte de charge au flux de chaleur ainsi qu'au titre. Plusieurs dispositions de charges calorifiques ont été ainsi implementées et comparées. Les résultats de simulation ont montré un effet non négligeable de la diffusion thermique entre les puces empilées, étant donné que celles-ci sont dotées d'une petite résistance thermique comparé au coefficient de transfert de chaleur par convection aux microcanaux, ce qui aide à atténuer une potentielle disposition non uniforme de charges calorifiques à l'intérieur du module 3D.

Finalement, des études expérimentales ont été conduites sur l'évaporation des réfrigérants 236fa et 1234ze (R236fa & R1234ze) à l'intérieur de deux sections de test différentes, respectivement un module tri-dimensionnel de puces et une puce en silicium avec micro-structures intégrées. Des mesures de pertes de charge et de coefficients de transfert de chaleur ont été effectuées dans le but d'améliorer le design de ces micro-échangeurs de chaleur et de faciliter leurs implémentations respectives pour les futures modules tri-dimensionnels de puces commercialisés.

Mots-clés

Packaging électronique, management thermique, intégration 3D, empilement de puces, micro-soudure, évaporation de flux à échelle microscopique, réfrigérants.

Contents

Yassir MADHOUR .... **iii**

Acknowledgements .... **iii**

Abstract .... **vii**

Keywords .... **viii**

Résumé .... **ix**

Mots-clés .... **x**

List of Figures .... **xv**

List of Tables .... **xxiii**

Chapter 1 Of the importance of vertical integration and thermal management for processor and memory chips in the semiconductor industry **1**

1.1 Vertical integration 1

1.1.1 Motivation and importance [1] 1

1.1.2 Enabling technologies 3

1.2 Thermal management of ICs 4

1.2.1 Importance, past and current concepts: from air to liquid cooling [16] [17] 4

1.2.2 Microscale flow boiling of refrigerants 6

1.2.3 Chip stacks and thermal management limitations 9

1.2.4 Interlayer cooling: a scalable solution 9

1.3 Thesis outline and objectives of this work 11

Chapter 2 Patterned solder bonding for die-to-die attachment: novel structures **13**

2.1 Introduction: inter-tier thermal management 13

2.2 Electrodeposition and reflow of thin eutectic 3.5Ag96.5Sn 14

2.2.1 Thin film micro C4s 14

2.2.2 Rails 19

2.2.3 Sealing rings..19

2.3 Investigation of high fill factor solder patterns for power delivery and heat removal support 21

2.3.1 Motivation and implementation 21

2.3.2 Surface minimization method 23

2.3.3 Solder shape: engineering the dimensions 24

2.3.4 Modeling vs. experiments 26

2.4 Experimental campaign: flip-chip bonding of eutectic 3.5Ag96.5Sn 33

2.4.1 Thin film micro C4s for 3D chip stacking 33

2.4.2 Thermal resistance of high fill factor structures 43

2.5 Conclusions 46

Chapter 3 Intra chip stack dielectric evaporative flow 49

3.1 Experimental investigation: 2D silicon pin fin test vehicle 49

3.1.1 Nomenclature..49

3.1.2 Introduction..50

3.1.3 Test section 51

3.1.4 Test facility 54

3.1.5 Operating conditions..56

3.1.6 Data reduction..57

3.1.7 Results and discussion..59

3.2 Experimental investigation – 3D test vehicle 62

3.2.1 Introduction & purpose..62

3.2.2 Design, fabrication & assembly..63

3.2.3 Test facility 68

3.2.4 Operating conditions..68

3.2.5 Pressure drop results and discussion..69

3.3 Conclusions 71

Chapter 4 Modeling of three-dimensional multi-cavity dielectric evaporative heat transfer.. 73

4.1 Nomenclature 73

4.2 Design framework: CMOSAIC chip stack package 74
4.3 Method of simulation 74
4.4 Simulation cases 78
4.5 Results 80
4.6 Conclusions 90

Chapter 5 Conclusions and outlook

Chapter 5 Conclusions and outlook 93
5.1 Thesis contributions and impact 93
5.1.1 Solder bonding technology – novel structures 93
5.1.2 3D integrated chip stack with embedded cooling structures - fabrication, assembly and fluidic testing 94
5.1.3 Modeling of three-dimensional heat and mass transfer in multi-cavity systems 95
5.2 Looking into the Future 95
Appendix A 97
Appendix B 103
References 107
List of scientific publications 117
Curriculum Vitae 119

List of Figures

Figure 1.1 Shrinking transistor dimensions [4]..2

Figure 1.2 Gate delay versus interconnect delay for shrinking technology nodes [5]. 2

Figure 1.3 Left: SoC with multiple processor cores and cache memories. Right: Corresponding 3D stacked IC with considerably smaller area and shorter vertical interconnects [6]. 3

Figure 1.4 Module and chip heat flux densities for IBM chips, from the 1950s until early 2000s [22]. According to IBM Zürich Research, module heat fluxes between 0 and 14 W/cm^2 roughly correspond to chip heat fluxes between 0 and 80 W/cm^2, knowing that these chips occupy around 7/38th of the module area. 5

Figure 1.5 General size comparison between air-cooled heat sinks and single- or two-phase cooled heat sinks (Source: IBM Research, Zürich). 6

Figure 1.6 Chip stack configuration with acceptable, close to the limit and unacceptable junction temperatures with backside water heat removal. Maximum allowable MPU junction temperature is 80°C, acceptable memory temperature limit is 95°C, and fluid inlet temperature is 20°C [50]..10

Figure 2.1 Patterned thin film solder bond concept for mechanical and electrical connection in 3D chip stacks with integrated cooling capabilities. The highlighted part shows the needed patterned thin film solder interconnect. 14

Figure 2.2 Additional solder structures needed for a scalable cooling solution (top view on single die, blue is solder). A) Silicon-etched microchannels as heat removal structures. B) Silicon pin fins as heat removal structures. 14

Figure 2.3 Scanning Electron Microscopy (SEM) real-life images corresponding to the solder concepts presented in Figure 2.2. A & B) With silicon chip-embedded microchannels. C & D) With silicon chip-embedded pin fins...15

Figure 2.4 Silver Tin alloy phase diagram [58]..15

Figure 2.5 Thin film solder fabrication process. 16

Figure 2.6 *Left:* plated (8µm-thick) AgSn solder thin film pad (50µm diameter). *Middle and bottom:* after fluxless reflow at 265°C, with tin oxide layer on the surface. 17

Figure 2.7 FIB cross-section of fluxless reflowed solder bump. *Left:* top view of solder pad with oxide layer. *Right:* corresponding cross-section. ..17

Figure 2.8 Tin (Sn3d) XPS measurements for plated die (after deposition, blue), reflowed die without flux (ambient atmosphere, red) and reflowed die with flux treatment (green). 18

Figure 2.9 a) Flux-reflowed solder pads, 58µm in diameter and 12µm thick. b) FIB cross-section of a reflowed solder bump. 18

Figure 2.10 Solder fluidic sealing concept. a) Design and geometry. b) Range of studied combinations of parameters and their different designations....................19

Figure 2.11 a) Solder ring pads after electroplating. b) Ring pad structures 3A to 3D after reflow on hot plate and cleaning. 20

Figure 2.12 Experimental categorization of ring pad solder shapes after reflow for varying deposition heights H_0 and ring aspect ratios (deposition height H_0 to ring width W_r). Dome- (squares) and ball- (circles) like shapes were identified below and above the critical aspect ratio of 0.65. Inserts depict SEM photographs....................21

Figure 2.13 Isometric view of distinct solder shapes after reflow resulting from circular and rectangular pads as predicted by numerical modeling (see § 2.3.2). The initial height of 80 µm corresponds to the solder height after electrodeposition. The AxB metric indicates the size of the pad in unit cells with a pitch of 151 µm in X and Y direction. The width or diameter of the pads is 80 µm. 23

Figure 2.14 (a) Initial volume defined in the Surface Evolver, representing the solder after electroplating. (b) Geometry with minimal surface for a constant volume and constrained bottom surface, considering surface tension only. 24

Figure 2.15 Top view of solder arrays with Rail1 unit cells (Figure 2.13) in aligned (a) and staggered (b) arrangement. The minimal distance between rails is 3 times larger in case of (b) with an accordingly reduced shorting risk. 25

Figure 2.16 Bottom (left) and side (right) view of Bone Rails at varying bone width w_i. The height difference ΔH with respect to a Ball is depicted. The Ball height is smaller in case (a) and (b), but equal for (c). A topology change of the Bone Rail with two maxima can be observed for case (d)..26

Figure 2.17 Top view of pad and solder geometry for different solder shapes: Ball, Rail1, and Rail2. The patterns were arranged across their respective chips in arrays with a pitch of 151 µm (Ball, Rail1) and 302 µm (Rail2)...27

Figure 2.18 Top, side and front view SEM photographs of Rail1 structure after reflow, with their corresponding Surface Evolver model view. 28

Figure 2.19 SEM photograph of solder reflow shapes of 2 mm long rails with indicated varying widths in [µm], but equal initial solder height of 85 µm. Local solder accumulation, called "Balling", occurs for lines below a critical line width of 100 µm. Dome-shaped geometries result for wider rails. 29

Figure 2.20 Experimental (full) and numerical (empty) categorization of solder shapes after reflow for varying deposition heights H0 and rail aspect ratios (AR) (deposition height H0 to rail width wo). Dome- (green squares) and ball- (red circles) like shapes were identified below and above the critical aspect ratio of 0.6. Inserts depict SEM photographs and Surface Evolver results. 30

Figure 2.21 Isometric (a) and side-view (b) SEM photographs depicting Asymmetric Solder Accumulation from Bone Rail pads after reflow in comparison with numerical, symmetric results presented in Figure 2.16...31

Figure 2.22 (a) Asymmetric Bow Tie rail with an offset Δ of 10 µm of the lower right corner. (b) Modeling result depicting Asymmetric Solder Accumulation as observed in the experiment (Fig. 9) for the pad geometry shown in (a)..31

Figure 2.23 Bow Tie Phase diagram depicting three reflow phases in the width ratio to offset plane. The red points and their interpolation (dashed line) were derived numerically and indicate the phase transition. Geometrical representations of the phases are shown as isometric inserts. The pad geometry variation along the different dimensions is depicted as well (Bow Tie dimensions [µm]: L_L: 382, L_S: 171, w_o: 150, H_0: 60)...32

Figure 2.24 Test vehicle description–chip stack package with silicon embedded heat transfer structures. a) Ensemble view of package with all components. b) Vertical cross-section describing the multiple layers and their respective thicknesses. 33

Figure 2.25 Process integration flow for the fabrication of a middle die within the chip stack (LV2 to LV4, see Fig. 1b), after TSV implementation. 34

Figure 2.26 a) Illustration of the TSV process flow. b) Illustration of the two-step TSV electroplating process with a cross-section of the reults......35

Figure 2.27 Histogram of the calculated TSV resistance. Most of the TSVs have a value below 2Ω. 36

Figure 2.28 Flip chip bonding (force-controlled reflow) process used for die-to-die bonding and chip stacking. In blue: force control. In red: temperature control for both chip and carrier side...................................37

Figure 2.29 a) Isometric view of a 5-layer chip stack (4 fluid cavities, 4 active layers with TSVs). b) Front view of 100X100µm fluidic microchannels. c) Zoom-in on cavities, fin thickness is 100µm. d) View of the die-to-die thin-layer eutectic solder bond (5µm), the silicon fin as well as the fluidic microchannel. 38

Figure 2.30 a) Cross-section of the assembled chip stack. The LV1 to LV5 chips, the microchannels, the TSVs as well as the thin-layer solder bonds are all visible. b) Zoom-in on microchannels, TSVs and solder pads. 39

Figure 2.31 X-ray tomography pictures on a fabricated chip stack. A) 2D top view of LV2 chip surface, showing uniform presence of solder interconnects. Highlighted “missing spots” are the locations of the hot spot heaters’ electrical leads (design presented in § 3.2). B) 3D top view of chip stack showing the properly filled TSVs. Due to (already impressive) 8µm resolution, thin film solder interconnects are not visible. **The author would like to thank Prof. Dr. Bernhard Wunderle (TU Chemnitz, Germany) as well as Marcus Hildebrandt (Fraunhofer ENAS, Germany) for their tremendous help in obtaining these photographs.**....39

Figure 2.32 a) Schematic of the 4-point DC Kelvin measurement for a single TSV plus thin-layer solder pad combination. b) DC current sweep (-1 [mA] to 1 [mA]) with corresponding voltage response to determine the resistance of a single TSV plus thin-layer solder pad combination. A and B as well as C and D designate similar daisy-chain locations measured on different samples and are representative values. 40

Figure 2.33 Setup to shear test the thin-layer solder bonds. 41

Figure 2.34 a) Shear principle. b) Sheared state. c) Corresponding photo. .41

Figure 2.35 Shear test results..42

Figure 2.36 Failure modes observed across the sheared carrier and chip (left to right). a) Ductile through solder (carrier side). b) Partial solder lift (carrier side). c) Ductile through solder (chip side). d) Partial solder lift (chip side). All pad diameters are equal to 58µm. The schematics (e) and (f) describe the failure mode principle for each, ductile and partial solder lift. 42

Figure 2.37 EDX results of the different regions left behind after shearing: the partial solder lift (a) shows a clean separation between the solder components and the pad UBM metallization. 43

Figure 2.38 Front view SEM micrograph of a flip-chip bonded device using Rail1 structures. 43

Figure 2.39 Illustration of the bulk thermal tester. Heat is dissipated uniformly from the top copper stud into the specimen and finally out of the bottom copper stud. Thermal coupling from copper into the specimen is performed by a liquid metal interface. Temperature gradients are monitored with two pairs of four thermocouples to derive the copper stud surface temperature and the dissipated heat flux. The liquid metal interface resistance was determined in an upfront measurement. 45

Figure 2.40 Resulting bond-line effective thermal conductivity k_{eff} of the Ball, Rail1 and Rail2 specimens at their solder area fill factor. Three different specimens were characterized and compared in case of the rail shapes. The trend of the measured results is compared with theoretical values derived from effective solder thermal conductivities, published in [71], and the solder area fill factors. 46

Figure 3.1 A) Complete 3D CAD drawing of test package with metrology. B) Test package cross section. C) Flipped view of test chip showing the glass die as well as the fluid inlet and outlet slits. 51

Figure 3.2 A) Test chip cross section. B) Fabrication process flow. 52

Figure 3.3 A) Top view of NiCr background heater with indicated feeding pads and flow direction. B) Top view of RTD inside outlet plenum. 53

Figure 3.4 A) Schematic of silicon pin fins test chip, top view. B) SEM image of Silicon pin fins. C) Top view microscope image of test chip, showing a potential flow deviation due to staggered position of pins, as seen in [82]. 53

Figure 3.5 Top view of PC manifold, showing the flow path from inlet to outlet as well as the available metrology. 54

Figure 3.6 Complete test section attached to the experimental facility, showing the inlet and outlet thermocouples, the pressure ports, the direction of the flow as well as the background heater and its external electrical connections. 54

Figure 3.7 Flow boiling test facility. 55

Figure 3.8 A) Left: Test facility's power supply and data acquisition system. Right: complete test facility. B) Test section and IR camera setting. 56

Figure 3.9 Pressure drop components evolution for increasing base heat fluxes at a mass flow rate of 11.5kg/hr for R1234ze. 60

Figure 3.10 Total pressure drop relative contributions for increasing base heat fluxes at a mass flow rate of 11.5kg/hr for R1234ze. 60

Figure 3.11 Background heater junction temperatures along flow direction for increasing base heat fluxes at a mass flow rate of 11.5kg/hr for R1234ze, at two locations across the test section width, for an inlet subcooling of 13°C and inlet saturation temperature of 30°C. 62

Figure 3.12 CMOSAIC Test Vehicle description–chip stack package with silicon embedded heat transfer structures. a) Ensemble view of package with all components. b) Vertical cross-section describing the multiple layers and their respective thicknesses. 63

Figure 3.13 Exploded views of the 3D chip stack package showing all different components. 64

Figure 3.14 Assembled CMOSAIC demonstrator. Manifold parts here are PMMA for visual and aesthetic purposes only. 64

Figure 3.15 A) SEM photograph of chip stack on interposer. B) SEM photograph of aluminium wire-bonds between interposer chip and PCB1.65

Figure 3.16 A) Chip stack with interposer glued to PCB1 and plugged into LGA/BGA socket. The socket is C4 bonded to PCB2. B) Complete 3D module attached to PCB2, showing inlet and outlet tubing as well as inlet and outlet temperature and pressure taps locations. 65

Figure 3.17 Chip-level design, with all frontside and backside structures visible. 66

Figure 3.18 Top view illustration of the design of a Hot Spot (HS) sputter-deposited heater with its own RTD, both 500nm-thick. The heater requires a current of 211 mA and a voltage drop of 8.92 V to output 50 W/cm^2. The resistance of the heater at ambient temperature is 34.9 Ohms. 67

Figure 3.19 A) SEM photograph of the LV2 chip frontisde, showing the added solder sealing structures (UBM side). B) SEM photograph of the LV3 chip backside, showing the solder interconnects and added sealing structures..67

Figure 3.20 Complete 3D chip stack module test section attached to experimental facility (Test Section 1, Figure 3.7), with inlet and outlet manifold temperature and pressure measurements.................................69

Figure 3.21 Total adiabatic pressure drop values for increasing channel mass fluxes from 183 to 549 kg/m^{2}s. Inlet and outlet temperature conditions are indicated for each pressure drop data point. 70

Figure 3.22 SEM photographs of defects due to the DRIE process of the microchannels on the backside of chips LV1 to LV5. A) Blocked microchannels. B) Narrower than expected microchannels. C) Much smaller depth of cavity for inlet orifices in front of microchannels............71

Figure 4.1 Discretization scheme of chip stack. 75

Figure 4.2 Block diagram of solution technique...75

Figure 4.3 front view of single 10×10 mm2 chip with 3x3 hot spot array layout. Microchannels are etched on the back. 79

Figure 4.4 Illustrations of the various patterns of active heaters applied to studied chip stack package. 80

Figure 4.5 Temperature vs. vertical position within the chip stack for Heat Load Pattern 1 at 50 W/cm^2 per chip. 81

Figure 4.6 Temperature vs. vertical position within the chip stack for Heat load Pattern 2 at 50 W/cm^2 per chip...82

Figure 4.7 Mass flux by channel across each evaporator; 10×10 mm^2 chip; Heat Load Pattern 3 at 38 W/cm^2; T_{SAT} = 60°C. 83

Figure 4.8 Mass flux by channel across each evaporator; 10×10 mm^2 chip; Heat Load Pattern 4 at 24 W/cm^2; T_{SAT} = 60°C. 84

Figure 4.9 Mass flux by channel across each evaporator; 10×10 mm^2 chip; Heat Load Pattern 5 at 50 W/cm^2; T_{SAT} = 60°C. 84

Figure 4.10 Mass flux by channel across each evaporator; 10×10 mm^2 chip; Heat Load Pattern 5 at 82 W/cm^2; T_{SAT} = 60°C. 85

Figure 4.11 Heat flux and heat transfer coefficient versus axial position along the center channel. Heat Load Pattern 5 at 82 W/cm^2; T_{SAT} = 60°C...86

Figure 4.12 Fluid pressure along the center channel, Heat Load Pattern 5 at 82 W/cm^2; T_{SAT} = 60°C. 87

Figure 4.13 Mass flux by channel across each evaporator; 10×10 mm^2 chip; Heat Load Pattern 4 at 24 W/cm^2; T_{SAT} = 30°C. 89

List of Tables

Table 2.1 Initial (after deposition) and final (after reflow) solder shape dimensions considering different pad geometries (Figure 2.13). 25

Table 2.2 Experimental solder height after reflow (He) versus height prediction by Surface Evolver (Hm), for Rail2 and Ball structures. 29

Table 2.3 Shear test results. 43

Table 2.4 Average initial solder height H0, average final bond-line height and bond-line thermal resistance for different solder joint types..............44

Table 3.1 Thermo-physical saturation properties of R1234ze at 30°C. 59

Table 4.1 Chip stack relevant thermal conductivities in W/mK. 74

Table 4.2 R236fa saturation properties at 30 and 60°C. 78

Table 4.3 Results for Heat Load Pattern 1 at 50 W/cm^2 per chip. 82

Table 4.4 Results for Heat Load Pattern 2 at 50 W/cm^2 per chip. 83

Table 4.5 Summary of results for parallel-to-flow hot spots. 87

Table 4.6 Summary of results for perpendicular-to-flow hot spots............88

Table 4.7 Comparison of results for Heat Load Pattern 4 at 24 W/cm^2 per HS, for two different fluid inlet temperatures. The junction temperatures are only about 9-10 K above the saturation temperatures in both cases, illustrating the effectiveness of the interlayer cooling approach. 90

Chapter 1 Of the importance of vertical integration and thermal management for processor and memory chips in the semiconductor industry

1.1 Vertical integration

1.1.1 Motivation and importance [1]

In the semiconductor industry, integrated-circuit (IC) feature sizes have been gradually reduced to integrate more transistors. This trend, as predicted by Moore's Law [2], consists in shrinking the transistors' gate dimensions to allow the reduction of the gate delay, the switching time of an individual transistor, thus decreasing operating voltages, improving electrical performance and of course increasing the number of transistors on a single chip [3] (Figure 1.1, [4]). However the speed of an electrical signal in an IC is also governed by the signal propagation time between transistors, and the performance of the interconnect wires is degraded as technology nodes continue to scale down, since smaller cross section wires have increased resistance and narrower metal pitches due to increased transistor density can raise the capacitance, as it can be seen on Equation 1.1 where R is the metal wire resistance, C the interlevel dielectric capacitance, L the line length, and P is the metal pitch. The sum of the two delays will thus increase with each new technology node as the interconnect delay starts to take over the gate delay [3] [5] (see Figure 1.2).

$$RC\ delay = 2\rho\varepsilon(4L^2/P^2 + L/T^2) \tag{1.1}$$

Remaining in a two dimensional plane and switching to larger System-On-Chip (SOC) dies with mixed technology designs does not provide a long term solution, since the integration of different technologies on a single chip would, on top of increasing the die area, require different processes to produce these different functions, which would raise materials, fabrication and cost issues. Meanwhile, the form factor of computing systems continues to be reduced for several applications, from servers to handheld devices.

Three-dimensional (3D) stacking of integrated-circuit dies presents itself as an interesting alternative. It corresponds to the integration in the Z direction of multiple 2D devices [3] (see Figure 1.3). It increases system density and package functionality by vertically integrating two or more chips. The vertical integration of IC chips using Through Silicon Vias

(TSVs) reduces the length of global interconnects and accordingly the signal delay time, while also improving bandwidth. Furthermore, the shorter communication distances help improve energy efficiency, by reducing power dissipation. Aside from the gain in electrical performance, other drivers such as a decrease in power consumption and noise, a form factor improvement, lower costs and more functionality show the significant benefits of 3D integration.

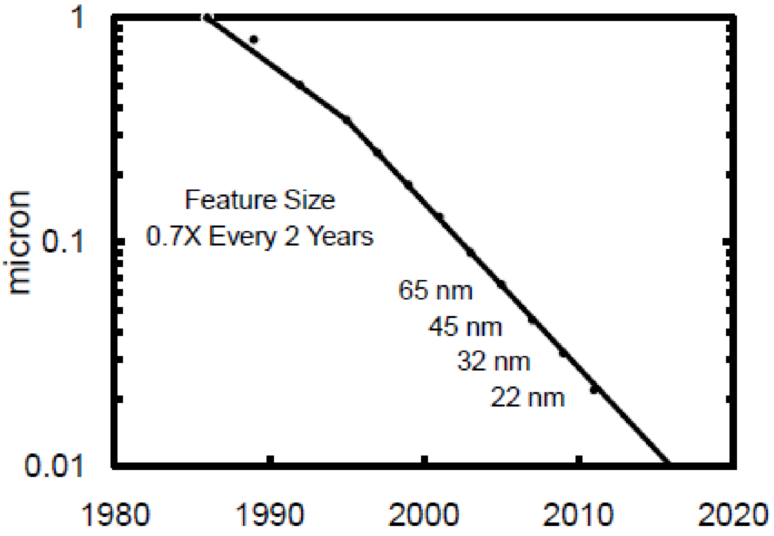


Figure 1.1 Shrinking transistor dimensions [4].

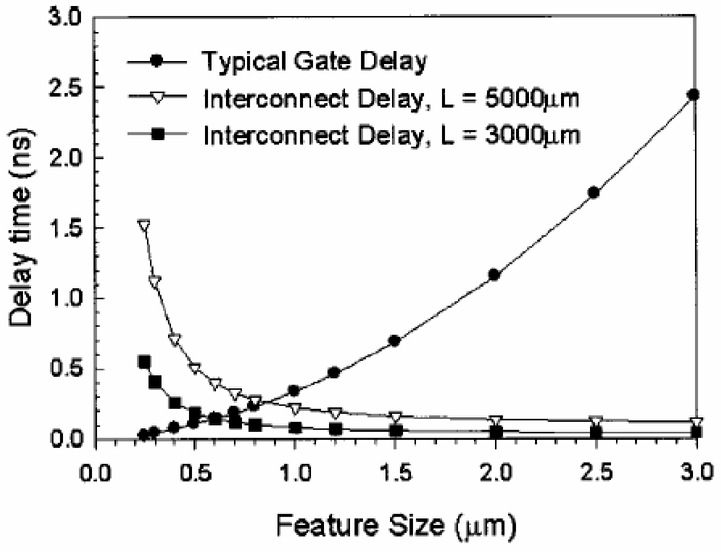


Figure 1.2 Gate delay versus interconnect delay for shrinking technology nodes [5].

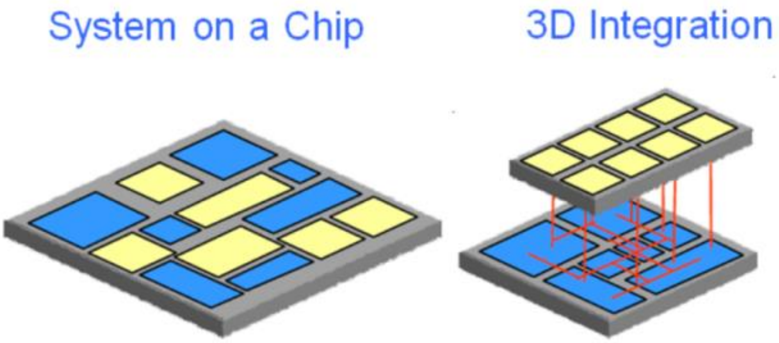


Figure 1.3 Left: SoC with multiple processor cores and cache memories. Right: Corresponding 3D stacked IC with considerably smaller area and shorter vertical interconnects [6].

1.1.2 Enabling technologies

3D integration of ICs would not be possible without the establishment and development of some of the following technologies. For an exhaustive list, the reader is encouraged to consult [7].

Through-Silicon-Via (TSV) technology

In layman’s terms, a Through Silicon Via (TSV) is a metal-filled hole “drilled” in a silicon chip or wafer. It serves to electrically connect one side of a silicon chip or wafer to its other side by creating a metallic and electrically conductive via within the bulk silicon between the two surfaces. Thus, they are the key element to 3D stacking of ICs, in that they enable the communication from the bottom most die in a stack to the top most die, and they most importantly allow the integration of different types of components onto a single stack (e.g. sensors, CMOS, DRAM etc.) [8]. Easier packaging, increased silicon area dedicated to electronics and optimized technology for each chip layer are enabled through the use of TSVs [8].

Several fabrication technologies need to be combined in order to create such vias. The following describes some of the essential techniques necessary to the creation of a TSV (presented later in detail in §2.2). For more TSV fabrication subtleties, the reader is encouraged to consult [8] and [9].

- **Deep Reactive Ion Etching (DRIE) technique**, also known as the Bosch process, introduced by Bosch in the mid-1990s [10] [11], used to etch the TSVs into the silicon. Its high etching rate and compatibility with high aspect ratio vias make it very popular for high interconnect density applications [12].
- **Thermal oxidation process**, necessary for the creation of a silicon dioxide (SiO_2) dielectric coating to electrically isolate the bulk silicon from the metal-filled TSVs. The thickness of the liner depends on its growth temperature and the time spent at that temperature, as well as on the quality of isolation desired. The definition of the high-

est allowable temperature for oxide growth on silicon is set by the number of pre-existing metallization layers. If none, the temperature can be in the range of 700-900°C or even higher. Oxide growth is also possible by Chemical Vapor Deposition (CVD) [13].

- **Electrochemical deposition of metal** (also called electroplating), used to fill the etched TSV with an electrical conductor. Currently copper (Cu) and tungsten (W) are the most widely used metals, but other materials such as poly-silicon are also being explored. Overall, several techniques are possible to realize metal deposition: electroplating, CVD, electroless plating and Physical Vapor Deposition (PVD, sputter-deposition). All are all capable of filling high aspect ratio TSVs except for the sputtering method [14]
- **Chemical Mechanical Polishing**, used to planarize both surfaces of the wafer. This process follows directly the metal filling of the TSV, and is mainly designed to remove any over-deposited metal that might be protruding from the TSV trench [8]. Following this step, development on the surfaces of the wafer can begin.

Wafer thinning technology

Wafer thinning is used to reduce the thickness of a wafer prior to its dicing, in order to facilitate the stacking and high density packaging of ICs, by improving and reducing the form factor of electronic components whose sizes need to adapt to the more and more compact electronic products, such as smartphones [7].

Alignment and bonding technologies

In the MEMS fabrication world, alignment techniques are generally used for lithography and wafer or die-level bonding purposes. Bonding is a necessary technique to build 3D ICs, and is possible at different levels: wafer-to-wafer (W2W), die-to-wafer (D2W) and die-to-die (D2D) techniques, using interconnect technology. Wafer-to-wafer is mostly used for industry and production purposes, while die-to-die is mostly done at research level for prototype building [7], as is the case for this thesis (Chapter 2). Several bonding techniques are available today, such as solder, wire, polymer or anodic bonding [15].

1.2 Thermal management of ICs

1.2.1 Importance, past and current concepts: from air to liquid cooling [16] [17]

Efficient heat dissipation in IC packages is crucial to support the packing density and performance scaling of future systems [18] [19]. The ongoing miniaturization trend of ICs results in constantly increasing chip-level power densities (Figure 1.4). The demand for higher computational performance results in microchips with more and more cores and cache memory. These cores communicate via long wires which consume a lot of energy and generate a considerable amount of heat. The International Technology Roadmap for Semiconductors (ITRS) projects that the power density of a single chip package will increase to 108 W/cm^2 for cost performance applications in 2018 [20], from the current power density of 60–80 W/cm^2. Thus, heat removal has become an ever increasing challenge, and the development of new chip cooling concepts is of utmost importance. Indeed, the reliability, performance, and power dissipation of interconnects and transistors are heavily dependent on their operating temperature.

These IC packages are traditionally air-cooled. Through forced (or natural) convection, heat is forced out of an IC package via a backside-attached copper heat sink and released into the atmosphere, which allows modern microprocessors nowadays to operate at safe temperatures. However the increase in typical microprocessor heat fluxes in the recent years as mentioned above has rendered air-cooled packages very large in size and complexity, as shown on Figure 1.5, and they are becoming inadequate in meeting the demands brought by the ongoing miniaturization trend of ICs. Therefore, backside micro-channel fluidic cooling concepts, be it single-phase water or two-phase dielectric evaporative cooling using environmentally-friendly refrigerants, were introduced into high-end server products [21] [17].

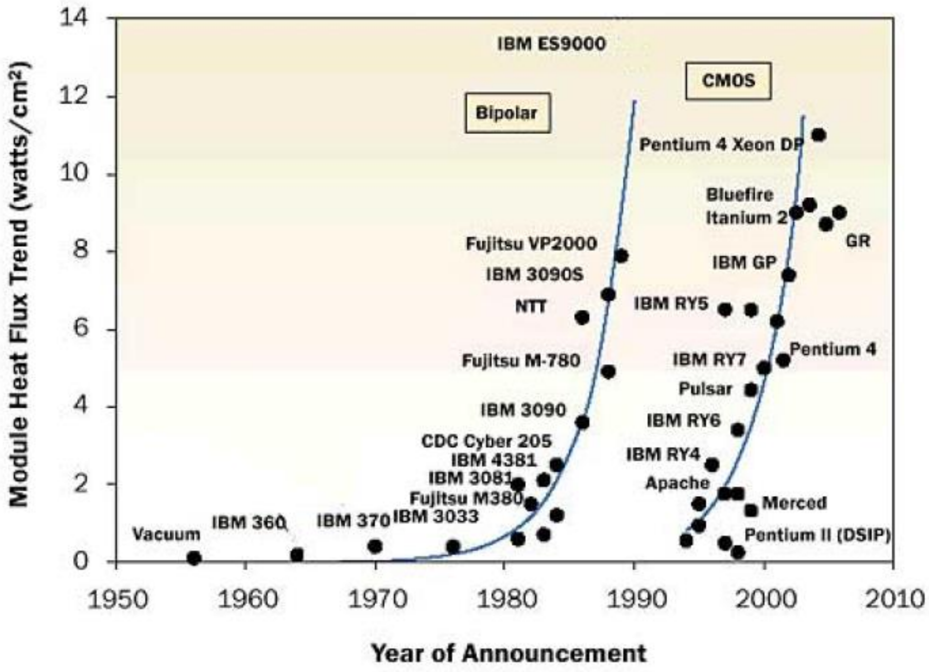


Figure 1.4 Module and chip heat flux densities for IBM chips, from the 1950s until early 2000s [22]. According to IBM Zürich Research, module heat fluxes between 0 and 14 W/cm^2 roughly correspond to chip heat fluxes between 0 and 80 W/cm^2, knowing that these chips occupy around 7/38th of the module area.

Due to this, microscale heat transfer has gained attention in the heat transfer community, and in the last few years, a significant research effort has begun around the world to develop the necessary methods for designing and optimizing microscale heat spreaders for cooling of processor chips. Single-phase water cooling has seen the most interest to date because of its ease of use, low pressures involved, and water's high heat capacity. The feasibility of electronic cooling using water as coolant has been demonstrated [23] and resulted in sophisticated designs for single cavity backside heat removal [24] [25] [26] [27]. Water has the obvious disadvantages, however, of significant temperature gradients along the cooled device, a high freezing point temperature for shipping, and the danger of having water near electrical connections. This is where two-phase flow boiling in microscale heat sinks becomes interesting.

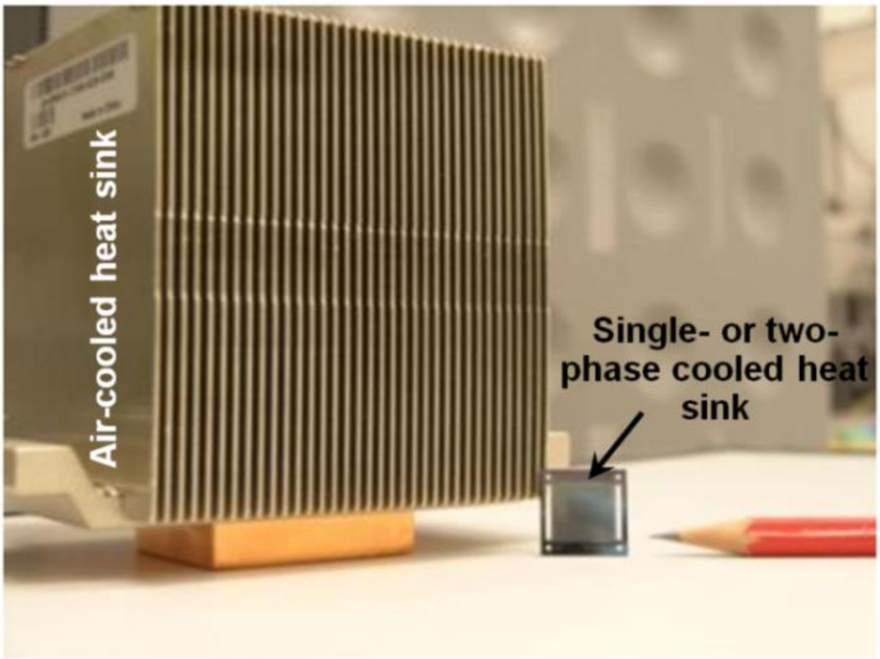


Figure 1.5 General size comparison between air-cooled heat sinks and single- or two-phase cooled heat sinks (Source: IBM Research, Zürich).

1.2.2 Microscale flow boiling of refrigerants

Introduction [17]

Although liquid cooling may be the preferred near-term solution due to reasons mentioned above, cooling of processors through flow boiling of refrigerant does not encounter the problems described above and seems to be the ideal long-term solution, especially because it answers several of the desirable features in electronic cooling systems, as outlined by Agostini et al. [28].

For example, taking advantage of the latent heat liberated during boiling allows operation at lower mass flow rates and thus reduces pumping power, resulting in a more energy-efficient cooling system. Two-phase flow boiling is also interesting in terms of thermal interface durability, since phase change occurs at almost constant temperature along the channels, which is beneficial for electronic chips since large temperature gradients reduce their efficiency or even damage them. In addition, the process is favorable for hotspot management, since the primary trend observed in flow boiling in microchannels is that the heat transfer coefficient increases with heat flux and is mildly dependent on vapor quality [29]. Furthermore, many hydrofluorocarbons are available with a large choice of properties, and the refrigerant fluids are in most cases dielectric and nonflammable, with the latest ones having a low toxicity and smaller global warming potentials.

Heat transfer coefficient [1] [17]

Many studies have been carried out on two-phase cooling in microscale heat transfer structures. A selected few examples are summarized in this section. Agostini et al. [30] presented a comprehensive state-of-the-art review of high heat flux cooling technologies that include liquid jet impingement, single-phase liquid cooling, and two-phase flow boiling in copper or silicon microstructures.

For example, a study of refrigerant flow boiling at high heat fluxes in microchannel heat sinks was carried out by Lee and Mudawar [31] with refrigerant R134a flowing in 0.231-mm-wide and 0.713-mm high parallel copper microchannels, with base heat fluxes as high as 93.8 W/cm^2. Their study showed that the heat transfer coefficients increase with heat flux and decrease with vapor quality, which seems to be the typical trend in microchannels. They were not able to show local effects along the channels, however, since their test section had only one thermocouple to measure the multichannel base temperature.

Agostini et al. [29] measured local heat transfer coefficients for refrigerant R236fa boiling in a silicon multi-microchannel heat sink, at a saturation temperature of 25°C, for a large range of heat fluxes, mass velocities, and vapor qualities. A split-flow design, as will be used here, was tested with one central inlet and two outlets. Two-phase cooling performances as high as 255 W/cm^2 were measured, showing that the base temperature of a chip can be maintained below 52°C with 90 kPa of pressure drop and a coolant flow rate of 0.49 l/min. The heat transfer coefficient during flow boiling of R236fa increased with heat flux, decreased with mass velocity, and decreased slightly with vapor quality. At a base heat flux of 200 W/cm^2, the temperature uniformity was <±1 K.

Flow boiling heat transfer of R134a, R236fa, and R245fa was researched by Ong et al. [32] for a horizontally heated tube with a 1.03mm diameter. The authors observed a dependence of the heat flux on heat transfer coefficients for low vapor qualities, for all tested fluids. A dominance of the convective boiling mechanism with a parallel vapor quality increase was additionally reported for the annular flow regime, for low pressure fluids such as R236fa and R245fa.

A series of experimental campaigns under hot spot conditions were conducted by Costa-Patry et al. [33] [34], and via these experiments it was shown that the prediction methods of Thome et al. [35] and Bertsch et al. [36] were suitable for non-uniform heat flux applications. Costa-Patry and Thome [37] later published a new flow pattern-based prediction method for heat transfer coefficient in microchannels, by combining the three-zone model of Thome et al. [35] and the Cioncolini and Thome [38] annular flow model for convective boiling.

Marcinichen et al. [39] proposed a multi-microchannel two-phase refrigerant evaporation system as a green solution for the cooling of supercomputer blade servers and clusters, which can contain up to 64 blades per rack (56 for 4 blade centers in a normal 2m-tall rack and 70 for 5 blade centers in a high 2.3m-tall rack) cabinet, including their respective memory.

Most recently, Szczukiewicz et al. [40] [41] have presented test results for a 67 channel-microevaporator with 100×100 μm^2 silicon channels at heat fluxes approaching 50 W/cm^2. These 2D tests were conducted as a test case for 3D stacks with the same channel dimensions.

Pressure Drop [42]

Pressure drop is an important parameter when designing a micro-evaporator for microelectronics cooling. Indeed, the less the total pressure drop of the flow boiling cooling system, the less pumping power is needed, and the more energy efficient the system will become. The goal when designing and optimizing a multi-microchannel cooling system is to try and achieve the highest cooling performance with the lowest pressure drop possible. In general, pressure drop increases with vapor quality and mass flux. Bergles et al. [43] found that a multi-microchannel setup requires both inlet and outlet manifolds with slits, which help in preventing back flow due to the nature of the boiling process.

Agostini et al. [29] [44] showed for refrigerant R236fa that at low vapor quality (< 0.1) the total pressure drop was mainly due to the single-phase component. As the vapor quality increased though, the two- phase pressure drop component quickly became the dominant mechanism. For vapor qualities greater than 0.1 the two-phase component remained the dominant mechanism, contributing to 80% of the total pressure drop. The contribution of the outlet pressure drop, meanwhile, remained constant or decreased at high ranges of mass flow rate. At higher ranges of vapor quality, the outlet pressure drop ratio increased and the two-phase pressure drop ratio either remained constant or decreased, depending on the mass velocity. For R245fa, the trends are similar but can differ depending on the mass flow rate.

A novel annular flow model capable of predicting two-phase flow frictional pressure drops was established by Cioncolini et al. [45], while considering the Lockhart and Martinelli [46] method for the isolated bubble regime. This new method enabled the best prediction in the isolated bubble (IB) and coalescing bubble (CB) regimes, defined by Ong and Thome [32], as it was shown in Costa-Patry et al. [47].

Two-phase flow boiling of R245fa and R236fa was investigated by Costa-Patry et al. [47] [48], on a test section comprised of 135 silicon multi-microchannels, each 85 µm-wide, 560 µm-high as well as 12.7 cm-long and separated by 46µm-wide fins. All channels were heated by 35 local heaters. It was found that the outlet restriction pressure drop losses corresponded to up to 30% of the total pressure drop through the micro-evaporator and thus could not be ignored. When combined with the Lockhart and Martinelli [46] method for the isolated bubble regime, it was observed that the annular flow model of Cioncolini et al. [38] correctly approximated the measured microchannels pressure drop values in [47].

1.2.3 Chip stacks and thermal management limitations

Building on what was explained in §1.2.1, cooling 3D chip stacks is a major challenge because every level of such a three dimensional chip stack generates high heat fluxes. Keeping the junction temperature of stacked chips below 85°C for heat fluxes up to 250 W/cm^2 requires a different and improved approach. Applying the backside cooling concepts mentioned above to the backside of 3D stacks instead of single chips will only be of temporary efficiency (see Figure 1.6), as a major limitation of vertically integrated packages is that heat fluxes and thermal interface resistances accumulate with each layer. Therefore, scalable cooling solutions, such as interlayer cooling, need to be investigated.

1.2.4 Interlayer cooling: a scalable solution

Advantages and challenges

The main advantage of interlayer cooling is that it scales with the number of dies, since every die within the chip stack would get its own embedded heat transfer geometry, contrary to backside cooling [22]. But because of that, other aspects then become very challenging. Constrained by the interconnect pitch, the through-silicon via (TSV) aspect ratio and future thin chip thickness (<100µm), the active heat transfer area, or the hydraulic diameter, will tend to be smaller because of the limited space and in turn reduce the possible flow cross-section. According to [49], the flow rate can be up to 10 times reduced when compared to backside coldplates.

Additionally, the fact that fluid is actually supposed to “enter” the stack creates a sealing challenge, especially when working with electrically conductive coolants like water (less of a problem with refrigerants): the active solder pads and TSVs need to be isolated from the conductive coolant. Also, when working with a potentially high pressure coolant, the chip stack, whose chips already have a compromised structure due to the etching of backside embedded microchannels or pin fins, has to be able to sustain that mechanical stress. New solutions need to be found to increase die-to-die mechanical strength, ideally by using additional solder. However, historically solder joints have had an electrical duty, not a mechanical one. Finally, the edges of the chips need to be closed to avoid leakage of the coolant from the sides of the chip stack.

Nevertheless, interlayer cooling's main advantage is more powerful than the sum of its created challenges.

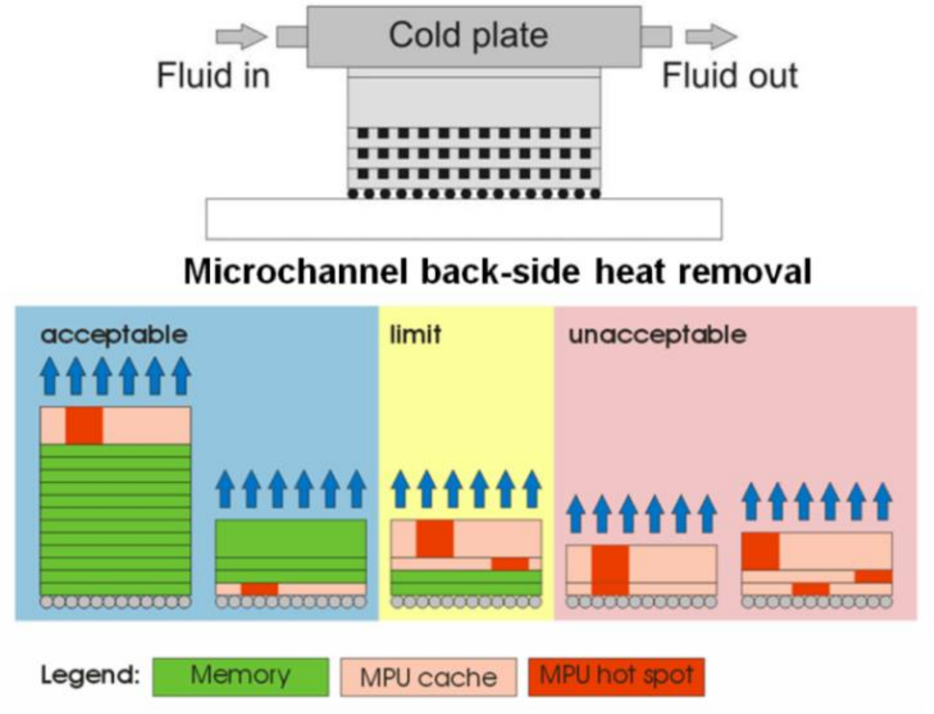


Figure 1.6 Chip stack configuration with acceptable, close to the limit and unacceptable junction temperatures with backside water heat removal. Maximum allowable MPU junction temperature is 80°C, acceptable memory temperature limit is 95°C, and fluid inlet temperature is 20°C [50].

Existing concepts and their implementations [1]

Dang et al. [51] showed the feasibility of a silicon chip with an embedded microchannel heat sink and novel thermofluidic chip input/output (I/O) interconnects, fabricated using wafer-level and CMOS compatible batch processing, with its extension to a 3D chip stack using Through-Silicon-Vias (TSVs) for electrical vertical integration.

King et al. [52] reported for the first time the configuration, fabrication, and experimental testing of a 3D integrated system that can support the power delivery, signaling, and heat removal requirements for high performance chips. However focus was directed on fabrication as well as assembly, and no thermal measurements were performed nor presented.

Brunschwiler et al. [49] presented an interlayer cooling concept, consisting of a 5-layer chip stack where every chip is connected individually via wire-bonding. A hot-spot aware heat transfer study was performed with water as working fluid. The authors identified that microchannels efficiently mitigated hot spots by distributing the dissipated heat to multiple cavities due to their low porosity and that pin fins with improved permeability and convective heat dissipation are advantageous at small power map contrast and aligned hot spots on the different tiers. The authors concluded that large stacks of 4 cm^2 can be cooled sufficiently with a 4-port fluid delivery architecture, which improves the flow rate four times compared to the 2-port version.

1.3 Thesis outline and objectives of this work

The aim of this thesis is the development of the first ever 3D stack of silicon computer chips that includes a high fill factor and high aspect ratio TSVs as well as chip-level embedded heat transfer structures, and its fluidic testing with the flow boiling of a commercial refrigerant.

The thesis will start by presenting a concept for interlayer cooling, which will justify the development of the novel solder interconnect structures presented in Chapter 2. These novel structures will enable the inclusion of heat transfer geometries within the chip stack without additional costs or fabrication processes and still be compatible with wafer-level packaging assembly techniques. Reflow, electrical, mechanical and thermal resistance tests were performed on these novel solder interfaces to assess their viability and reliability within “packaging for cooling” processes.

Chapter 3 will then showcase the design, fabrication and assembly of the first worldwide 3D chip stack module, with high aspect ratio TSVs and integrated interlayer cooling capabilities, that uses some of the novel solder structures presented in Chapter 2. This will be followed by the initial fluidic testing in two-phase flow regime with flow boiling of refrigerant R236fa at a saturation pressure of 3.3 bar. This chapter will also present initial pressure drop and infrared camera thermal measurements for the flow boiling of refrigerant R1234ze within a 2D single cavity staggered pin fins test section, to assess the cooling performance of such a package and its compatibility within a three-dimensional multi-cavity system.

Chapter 4 will describe the implementation of a new thermal model and simulation method, created to optimize heat spreading and fluid flow using interlayer two-phase evaporative cooling within a multi-microchannel evaporator chip stack. This model, as a first step, will be used to study ideal local heat load placement within a chip stack.

Finally, Chapter 5 will conclude the thesis and offer recommendations for a potential follow-up work to this dissertaion.

Chapter 2 Patterned solder bonding for die-to-die attachment: novel structures

This chapter presents the challenges brought by the integration of enhanced cooling micro-structures in a 3D chip stack [53] and concentrates on the challenges put upon the die-to-die solder interconnect. Switching to 3D chip stacks with integrated cooling demands a new solution for die-to-die soldering. So far, the industry relied heavily on the C4 (controlled-collapse chip connection) solder bonding technology that was developed by IBM in the 1960s, and has been widely used for high-I/O-count applications [54]. This chapter proposes to put into consideration thin film solder joints as die-to-die interconnects, where a thin 5 to 10µm thick patterned layer of solder acts as the mechanical and electrical interconnect between the two dies, and as the sealing structure between interconnects and a conductive liquid coolant such as water. Higher fill factor solder rails will also be presented as a new concept to remove thermal stress within a microelectronic package. The results presented in the following chapter are published in [16], [55] and [56].

2.1 Introduction: inter-tier thermal management

Figure 2.1 shows the concept a 3D stack of chips with an integrated inter-tier cooling system. In this design, the coolant, whether water or a dielectric fluid enters via the manifold and flows through the microchannel cavities that are etched into the backside of every die that is part of the stack. Patterned thin film solder (5 – 10µm thick) is needed to bond the dies together (Figure 2.1, bottom), in order to minimize the gap between the tiers. TSVs are integrated for vertical communication within the package, and these can be implemented either at the edge of the chip (as shown on Figure 2.1) or alternatively placed in-between the channels. Depending on the positioning of these TSVs across the dies, some or all thin film solder pads can be electrically active. The electrically active ones need to be insulated from the coolant, should the latter be conductive. Figure 2.2A and 2.2B propose solutions where a ring made of solder would protect and “seal” the electrically active pads. Additionally, since a small gap (corresponding to the solder interconnect thickness) exists between the different dies, coolant fluid would be leaking from the edges of the dies during operation. To prevent this from happening, outer-die sealing structures need to be implemented, during the same fabrication step as the thin film solder pads. An example of these structures is shown on Figures 2.2B and 2.3.

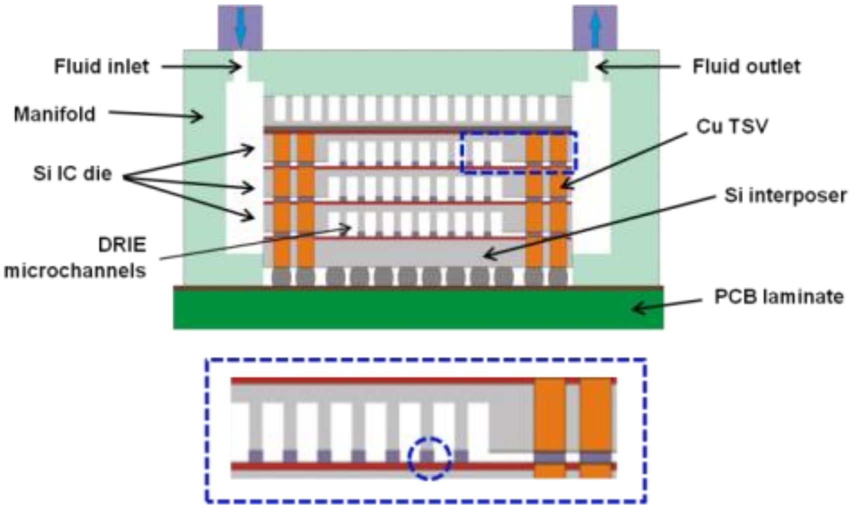

Fluid inlet
Fluid outlet
Manifold
Cu TSV
Si IC die
Si interposer
DRIE
microchannels
PCB laminate

Figure 2.1 Patterned thin film solder bond concept for mechanical and electrical connection in 3D chip stacks with integrated cooling capabilities. The highlighted part shows the needed patterned thin film solder interconnect.

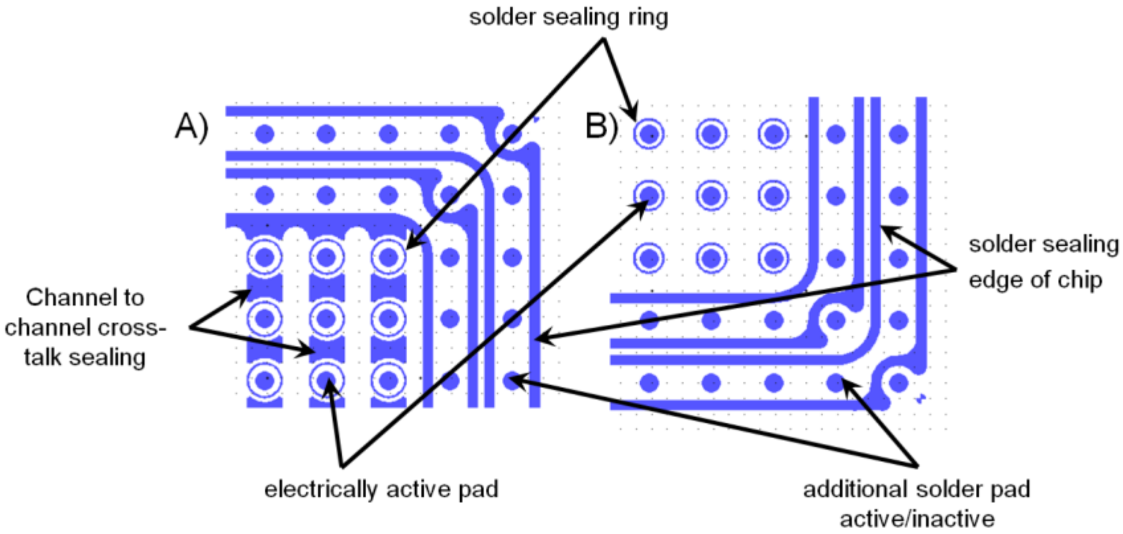

solder sealing ring
A)
B)
Channel to
channel cross-
talk sealing
solder sealing
edge of chip
electrically active pad
additional solder pad
active/inactive

Figure 2.2 Additional solder structures needed for a scalable cooling solution (top view on single die, blue is solder). A) Silicon-etched microchannels as heat removal structures. B) Silicon pin fins as heat removal structures.

2.2 Electrodeposition and reflow of thin eutectic 3.5Ag96.5Sn

2.2.1 Thin film micro C4s

Based on what was presented above, die-to-die flip-chip bonding experiments involving thin films of solder need to be conducted. Eutectic 3.5Ag96.5Sn was chosen as the lead-free solder (see Figure 2.4). The choice of the eutectic phase was driven by its low-melting temperature (221°C) as well as its thermodynamic and mechanical stability (no plastic phase means minimized stress due to the heating and quicker wetting of the solder) [57].

It should be noted that the silver tin solder will be subsequently used for all soldering activities (reflow and flip-chip).

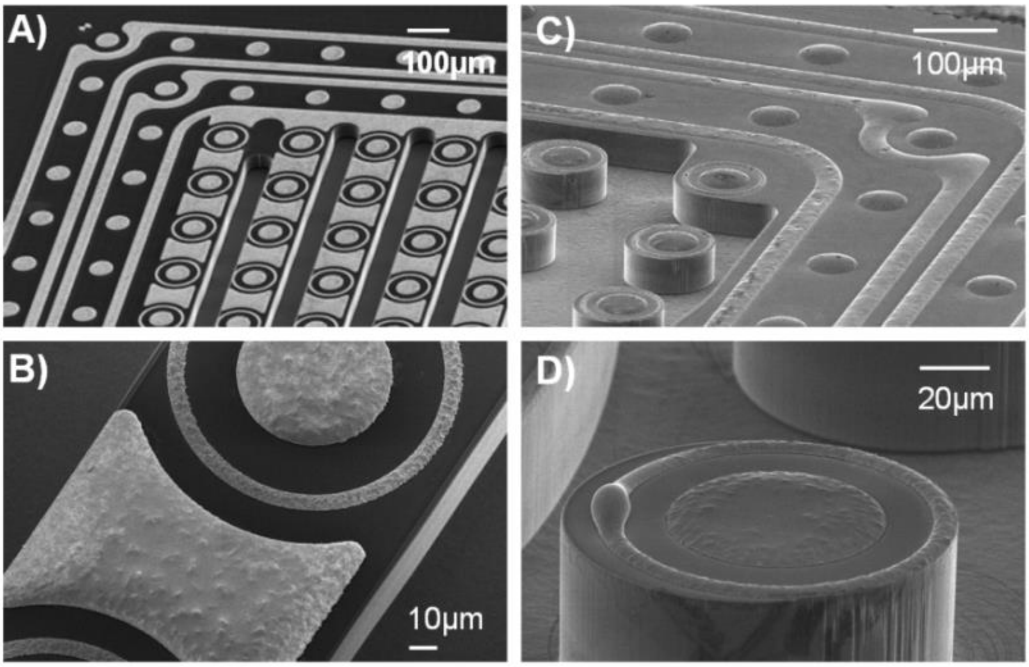


Figure 2.3 Scanning Electron Microscopy (SEM) real-life images corresponding to the solder concepts presented in Figure 2.2. A & B) With silicon chip-embedded microchannels. C & D) With silicon chip-embedded pin fins.

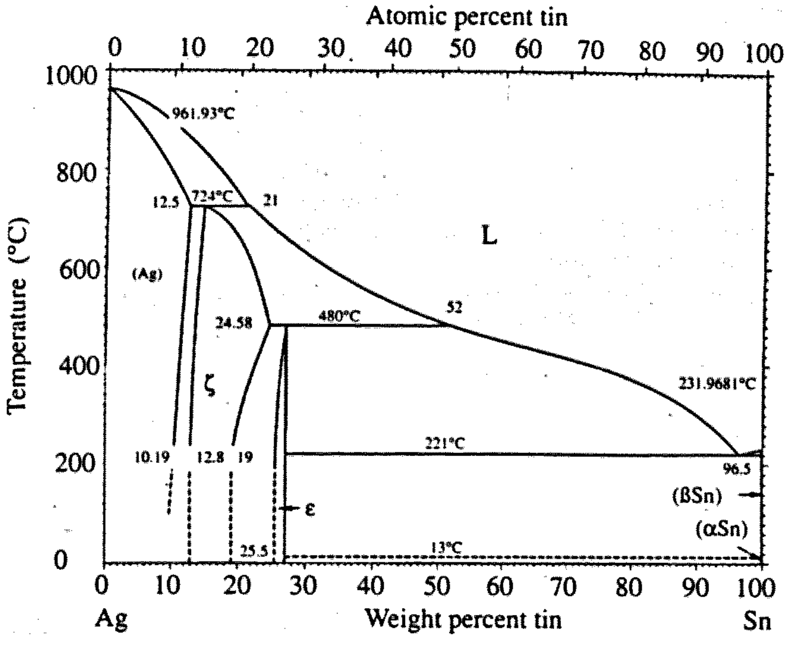


Figure 2.4 Silver Tin alloy phase diagram [58].

Figure 2.5 shows the fabrication steps for the deposition of AgSn solder through an electroplating process ("chip" wafer). Starting from a 4 inch silicon wafer (containing a native oxide layer), 650nm-thick copper (Cu) lines were deposited via a sputter-deposition process (steps A & B). These lines are the links of the daisy-chain, used for electrical probing, once the finalized chip wafer is flip-chip bonded to a carrier wafer. Step C shows the coating and patterning via Reactive Ion Etching (RIE) of a 2µm-thick polymer solderstop layer, preventing electrical shorting on the daisy-chain lines after reflow. A 150nm-thick Cu seed layer, necessary for the electro-deposition of solder, was then sputtered in step D. In step E, a positive photoresist was coated (AZ4662, AZ Electronic Materials), exposed and developed in order to pattern the solder deposition. Plating then occurred in step F, where nickel (Ni, 1-2µm), gold (Au, 0.5µm) as well as silver tin (AgSn, 5-10µm) were sequentially deposited. Nickel and gold formed the Under Bump Metallization (UBM). Silver-tin was directly plated in its desired eutectic phase (bath SOLDERON BP TS 4000). The solder bulk composition was controlled via Energy Dispersive X-ray Spectroscopy. Finally, the photoresist was stripped and the seed layer removed (step G). The pad diameter was 50 µm (solder & UBM) and the pitch between two solder pads was 200µm.

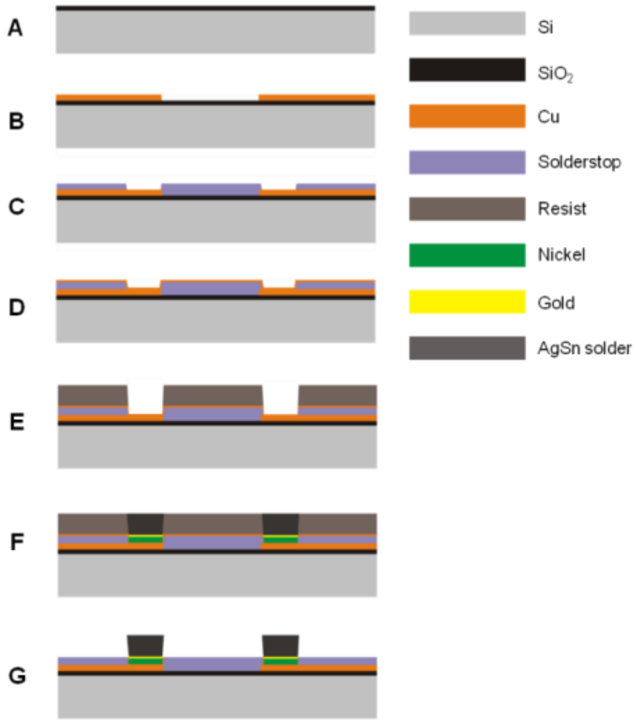


Figure 2.5 Thin film solder fabrication process.

The majority of flip-chip reflow soldering processes requires the use of a flux [9] [59]. For the concept proposed earlier (Figure 2.1), flux is not acceptable, for the simple reason that when used during the bonding process it would fill the cooling micro-structures, etched into the silicon. The possibility of having a semi-fluxless reflow process was thus considered. With this particular solder alloy under a fluxless reflow, an oxide layer on the surface was found to prevent the proper wetting of the carrier substrate pad during flip-chip bonding (Figure 2.6). The reflow temperature was 265°C.

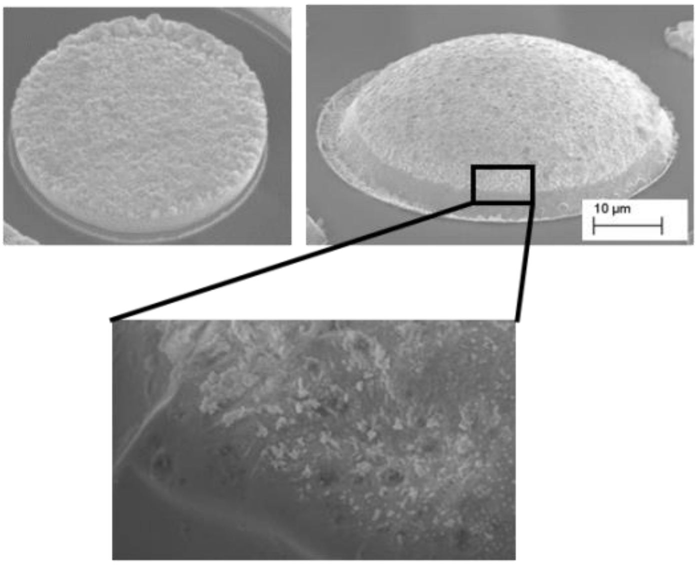


Figure 2.6 *Left:* plated (8µm-thick) AgSn solder thin film pad (50µm diameter). *Middle and bottom:* after fluxless reflow at 265°C, with tin oxide layer on the surface.

A Focused Ion Beam (FIB) treatment was then used on a reflown thin film pad, investigating the solder cross-section to determine the in-bulk depth of this oxide layer. Figure 2.7 shows that it clearly consists only of very thin surface layers.

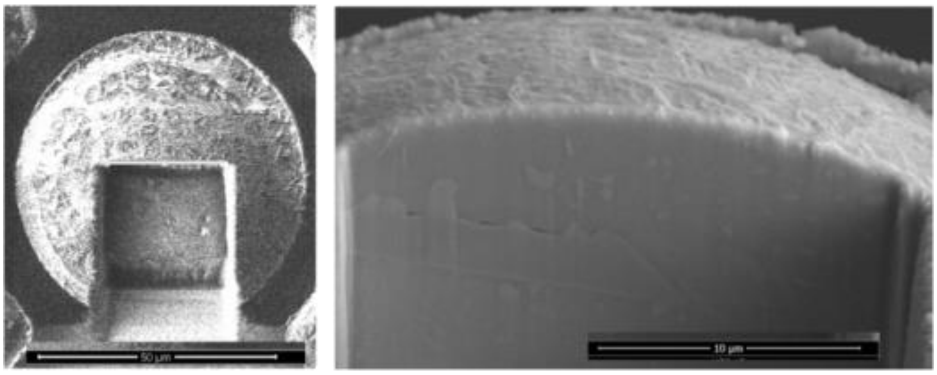


Figure 2.7 FIB cross-section of fluxless reflowed solder bump. *Left:* top view of solder pad with oxide layer. *Right:* corresponding cross-section.

Based on this, a parametric X-ray Photoelectron Spectroscopy analysis (XPS) on the solder joint's top surface (measured layer was 6nm thick) demonstrated that it was a tin oxide layer (the eutectic silver-tin alloy being tin rich), and not one of the underlying metallic layers, whether silver, gold, nickel or copper (see Figure 2.5), segregating to the top. Indeed Figure 2.8 shows the measurements of Sn3d for three different test cases: surface analysis directly after electro-deposition (no treatment), after reflow without flux and finally after flux driven reflow (plus cleaning). After deposition or reflow with flux treatment, metallic Sn can be detected, whereas after reflow at ambient conditions, only SnO_2 can be detected, meaning that the oxide layer is thicker in this case.

To reduce the solder joint's surface, flux driven reflow outside and prior to the bonding process was investigated, and Figure 2.9 shows the disappearance of the tin-oxide layer. After the prior reflow the flux needed to be removed since it could cause blockage of the integrated cooling structures (Figure 2.1). This was done via hot water cleaning, to remove any remaining flux residue. This process of reflowing and cleaning prior to the bonding step is also compatible with wafer-level packaging.

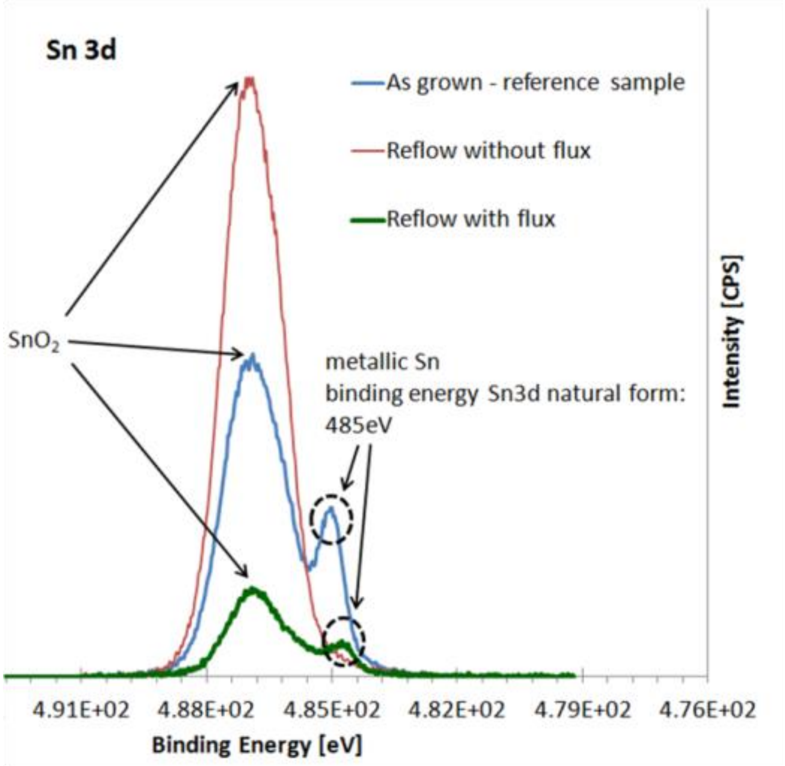


Figure 2.8 Tin (Sn3d) XPS measurements for plated die (after deposition, blue), reflowed die without flux (ambient atmosphere, red) and reflowed die with flux treatment (green).

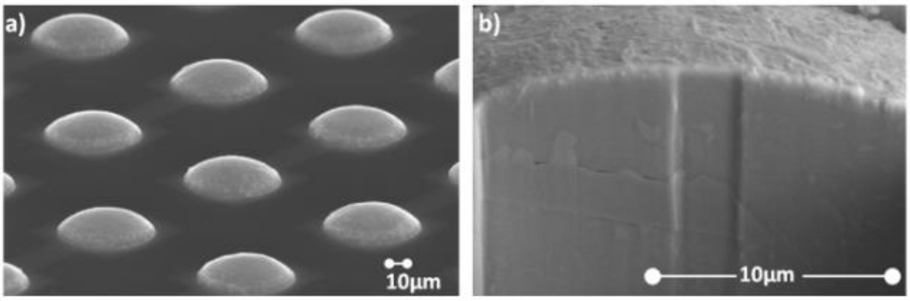


Figure 2.9 a) Flux-reflowed solder pads, 58µm in diameter and 12µm thick. b) FIB cross-section of a reflowed solder bump.

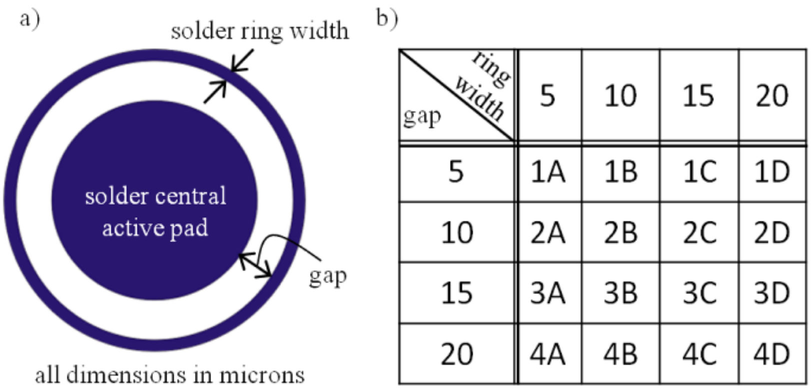
2.2.2 Rails

The reader is kindly redirected towards § 2.3. Thick solder rail structures will be presented, but it should be noted that thin-film solder rails will also be used later in § 3.2 as a sealing structure for the side of the chip, stretching between the top and bottom of the die. However the solder reflow behavior of such thin-film solder rails was found to be similar to the one of the ring structures described in the following section § 2.2.3.

2.2.3 Sealing rings

Design and fabrication

The use of water as a coolant requires additional sealing methods, to protect the electrical interconnects from shorting through the water. A ring-pad design (Figure 2.10a) is proposed, compatible with the presented thin-layer solder technique, to seal the inner solder pad (covering the TSV) from the liquid coolant with an additional solder ring structure. Figure 2.10b shows the range of values experimented with for the two main ring geometry parameters, namely the gap between the central active pad and the ring as well as the ring width.



gap / ring width	5	10	15	20
5	1A	1B	1C	1D
10	2A	2B	2C	2D
15	3A	3B	3C	3D
20	4A	4B	4C	4D

Figure 2.10 Solder fluidic sealing concept. a) Design and geometry. b) Range of studied combinations of parameters and their different designations.

Since the ring-pads are novel structures, before the actual fluidic sealing tests, their fabrication and reflowability must be assessed. The fabrication process for the sealing rings is the same as the one presented in Figure 2.5. Because of the difference in dimensions between the rings themselves and their corresponding central pads, different solder heights were deposited since local current densities differed during electroplating, which in turn resulted in discrepancies in solder quality (same for the Ni plus Au UBM). It was generally observed that less solder was deposited on the rings than on the central pads.

Reflow tests

After fabrication, 10x10mm^2 chips containing homogeneous arrays of different ring-pad structures (from 1A to 4D, Figure 2.10) were reflown on a hot plate at a temperature of

265°C, using hot water-soluble flux, and then cleaned to improve SEM inspection quality. Figure 2.11 shows the SEM pictures for geometries 3A to 3D after reflow. These representative SEM photographs show that after the reflow, dome-shaped rings and rings with local solder accumulation, called balling, were observed for wide (3B to 3D) and narrow (3A) widths respectively.

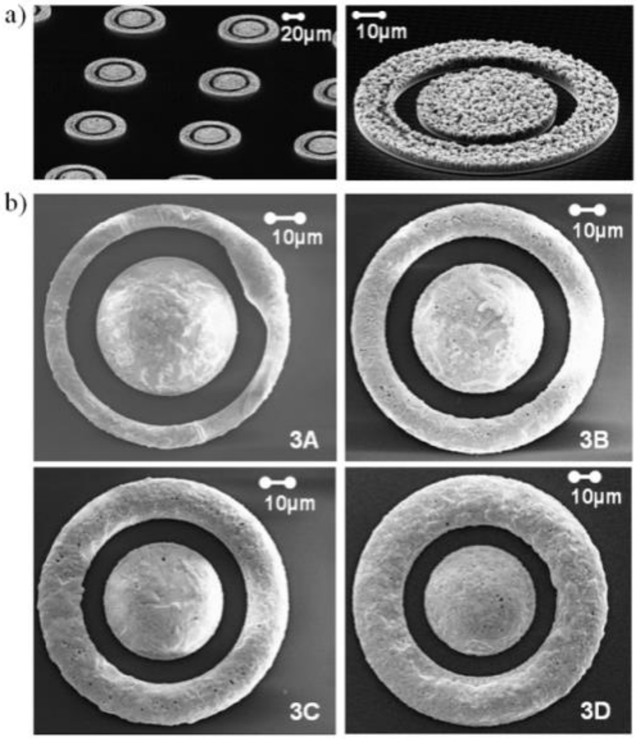


Figure 2.11 a) Solder ring pads after electroplating. b) Ring pad structures 3A to 3D after reflow on hot plate and cleaning.

Due to their very small gap between the ring and the central pad, structures 1A to 1D all shorted after reflow. The compiled reflow results are presented on Figure 2.12 for geometries 2A to 2D and 3A to 3D since their dimensions correspond best to the silicon fins embedded in the chip stack. The aspect ratio of the initial plated ring solder height H_0 to the ring width W_r is plotted against the initial solder height H_0. Squares and circles indicate respectively dome-shaped rings and rings with balling. From these results, a close to constant critical aspect ratio of approximately 0.65 can be extracted, similar to the one established for thicker solder structures in [56] and presented in § 2.3 below, thus adding to the range of experimented deposited solder heights. Structures 4A to 4D behaved similarly. It will be shown in § 2.3 that for long solder rails an invariant critical aspect ratio for different rail widths could be explained theoretically without the influence of gravitational forces (Bond numbers below one, see Equation 2.1). In that case the minimal energy state is equivalent to the geometry with the minimal surface area and hence that geometry is independent of size, and only depends on the aspect ratio of the solder rail cross-section. Since it can be extrapolated that the ring-pad structures are basically curved rails, the same reasoning can be applied here.

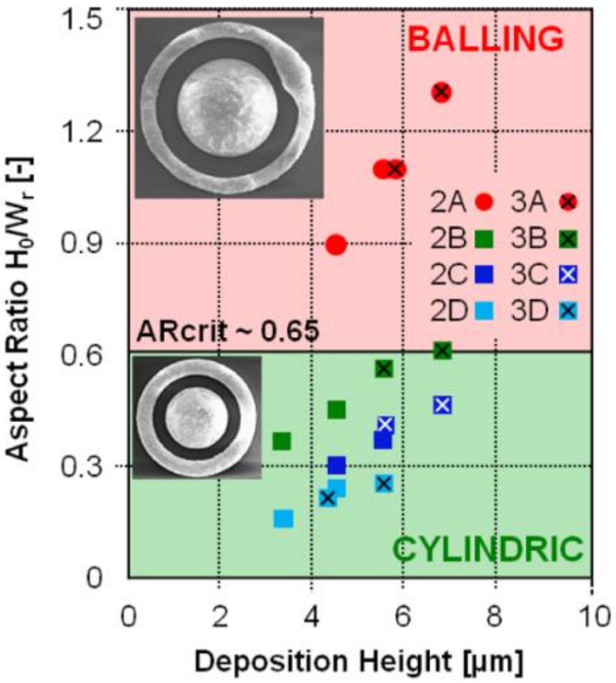


Figure 2.12 Experimental categorization of ring pad solder shapes after reflow for varying deposition heights H_0 and ring aspect ratios (deposition height H_0 to ring width W_r). Dome- (squares) and ball- (circles) like shapes were identified below and above the critical aspect ratio of 0.65. Inserts depict SEM photographs.

2.3 Investigation of high fill factor solder patterns for power delivery and heat removal support

2.3.1 Motivation and implementation

The ongoing trend of miniaturization and system complexity of integrated circuits results in ever increasing power density in electronic packages. Accordingly, the development of power delivery and heat removal concepts are of paramount importance. Overall, the volumetric integration density improves the computing efficiency and performance due to short communication distances with low capacitance, resistance and latency [19]. This statement is especially true for data centric workloads which benefit tremendously from systems with large memory and cache size in close proximity and high bandwidth to logic blocks [60].

Stanley-Marbell et al. [61] predicted future current density demands based on the analysis of past and current microprocessor products. They depict an ever increasing competition between signal and power pins, culminating in the so called “bandwidth and power density wall”. This limitation hampers the system performance gains achieved through further transistor miniaturization while utilizing existing packaging technology. Even the introduction of vertically integrated chip stacks for high-performance applications is threatened by the power wall. Multiple dies in the stack have to share the power provided through the invariant solder ball count from the bottom most chip [62].

In addition, heat removal becomes an ever increasing challenge. Therefore, microchannel liquid cooling concepts were introduced into high-end server products [63] [64]. Advanced thermal interface materials with tri-modal particle loading are applied between chip-backside and cold plate [65] [66]. And as stated in Chapter 1, heat removal of 3D stacks will be a major limitation as heat fluxes and thermal interfaces are adding up.

A large body of literature is available disclosing concepts to increase the current density feed to an integrated circuit through solder ball arrays. Electromigration (EM) dictates the maximal current supported by a solder ball. It can be improved by the use of advanced under bump metallizations (UBM), resulting in intermetallic compound (IMC) formation with increased EM resistance [67]. In addition, copper pedestals are proposed to mitigate current crowding in the IMC and solder compound [68].

Thermal underfills are under development to alleviate the effective thermal resistance of electrical joints between individual tiers in a chip stack [69] [70]. The electrical joint is a major thermal bottleneck due to the low area fill fraction of approximately 21% in case of fully populated solder ball arrays (dummy solder balls are inserted to yield full population) [71] [72].

All these technologies constitute a major deviation from current interconnects and choice of materials with the corresponding investments and risks.

This section proposes and reports on the utilization of mixed solder shapes to satisfy power delivery, heat removal, and signaling of high-performance dies, in particular 3D chip stacks or embedded components with heat dissipation from the chip face into the substrate. The current approach of a monoculture of solder balls certainly supports the high-speed communication at a high-pin count. In contrast, solder rails can yield a larger solder fill factor of up to 70% supporting current feed and heat dissipation (Figure 2.13). The rail topology is also in agreement with the electrical interconnect floorplan, where the positive supply voltage (Vdd) and ground (GND) interconnects are typically arranged in lines [73].

To the best of our knowledge, neither logic nor power electronic packages take advantage of rail-shaped solder interconnects. However, rail-like sealing rings are applied by the MEMS industry, to form vacuum cavities for sensor applications [74]. Thin solder thicknesses of smaller than 10 µm can typically be applied to the precision components with minimal warpage due to the matched thermal expansion. In contrast, solder heights of 60 µm are standard in flip-chip-on-board (FCOB) applications to provide process robustness and the needed stress relief by solder yielding while joining a chip to an organic laminate.

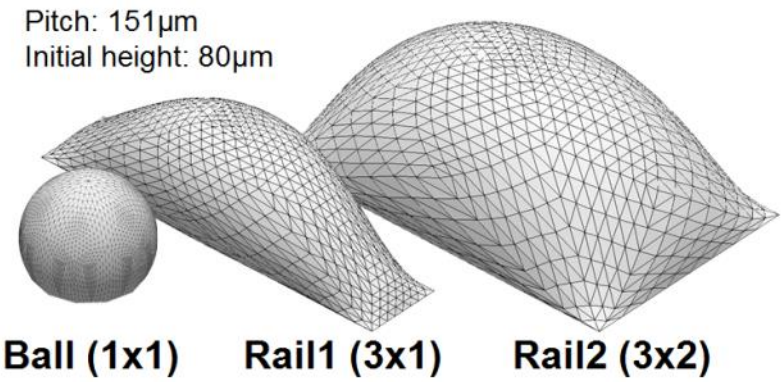


Figure 2.13 Isometric view of distinct solder shapes after reflow resulting from circular and rectangular pads as predicted by numerical modeling (see § 2.3.2). The initial height of 80 µm corresponds to the solder height after electrodeposition. The AxB metric indicates the size of the pad in unit cells with a pitch of 151 µm in X and Y direction. The width or diameter of the pads is 80 µm.

Solder shape engineering is a key requirement to allow the coexistence of rails and balls with a thick solder thickness on a single chip with a high reflow process yield. Accordingly, the solder rail shape after pre-reflow (the reflow before bonding) was investigated numerically by surface energy minimization methods using the Surface Evolver software (Mathematics Department, Susquehanna University, PA) and is discussed in the first sub-section. In the solder shape engineering section, a solder height modulation strategy is discussed. The shape validation with experimental results will then be depicted and two instability mechanisms will be discussed. Finally in § 2.4.2, thermal performances of bonded chips will be benchmarked.

2.3.2 Surface minimization method

The surface of a liquid with a volume V in the thermodynamic equilibrium is defined by body forces, such as gravity and its surface tension. The dimensionless Bond number Bo can be used to determine the significance of the mentioned forces at a characteristic length scale L. It reads:

$$Bo = \frac{\rho g L^2}{\gamma}, \tag{2.1}$$

with ρ being the fluid density, γ the surface tension of its interface to air, and the gravitational acceleration $g = 9.81$ m/s^2. Surface tension starts dominating at Bond numbers below one. Considering material values for Sn-3.5Ag provided by the National Institute of Standards and Technology (NIST [75]) (ρ = 7’500 kg/m^3, γ = 0.43 N/m) and a characteristic length of 100 µm yields a Bond number of 1.71e-3. This result indicates the diminishing effect of gravitational forces on the solder shape and allows the consideration of surface tension only.

In this study the Surface Evolver software [76] was used to numerically derive the surface shape of solder volumes on different pad geometries. The initial solder shape, representing solder deposited through a thick photoresist by electroforming, is the extrusion of the solder pad with the height H0 and volume V0 (Figure 2.14a). The gradient descent method is used to derive the solder shape with the minimal surface energy E, equivalent to the minimal surface area A for a given volume at constant surface tension according to the following integral:

$$E = \int_A \gamma dA. \tag{2.2}$$

The bottom surface of the solder volume was constrained, representing the wetted pad. The mesh gets refined through the minimization procedure to minimize computational cost (Figure 2.14b).

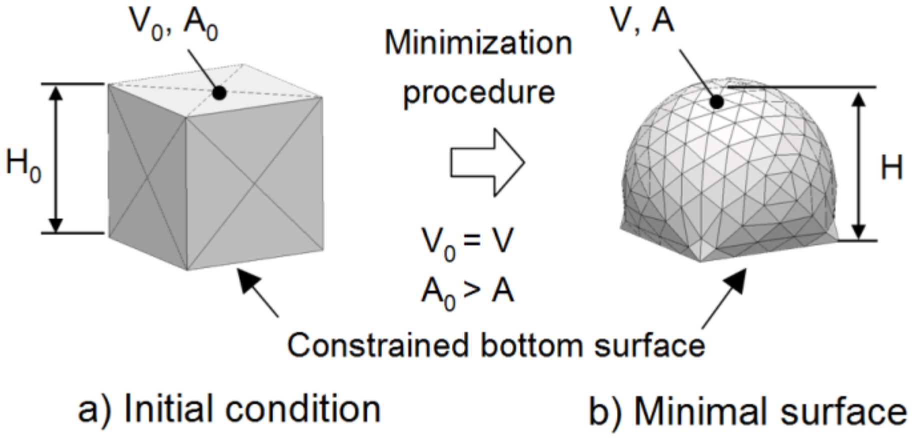


Figure 2.14 (a) Initial volume defined in the Surface Evolver, representing the solder after electroplating. (b) Geometry with minimal surface for a constant volume and constrained bottom surface, considering surface tension only.

2.3.3 Solder shape: engineering the dimensions

With the modeling method at hand, we computed the resulting geometry of solder deposited on one circular and two rectangular pads with a diameter of 80 µm (Ball) and a width to length relation of 80 µm to 382 µm (Rail1) and of 231 µm to 382 µm (Rail2), respectively. The initial height H0 was 80 µm (Figure 2.13). The resulting solder height H and maximal width is depicted in Table 2.1. The final solder height is monotonically increasing with larger solder pad surface. The maximal solder width in case of Rail1 is 48 µm wider compared to its pad and can affect the minimal spacing between two Rail1 structures.

Table 2.1 Initial (after deposition) and final (after reflow) solder shape dimensions considering different pad geometries (Figure 2.13).

Type	Pad width [µm]	Initial height H0 [µm]	Final maximal width [µm]	Final height H [µm]
Ball	80	80	94	74
Rail1	80	80	128	110
Rail2	231	80	237	133

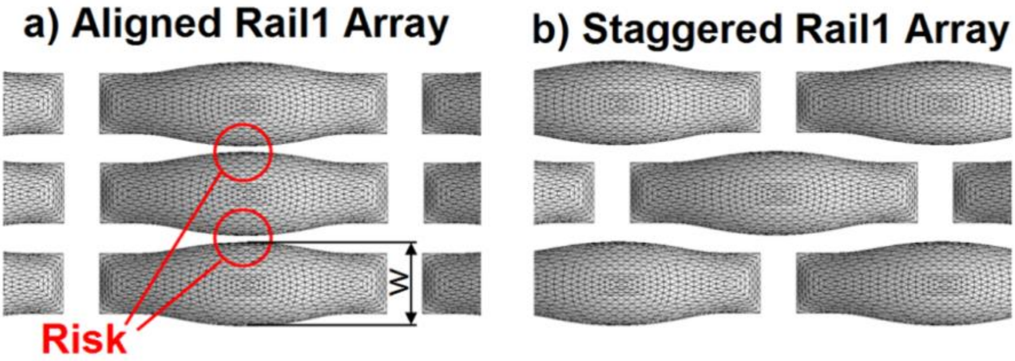


Figure 2.15 Top view of solder arrays with Rail1 unit cells (Figure 2.13) in aligned (a) and staggered (b) arrangement. The minimal distance between rails is 3 times larger in case of (b) with an accordingly reduced shorting risk.

Shorting risk

The arrangement of Rail1 in an aligned array is depicted in Figure 2.15a at a pitch of 140 µm. The maximal solder rail width after reflow is 128 µm and represents a serious shorting risk. Therefore, a staggered rail arrangement (Figure 2.15b) is preferred with a minimal solder distance of 36 µm instead of 12 µm.

Solder Height Engineering

The height difference ΔH of Rail1 compared to the Ball shape for an equal initial solder plating height H0 is positive after reflow, as solder is pulled towards the rail center as depicted in Figure 2.16a. The chip attach yield might suffer considerably considering the coexistence of rails and balls at different heights due to following reasons:

- Temperature difference of solder during reflow resulting in different metallurgy (Rails are in contact with pads while solid).
- Time difference when collapsing might result in different wetting qualities and potential rotation of the die.

- Die might tilt depending on rail / ball array floorplan.
- Increased short / open circuit risk on warped laminate.

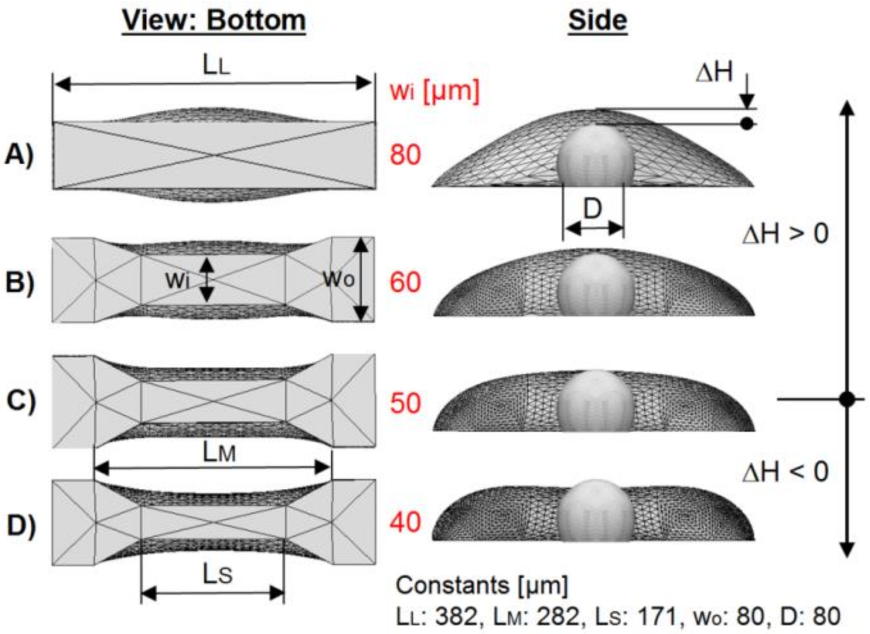


Figure 2.16 Bottom (left) and side (right) view of Bone Rails at varying bone width w_i. The height difference ΔH with respect to a Ball is depicted. The Ball height is smaller in case (a) and (b), but equal for (c). A topology change of the Bone Rail with two maxima can be observed for case (d).

In reality, even larger solder height non-uniformities between Balls and Rails can be expected due to shape dependent deposition rates of the electroplating process [77]. Accordingly, bone-shaped pads (Bone Rail) are proposed to tailor the rail height after reflow at a minimal loss of surface area as depicted in Figure 2.16b to d. Solder is pulled towards the Bone Rail ends at decreasing bone width wi, resulting in reducing rail height which becomes equivalent to the Ball height at a bone width of 50 µm (Figure 2.16c). The topology of the Bone Rail changes at smaller bone widths from a single to a double dome shape surface with two maxima towards the bone ends with width wo, instead of the initial central maxima. From this point on, the solder thickness increases again. In addition, two contact points during wetting might result in void formation and hence, should be excluded.

2.3.4 Modeling vs. experiments

Sample preparation

Chips containing solder bumps and respective carriers with pads were fabricated. The backsides of 525 µm-thick silicon wafers were coated with a 10 nm Titanium and a 100 nm platinum layer using sputter-deposition. The platinum layer will act as a wetting layer for the liquid metal used in the thermal characterization, as described in section §2.4.2. The deposition of lead-free eutectic 3.5Ag-96.5Sn solder with respective Under Bump Metallization (UBM) was performed on the chip wafer front-side by an electroplating process. Initially, a 150 nm-thick Copper seed layer was sputter-deposited onto a 10 nm Titanium layer. The electro deposition of the NiAu UBM (3 µm Ni, 1.2 µm Au) and the eutectic AgSn (bath SOLDERON BP TS 4000) was performed sequentially through a positive photoresist (AZ40XT-11D, AZ Electronic Materials) with 70 µm thickness. Finally, the photoresist was stripped and the seed layer removed by wet chemical etching. A thinner (6.2 µm) photoresist (AZ4662, AZ Electronic Materials) was used in case of the UBM-only deposition on the carrier wafer front-side. The UBM layers and shapes are equivalent to those on the chip side.

Figure 2.17 shows three of the distinct solder structures that were investigated: Rail1, Rail2 and the standard Ball (as described previously). As mentioned earlier, the solder electrodeposition rate proved to be quite dependent on the photoresist opening and on the wafer location, resulting in different plated heights for the structures described in Figure 2.17. The measured average heights for Rail1, Rail2 and the Ball were 58µm, 50µm and 90µm, respectively.

The resulting chips were reflown on a hot-plate at a temperature of 265°C, using water soluble flux. Subsequently, the samples were cleaned to enhance scanning electron microscope (SEM) inspection quality, to determine and quantify solder shape dimensions.

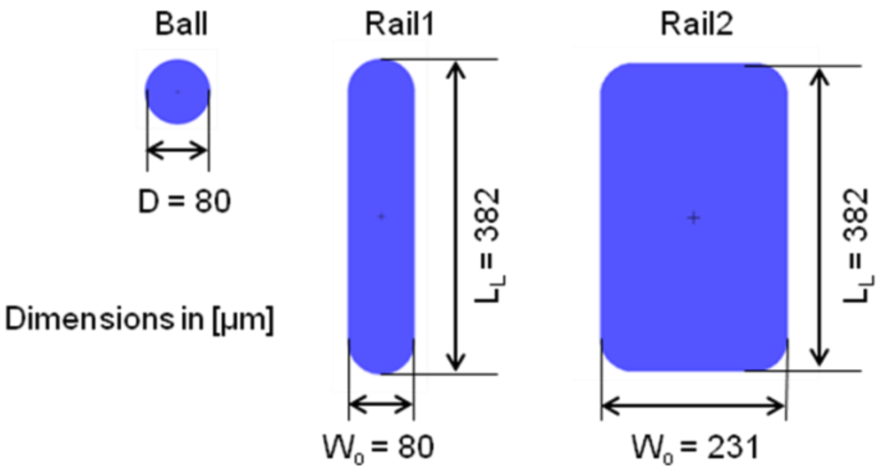


Figure 2.17 Top view of pad and solder geometry for different solder shapes: Ball, Rail1, and Rail2. The patterns were arranged across their respective chips in arrays with a pitch of 151 µm (Ball, Rail1) and 302 µm (Rail2).

Shape comparison after reflow

The resulting solder shape after reflow for Rail1 is compared with numerical predictions (Figure 2.18). Qualitative agreement can be observed for all views (whether looking from the top, side or front). However, the numerical results predict a more significant accumulation of solder in the rail center, with the resulting increased slope in the side view and a pronounced solder width in the rail center (top view).

To quantify the prediction quality, the relative height difference ε_r is calculated as follows:

$$\varepsilon_r: |H_m - H_e|/H_m, \tag{2.3}$$

where H_m is the height computed by the Surface Evolver and H_e is the solder height measured in the SEM. For the Rail1 structure, this value is 3.68%. Table 2.2 displays a similar comparison for the Rail2 and Ball structures. For all cases a prediction uncertainty of less than 9% could be identified, qualifying the numerical modeling approach as a solder shape design tool.

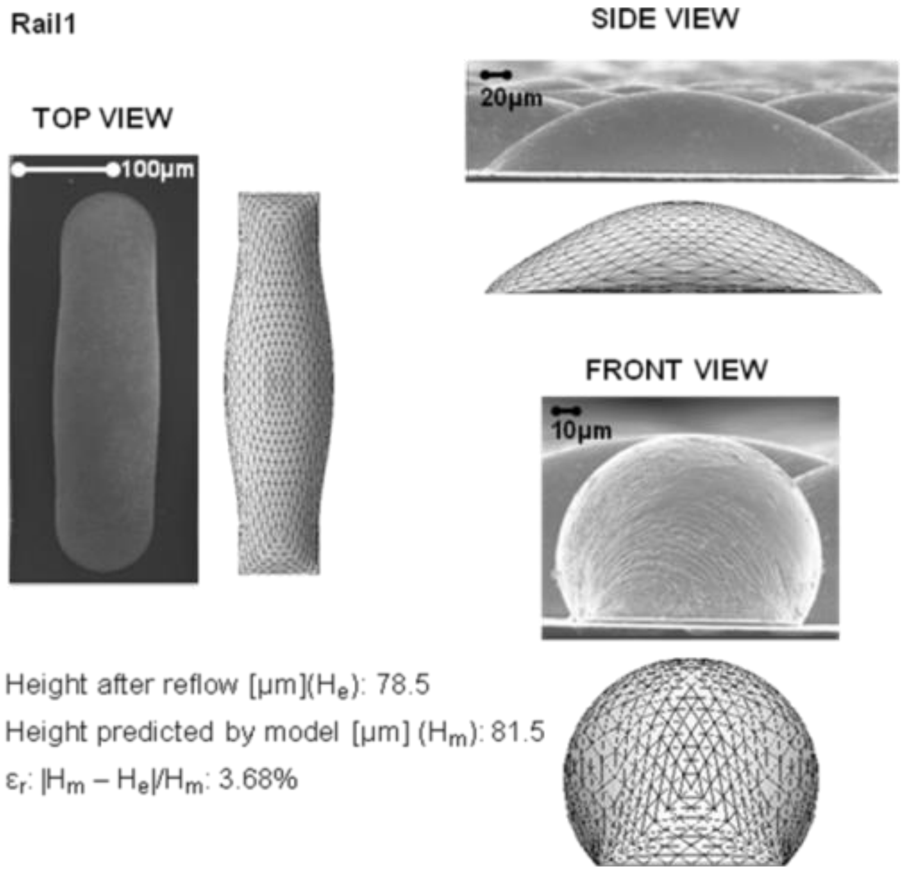

Rail1
SIDE VIEW
TOP VIEW
20µm
100µm
FRONT VIEW
10µm
Height after reflow [µm](H_e): 78.5
Height predicted by model [µm] (H_m): 81.5
ε_r: $|H_m - H_e|/H_m$: 3.68%

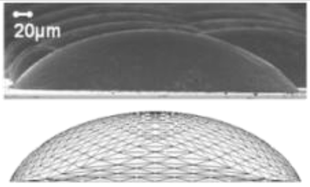
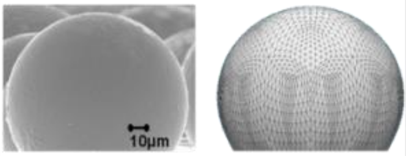
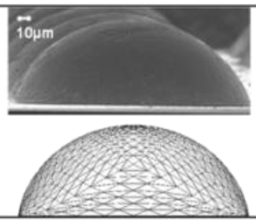
Figure 2.18 Top, side and front view SEM photographs of Rail1 structure after reflow, with their corresponding Surface Evolver model view.

Rail reflow instabilities

Two types of solder rail reflow instabilities, namely Balling and Asymmetric Solder Accumulation were experimentally observed, limiting the design freedom of rails. Therefore, an extended numerical and experimental investigation was performed to derive new design rules.

Balling. Solder was deposited in the form of lengthy rails (2 mm length) with varying widths. The initial solder height was close to uniform for all the lines. After the reflow, dome-shaped rails and rails with local solder accumulation, called Balling, were observed for wide and narrow rails, respectively (Figure 2.19).

Table 2.2 Experimental solder height after reflow (He) versus height prediction by Surface Evolver (Hm), for Rail2 and Ball structures.

	Rail2	Ball
SIDE VIEW		
FRONT VIEW		
HEIGHT (µm)	H_e: 90 H_m: 98 ε_r: $\lvert H_m - H_e \rvert / H_m$: 8.16%	H_e: 89.4 H_m: 95 ε_r: 5.89%

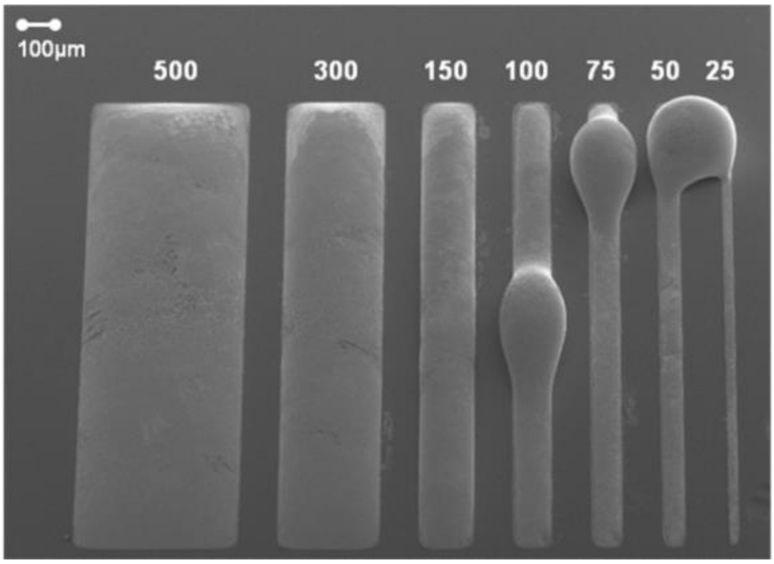


Figure 2.19 SEM photograph of solder reflow shapes of 2 mm long rails with indicated varying widths in [µm], but equal initial solder height of 85 µm. Local solder accumulation, called “Balling”, occurs for lines below a critical line width of 100 µm. Dome-shaped geometries result for wider rails.

Additional samples with varying initial solder heights of 5 µm, 25 µm, and 40 µm as well as varying line widths were fabricated and reflown. The results are presented in Figure 2.20

with the aspect ratio (AR) of the initial solder height H_0 to rail width w_o, versus initial solder height H_0 (deposition height). Full green squares and full red circles indicate dome-shaped rails and rails with Balling, respectively. From these results, a close to constant critical aspect ratio of approximately 0.6 can be extracted. As mentioned in § 2.2.3, an invariant critical aspect ratio for different rail widths can be explained theoretically for infinitely long rails without the influence of gravitational forces (low Bond numbers). In this case the minimal energy state is equivalent to the geometry with the minimal surface area. This geometry is independent of size, but only depends on the AR of the rail cross-section.

Surface Evolver models of rails with a pad length 20 times the width and varying aspect ratios were performed to validate the numerical prediction quality with respect to the Balling instability. Results are shown with empty red circles and empty green squares for rails without and with balling, respectively (Figure 2.20). The predicted critical aspect ratio seems to be in accordance with the experiments.

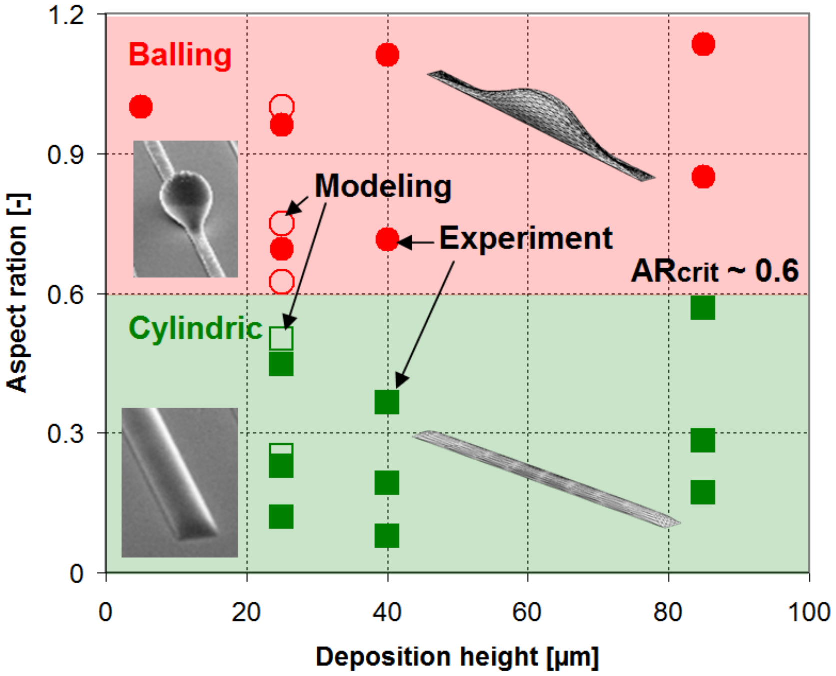


Figure 2.20 Experimental (full) and numerical (empty) categorization of solder shapes after reflow for varying deposition heights H0 and rail aspect ratios (AR) (deposition height H0 to rail width wo). Dome- (green squares) and ball- (red circles) like shapes were identified below and above the critical aspect ratio of 0.6. Inserts depict SEM photographs and Surface Evolver results.

Asymmetric Solder Accumulation. The reflow of Bone Rails with the wider endings towards the bone end resulted in an asymmetric accumulation of solder (Figure 2.21) compared to the numerical prediction (Figure 2.16).

An asymmetric Bow Tie Rail was modeled to investigate the influence of geometrical asymmetries caused from process imperfections, such as limited resolution of thick photoresists or misalignment between UBM and solder. An offset Δ of 10 µm of the lower right corner in X and Y-direction (Figure 2.22a) resulted in the same Asymmetric Solder Accumulation (Figure 2.22b) as observed in the experiment (Figure 2.21). The solder accumulates on the rail end with larger width w_o.

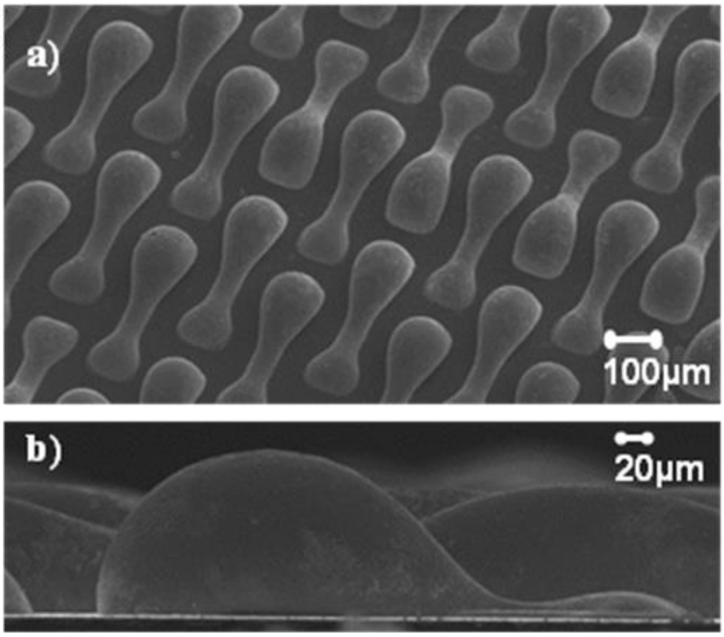


Figure 2.21 Isometric (a) and side-view (b) SEM photographs depicting Asymmetric Solder Accumulation from Bone Rail pads after reflow in comparison with numerical, symmetric results presented in Figure 2.16.

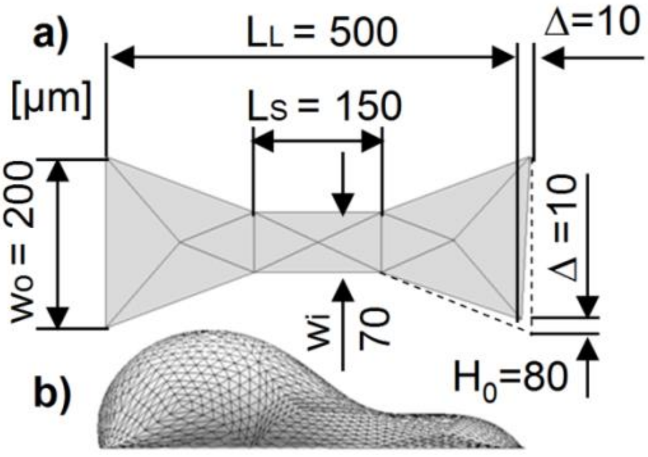


Figure 2.22 (a) Asymmetric Bow Tie rail with an offset Δ of 10 µm of the lower right corner. (b) Modeling result depicting Asymmetric Solder Accumulation as observed in the experiment (Fig. 9) for the pad geometry shown in (a).

The asymmetric solder accumulation instability caused by geometrical imperfections seems to render the proposed solder height engineering approach (Figure 2.16) with Bone Rails impractical. Therefore, a numerical sensitivity analysis of Bow Tie Rails at different w_o to w_i width ratios was performed considering different offsets as depicted in Figure 2.23. Three distinct solder shapes, called phases with the following attributes were identified:

- **Phase 1:** Single local and identical global height maximum
- **Phase 2:** Two very different local height maxima
- **Phase 3:** Two similar local height maxima

The transition between the phases is depicted with the dashed line which is the interpolation of the red data points. To define those points, several surfaces were modeled with constant width ratio, but varying offsets. A point resulted as the average offset value from two distinct phases with minimal offset difference.

The phase diagram allows judging the stability of Bow Tie designs to yield Phase1 with respect to imperfections (offsets). Geometries with a width ratio smaller than three tolerate large offsets. Minimal perturbations yield in Phase 2 at width ratios between five and six. For larger width ratios the solder in the Bow Tie center is drained symmetrically towards the pads.

Some additional modeling results (not shown) indicate a solder height dependence of the phase diagram. Therefore, additional investigations need to be performed. The phase stability should also be validated with reflow experiments of defined asymmetric pads.

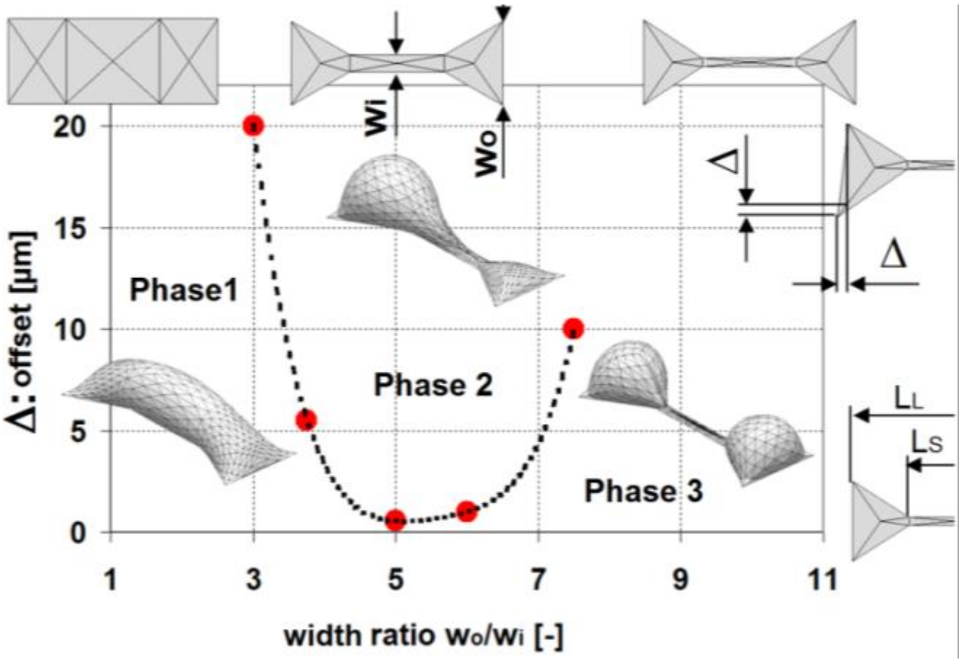


Figure 2.23 Bow Tie Phase diagram depicting three reflow phases in the width ratio to offset plane. The red points and their interpolation (dashed line) were derived numerically and indicate the phase transition. Geometrical representations of the phases are shown as isometric inserts. The pad geometry variation along the different dimensions is depicted as well (Bow Tie dimensions [µm]: L_L: 382, L_S: 171, w_o: 150, H_0: 60).

2.4 Experimental campaign: flip-chip bonding of eutectic 3.5Ag96.5Sn

2.4.1 Thin film micro C4s for 3D chip stacking

Figures 2.24a and 2.24b show a concept for an intra-chip stack thermal management system, developed for the CMOS Advanced Interlayer Cooling consortium (CMOSAIC), whose principal aim is to build a first-of-its-kind package and investigate heat transfer effects in such systems using water as well as refrigerant cooling. The purpose of this particular test vehicle is to demonstrate the feasability of intra chip stack fluidic cooling via two-phase evaporative heat transfer in the multiple evaporators (*E1* to *E4* on Figure 2.24). Fluid delivery into the stack is done through a cover manifold (not shown on Figure 2.24) for which details are given in [55]. The package consists of a chip stack attached to a larger silicon interposer. Five 380µm-thick 10x10mm^2 silicon chips (LV1 to 5, see Figures 2.24a and 2.24b) are flip-chip bonded using thin-layer eutectic solder bonding as interconnects to form the chip stack, as shown on Figure 2.24a. Individual dies were processed on both sides, at wafer-level, with embedded microchannels on their backside for integrated cooling. The fabrication process is described in the following sub-sections, according to Figure 2.25.

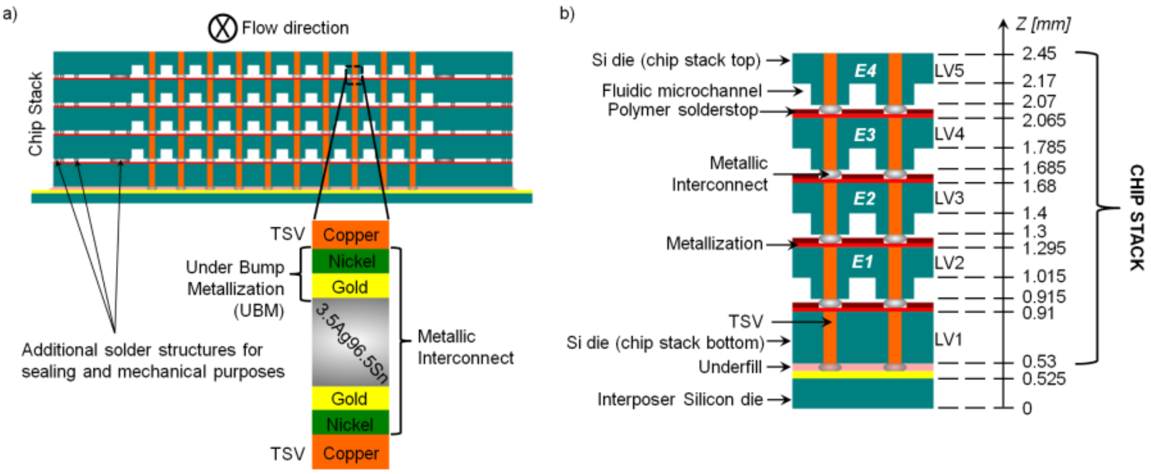

a)
Flow direction
Chip Stack
TSV
Copper
Under Bump Metallization (UBM)
Nickel
Gold
3.5Ag96.5Sn
Metallic Interconnect
Gold
Nickel
TSV
Copper
Additional solder structures for sealing and mechanical purposes
b)
Z [mm]
Si die (chip stack top)
Fluidic microchannel
Polymer solderstop
Metallic Interconnect
Metallization
TSV
Si die (chip stack bottom)
Underfill
Interposer Silicon die
E4
E3
E2
E1
LV5
LV4
LV3
LV2
LV1
2.45
2.17
2.07
2.065
1.785
1.685
1.68
1.4
1.3
1.295
1.015
0.915
0.91
0.53
0.525
0
CHIP STACK

Figure 2.24 Test vehicle description–chip stack package with silicon embedded heat transfer structures. a) Ensemble view of package with all components. b) Vertical cross-section describing the multiple layers and their respective thicknesses.

Sample preparation

Step A: TSVs [78] *and Metallization.* Step A shows the TSV implementation as well as the front side metallization, which can either be the daisy-chain wires (for electrical measurements through the stack) or wires acting as resistive heaters mimicking the power map of a microprocessor in future heat transfer tests.

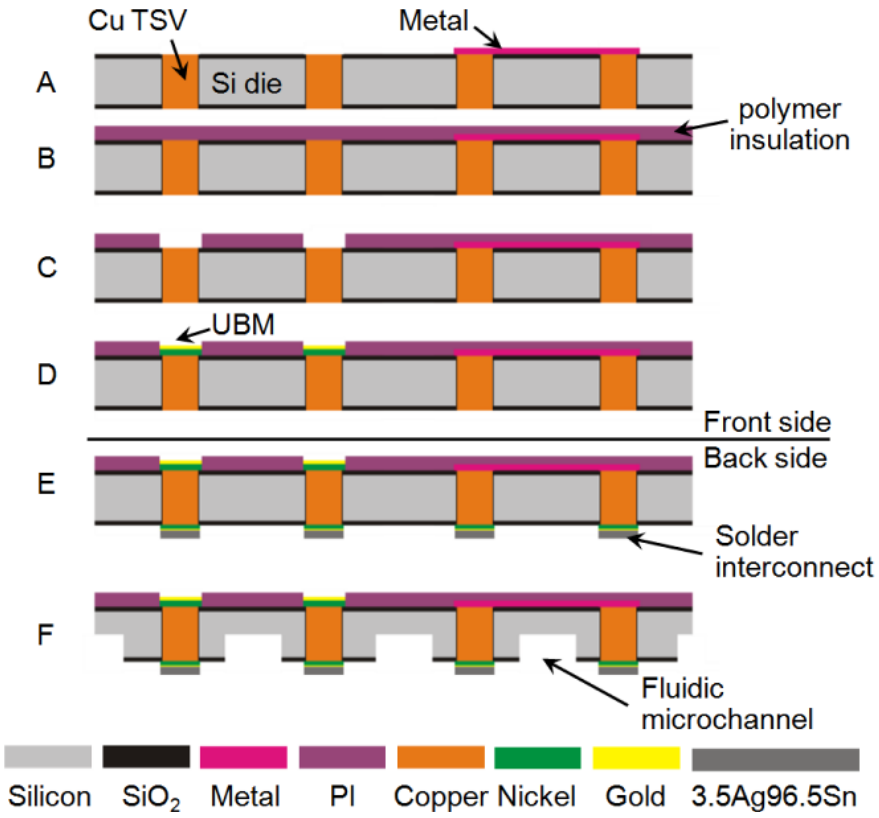


Figure 2.25 Process integration flow for the fabrication of a middle die within the chip stack (LV2 to LV4, see Fig. 1b), after TSV implementation.

380µm tall TSVs were integrated into a double-side polished silicon wafer with equal thickness, to allow the implementation of microchannels with a fin height of 100µm. A rather aggressive aspect ratio (diameter to height) of 1:7 was targeted for the TSVs, setting the TSV diameter to 60µm. The complete fabrication process of the copper TSVs is discussed in [78] and is shown on Figure 2.26a: (1) lithography, (2) silicon etching, (3) wafer cleaning, (4) dielectric coating, (5) seed layer deposition, (6) two-step TSV electroplating, and (7) Chemical Mechanical Planarization (CMP). As discussed in [78], the silicon etching was performed using the Deep Reactive Ion Etching (DRIE) technique to ensure a high etching rate. The notching artifacts at the bottom of the TSVs result from surface charging of the dielectric etch stop and need to be considered in the mask design. Therefore, the TSV diameter on the mask required an offset of 15µm to ensure the desired diameter of 60µm. Finally, the dielectric layer in the TSV was obtained by wet oxidation of the silicon.

The electroplating step was also fine-tuned for this specific design. Before electroplating, the following preparation steps were performed: (1) low power oxygen (O_2) plasma for 1 minute, (2) deionized (DI) water rinse for 30 seconds, (3) 4% sulfuric acid (H_2SO_4) dip for 40 seconds, (4) bath conditioning for 90 seconds, and (5) copper electroplating at 10mA/cm^2 for 30 seconds. The above sequence was used for both electroplating steps (see Figure 2.26b) and their roles were to increase the wettability of the surface, clean the copper oxide from the seed layer and reduce the amount of contaminants, give sufficient time for the bath species to diffuse through the whole TSV length and finally increase the thickness of the seed layer, thus reducing its resistivity and closing any residual small voids.

The electroplating setup was also refined from its original state by adding a diffuser and optimizing the position of the showerhead, thus allowing increased uniformity and coplanarity acroos the electroplated wafer. With the above measures taken the occurrence of bump void defects (BVD) was limited to areas with lithographic/etching defects, due to the higher mass transfer on these locations.

Furthermore, the CMP process was revamped using an in-house slurry that offered increased removal rate. During CMP the temperature was kept below 25°C and the backside pressure was regulated for both faces of the wafer, to ensure homogenous removal on the latter's surface. The backside pressure was regulated at different values, due to the large wafer bowl increase induced by the high stress of the thick copper overburden. Moreover, an additional annealing plus CMP steps might be necessary to induce and mitigate copper pumping.

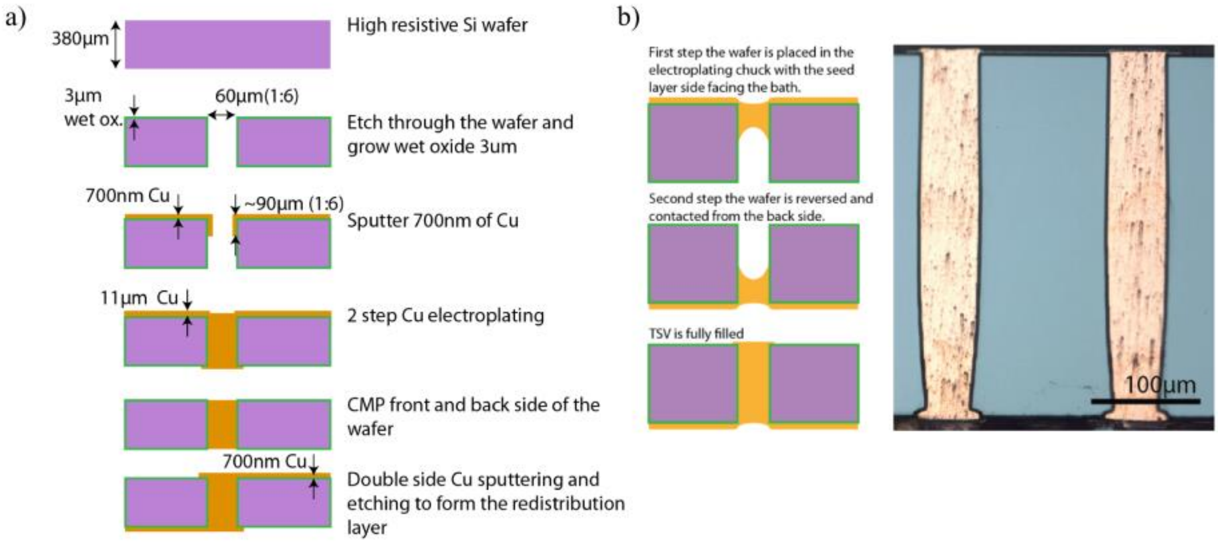

a)
380µm
High resistive Si wafer
3µm
wet ox.
60µm(1:6)
Etch through the wafer and grow wet oxide 3um
700nm Cu
~90µm (1:6)
Sputter 700nm of Cu
11µm Cu
2 step Cu electroplating
CMP front and back side of the wafer
700nm Cu
Double side Cu sputtering and etching to form the redistribution layer
b)
First step the wafer is placed in the electroplating chuck with the seed layer side facing the bath.
Second step the wafer is reversed and contacted from the back side.
TSV is fully filled
100µm

Figure 2.26 a) Illustration of the TSV process flow. b) Illustration of the two-step TSV electroplating process with a cross-section of the reults.

To validate that the TSVs are fully filled and electrically conductive, daisy chain measurements were performed and optical cross sections were examined. Based on the daisy chain measurements, the resistance per TSV could be extrapolated, as shown on Figure 2.27. Most of the TSVs were found to have a lower than 2[Ω] resistance, with an averaged value of 0.7[Ω] for all measured samples. The cross section of the fabricated TSV is presented on the left side of Fig. 3b and shows no major defects.

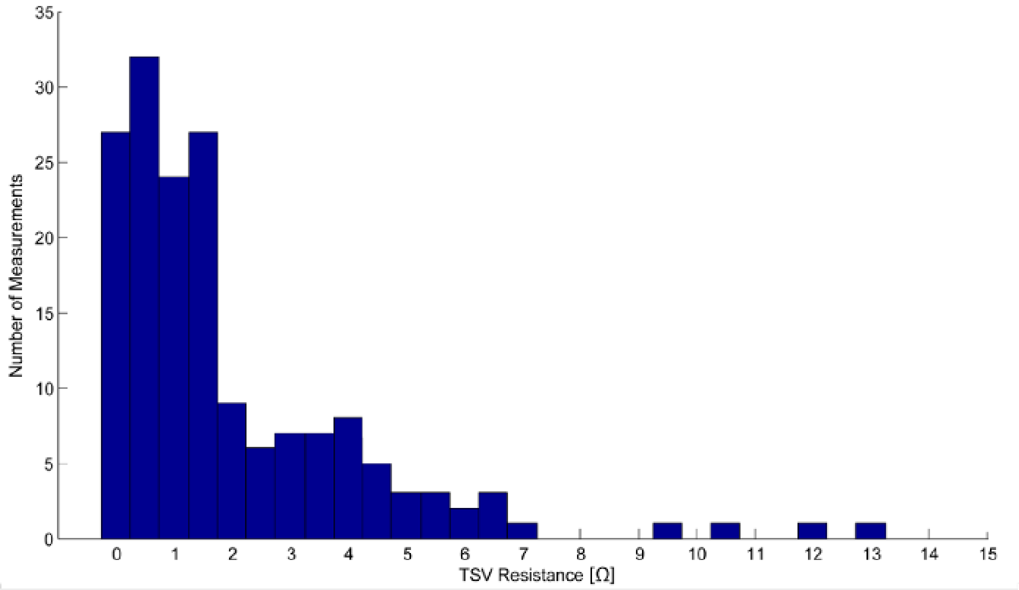


Figure 2.27 Histogram of the calculated TSV resistance. Most of the TSVs have a value below 2Ω.

Finally, the front-side metal layer was sputter-deposited (750nm for copper daisy-chain lines, 250nm aluminum for heaters) directly on top and around the open vias (for LV1 to 4), some of these connecting the pads for the daisy-chain lines or the heaters at each level.

Steps B, C, D. Steps B and C show the spin coating, curing and patterning via a Reactive Ion Etching (RIE) process of a 2µm-thick polymer solderstop layer made of polyimide, preventing electrical shorting after solder reflow on the previously deposited metal lines. The peak temperature reached during curing was 300°C.

In step D the Under Bump Metallization (UBM, 1µm nickel plus 500nm gold) was sequentially deposited on the same wafer side via sputtering on top of the still open vias (for LV1 to 4), thus forming carrier pads and allowing the flip-chip bonding of the superior chips. The UBM shape is equivalent to the one on the solder side (see Step E).

Step E: thin-layer solder interconnects. On the back side of the wafer, solder interconnects with their respective UBM pads were electroplated (58µm in diameter, 2µm-thick nickel, 1µm gold, 12µm eutectic silver tin) for the bonding to the inferior chip (for LV1 to 5). Eutectic 3.5Ag96.5Sn was chosen as lead-free solder. Initially, a 150 nm-thick copper seed layer was sputter-deposited on top of the silicon dioxide. The electro-deposition of the nickel gold UBM and the eutectic AgSn (bath SOLDERON BP TS 4000) was performed sequentially through a positive photoresist (AZ4662, AZ Electronic Materials) with a 15 µm thickness. Finally, the photoresist was stripped and the seed layer removed by wet chemical etching.

Step F: microchannels. Step F shows the formation of the multiple evaporator layers where flow boiling heat transfer will occur within the chip stack (*E1* to *4* on Figure 2.24b). Fifty 100x100µm microchannels were patterned etched on the backside of each chip (for LV2 to 5) via a two-step DRIE process, with the patterning done trough lithography on a thick positive photoresist (AZ Electronic Materials).

Flip-chip bonding

Chip stacks were formed via sequential flip-chip bonding of their multiple dies (LV1 to LV5, Figure 2.24b). The bonding of a chip's solder backside to its corresponding inferior carrier front side was performed by a force-controlled reflow process utilizing a flip-chip bonder (SET FC150).

Initially, the solder on the chip backside was wetted with flux by a stamping process. The chip was then aligned with respect to the pads of the carrier on the inferior chip's front side (planar plus parallelism alignment). After touchdown between chip solder and carrier, the joining by force-controlled reflow is performed according to the force and temperature profiles presented in Figure 2.28. The force profile is imposed through the upper arm of the flip-chip bonder. The temperature profile is applied to both arm and bottom chuck, meaning to the chip and carrier. The process starts by ramp heating between ambient conditions and 150°C in 2 minutes (1.15°C/ sec), at which temperature the flux is activated. After a 15 seconds step, linear heating is resumed until 265°C in 100 seconds. The 12.6 [N] (0.6g/ pad) force was applied while the sample was at 150°C, still below the liquidus point of the solder. Once at 265°C, a 30 seconds dwell time was applied. The process resumes by cooling down both chip and carrier to room temperature.

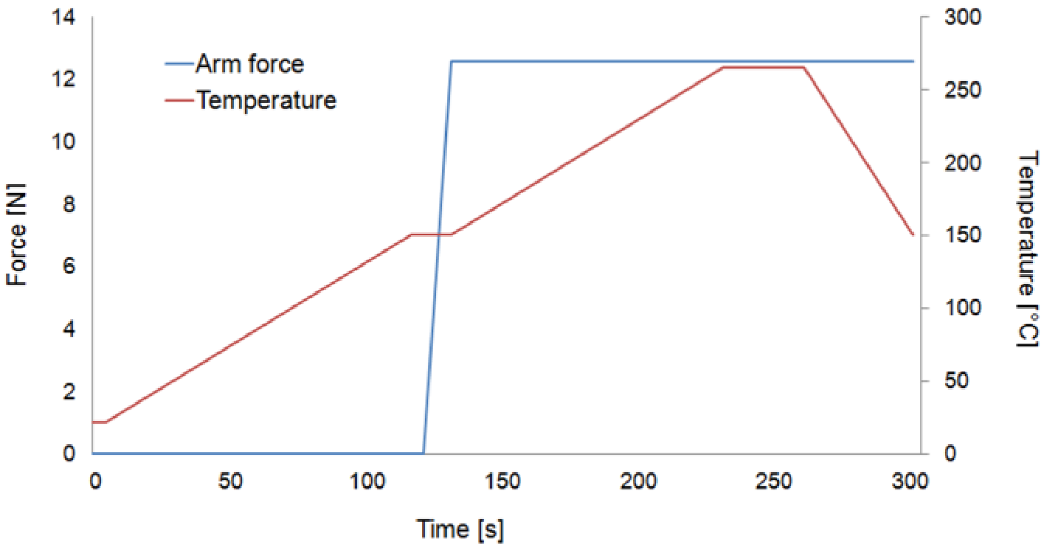


Figure 2.28 Flip chip bonding (force-controlled reflow) process used for die-to-die bonding and chip stacking. In blue: force control. In red: temperature control for both chip and carrier side.

Finally, this same bonding method was also used to manufacture die-on-die samples for electrical and mechanical tests (see below).

Visual inspection

SEM photographs on Figures 2.29, 2.30 and 2.31 show the successfully assembled chip stack, with the die-embedded microchannels and the formed thin solder bond line between the TSVs. The concave shape of the solder joint seen on Figure 2.29d insures that the solder was not squished during bonding, which can be a concern at such thin solder depositions. Cross-sectional SEM pictures (Figure 2.30) depict constant thicknesses of the formed solder joints and the proper alignement of TSVs within the chip stack. Additionally, the X-ray tomography photographs shown on Figure 2.31 demonstrate the thin film solder interconnect floorplan as well the proper filling and aligment of the TSVs.

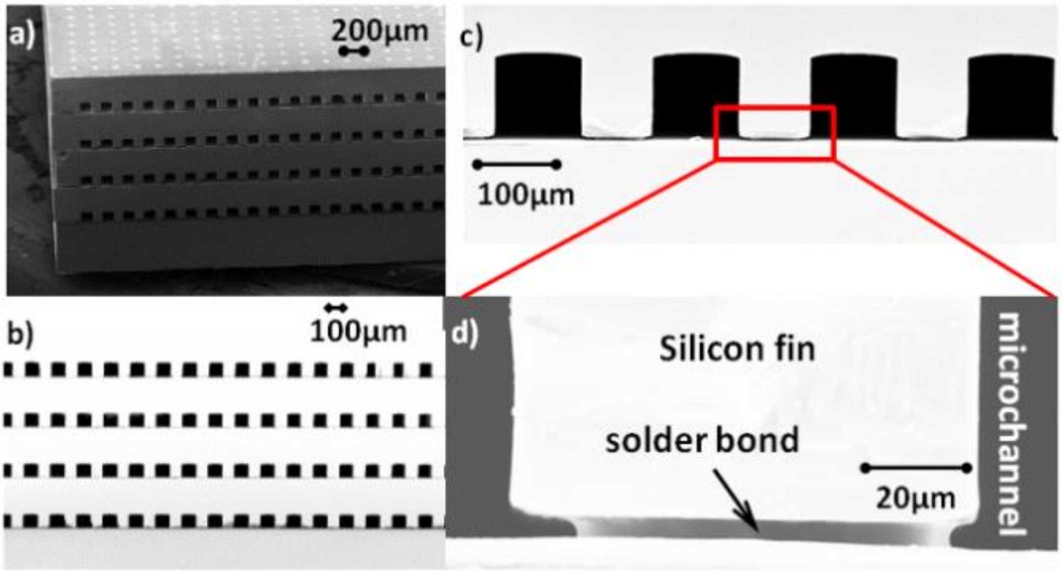


Figure 2.29 a) Isometric view of a 5-layer chip stack (4 fluid cavities, 4 active layers with TSVs). b) Front view of 100X100µm fluidic microchannels. c) Zoom-in on cavities, fin thickness is 100µm. d) View of the die-to-die thin-layer eutectic solder bond (5µm), the silicon fin as well as the fluidic microchannel.

Electrical characterization

Madhour et al. [55] calculated the resistance of the same thin-layer AgSn solder bond to be between 1 and 5 [mΩ] via direct current (DC) daisy-chain measurements that spun from 6 to 94 active pads between two solder bonded silicon dies (without TSVs). The same daisy-chain structure was used here to measure the combination of TSVs and thin solder pads, by preparing die-on-die solder bonded samples assembled via the process previously described (bottom die = carrier = 10x10mm^2, top die = chip = 9.5x10mm^2). The top die was an LV2 chip (Figure 2.24b) and the bottom die was a simple silicon 525µm-thick carrier. 4-point Kelvin resistive measurements on a manual probe station showed that an electrical connection was made after bonding and that the linear increase in the number of active pads from line to line was matched by the linear increase in line resistance.

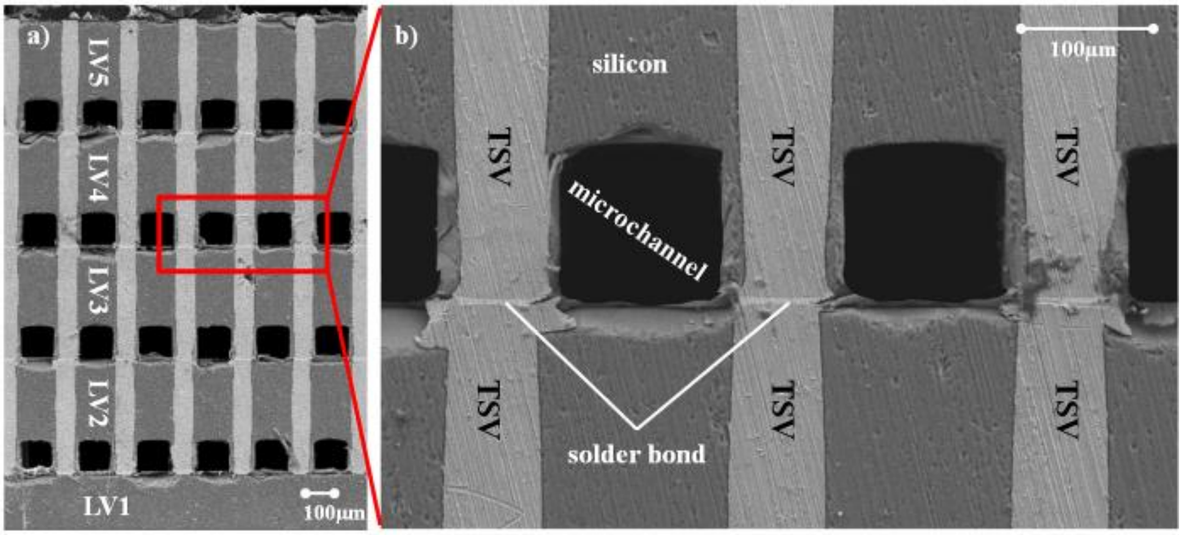


Figure 2.30 a) Cross-section of the assembled chip stack. The LV1 to LV5 chips, the microchannels, the TSVs as well as the thin-layer solder bonds are all visible. b) Zoom-in on microchannels, TSVs and solder pads.

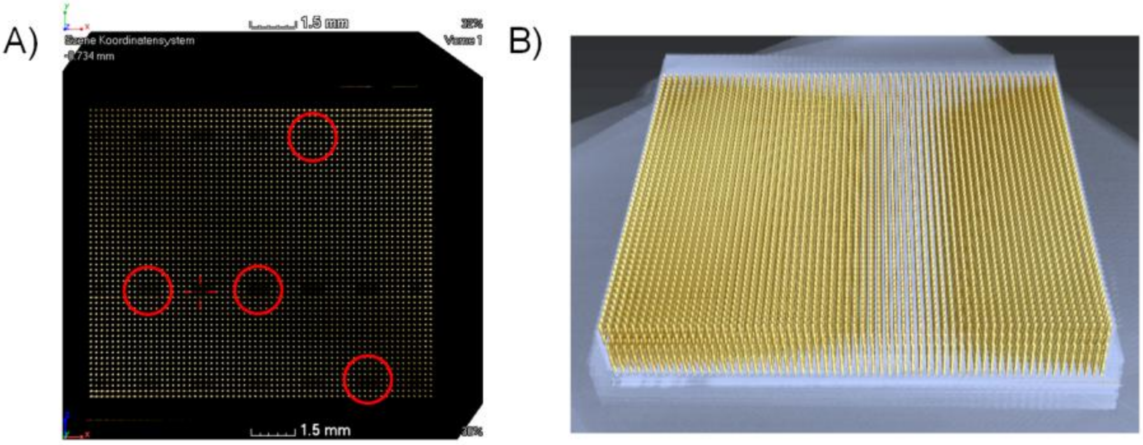


Figure 2.31 X-ray tomography pictures on a fabricated chip stack. A) 2D top view of LV2 chip surface, showing uniform presence of solder interconnects. Highlighted “missing spots” are the locations of the hot spot heaters’ electrical leads (design presented in § 3.2). B) 3D top view of chip stack showing the properly filled TSVs. Due to (already impressive) 8µm resolution, thin film solder interconnects are not visible. **The author would like to thank Prof. Dr. Bernhard Wunderle (TU Chemnitz, Germany) as well as Marcus Hildebrandt (Fraunhofer ENAS, Germany) for their tremendous help in obtaining these photographs.**

Figure 2.32a shows the schematic of the 4-point measurement used to determine the resistance of a single TSV plus solder pad combination. Figure 2.32b shows the results of said measurement, showing that the resistance varies between 0.6 and 1.8 [Ω], which is within the uncertainty of the TSV resistance values (Figure 2.27).

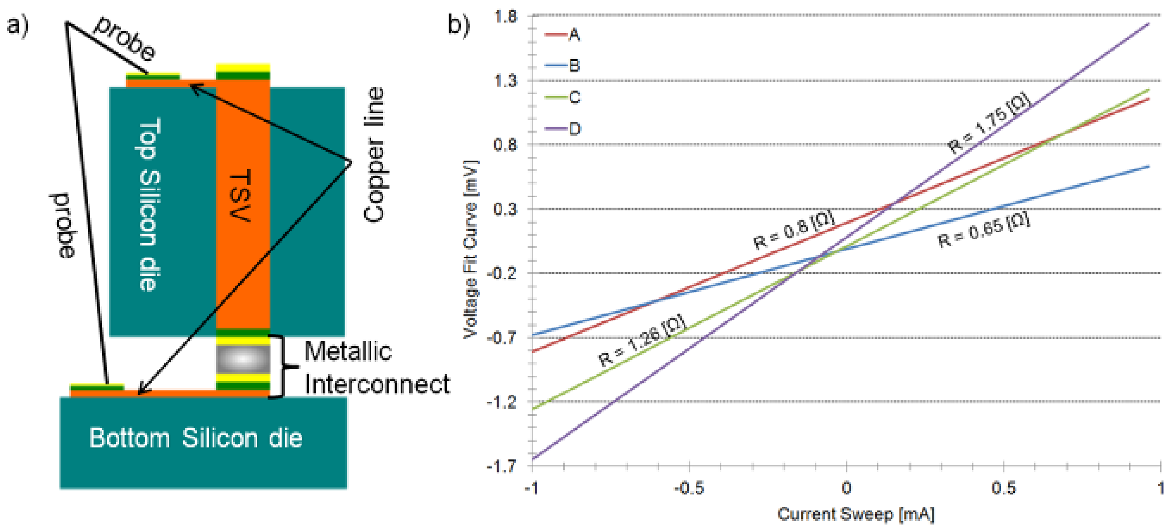


Figure 2.32 a) Schematic of the 4-point DC Kelvin measurement for a single TSV plus thin-layer solder pad combination. b) DC current sweep (-1 [mA] to 1 [mA]) with corresponding voltage response to determine the resistance of a single TSV plus thin-layer solder pad combination. A and B as well as C and D designate similar daisy-chain locations measured on different samples and are representative values.

Mechanical Characterization

Mechanical shear tests. To evaluate the mechanical integrity of the stack, the previously described electrically measured die-on-die samples underwent mechanical testing. The bonding method of thin film solder joints limits the choice of structural testing to post-bond testing. Thus, die shear testing was carried out with a dedicated test setup. Because the applied critical load scales with the number of bonds per die, the shear setup ideally measures the load reaction in-line with the loading movement. For this purpose, we used a SELmaxi load frame (Thelkin AG, dual column tension and compression tester [79]) and mounted the samples vertically in-line with the load axis, as Fig. 2.33 demonstrates.

One of the two dies rests in a pocket that forms a dead stop against the load axis. The other die is only constrained in the out of plane translation and rotation (*x* and rotation around *y*) using a dedicated bearing and sample holder fixed in a vise. Figure 2.34 shows the load chisel that applies the shear load on the entire width of the die by displacing the same die vertically relative to the bonded die in the pocket. The chisel clamping allows a rotational alignment around the *z*-axis for an optimal load line.

To monitor the sample reaction, a displacement controlled shear speed of 10µm/second was chosen, which is a factor of 10 below standard JEDEC [80] low speed ball shear testing of 100 to 800µm/sec. Each shear test stopped prior to half bond pitch displacement. This avoided collisions of neighboring bonds for clear post-shear imaging. Two different aspects of this mechanical loading were of interest: the load reaction giving the bond's shear strength, and the way the bond separates, the failure mode. Figure 2.35 shows the load reactions, and the resulting shear strength values. Table 2.3 summarizes the results.

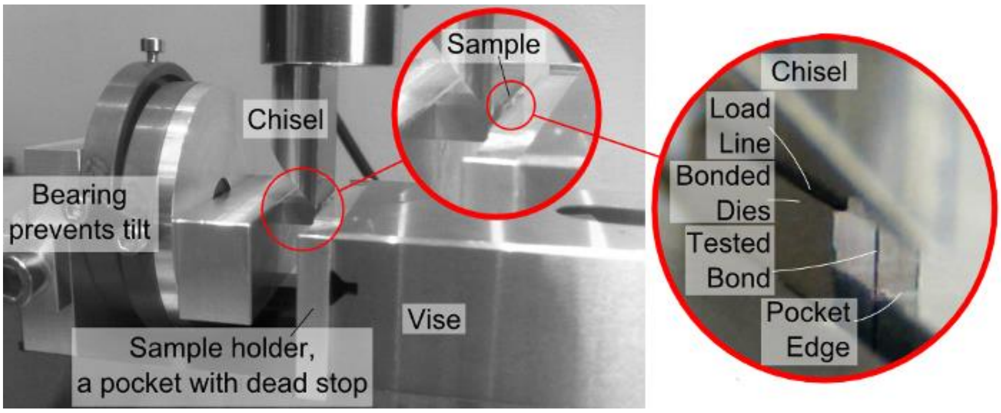

Sample
Chisel
Bearing prevents tilt
Vise
Sample holder, a pocket with dead stop
Chisel
Load Line
Bonded Dies
Tested Bond
Pocket Edge

Figure 2.33 Setup to shear test the thin-layer solder bonds.

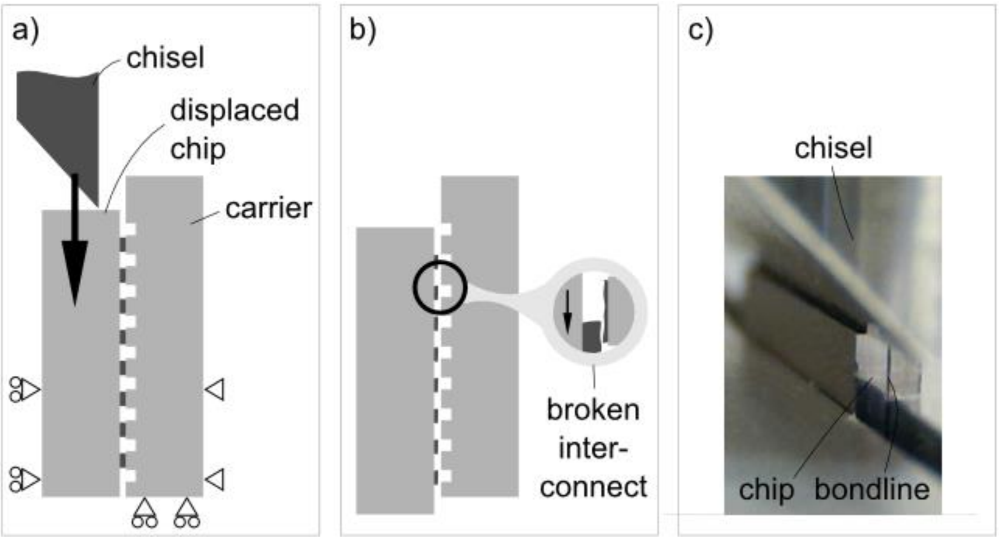

a)
chisel
displaced chip
carrier
b)
broken inter-connect
c)
chisel
chip
bondline

Figure 2.34 a) Shear principle. b) Sheared state. c) Corresponding photo.

Although other experiments have shown that the onset of shear failure can occur before the maximum load reaction [81], usually the maximum force reading is used for the shear strength calculation. The crucial detail is to which sheared area the force relates to. The calculation was based on the full pad diameter of 58µm of all 2156 sheared bonds per die and used the average obtained maximum force value. The strength of the flux-assisted bonds is more than twofold higher (16MPa) than the bonds formed without flux (7MPa).

While assuming that all bonds break at the very same displacement generally overpredicts the shear strength, the assumption of the full pad area being sheared instantly underpredicts the shear strength value. Figure 2.36 shows the typical failure modes observed.

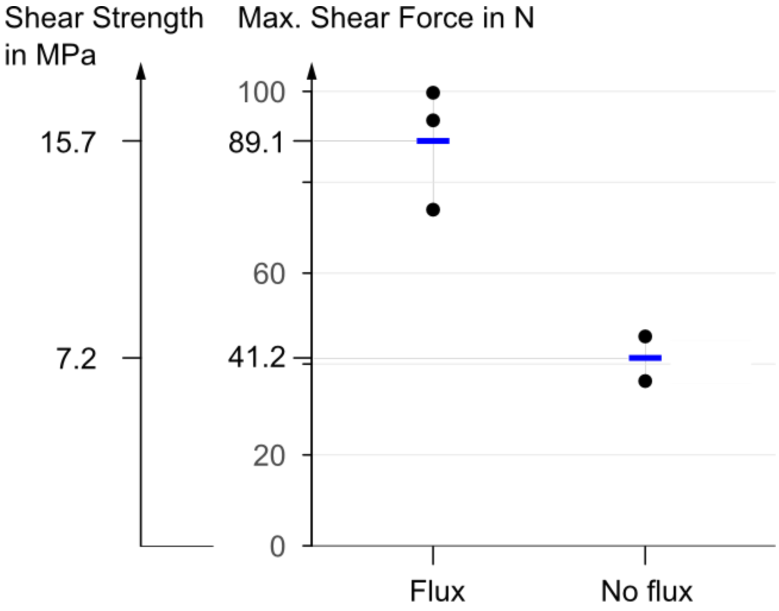


Figure 2.35 Shear test results.

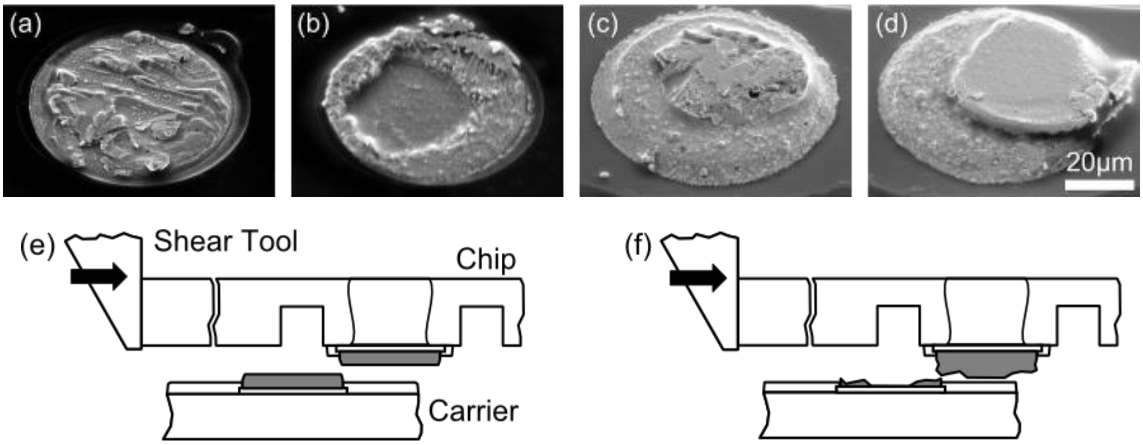


Figure 2.36 Failure modes observed across the sheared carrier and chip (left to right). a) Ductile through solder (carrier side). b) Partial solder lift (carrier side). c) Ductile through solder (chip side). d) Partial solder lift (chip side). All pad diameters are equal to 58µm. The schematics (e) and (f) describe the failure mode principle for each, ductile and partial solder lift.

Table 2.3 Shear test results.

Bond type	Die-on-die solder bond shear tests – averaged values		
	Critical Force [N]	Area [mm2]	Total Stress [MPa]
Flux	89.1	5.7	15.7
No Flux	41.2	5.7	7.2

All bonds separated either within the solder bulk material, or partly at the pad-to-solder interface (Figure 2.37). None of the bonds showed any lifted pads, or cracks kinking into the substrate. Also channels and TSVs remained intact.

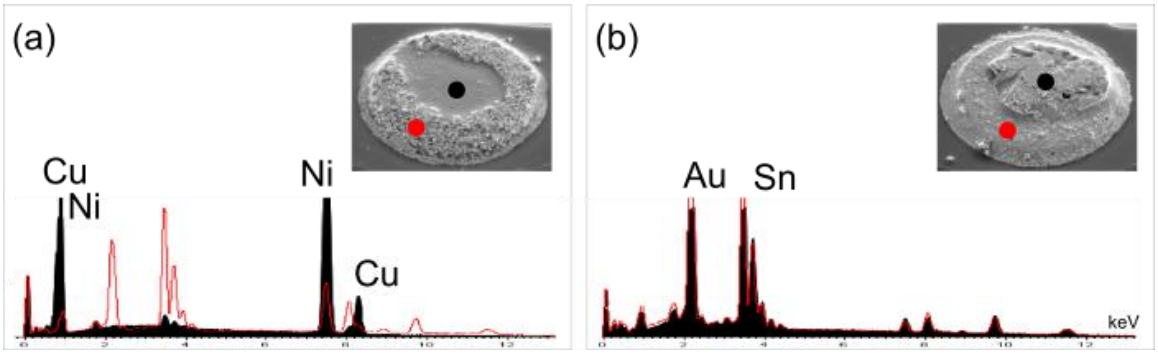


Figure 2.37 EDX results of the different regions left behind after shearing: the partial solder lift (a) shows a clean separation between the solder components and the pad UBM metallization.

2.4.2 Thermal resistance of high fill factor structures

Chip to carrier bonding

The bonding of the solder chips described in §2.3.4 to their respective carriers was performed by a reflow process utilizing a flip-chip bonder (SET FC150). Initially, the solder of the chip was wetted with flux by a stamping process. The chip is then aligned with respect to the pads of the carrier. Both chip and carrier dimensions were equal to 10x10mm^2. The chip is released from the top chuck after its placement on the carrier. The joining by reflow is performed at a chuck temperature of 265°C (Figure 2.38). Resulting bond-line heights for the various pad types are depicted in Table 2.4.

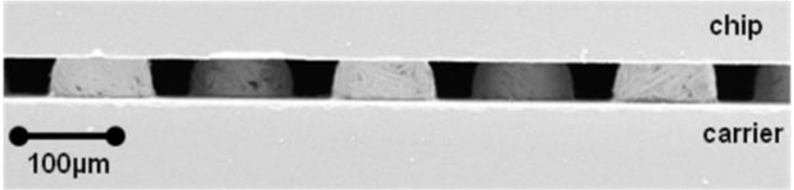


Figure 2.38 Front view SEM micrograph of a flip-chip bonded device using Rail1 structures.

Table 2.4 Average initial solder height H0, average final bond-line height and bond-line thermal resistance for different solder joint types.

Type	Initial height H0 [µm]	Bond-line height [µm]	Bond-line thermal resistance [K*mm2/W]
Ball	90	73	23.5 +1.7/ -1.1
Rail1	58	42	3.2 +7.6/ -4.1
Rail2	50	43	3.2 +8.1/-4.4

Thermal resistance measurements

Thermal bond-line measurements were performed to demonstrate the superiority of solder rails compared to balls with respect to efficient heat removal from within a chip stack or from chip to laminate.

Bulk thermal resistance characterization method. The thermal conductivity of the solder interconnects (bond-line) was measured from the 10 x 10 mm^2 flip-chip bonded samples. The measurement device is illustrated in Figure 2.39. The device consists of two copper studs, equipped with thermocouples, a heater and cooling blocks on top and below the copper studs [71]. The copper studs homogenize the non-uniform heat flow of the resistor to allow the consideration of a one-dimensional heat flux in the subsequent calculation. The equidistant positioning of the thermocouples in combination with the copper thermal conductivity allows the determination of the heat flux and the copper stud surface temperature. The cold plate finally acts as a heat sink. The surfaces of the studs and the specimen are wetted with liquid metal (InGaSn, Indalloy 51, Indium Corp.) prior to the placement of the specimen between the studs, in order to achieve a predictable and low thermal impedance interface. Therefore, the specimen back-side was coated with a wetting layer as described earlier. The thermal resistance of the liquid metal interface is defined in advance with measurements of bulk silicon samples of known thermal conductivity and thickness.

The thermal resistance R_{th} of the specimen and liquid metal interface is determined via the temperature gradient from the top to the bottom copper surface at a given heat flux. The thermal resistance of the solder interface $R_{interface}$ is calculated by subtracting the thermal resistances of the silicon chips and liquid metal interfaces from R_{th} ($R_{interface} = R_{th} - 2\cdot R_{Liq.\ metal} - 2\cdot R_{si}$). In order to compare the results of solder interconnect types with varying bond-line heights, an effective thermal conductivity value ($k_{eff} = H_{interface}/R_{interface}$) is calculated from the extracted thermal resistance. It should be mentioned, that k_{eff} contains the constriction and spreading resistance in the silicon and the heat transfer through the UBM, in addition to the thermal resistance of the solder shape.

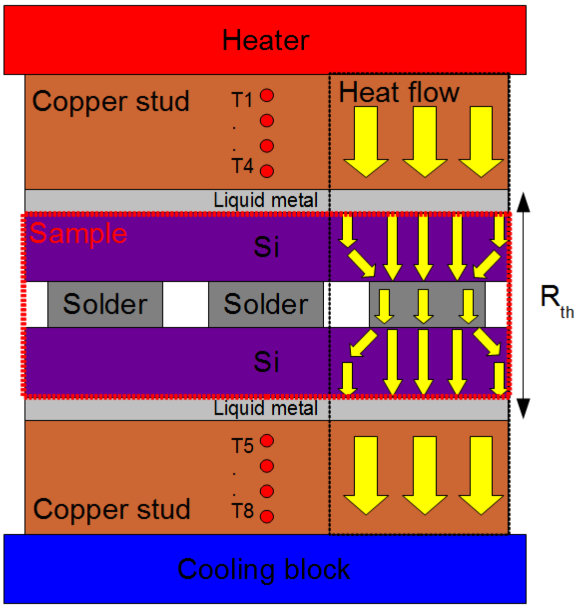


Figure 2.39 Illustration of the bulk thermal tester. Heat is dissipated uniformly from the top copper stud into the specimen and finally out of the bottom copper stud. Thermal coupling from copper into the specimen is performed by a liquid metal interface. Temperature gradients are monitored with two pairs of four thermocouples to derive the copper stud surface temperature and the dissipated heat flux. The liquid metal interface resistance was determined in an upfront measurement.

Main contributors to the thermal resistance measurement uncertainty of the setup are the estimated temperature measurement accuracy (± 0.05 K), accuracy of the solder interface height measurement (±2.5µm) and the variation in the liquid metal thermal interface resistance $R_{Liq.\ Metal}$ of 1 ± 0.5 Kmm^2/W.

Bond-line thermal resistance. The measured $R_{interface}$ and the corresponding k_{eff} values for multiple samples with Rail1 (R1), Rail2 (R2) and Ball solder interconnects are listed in Table 2.4 and are plotted in Figure 2.40, respectively. In addition, theoretical k_{eff} values for the interface were calculated for varying solder area fill factors, based on the effective thermal conductivity of solder derived by Matsumoto et al. [71] (18-24 W/m-K).

As expected, the thermal resistance of the rail interfaces is substantially lower than that of the ball array. The rail $R_{interface}$ values are actually close to the inherent measurement uncertainty of the setup and result in large error bars and differences between samples of the same rail type in the k_{eff} graph. Nevertheless, the measured values follow the expected trend and are close to the predicted values of theoretical k_{eff}. In order to characterize the thermal performance of the solder joints more accurately, the measurement setup needs to be improved and more samples need to be measured.

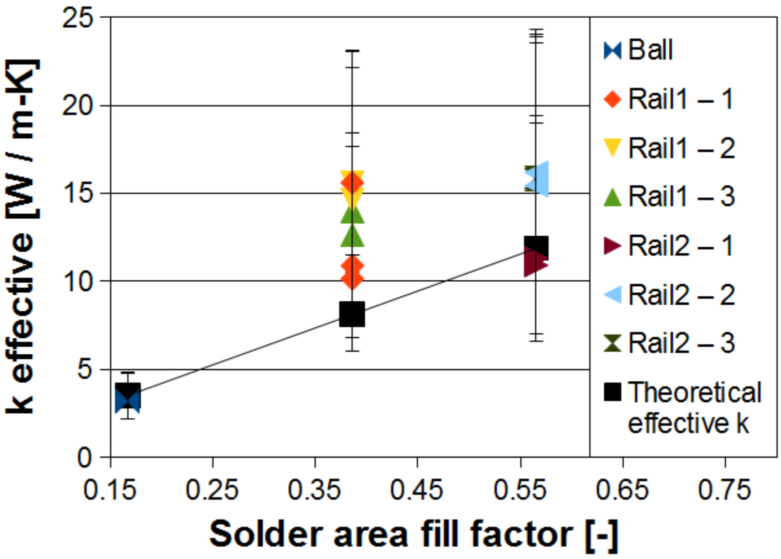


Figure 2.40 Resulting bond-line effective thermal conductivity k_{eff} of the Ball, Rail1 and Rail2 specimens at their solder area fill factor. Three different specimens were characterized and compared in case of the rail shapes. The trend of the measured results is compared with theoretical values derived from effective solder thermal conductivities, published in [71], and the solder area fill factors.

2.5 Conclusions

A new concept for a high performance chip stack with integrated cooling, high TSV aspect ratio and thin-layer patterned solder bonding was introduced. The design, fabrication and integration of the different elements were discussed, and the assembly via sequential solder flip-chip bonding of the multiple dies was presented.

SEM photographs of a 5-layer chip stack and its corresponding cross-sections after assembly via flip-chip bonding showed the proper formation of the thin solder bond line (shape) between the multiple dies and its repeatable thickness (5µm ±1µm). Daisy-chain measurements on die-on-die samples showed successful electrical conductivity after solder bonding and allowed the resistance determination of a single TSV combined with a thin-layer solder pad. Results varied between 0.6 and 1.8 [Ω], which is within the uncertainty of the individual TSV resistance values (between 0.7 and 2[Ω]).

Shear tests were performed on die-on-die bonded samples to determine the stack's mechanical integrity. It was observed that the strength of the flux-assisted solder bonds was more than twofold higher (16MPa) than the bonds formed without flux (7MPa). Additionally, failure modes were identified. All bonds separated either within the solder bulk material, or partly at the pad-to-solder interface. None of the bonds showed any lifted pads, or cracks within the substrate. Also, channels and TSVs remained intact after the destructive tests.

Finally a new ring-pad design was presented, compatible with the patterned thin-layer solder technique, to seal the electrically active pad covering the TSV from the liquid coolant with a solder ring structure, should the cooling medium be water. A parametric reflow study on such solder geometries showed the appearance of a balling effect along the ring line and it seemed that the narrow solder ring pads demonstrated that effect the most, compared to the wider ones which yield in uniform dome-shapes. This balling can be mitigated when the ring aspect ratio (deposited solder height to ring width ratio) is kept below the experimentally observed critical value of 0.65.

Thick rail solder shapes were experimentally demonstrated, resulting in a three times improved solder area fill factor compared to solder balls, supporting efficient heat transfer and power delivery from within 3D chip stacks or chip to laminate. The experimental investigation was complemented with numerical modeling using the Surface Evolver software. A reflow shape prediction quality of less than 9% could be identified.

Solder height engineering using bone shaped pads was demonstrated as an efficient means to yield uniform solder heights for balls and rails enabling their coexistence, for high pin count signaling and high current density power delivery, respectively. However, two types of solder reflow instabilities were identified: balling and asymmetric solder accumulation.

Nevertheless, an improved solder interface with an effective thermal conductivity increase of up to four times could be demonstrated from solder balls to rails.

The following design rules should be considered to yield robust rail designs:

- A staggered rail arrangement maximizes the minimal spacing between rails and therefore their shorting risk.
- Bone Rails with a 50 µm bone width w_i and 80 µm pad width w_o result in equal ball (pad diameter 80 µm) and rail height.
- The plated solder height to width ratio needs to stay below approximately 0.6 to prevent Balling on long rails.
- The width ratio modulation of Bow Tie Rails needs to stay below three to prevent Asymmetric Solder Accumulation induced by expected fabrication imperfections.

Chapter 3 Intra chip stack dielectric evaporative flow

3.1 Experimental investigation: 2D silicon pin fin test vehicle

Rather than the 3D test section described in Chapter 2 (whose electrical contacts failed during the first set of thermal experiments, see §3.2), the following 2D pin-fin test section was tested. Its results are presented in section 3.1 while those obtained for the 3D test section before its failure are then presented in section 3.2.

The work of chapter 3.1 is partially sponsored by Defense Advanced Research Projects Agency, Microsystems Technology Office (MTO), under contract no. ***HR0011-12-C-0035***. The views expressed are those of the author and do not reflect the official policy or position of the Department of Defense or the U.S. Government.

For the sake of simplicity, this chapter will be introduced with its own nomenclature.

3.1.1 Nomenclature

α_b	footprint heat transfer coefficient [W/m^{2}K]
A	cross-sectional flow area [m^2]
B	pin fins footprint width [m]
$c_{p,l}$	specific heat capacity, liquid phase [J/kgK]
$c_{p,v}$	specific heat capacity, vapor phase [J/kgK]
G	mass flux [kg/m^{2}s]
h_{lv}	latent heat of vaporization [J/kg]
IR	InfraRed
I	current [A]
k_{Si}	thermal conductivity [W/mK]
P_{adb}	measured pressure before the outlet plenum [kPa]

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P_{inlet}	measured inlet plenum pressure [kPa]
P_{ori}	measured pressure after the inlet orifice [kPa]
P_{outlet}	measured outlet plenum pressure [kPa]
$p(z)$	local pressure along the flow path (single- or two-phase flow) [kPa]
q_b	background heater heat flux [W/m^2]
RTDin	resistive thermal detector inside inlet plenum
RTDout	resistive thermal detector inside outlet plenum
t_{Si}	silicon chip thickness [m]
$T_{base, fin}$	calculated Silicon pin fin wall temperature [°C]
$T_{c,inlet}$	measured inlet temperature polycarbonate block [°C]
$T_{c,outlet}$	measured outlet temperature polycarbonate block [°C]
T_{fl}	calculated fluid temperature along flow path (single- or two-phase flow) [°C]
T_{sat}	refrigerant saturation temperature [°C]
$T_{surface}$	Infrared-measured chip surface temperatures [°C]
U	voltage [V]
x	vapor quality [-]
y	direction perpendicular to the flow, local along y
z	direction along the flow path, local along z

3.1.2 Introduction

In order to correctly implement novel electrically and mechanically viable concepts that allow the removal of high heat fluxes and thermal management of hot spots within a three-dimensionally arranged stack of silicon chips using dielectric evaporative cooling, initial experiments have to be performed on individual chips. With this approach trends in flow distribution, flow patterns, as well as pressure drop and Heat Transfer Coefficient (HTC), all important aspects of dielectric evaporative flow, can be identified and optimized, in addition to allowing design modifications to a subsequent implementation of these concepts in a 3D chip stack. The test section described below was recently designed and tested in that respect. The initial results are shown in the following.

3.1.3 Test section

The experimental test section is a package (Figure 3.1) consisting of a test chip, a fluid manifold and a Printed Circuit Board (PCB) (Figure 3.1A, B, C). A single 14x14mm^2 silicon chip that was anodically bonded to an equally-sized borofloat glass die formed the test chip. This silicon chip (525 µm-thick, ± 25 µm) was double-side processed at wafer-level, as shown on Figure 3.2. On its front side facing up, a 200nm-thick Nickel Chromium (NiCr) background (BG) surface heater (9.6mm x 9.65mm) was sputter-deposited on a 300nm silicon dioxide (SiO_2) layer with a 10nm Titanium (Ti) adhesion layer. A 300nm Platinum (Pt) serpentine Resistive Thermal Detector (RTD) complemented the heater via the same deposition procedure (Figure 3.3A & B). Additional features were possible (shown on Figure 3.2), allowing the simultaneous use of a BG heater as well as a hot spot (HS) heater for enhanced thermal experiments. In order to do that, a 1µm Silicon Nitride (Si_xNi_x) and 50nm Aluminum Oxide (Al_2O_3) insulation layer could be added to electrically and thermally isolate the BG and HS heaters. The HS heaters would be of the same metallic composition as the BG heater, only with smaller dimensions to accommodate their numbers and floorplan distribution. These additional features were not used in the experiments described in this chapter.

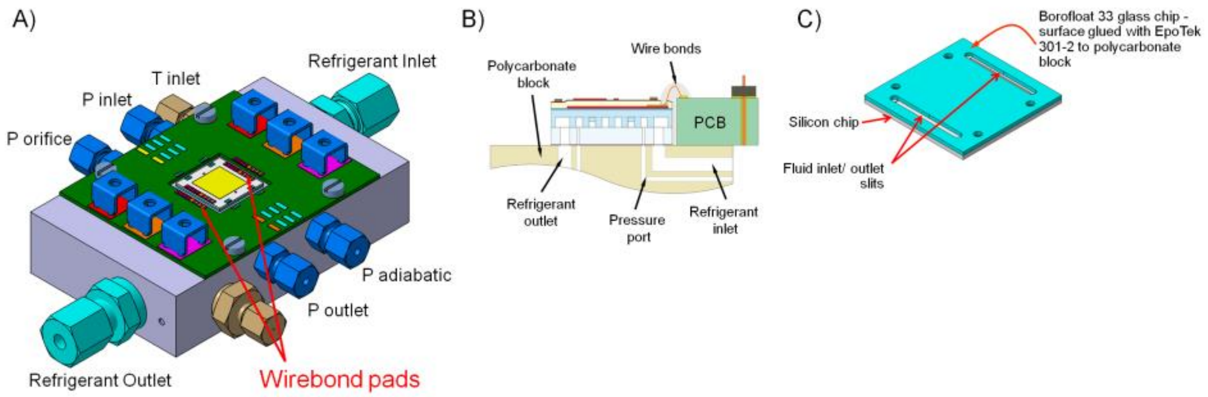
A)
Refrigerant Inlet
T inlet
P inlet
P orifice
P adiabatic
P outlet
Refrigerant Outlet
Wirebond pads
B)
Wire bonds
Polycarbonate block
PCB
Refrigerant outlet
Pressure port
Refrigerant inlet
C)
Borofloat 33 glass chip - surface glued with EpoTek 301-2 to polycarbonate block
Silicon chip
Fluid inlet/ outlet slits

Figure 3.1 A) Complete 3D CAD drawing of test package with metrology. B) Test package cross section. C) Flipped view of test chip showing the glass die as well as the fluid inlet and outlet slits.

On the back side of the silicon chip, a 120µm-deep heat transfer cavity consisting of circular silicon pin fins with an 80µm pin diameter and a 200µm pin-to-pin pitch (Figure 3.4), was etched into the silicon using a Deep Reactive Ion Etching (DRIE) method. The inlet and outlet plenums (9.6mm x 1mm, Figure 3.4), the first one responsible for bringing the refrigerant through the front orifices (width x length, 75µm x 100µm, Figure 3.4) before the flow continues along the pins, were etched at the same time. Simultaneously etched were also four circular 1mm diameter ports allowing local pressure measurements (P_{inlet}, P_{ori},

P_{adb}, P_{outlet}, Figure 3.4). The silicon pin fins are staggered with a 27 degrees deviation angle (Figure 3.4). To complete the test chip, a 500µm-thick borofloat glass die was anodically bonded to the back side of the silicon chip, with corresponding ultrasonically drilled openings, for the pressure ports and the inlet/outlet plenums (Figure 3.1C & 2).

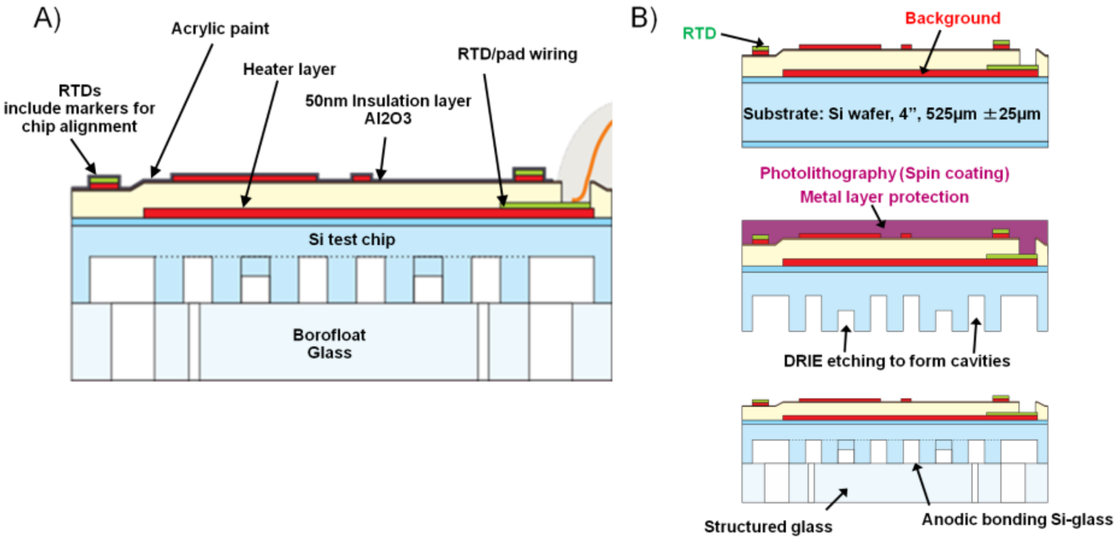
A)
Acrylic paint
Heater layer
RTD/pad wiring
RTDs
include markers for
chip alignment
50nm Insulation layer
Al2O3
Si test chip
Borofloat
Glass
B)
RTD
Background
Substrate: Si wafer, 4", 525µm ±25µm
Photolithography (Spin coating)
Metal layer protection
DRIE etching to form cavities
Structured glass
Anodic bonding Si-glass

Figure 3.2 A) Test chip cross section. B) Fabrication process flow.

The glass side of the test chip was glued (using EpoTeK 301-2, around 50 µm-thick layer) to a 80mm x 50mm milled PolyCarbonate (PC) block that was initially drilled to allow the refrigerant path delivery into the chip and the creation of multiple ports for pressure and temperature measurements (Figure 3.1a and Figure 3.5). The PC block has a 20mm thickness.

The PCB was glued on top of the polycarbonate block and around the test chip facing upwards, thus allowing the connection of the heaters and RTDs to external power supplies via Aluminum wedge-wedge wire-bonding (20µm-thick wires, Figure 3.6) between the PCB and the front side of the silicon chip. It should be noted that the BG heater requires a 48.63V voltage and a 9.85A current to dissipate a maximum heat flux of 520 W/cm^2, and to that end 96 wire-bonds were needed.

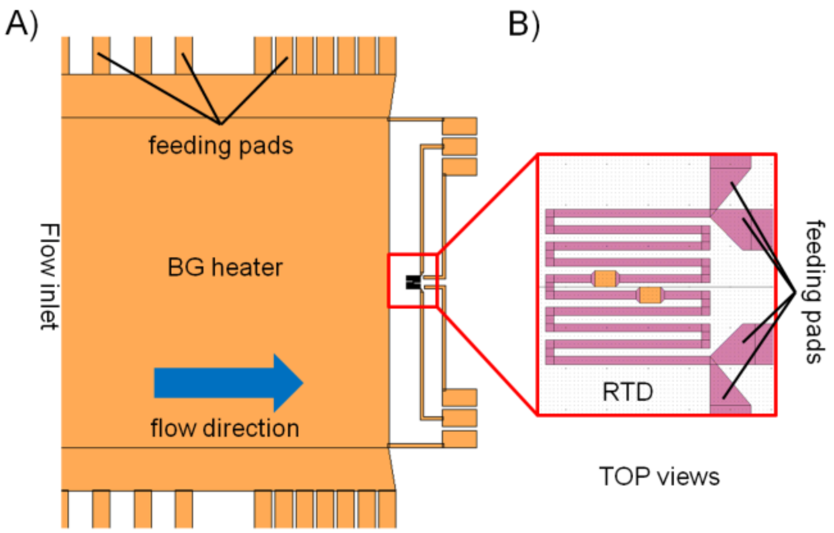
A)
B)
feeding pads
Flow inlet
BG heater
flow direction
RTD
feeding pads
TOP views

Figure 3.3 A) Top view of NiCr background heater with indicated feeding pads and flow direction. B) Top view of RTD inside outlet plenum.

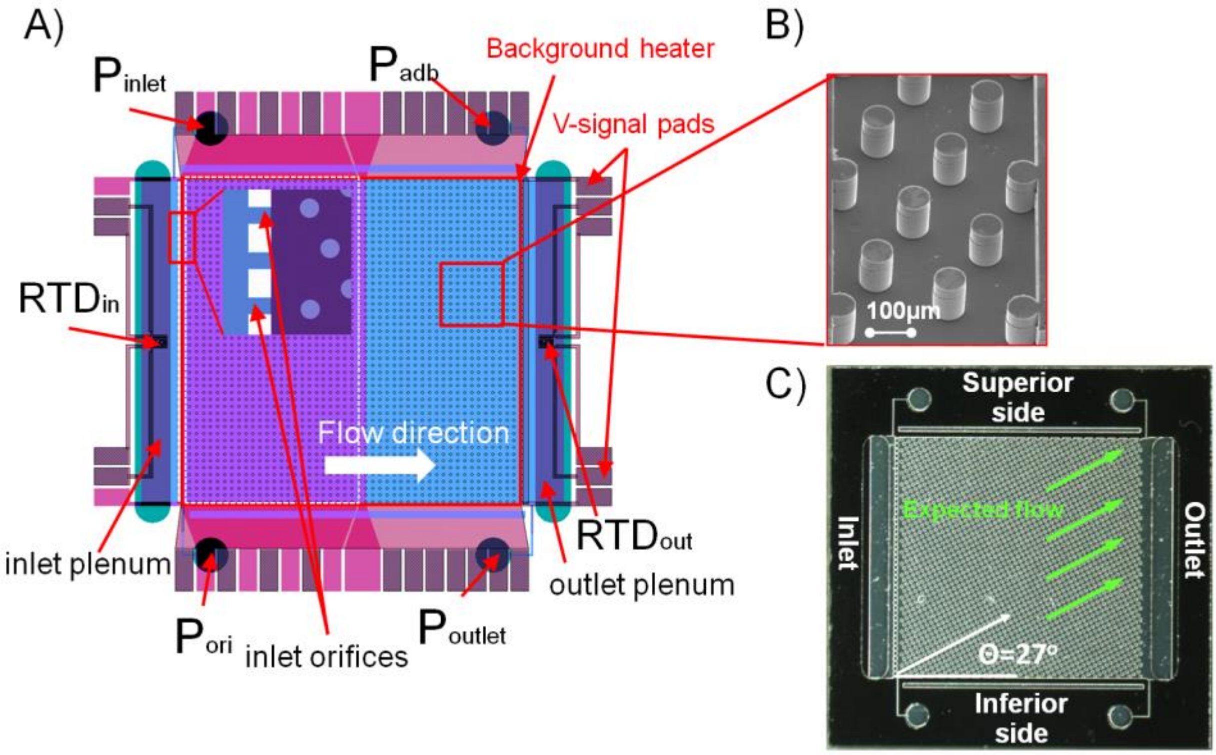
A)
P_{inlet}
P_{adb}
Background heater
V-signal pads
RTD_{in}
Flow direction
inlet plenum
RTD_{out}
outlet plenum
P_{ori}
inlet orifices
P_{outlet}
B)
100μm
C)
Superior side
Inlet
Expected flow
Outlet
Θ=27°
Inferior side

Figure 3.4 A) Schematic of silicon pin fins test chip, top view. B) SEM image of Silicon pin fins. C) Top view microscope image of test chip, showing a potential flow deviation due to staggered position of pins, as seen in [82].

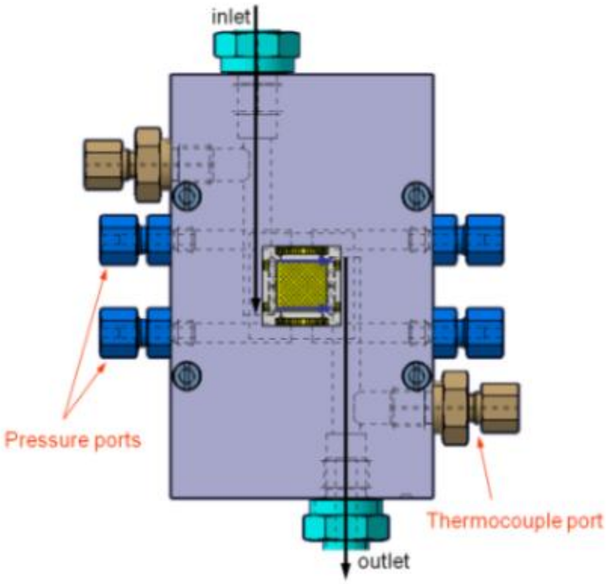
inlet
Pressure ports
Thermocouple port
outlet

Figure 3.5 Top view of PC manifold, showing the flow path from inlet to outlet as well as the available metrology.

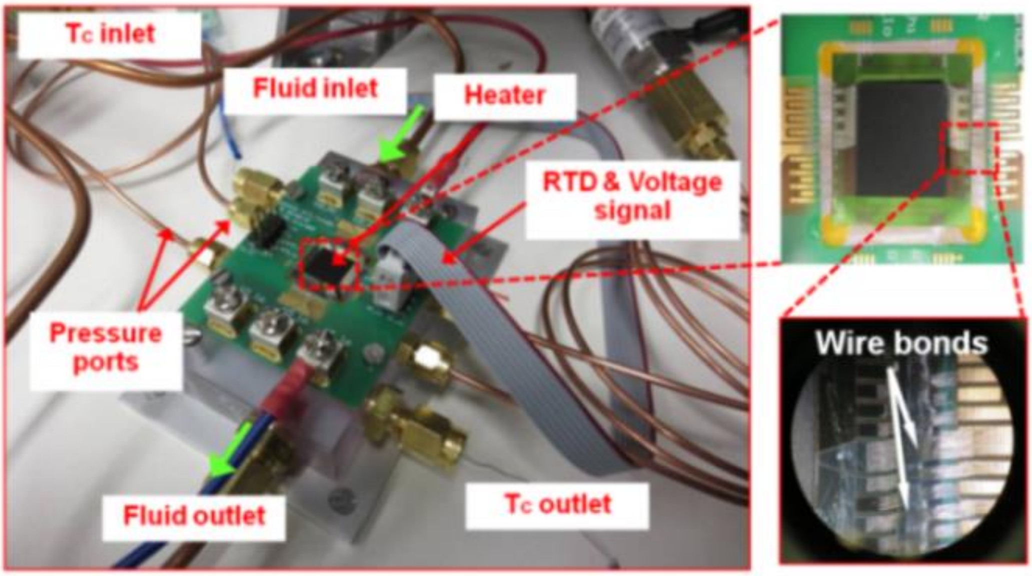
Tc inlet
Fluid inlet
Heater
RTD & Voltage signal
Pressure ports
Fluid outlet
Tc outlet
Wire bonds

Figure 3.6 Complete test section attached to the experimental facility, showing the inlet and outlet thermocouples, the pressure ports, the direction of the flow as well as the background heater and its external electrical connections.

3.1.4 Test facility

An experimental setup was assembled to perform two-phase heat transfer coefficients and pressure drop as well as Infra-Red (IR) thermal measurements within the above defined test package. A schematic of this setup, located at the IBM Research Laboratory in Zurich, is shown on Figure 3.7. It is composed of a computer with a data acquisition system (Figure 3.8a, left), two possible test section locations (Figure 3.8a, right), a condenser (tube-in-tube heat exchanger) controlled by the building's cooling loop, a magnetically-driven gear pump for liquids, a pre-heater (tube-in-tube heat exchanger) controlled by a heating bath and a Coriolis mass flow meter (Figure 3.8a, right). Two reservoirs that store the different refrigerants used in the possible test sections (R1234ze and R236fa, both hydro-fluoro-carbons) are connected to the loop to control the experimental saturation pressure. The control is done with a temperature controlled thermal bath. To measure the inlet, outlet and surface temperatures of the Test Section 2, respectively two K-type thermocouples with a diameter of 200µm were used ($T_{c,inlet}$, $T_{c,outlet}$, Figure 3.6) as well as an IR camera (Figure 3.8b). The thermocouples were calibrated to within 0.1°C. Four absolute pressure transducers (Figure 3.4a, Figure 3.6), with an accuracy of 0.1% Full Scale (FS) and a FS value of 10 bar were instrumented to measure the fluid inlet pressure (P_{inlet}), the fluid pressure across the inlet orifices (P_{ori}), the pressure at the end of the fluid path (P_{adb}) and the pressure in the outlet plenum (P_{outlet}), respectively. Sight glasses were used to inspect the possibility of having two-phase flow. To that effect the test section's inlet and outlet temperatures were also monitored.

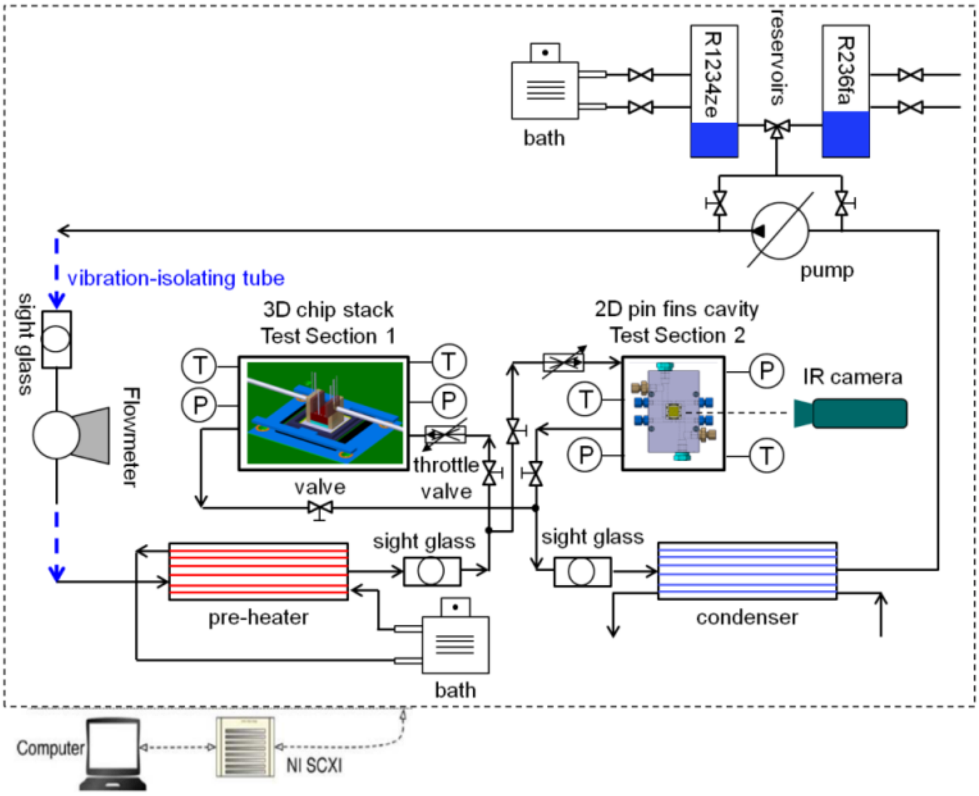
bath
R1234ze
reservoirs
R236fa
pump
vibration-isolating tube
sight glass
Flowmeter
3D chip stack
Test Section 1
2D pin fins cavity
Test Section 2
T
P
IR camera
throttle
valve
valve
sight glass
sight glass
pre-heater
condenser
bath
Computer
NI SCXI

Figure 3.7 Flow boiling test facility.

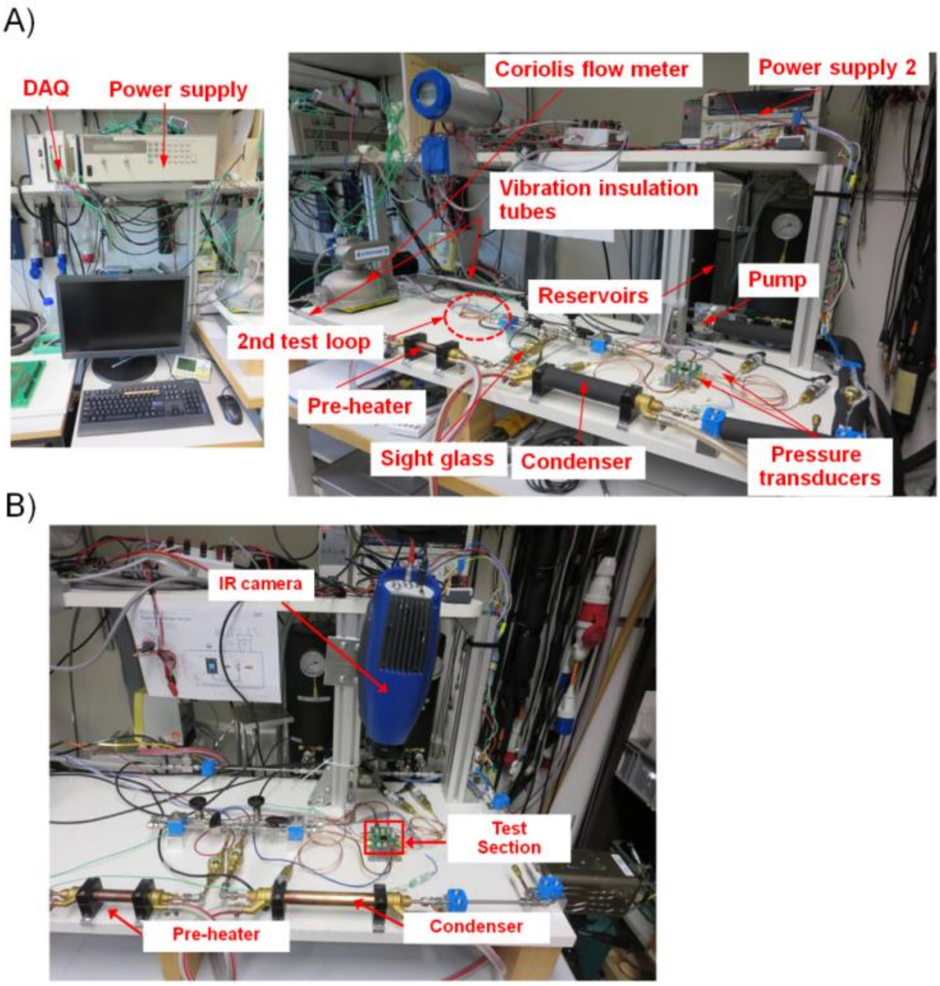
A)
DAQ
Power supply
Coriolis flow meter
Power supply 2
Vibration insulation tubes
Reservoirs
Pump
2nd test loop
Pre-heater
Sight glass
Condenser
Pressure transducers
B)
IR camera
Test Section
Pre-heater
Condenser

Figure 3.8 A) Left: Test facility's power supply and data acquisition system. Right: complete test facility. B) Test section and IR camera setting.

3.1.5 Operating conditions

This facility was built and adapted to handle pressures of up to 25 bar (2500 kPa). This was done due to the fact that the working saturation temperature was set at 30°C, which corresponds to working pressures of 578.3 kPa for R1234ze. This pressure was kept constant within 10 kPa due to the temperature control inside the reservoir. The condenser inlet temperature was set at 8°C (±2°C) so that the sub-cooling at the inlet of the pump was large enough to avoid cavitation. The pre-heater temperature was set in such a way that the subcooling at the inlet of the test section was kept to 13°C (±1°C), with the help of a throttle valve (Figure 3.7). A flow rate of 11.5 kg/hr (0.167 l/min) was tested with refrigerant 1234ze. The working saturation temperature was set at 30°C, corresponding to a 578.3 kPa saturation pressure (in the reservoir). A pressure drop occurs between the reservoir and the inlet of the test section, resulting in a pressure of 575 kPa at the inlet. The targeted subcooling during the experiments was 13°C. At the mass fluxes for which subcooled fluid entered the test chip, boiling was initiated by increasing the background heat flux q_b until evaporation started somewhere along the fluid path (inlet plenum, inlet orifice, pin fins, outlet plenum). Depending on the inlet subcooling and at higher mass flow rates, one could expect boiling to be initiated by cavitation flashing through the cross-sectional inlet orifices (Figure 3.4), which was not the case here. The background base heat flux was increased until the maximum possible value for the tested mass velocity was reached. The maximum heat flux value is determined either by keeping the chip junction temperature below 85°C, the standard maximum sustainable temperature for integrated circuits, or by reaching the maximum pressure drop sustainable by the pressure measurement equipment or the loop pump. The latter was the case in the described experiments. For each background base heat flux, between 5 and 115 data points were saved after steady-state conditions were reached (which took approximately 2 minutes).

3.1.6 Data reduction

Given the measured local pressures, the following pressure drop relations were established as follows:

- The pressure drop through the inlet orifices:

$$\Delta P_{orifice} = P_{inlet} - P_{ori} \tag{3.1}$$

- The pressure drop due to the pin fins fluid path:

$$\Delta P_{pins} = P_{ori} - P_{adb} \tag{3.2}$$

- The total pressure drop through the test chip:

$$\Delta P_{total} = P_{inlet} - P_{outlet} \tag{3.3}$$

- The contribution of the pressure drop through the orifices, w_1:

$$w_1 = \Delta P_{orifice} / \Delta P_{total} \tag{3.4}$$

- The contribution of the pressure drop through the pin fins, w_2:

$$w_2 = \Delta P_{pins} / \Delta P_{total} \tag{3.5}$$

The two-phase pressure drop is generally high in microscale cavities so that the saturation pressure can decrease by several degrees along the pin fins. Thus, the local pressure must be calculated in order to know the local saturation temperature.

The local base footprint heat transfer coefficients were calculated via the following formula

$$\alpha_b(y,z) = \frac{q_b}{T_{base,fin}(y,z) - T_{fl}(z)} \tag{3.6}$$

where q_b is the base heat flux emitted by the BG heater (§ *Test section*) and is calculated using

$$q_b = \frac{U \times I}{L \times B} \tag{3.7}$$

where *y* is the position perpendicular to the flow direction, *z* the one along the flow direction, *L* is the heated length along the flow path and *B* the heated width of the test section.

$T_{base,\,fin}$ is the pin fin wall temperature and is calculated using one-dimensional heat conduction through the silicon chip thickness, from the surface temperature measured with the IR camera until the base of the pin fins. It is assumed that the pin fin temperature is uniform over its entire surface.

$$T_{base,fin}(y,z) = T_{surface}(y,z) - \frac{q_b \cdot t_{Si}}{k_{Si}} \tag{3.8}$$

where t_{Si} and k_{Si} respectively are the silicon chip's thickness and the material's thermal conductivity (140 W/mK).

For the fluid temperature to be calculated along the flow direction, the refrigerant state, i.e. either single-phase (sp) or two-phase flow (tp) has to be determined first. It is assumed that the pressure across the test chip width perpendicular to the flow direction, at the same location along the flow path, was the same.

To determine the starting point of two-phase flow in the test section, the local pressure drop until pressure and rising fluid temperature intersect and reach saturation conditions must be calculated. From there, the pressure drop in the two-phase regime is linear and thus a second reference point is needed, $T_{c,\,outlet}$.

For subcooled single-phase flow, the local fluid temperature was calculated iteratively along the pins through an energy balance:

$$T_{fl}(z) = T_{fl}(0) + \int_0^z \frac{B \cdot q_b \cdot dz}{A \cdot G \cdot c_{p,l}(z)} \tag{3.9}$$

where $T_{fl}(0)$ is equal to $T_{c,\,inlet}$.

In the flow boiling regime, the fluid saturation temperature was calculated from the vapor pressure curve, knowing the local pressure:

$$T_{fl}(z) = T_{sat}\big(p(z)\big) \tag{3.10}$$

The two equations above must be solved iteratively by dividing the corresponding flow length into for example 100 increments, *dz* = *L*/100.

All of the above described equations then give us, according to Equation (3.6), the local footprint heat transfer coefficient.

Finally, all R1234ze properties were calculated with the REFPROP 9 software from NIST. The thermo-physical properties of R1234ze at a saturation temperature of 30°C are shown in Table 3.1.

3.1.7 Results and discussion

To achieve the lowest total pressure drop for the highest cooling performance is a crucial requirement in order to design and optimize a multi-microchannel cooling system. Thus, it is useful to deconstruct the total pressure drop and calculate the relative contribution of each one of its different components. Figure 3.9 shows the three different pressure drops, measured and determined according to Equations 3.1 to 3.3.

The total measured pressure (Equation 3.3) drop is plotted for increasing heat fluxes at the fixed tested mass flow rate (11.5kg/hr). The pressure drop stays constant as long as the whole flow path remains in a liquid state, but increases with heat flux as soon as flow boiling starts occurring, as expected given the observations of Agostini et al. [44]. The maximum measured pressure drop, at the highest base heat flux (q_b = 66.6 W/cm^2), is 239 kPa. This pressure drop value marked the end of the experimental campaign for this flow rate, since the maximum pressure drop sustainable by the test loop pump was reached.

Table 3.1 Thermo-physical saturation properties of R1234ze at 30°C.

Thermo-physical saturation properties of R1234ze at 30°C	
psat (kPa)	578.3
ρl (kg/m3)	1146.4
ρv (kg/m3)	30.523
cp,l (kJ/kgK)	1.4029
cp,v (kJ/kgK)	0.99857
hlv (kJ/kg)	163.06
kl (mW/mK)	76.548
kv (mW/mK)	14.021
µl (µPa·s)	187.98
µv (µPa·s)	12.458
σ (mN/m)	8.2092

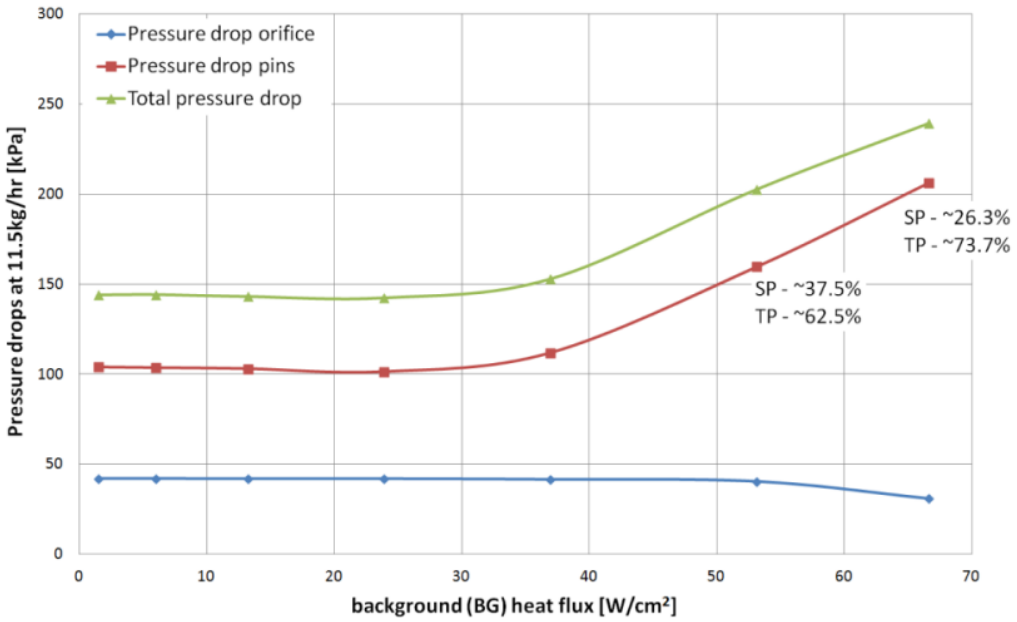

Figure 3.9 Pressure drop components evolution for increasing base heat fluxes at a mass flow rate of 11.5kg/hr for R1234ze.

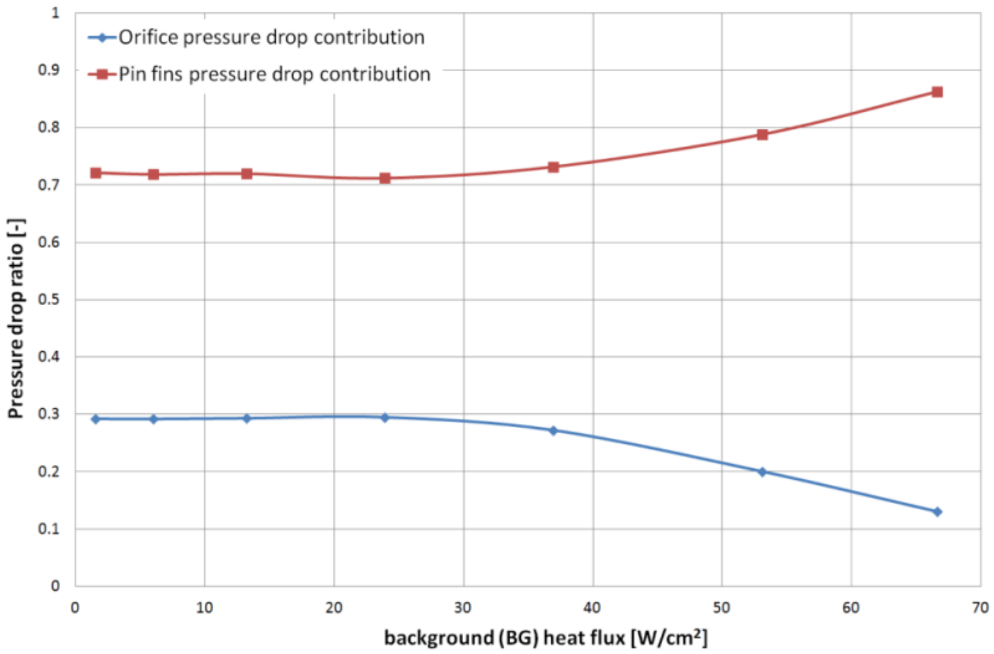

Figure 3.10 Total pressure drop relative contributions for increasing base heat fluxes at a mass flow rate of 11.5kg/hr for R1234ze.

The evolution of the pressure drop through the inlet orifices as well as that along the pin fins are also shown on Figure 3.9. The pin fins' pressure drop behaves the same way as the total pressure drop, increasing with the base heat flux in the two-phase flow regime. It was observed during experiments that, above 36.9W/cm^2 and thus for the base heat fluxes

53.1W/cm^2 and 66.6W/cm^2, flow boiling occurred along the pin fins flow path. The values shown on Figure 3.9 next to the pin fins pressure drop curve indicate the contribution of each flow phase to that particular pressure drop, i.e. for 53.1W/cm^2, the part of the flow that remained in liquid phase contributed 37.5% of that pressure drop. The two-phase part contributed 62.5% in that case. That contribution increases when moving to the next higher base heat flux (66.6W/cm^2), to 73.7%, which is expected due to the earlier onset of flow boiling along the flow path and higher achieved outlet vapor quality. Finally, the pressure drop through the inlet orifices remained roughly constant for increasing base heat fluxes, since that part of the flow path always remained in single-phase flow.

Figure 3.10 shows the respective contributions to the total pressure drop (shown on Figure 3.9) of the inlet orifices pressure drop as well as the pin fins pressure drop. As expected, the pin fin pressure drop contribution stays constant at around 70% as long as the whole flow path remains in liquid phase but starts increasing when flow boiling occurs after 36.9W/cm^2, until for the highest measured heat flux it reaches almost 90%, since this part of the flow path is the longest where two-phase flow can occur and vapor quality can increase. Regarding the inlet orifices contribution, since that pressure drop is always constant, its contribution remains logically constant in single-phase regime (30%) and decreases in the two-phase flow regime due to the increase of the total test section pressure drop, to almost 10%.

Figure 3.11 shows the BG heater's surface temperatures obtained via InfraRed imaging (see Appendix B for IR images), for increasing base heat fluxes, at two locations across the width of the test chip. **These locations are the superior and the inferior sides of the device, at the edges of the chip, according to the explanation on Figure 3.4C**. Figure 3.11 confirms that for heat fluxes until 36.9W/cm^2, flow boiling does not occur within the entire flow path. Above that value, surface temperatures can be seen decreasing after a certain point in the flow direction, for heat fluxes 53.1 and 66.6W/cm^2, indicating the presence of two-phase flow regime, where the temperature decreases with the pressure drop after reaching saturation point.

However, there seems to be a slight mismatch in terms of onset of flow boiling point, between the inferior and the superior sides of the flow path, for the highest tested base heat fluxes. Evaporation seems to occur earlier along the flow path for the inferior side, which could be explained by a slightly smaller quantity of coolant delivered to that area, caused by a potential flow deviation due to the staggered arrangement of the pin fins (Figure 3.4C). This is a phenomenon that was also observed in [82]. It can also be seen when looking at the base heat transfer coefficient values. Figure 3.11 shows that, for both heat fluxes 53.1 and 66.6 W/cm^2, the footprint heat transfer coefficient at the start of flow boiling (calculated using Equation (3.6)) on the inferior side is lower than its superior side counterpart. This could explain the slightly higher junction temperatures on the inferior side.

However, an error propagation calculation is necessary here to determine the exactitude of that phenomenon and rule out the effect of measurement inaccuracies.

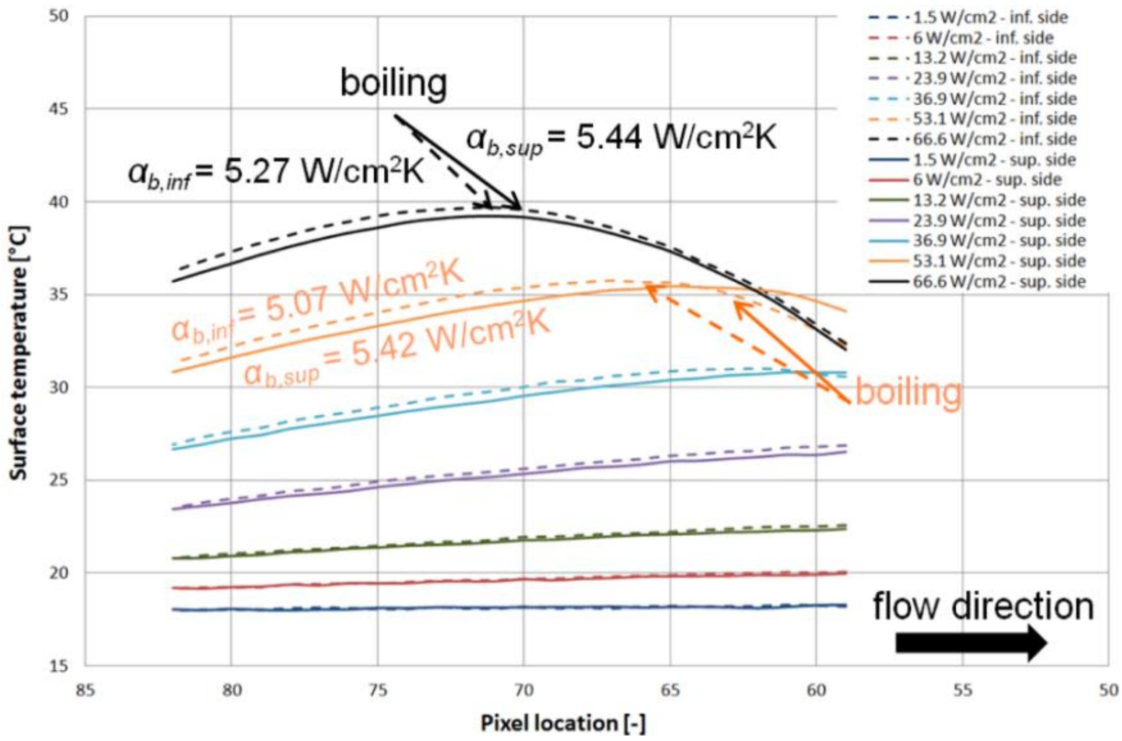

Figure 3.11 Background heater junction temperatures along flow direction for increasing base heat fluxes at a mass flow rate of 11.5kg/hr for R1234ze, at two locations across the test section width, for an inlet subcooling of 13°C and inlet saturation temperature of 30°C.

Finally, Figure 3.11 shows that even for high base heat fluxes (66.6 W/cm^2), the junction temperature remains at or below 40°C, far from the maximum allowed 85°C, which shows that a large margin remains to increase the device's heat output and take advantage of the evaporative cooling process by pushing the outlet vapor quality.

3.2 Experimental investigation – 3D test vehicle

3.2.1 Introduction & purpose

The main focus of this sub-chapter is to demonstrate the potential feasibility and/or limits of a first-of-a-kind 3D chip stack package with integrated interlayer cooling capabilities. As part of this effort, a 3D stack of silicon chips with TSVs and integrated cooling capabilities was designed, manufactured, assembled and experimental investigation of refrigerant two-phase flow (pressure drop measurements) was performed on it.

3.2.2 Design, fabrication & assembly

Figure 3.12 and 3.13 show the test vehicle, a prototype package for an intra-chip stack thermal management system, developed for the CMOS Advanced Interlayer Cooling consortium (CMOSAIC), whose principal aims were the development of a prototype 3D stack of chips with integrated cooling capabilities and the investigation of heat transfer effects in such systems, using water as well as refrigerant cooling. The purpose of this particular test vehicle is to demonstrate the feasibility of intra chip stack fluidic cooling via two-phase evaporative heat transfer.

The package consists of a chip stack attached to a larger silicon interposer, as shown in Figures 3.12, 3.13 and 3.14, acting as an intermediate between PCB1 (40mm x 40mm x 1.6mm) and the stack (12.7mm x 12.7mm x 2mm). This interposer is a 525µm-thick 22mm x 22mm chip that is glued using the thixotropic EpoTek epoxy H70E-4 (two component, thermally conductive, thermally insulating epoxy adhesive) and wedge-wedge wire-bonded to the PCB1 using 25µm-thick aluminum wires (Figure 3.15). The electrical connection from PCB1 to PCB2 (180mm x 250mm x 2.4mm) is done via a standard Foxconn LGA/BGA socket system (see Figure 3.16 and Appendix A for details on the socket). The socket, with the PCB1 plugged inside, is C4 bonded to the PCB2 prior to the application of underfill U300-2 from EpoTek (two component epoxy for capillary underfill). External wires/ connectors on PCB2 are used to connect the package to external power supplies. A stainless steel frame (Figures 3.12a, 3.13a and 3.16) is coupled with the socket to ensure proper electrical contact between PCB1 and the LGA/ BGA socket.

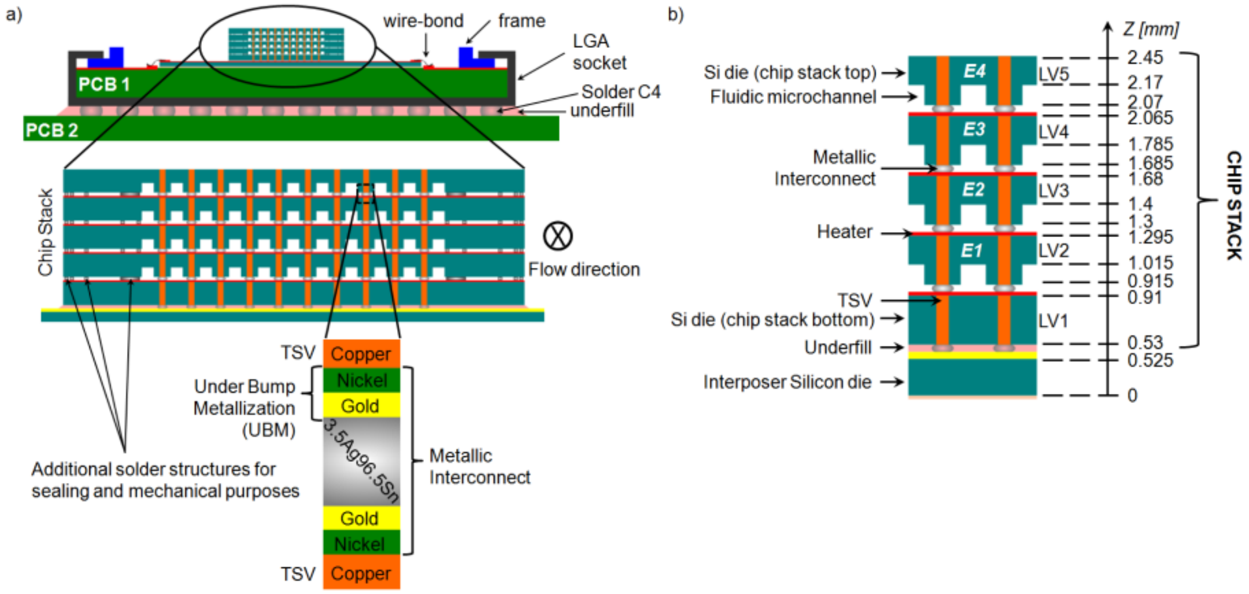
a)
wire-bond
frame
LGA socket
PCB 1
Solder C4
underfill
PCB 2
Chip Stack
Flow direction
TSV
Copper
Under Bump Metallization (UBM)
Nickel
Gold
3.5Ag96.5Sn
Metallic Interconnect
Gold
Nickel
TSV
Copper
Additional solder structures for sealing and mechanical purposes
b)
Z [mm]
Si die (chip stack top)
Fluidic microchannel
Metallic Interconnect
Heater
TSV
Si die (chip stack bottom)
Underfill
Interposer Silicon die
E4
E3
E2
E1
LV5
LV4
LV3
LV2
LV1
2.45
2.17
2.07
2.065
1.785
1.685
1.68
1.4
1.3
1.295
1.015
0.915
0.91
0.53
0.525
0
CHIP STACK

Figure 3.12 CMOSAIC Test Vehicle description–chip stack package with silicon embedded heat transfer structures. a) Ensemble view of package with all components. b) Vertical cross-section describing the multiple layers and their respective thicknesses.

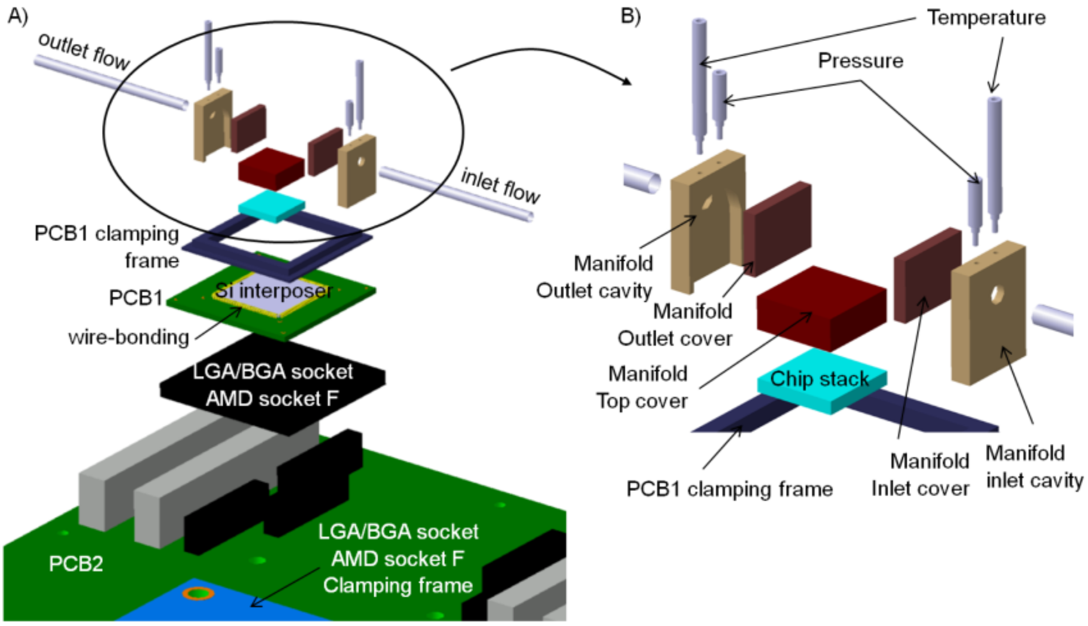
A)
outlet flow
inlet flow
PCB1 clamping frame
PCB1
Si interposer
wire-bonding
LGA/BGA socket AMD socket F
PCB2
LGA/BGA socket AMD socket F Clamping frame
B)
Temperature
Pressure
Manifold Outlet cavity
Manifold Outlet cover
Manifold Top cover
Chip stack
PCB1 clamping frame
Manifold Inlet cover
Manifold inlet cavity

Figure 3.13 Exploded views of the 3D chip stack package showing all different components.

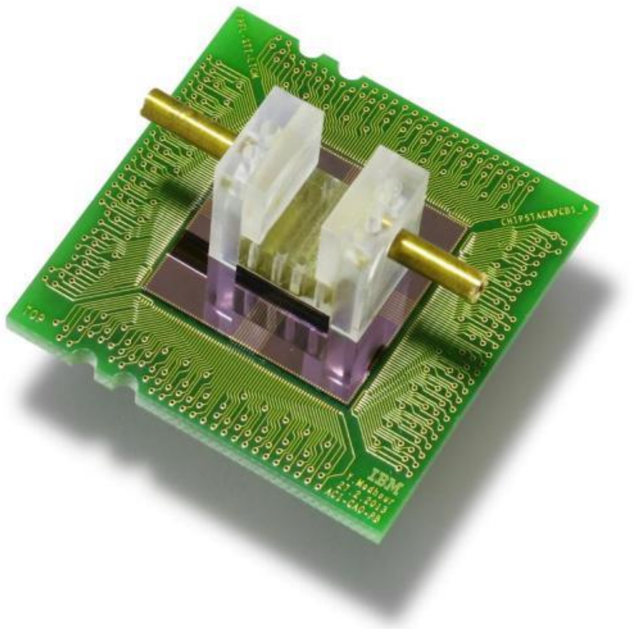

Figure 3.14 Assembled CMOSAIC demonstrator. Manifold parts here are PMMA for visual and aesthetic purposes only.

Five 380 µm-thick 12.7×12.7 mm^2 silicon chips (LV1 to 5, see Figure 3.12a and 3.12b) are flip-chip bonded to form the chip stack, as shown on Figure 3.12a and b. These chips have been double-side micro-processed at wafer-level, and represent mock-ups of real devices, with controlled heaters acting as cores on the front side and embedded microchannels on the back for integrated cooling. First, copper TSVs are etched through the silicon and filled, with a diameter of 64 µm per TSV (for LV1 to 5). The TSVs are electrically insulated with a

1.5 µm silicon dioxide liner that is oven-grown at 1000°C overnight right after via etching. Copper filling is done via double-sided electroplating.

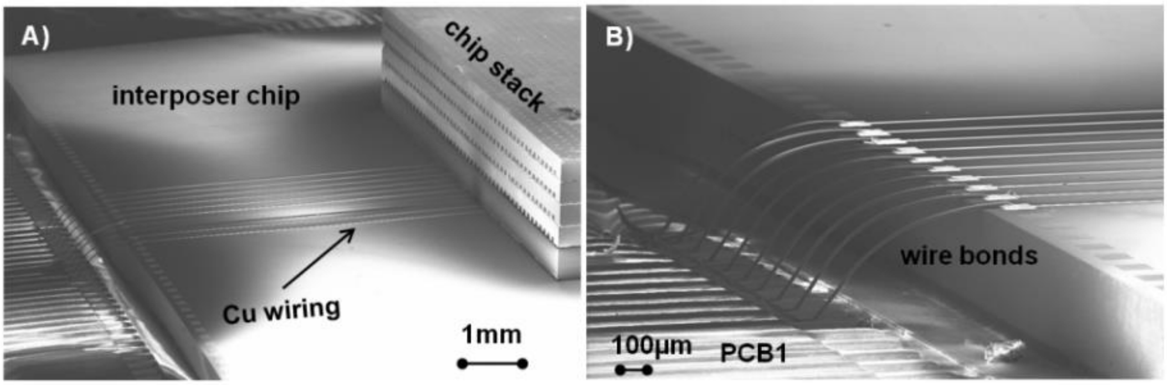
A)
interposer chip
chip stack
Cu wiring
1mm
B)
wire bonds
100µm
PCB1

Figure 3.15 A) SEM photograph of chip stack on interposer. B) SEM photograph of aluminium wire-bonds between interposer chip and PCB1.

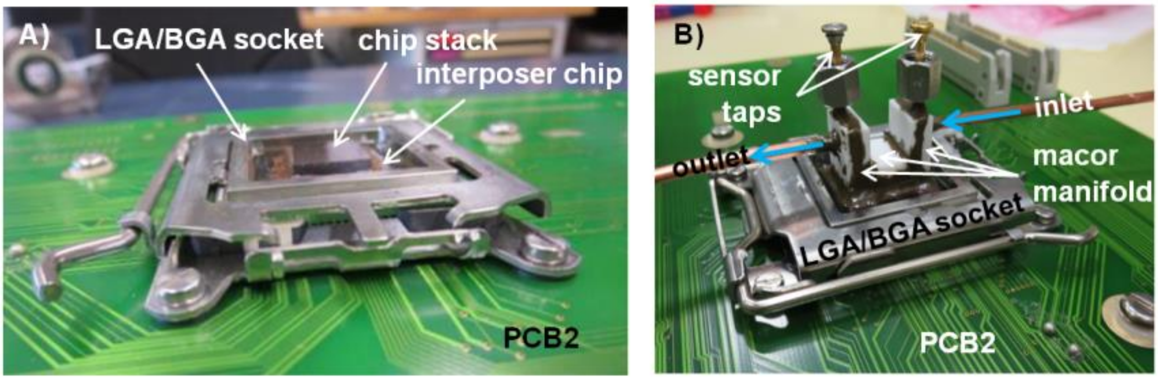
A)
LGA/BGA socket
chip stack
interposer chip
PCB2
B)
sensor taps
inlet
outlet
macor manifold
LGA/BGA socket
PCB2

Figure 3.16 A) Chip stack with interposer glued to PCB1 and plugged into LGA/BGA socket. The socket is C4 bonded to PCB2. B) Complete 3D module attached to PCB2, showing inlet and outlet tubing as well as inlet and outlet temperature and pressure taps locations.

As shown on Figure 3.17, on the front side of the wafer, the aluminum heaters, complete with their own RTD (see Figure 3.17), are deposited (in a 3x3 floorplan) via sputter deposition (500 nm) directly on top and around the open vias (for LV1 to 5, see Figures 3.17 and 3.18), some of these connecting the pads for the heaters at each level. The Under Bump Metallization (UBM, 2 µm nickel plus 500 nm gold) is then sequentially deposited on the same side via sputtering on top of the still open vias (for LV1 to 4), to allow the flip-chip bonding of the superior chip (**see Chapter 2 for the detailed description of the chip stack's fabrication and assembly processes**).

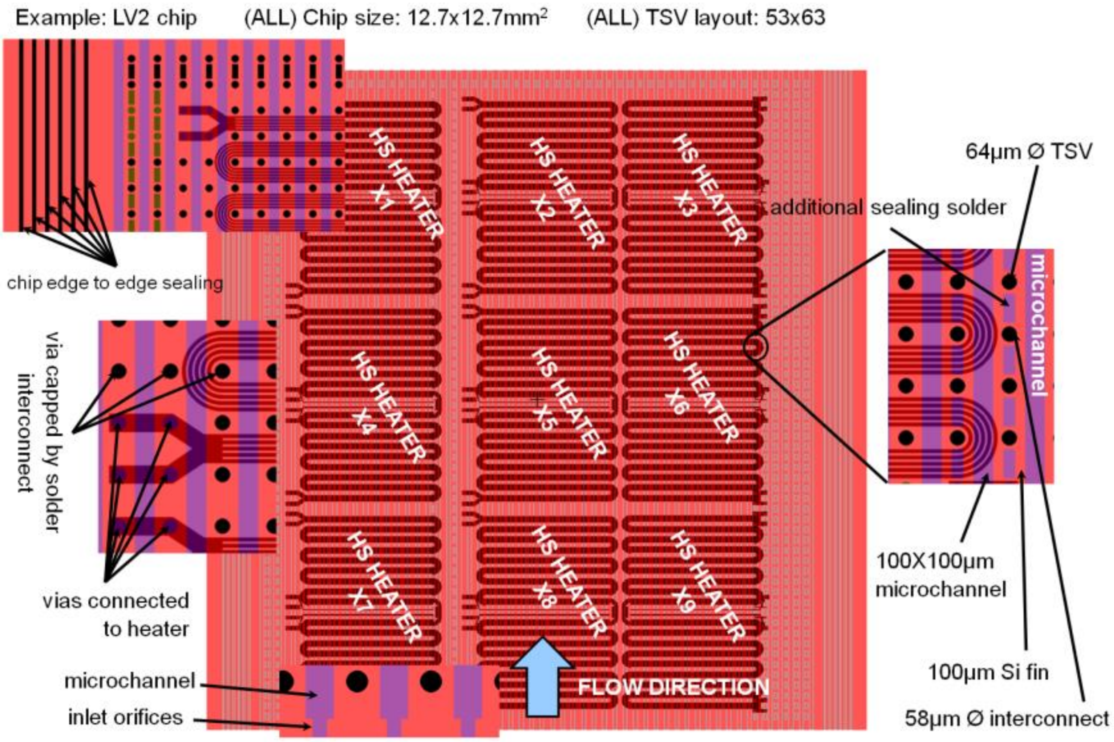
Example: LV2 chip
(ALL) Chip size: 12.7x12.7mm²
(ALL) TSV layout: 53x63
HS HEATER X1
HS HEATER X2
HS HEATER X3
HS HEATER X4
HS HEATER X5
HS HEATER X6
HS HEATER X7
HS HEATER X8
HS HEATER X9
64µm Ø TSV
additional sealing solder
microchannel
chip edge to edge sealing
via capped by solder interconnect
vias connected to heater
microchannel
inlet orifices
FLOW DIRECTION
100X100µm microchannel
100µm Si fin
58µm Ø interconnect

Figure 3.17 Chip-level design, with all frontside and backside structures visible.

On the back side of the wafer, solder interconnects with their respective UBM pads are electroplated (2 µm nickel, 1 µm gold, 15 µm eutectic silver tin, 58 µm diameter) for the bonding to the inferior chip (for LV1 to 5). Figures 3.17 and 3.19A show the additional solder features that were implemented in order to seal the edges of the chip so that the coolant cannot run away from the side. Complementary sealing structures (Figure 3.19B) were also added to prevent mass flow cross-talk between the microchannels that could happen due to the small 5 µm gap left between two stacked dies, as showcased in Chapter 2.

Additionally fifty-four 100×100 µm microchannels, each with its own inlet restriction (Figure 3.17) to counter backflow instability effects during flow boiling of refrigerants (as witnessed by [40]) are etched on the back side of each chip (for LV2 to 5) via a Deep Reactive Ion Etching (DRIE) process, thus forming the multiple evaporator layers where flow boiling will occur (*E1* to *E4* on Figure 3.12b). **The detailed fabrication steps and flip-chip bonding of these chips is described in Chapter 2**.

After formation of the chip stack via flip-chip bonding of the LV1 to LV5 chips, underfill U300-2 is applied between the stack and the interposer chip (Figure 3.12b).

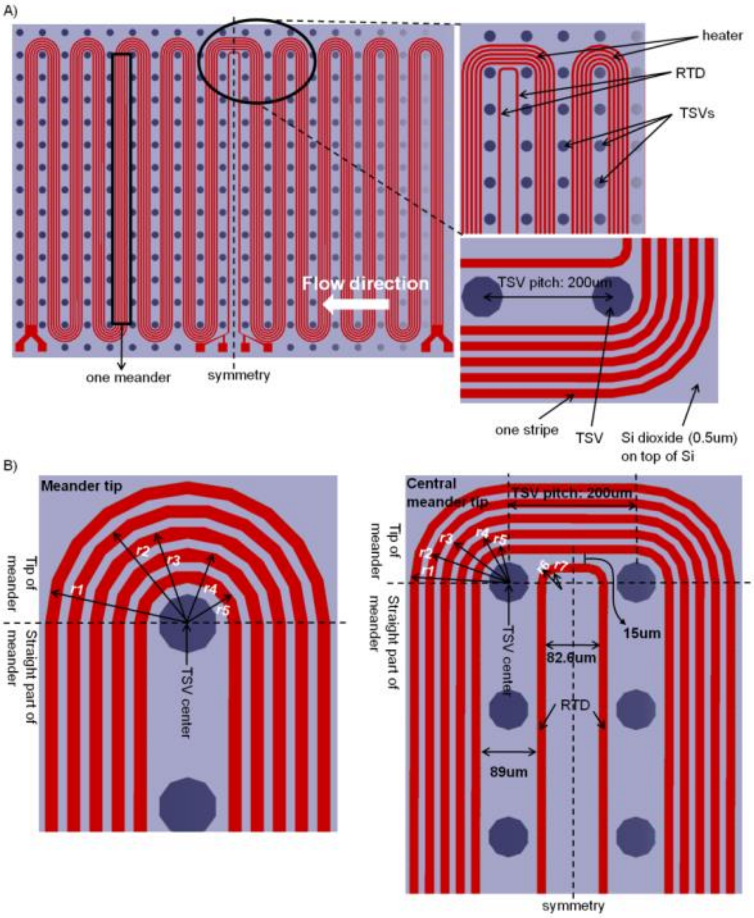
A)
heater
RTD
TSVs
Flow direction
one meander
symmetry
TSV pitch: 200um
one stripe
TSV
Si dioxide (0.5um) on top of Si
B)
Meander tip
Tip of meander
Straight part of meander
r1
r2
r3
r4
r5
TSV center
Central meander tip
TSV pitch: 200um
Tip of meander
Straight part of meander
r1
r2
r3
r4
r5
r6
r7
15um
82.6um
RTD
TSV center
89um
symmetry

Figure 3.18 Top view illustration of the design of a Hot Spot (HS) sputter-deposited heater with its own RTD, both 500nm-thick. The heater requires a current of 211 mA and a voltage drop of 8.92 V to output 50 W/cm^2. The resistance of the heater at ambient temperature is 34.9 Ohms.

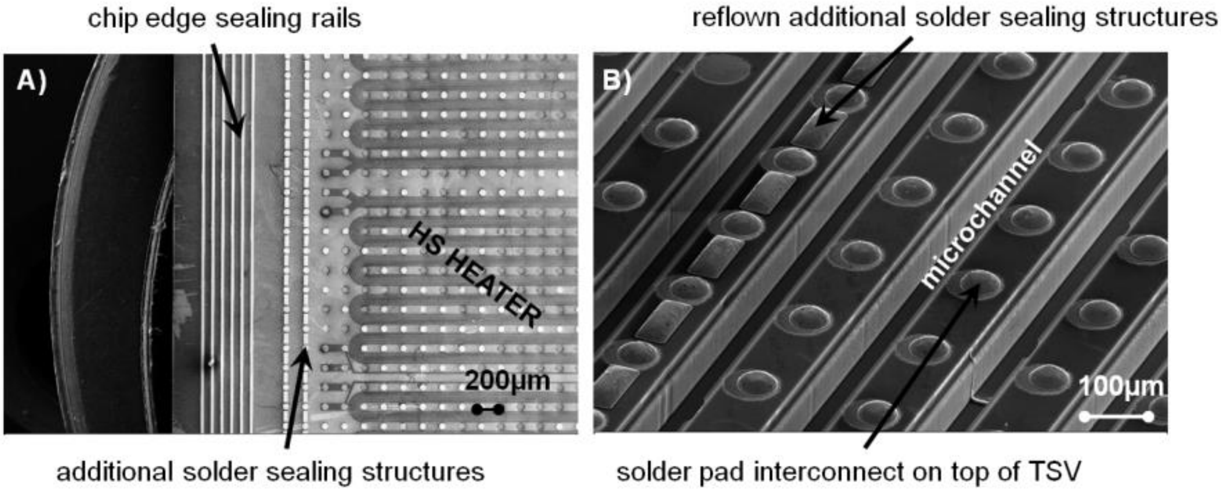
chip edge sealing rails
A)
HS HEATER
200µm
additional solder sealing structures
reflown additional solder sealing structures
B)
microchannel
100µm
solder pad interconnect on top of TSV

Figure 3.19 A) SEM photograph of the LV2 chip frontisde, showing the added solder sealing structures (UBM side). B) SEM photograph of the LV3 chip backside, showing the solder interconnects and added sealing structures.

Finally, to supply coolant fluid, a manifold made of 5 macor (material chosen for its low Coefficient of Thermal Expansion (CTE)) parts is fitted over the chip stack. The dimensions of the inlet and outlet manifold's cavity are 10.7mm x 14.03mm x 2mm (respectively Width x Height x Depth of cavity). As explained in Figures 3.13b and 3.16, the fluid enters through a 3mm diameter copper inlet tube, flows down through the inlet header, turns 90° into the individual channels of the chip stack, and then exits up the outlet header and into the outlet copper tube (Figure 3.20).

3.2.3 Test facility

The test facility used to perform the two-phase flow experiments described in § 3.1.4 and Figure 3.7 contains two locations for possible test sections. In § 3.1, Test Section 2 was described, where the 2D pin fins test vehicle was set up. The 3D chip stack module was set up in the Test Section 1 location, as indicated in Figure 3.7. The facility remains the same, and this time the inlet and outlet temperatures (T_{inlet} and T_{outlet}) within the manifold were measured using 200µm K-type thermocouples, calibrated to within 0.1°C. Two absolute pressure transducers (Figure 3.20, P_{inlet} and P_{outlet}), with an accuracy of 0.1% Full Scale (FS) and a FS value of 16 bar, were instrumented to respectively measure the fluid inlet pressure as well as the fluid outlet pressure within the respective manifold parts. Likewise, sight glasses were used to inspect the possibility of having two-phase flow, in addition to the monitoring of the test section's inlet and outlet temperatures.

3.2.4 Operating conditions

As mentioned in § 3.1.5, this facility was built to handle pressures of up to 25 bar (2500 kPa). The coolant fluid used for the 3D module was Refrigerant 236fa (R236fa), at a working saturation temperature of 31°C, which corresponds to working pressures of 331 kPa. This pressure was kept constant within 10 kPa due to the temperature control inside the reservoir (± 1°C for the saturation temperature). The condenser inlet temperature was set at 10°C (±2°C) so that the sub-cooling at the inlet of the pump was large enough to avoid cavitation. The pre-heater temperature was set between 20 and 26°C (± 1°C), depending on how difficult it was to obtain steady-state conditions. Seven flow rates between 1.42 and 4.27 kg/hr (channel mass fluxes between 182 and 549 kg/m^{2}s) were tested with refrigerant 236fa for pressure drop measurements. The working saturation temperature was set at 31°C (± 1°C), corresponding to a 331 kPa saturation pressure (in the reservoir). A pressure drop occurs between the reservoir and the inlet of the test section (Figures 3.7 and 3.20), resulting in a pressure between 317 and 327 kPa at the inlet. The targeted subcooling during the experiments was 5 to 10°C. Depending on the inlet subcooling and the mass flux, one can expect boiling to be initiated by cavitation flashing through the cross-sectional inlet orifices (Figure 3.17), which was the case here during pressure drop measurements. The maximum experimental mass flow rate was attained by reaching the maximum pressure drop sustainable by the loop pump. For each mass flux, 100 data points were saved after steady-state conditions were reached.

3.2.5 Pressure drop results and discussion

The total measured pressure drop shown on Figure 3.21 is obtained via the following equation:

$$\Delta P_{total} = P_{inlet} - P_{outlet} \tag{3.11}$$

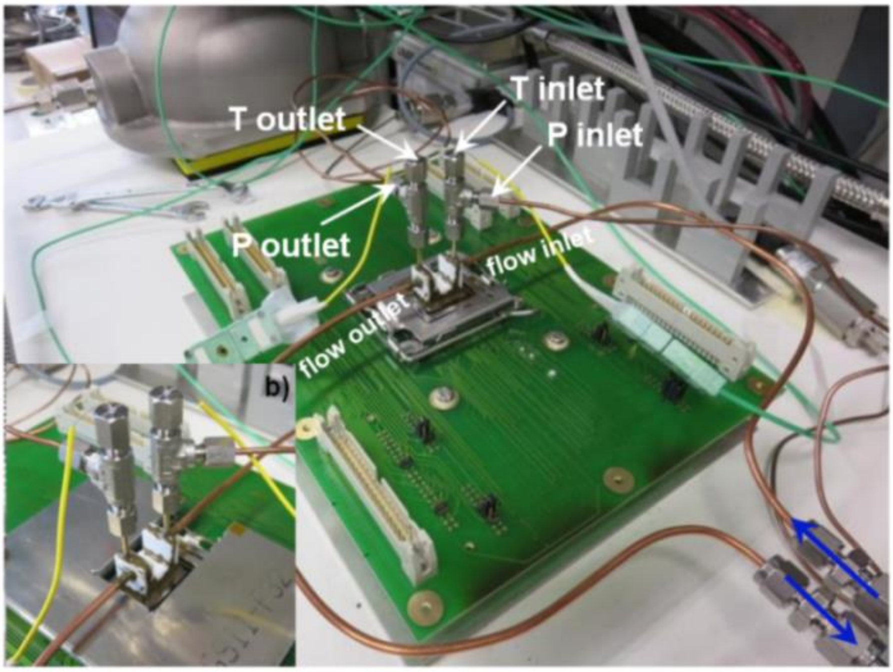

Figure 3.20 Complete 3D chip stack module test section attached to experimental facility (Test Section 1, Figure 3.7), with inlet and outlet manifold temperature and pressure measurements.

Based on the physical observations through the sight glasses during the experiments as well as the observed temperature drops from inlet to outlet, it can be seen that two-phase flow regime was reached adiabatically via refrigerant flashing through the test section, almost for every tested mass flux. It can be hypothesized that for the mass flux of 182.9 kg/m^{2}s, flow boiling is about to start, given the constant inlet to outlet temperature.

This behaviour is surprising given the high inlet subcooling conditions (5 to 10°C). Looking at other chips from the same wafer batch, fabrication defects appear to have modified and dramatically reduced the flow cross-sectional area. Shown on Figure 3.22, these defects range from clogged channels (Figure 3.22A), to narrower than expected channel width (85 instead of 100µm, Figure 3.22B), to finally much smaller inlet orifices (Figure 3.22C). Not only can these defects cause higher than usual pressure drops, they also make it not possible to compare results to the model described in the following chapter, since it is not known for how much of the total pressure drop these defects account.

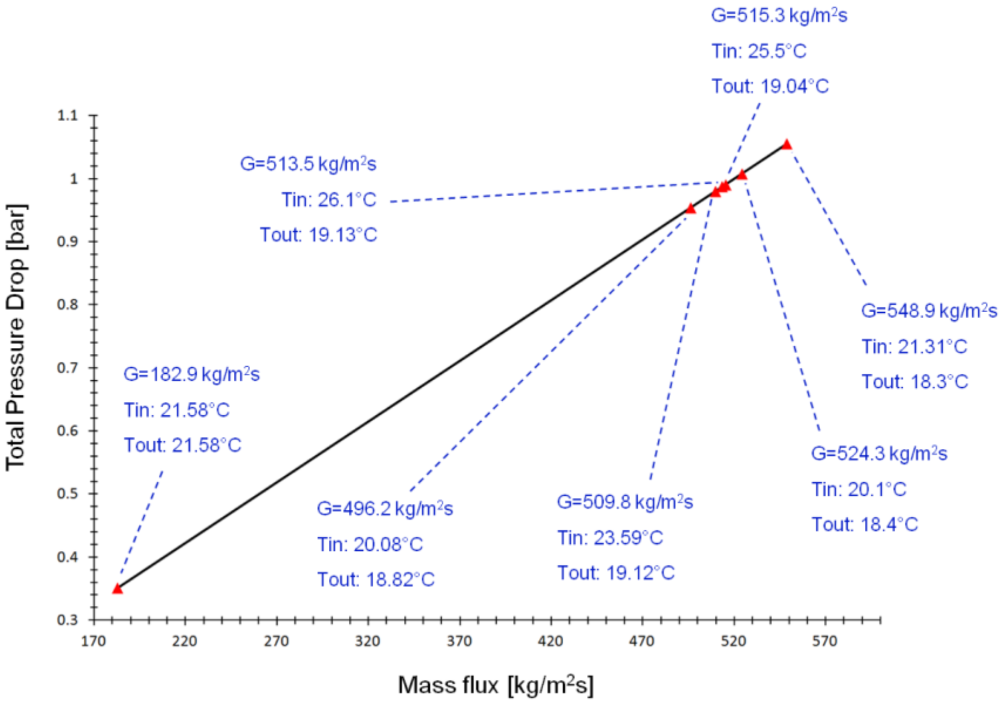

Figure 3.21 Total adiabatic pressure drop values for increasing channel mass fluxes from 183 to 549 kg/m^{2}s. Inlet and outlet temperature conditions are indicated for each pressure drop data point.

Figure 3.21 also shows that the total test vehicle pressure drop increases with mass flux, as it was observed by Agostini et al. [29] in microscale heat transfer structures.

Finally, regarding potential heat transfer tests within the 3D chip stack, it was observed that after prolonged exposure to high pressure, several die-to-die solder interconnects on each one of the five chips started failing (loss of electrical contact). This could have happened due to the fact that some of the solder sealing rails (Figure 3.19A) at the side edge did not survive the dicing process, where chips were separated from the wafer, and delaminated from their respective UBMs, probably because the rails extended from the top to the bottom of the chip (Figure 3.17) and were put in direct contact with the dicing saw. As a result, an epoxy (thixotropic EpoTek epoxy H70E-4, two components, thermally conductive, thermally insulating epoxy adhesive) was used and smeared over the sides of the chip stack to properly seal it, and in return this epoxy’s elasticity might have caused die-to-die interconnects to detach due to the prolonged exposure to high fluidic pressure. This unfortunately rendered the initially planned subsequential heat transfer tests impossible (after the initial pressure drop tests), given the scarce number of available TSV wafers on which to repeat the system fabrication. Hence, no heat transfer tests were possible with the 3D test section.

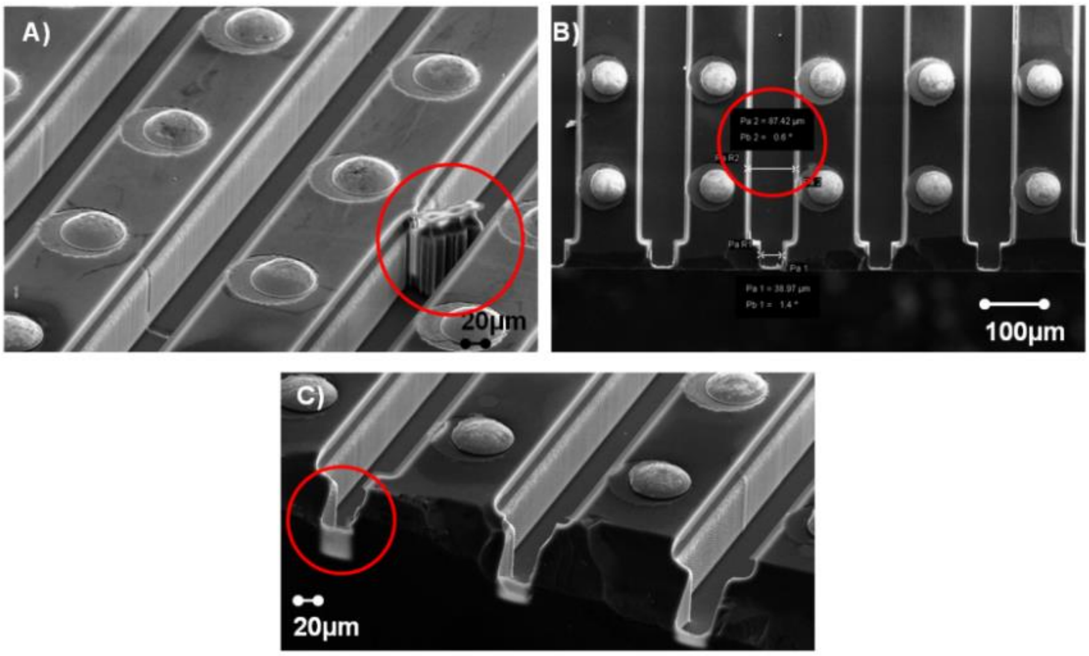

Figure 3.22 SEM photographs of defects due to the DRIE process of the microchannels on the backside of chips LV1 to LV5. A) Blocked microchannels. B) Narrower than expected microchannels. C) Much smaller depth of cavity for inlet orifices in front of microchannels.

3.3 Conclusions

Two different test sections were presented and experimentally tested with different refrigerants. Experiments were conducted for flow boiling of refrigerant R1234ze in a 2D test section with a 120µm-deep silicon staggerd pin fin cavity. High pressure drops (1.5 to 2.5 bar) were observed due to the small flow cross-sectional area for a mass flow rate of 11.5 kg/hr (0.167 l/min). Footprint heat transfer coefficients on the order of 5 W/cm^2K were obtained and a maximum device junction temperature of 40°C was measured for a base heat flux of 66.6 W/cm^2. This points to a good cooling performance and provides enough margin to take further advantage of the evaporation process by increasing the base heat flux and the outlet vapor quality of the system.

More importantly, first-of-a-kind high pressure fluidic tests were successfully achieved within a 3D chip stack with interlayer cooling capabilities and high aspect ratio TSVs. A maximum channel mass flux of 549 kg/m^2s (4.27 kg/hr, 0.053 l/min) was reached and generated an average pressure drop of 1.055 bar (105.5 kPa). However, microchannel fabrication defects reduced the flow cross-sectional area, thus causing the refrigerant to flash and generate large pressure drops for the tested flow rates, even with an inlet subcooling of 5 to 10°C. Finally, loss of electrical contacts occurred within the 3D test section, due to the prolonged high pressure exposure during the pressure drop tests, before the heat transfer tests could be completed.

Chapter 4 Modeling of three-dimensional multi-cavity dielectric evaporative heat transfer

The following results are published in [1]. For the sake of simplicity, this chapter will be introduced with the nomenclature used in the corresponding journal paper, published prior to the wrting of this chapter.

4.1 Nomenclature

F_{Cu}	Volume Fraction of TSVs (dimensionless)
G	Mass Flux (kg m^{-2}s^{-1})
h	Specific Enthalpy (J/kg)
k	Thermal Conductivity (W m^{-1} K^{-1})
L_{cw}	Channel Width (m)
L_{fh}	Fin Height (m)
L_{fw}	Fin Width (m)
L_{hw}	Header Width (m)
P	Pressure (Pa)
q''_{elec}	Metallization Layer Heat Flux (W m^{-2})
$R"$	Thermal contact resistance (K m^{2} W^{-1})
T	Temperature (K)
α	Heat Transfer coefficient (W m^{-2}K^{-1})
η	Fin efficiency (dimensionless)
χ	Vapor Quality (dimensionless)
x,y,z	Spatial Coordinates
LV	Level (1 to 5, chip vertical position in the stack, Figure 4.1b)

E	Evaporator (1 to 4, Figure 3.12b)

4.2 Design framework: CMOSAIC chip stack package

This chapter presents simulation results corresponding to the 3D chip stack module whose design is presented in § 3.2.2. The main differences between the aforementioned presented real design and the following modeling design framework are:

- 10mm x 10mm chip size instead of 12.7mm x 12.7mm.
- 50 microchannels per chip backside instead of 54.
- Chip surface area is equally divided between the 9 heaters for the 3x3 floorplan.

4.3 Method of simulation

The thermal simulations were carried out with the latest version of LTCM's in-house microchannel evaporator code [83] which has been recently modified to accommodate the arbitrary placement of multiple evaporator layers (*E1* to *E4,* Figure 3.12b) and heating layers (LV1 to LV5) within a single microelectronic package. This first-of-a-kind code iteratively considers 3D heat conduction in the solid materials of the microelectronic package (Table 4.1) via a finite difference solution (Figure 4.1) followed by heat transfer and pressure drop in the individual channels using experimentally validated correlations and models. The objective is a steady-state solution for heat and fluid flow which satisfies both thermal considerations and the requirement that each channel—as connected between two shared fluid headers—must have equal pressure drop. Since frictional pressure drop is a strong function of void fraction and the individual thermal path of each channel, the heat and fluid flow are strongly coupled, which unfortunately results in the channels most heavily loaded with heat receiving the least amount of flow. The code also allows calculation of the Critical Heat Flux (CHF) based on the flow in each channel for the analysis of safe operation.

Table 4.1 Chip stack relevant thermal conductivities in W/mK.

Nickel (Ni)	91
Gold (Au)	318
Silver Tin (3.5Ag96.5Sn)	55
Copper (Cu)	400
Silicon (Si)	150
Underfill	0.2
Silicon dioxide (SiO_2)	1.4

LTCM's microchannel code is implemented in MATLAB with fluid properties obtained from the NIST REFPROP (version 8.0) software library. The loop of iteration is depicted by the block diagram in Figure 4.2. The typical simulation time for one of the converging simulation cases presented in §4.4 was about 1 hour.

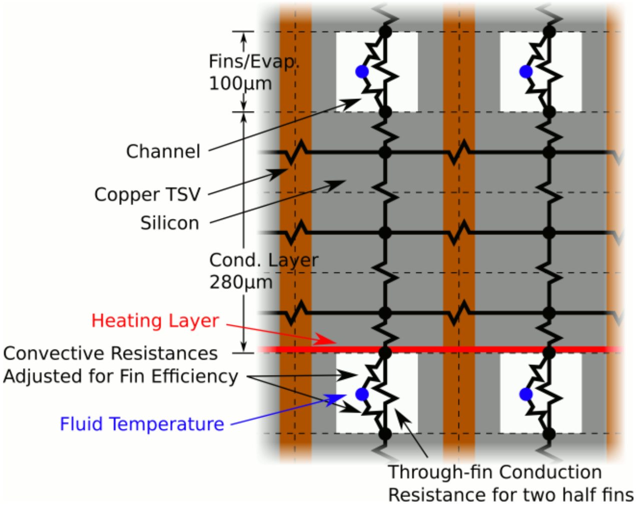
Fins/Evap.
100μm
Channel
Copper TSV
Silicon
Cond. Layer
280μm
Heating Layer
Convective Resistances
Adjusted for Fin Efficiency
Fluid Temperature
Through-fin Conduction
Resistance for two half fins

Figure 4.1 Discretization scheme of chip stack.

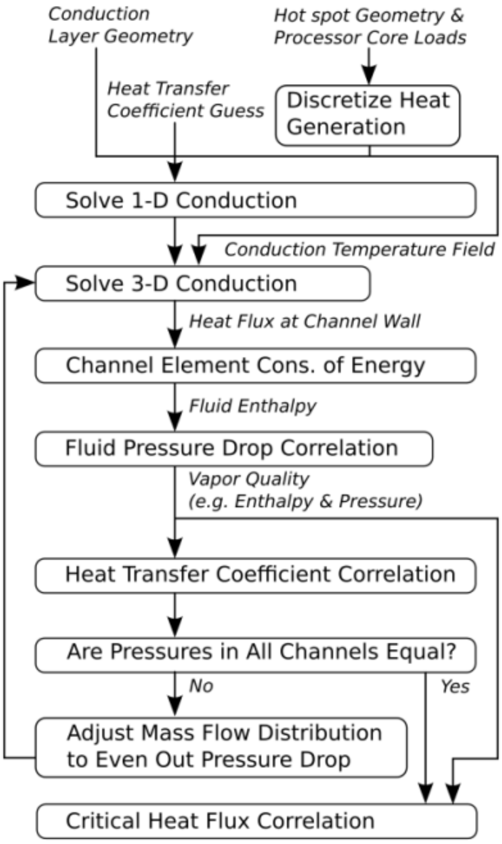
Conduction
Layer Geometry
Hot spot Geometry &
Processor Core Loads
Heat Transfer
Coefficient Guess
Discretize Heat
Generation
Solve 1-D Conduction
Conduction Temperature Field
Solve 3-D Conduction
Heat Flux at Channel Wall
Channel Element Cons. of Energy
Fluid Enthalpy
Fluid Pressure Drop Correlation
Vapor Quality
(e.g. Enthalpy & Pressure)
Heat Transfer Coefficient Correlation
Are Pressures in All Channels Equal?
No
Yes
Adjust Mass Flow Distribution
to Even Out Pressure Drop
Critical Heat Flux Correlation

Figure 4.2 Block diagram of solution technique.

In modeling the chip at the macro scale (i.e. accounting for but not resolving the TSVs), the chip was considered as a homogenous yet anisotropic composite of two isotropic materials. Expressions from Tavman [84] represent the bulk conductivity of a composite consisting of circular fibers spaced regularly on a rectangular array. The conductivity in the vertical direction, along the TSVs, is quite intuitively, an average of that of copper (Cu) and silicon (Si), weighted by the volume fraction of copper.

$$k_{\mathrm{V}} = k_{\mathrm{Si}} + (k_{\mathrm{Cu}} + k_{\mathrm{Si}})F_{\mathrm{Cu}}. \tag{4.1}$$

The conductivity in the horizontal direction, across the TSVs, is

$$k_{\mathrm{H}} = k_{\mathrm{Si}}\left(1 + \frac{2F_{\mathrm{Cu}}}{\frac{k_{\mathrm{Cu}}+k_{\mathrm{Si}}}{k_{\mathrm{Cu}}-k_{\mathrm{Si}}} - F_{\mathrm{Cu}} + \frac{k_{\mathrm{Cu}}-k_{\mathrm{Si}}}{k_{\mathrm{Cu}}+k_{\mathrm{Si}}}\left(0.30584{F_{\mathrm{Cu}}}^{4} + 0.013363\,{F_{\mathrm{Cu}}}^{8}\right)}\right). \tag{4.2}$$

The heat conduction equation is thus

$$\frac{d}{dz}\left(k_{\mathrm{H}}\frac{dT}{dx}\right) + \frac{d}{dz}\left(k_{\mathrm{H}}\frac{dT}{dy}\right) + \frac{d}{dz}\left(k_{\mathrm{V}}\frac{dT}{dz}\right) = 0 \tag{4.3}$$

with adiabatic boundary conditions applied at all edges of the domain. Where the domain is bisected by the evaporators, boundary conditions at the top (t) and bottom (b) of the evaporator come directly from energy balance with Tf being the fluid temperature:

$$\underbrace{\frac{L_{\mathrm{fh}}+L_{\mathrm{cw}}}{L_{\mathrm{fw}}+L_{\mathrm{cw}}}\eta\alpha(T_{\mathrm{t}} - T_{\mathrm{f}})}_{\text{convection}} + \underbrace{\frac{L_{\mathrm{fw}}}{L_{\mathrm{fw}}+L_{\mathrm{cw}}}\frac{k_{\mathrm{A}}}{L_{\mathrm{fh}}}(T_{\mathrm{t}} - T_{\mathrm{b}})}_{\text{cond. through fins}} = \underbrace{k_{\mathrm{A}}\frac{d\mathrm{T}_{\mathrm{t}}}{dz}}_{\text{chip cond.}} + \underbrace{q''_{\mathrm{t,elec}}}_{\substack{\text{heater}\\ \text{(where present)}}} \tag{4.4}$$

$$\frac{L_{\mathrm{fh}}+L_{\mathrm{cw}}}{L_{\mathrm{fw}}+L_{\mathrm{cw}}}\eta\alpha(T_{\mathrm{b}} - T_{\mathrm{f}}) + \frac{L_{\mathrm{fw}}}{L_{\mathrm{fw}}+L_{\mathrm{cw}}}\frac{k_{A}}{L_{\mathrm{fh}}}(T_{\mathrm{b}} - T_{\mathrm{t}}) = -k_{A}\frac{dT_{\mathrm{b}}}{dz} + q''_{\mathrm{b,elec.}} \tag{4.5}$$

The fin efficiency for the two-ended fin, η, including the finite contact resistance at each end of the fin, has been derived as

$$\eta = \frac{(T_{\mathrm{t}}+T_{\mathrm{b}})\,(\cosh(mL)-1) + m\,k(R''_{\mathrm{t}}T_{\mathrm{b}} + R''_{\mathrm{b}}T_{\mathrm{t}})\sinh(m\,L)}{k\,m^{2}(R''_{\mathrm{t}}+R''_{\mathrm{b}})\cosh(m\,L) + m(k^{2}m^{2}R''_{\mathrm{t}}R''_{\mathrm{b}}-1)\sinh(m\,L)} \tag{4.6}$$

where

$$m = \sqrt{\frac{2\,\alpha}{k\,L_{\mathrm{fw}}}}. \tag{4.7}$$

η represents, for the dual ended fin, the ratio of the total convective heat rate to a perfect fin in which temperature varies linearly from T_{t} to T_{b}. Notably, for the two-ended fin, the convective heat rate is not equal to the rate at either end.

The results of the conduction solution can be used to find the enthalpy in each channel

$$\frac{dh}{dz} = \frac{\eta\alpha(L_{\mathrm{fh}}+L_{cw})(T_{\mathrm{t}}+T_{\mathrm{b}}-2T_{\mathrm{f}})}{G\,L_{\mathrm{cw}}L_{\mathrm{fh}}} \tag{4.8}$$

where the numerator is the convective heat rate per unit length and the denominator is the mass flow rate. Meanwhile, pressure drop is solved according to a correlation (function f) which includes both frictional and momentum pressure drop

$$\frac{dP}{dx} = f(h, P, G, fluid, geom.). \tag{4.9}$$

Equations 4.8 and 4.9 are solved for boundary conditions $h(z=0) = h_{\mathrm{i}}$ and $P(z=0) = P_{\mathrm{i}} - \Delta P_{\mathrm{IN}}$, where h_{i} and P_{i} represent the imposed inlet condition. Any appropriate correlation may be used for α and dP/dx. The ones used in this study are described as follows.

Heat transfer coefficient

A new flow pattern-based method [85] uses the Three Zone Model of Thome et al. [35] for the intermittent flow regime and the model of Cioncolini and Thome [38] for the annular flow region (AF). The intermittent flow regime combines the isolated bubble flow (IB) and the coalescing bubble flow (CB) regimes into one. The remaining regime transition (CB-AF) was predicted using a new macro-microscale flow pattern map [86] that can be applied to both the smaller end of macroscale flows and the larger end of microscale flows. This method was recently proven by Szczukiewicz et al. [40] to work well for this fluid and channel size.

Pressure drop

A correlating approach [45], based on the vapor core Weber number, was developed from macroscale data, yet it has been extended to cover microscale conditions, resulting in a unified method for predicting annular flows covering both laminar and turbulent liquid films. The correlation proved accurate for the high aspect ratio channels down to 85 µm width in multi-microchannel experiments of Costa-Patry et al. [48] and the 100×100 µm^2 channels of Szczukiewicz et al [40]. An update of the correlation proposed by Cioncolini et al. [45] was used to consider flows of lower vapor qualities (IB and CB) and also microchannel inlet and outlet restrictions pressure drops, as proposed by Costa-Patry et al. [85]. The pressure loss at the inlet of each channel, P_{IN}, was calculated from single phase flow correlations [87] for an abrupt cross sectional area change from the header (i.e. 1 mm × 10 mm) to the channels (200 × 100µm × 100µm) added to that of the 90° bend. Also, the pressure drop at the outlet was estimated by an empirical correlation for microchannel evaporators [88], stating that

$$\Delta P_{\mathrm{OUT}} = \frac{G^2\chi}{\rho_{\mathrm{V}}}\left(\frac{L_{\mathrm{cw}}}{L_{\mathrm{hw}}}\right)^{0.2274} \tag{4.10}$$

The model assumes that the pressure is uniform across the inlet and outlet headers and considers only the inlet/outlet effects, frictional pressure drop in the channel, and acceleration pressure drop to control the flow distribution.

Critical heat flux (CHF)

Critical heat flux is estimated via a correlation by Ong and Thome [89]. This is based on the modification of a previous correlation by Wojtan et al. [90], which was ultimately proposed as a microscale variant of the Katto-Ohno correlation [91]. The method is also based on the silicon multi-microchannel evaporator experimental data of Agostini et al. for channels down to 223µm in width [28] [44] [92]. CHF is important to determining whether the converged solution is physically viable. Operation in excess of CHF risks severe thermal damage.

4.4 Simulation cases

The present simulation study focuses on the effect of hot spot patterns rather than the parametric design of the evaporators or of the package as a whole. Thus the geometry has been constrained to the design previously described in § 3.2.2, supplied with saturated R236fa at 60°C (see Table 4.2) at an average mass flux of 2300 kg/m^{2}s for all cases. These parameters were selected to represent the removal of high heat fluxes at temperatures suitable for heat recovery applications. However, an inlet condition of 30°C is also briefly considered at the end of the paper, decreasing the working fluid pressure and thus ensuring the mechanical integrity of the previously described package.

Table 4.2 R236fa saturation properties at 30 and 60°C.

Sat. Temperature [°C]	30	60
Sat. Pressure [bar]	3.21	7.64
Liquid Density [kg/m3] ρl	1342.8	1230.2
Vapor Density [kg/m3] ρv	21.57	51.87
Liquid Enthalpy [kJ/kg] hl	237.28	276.98
Vapor Enthalpy [kJ/kg] hv	380.23	399.59
Liquid Viscosity [µPas] µl	268.19	185.1
Vapor Viscosity [µPas] µv	11.036	12.298

Heat was applied in different patterns, all corresponding to variations of a 3 by 3 array (Figure 4.3) of equally sized and equally spaced Hot Spot Heaters (HS) on each of the 4 active layers (LV1 to 4, see Figure 3.12b and Figure 4.4). Based on a desired maximum outlet vapor quality of 33% for the simultaneous heat/two-phase flow spreading situation, the nominal heat flux was chosen to be 50 W/cm^2. Previous experiments in 2D configurations (one evaporator only) with the same channel size have shown that this level of heat flux can be safely supported [41].

First, as a baseline case, all heaters on all four layers (LV1 to LV4) were activated at 50 W/cm^2 for a total of 200 W within the chip stack (Heat Load Pattern 1, Figure 4.4a). Secondly, each heating layer was activated independently at 50 W/cm^2 per HS, including an additional case with a fifth layer at the extreme top of the chip stack. The latter case being the worst case scenario, it is presented as Heat Load Pattern 2 (Figure 4.4b). Next, beginning the study of parallel-to-flow hot spots, only heaters in the center column (see Figure 4.3, i.e. three heaters consecutively along the flow direction) were activated (Heat Load Pattern 3, Figure 4.4c). Then, only heaters in the left column were activated (Heat Load Pattern 4, Figure 4.4d). For symmetry reasons, the right column was not separately studied. Finally, Heat Load Pattern 5 (Figure 4.4e) activated columns in a staggered fashion (i.e. HS columns 2,1,3,2, see Figure 4.3, on layers LV1 through 4 of the stack respectively). In this case, the application of heat to each individual chip matches one of the previously tested configurations, but the overall distribution of heat across the package is substantially more uniform.

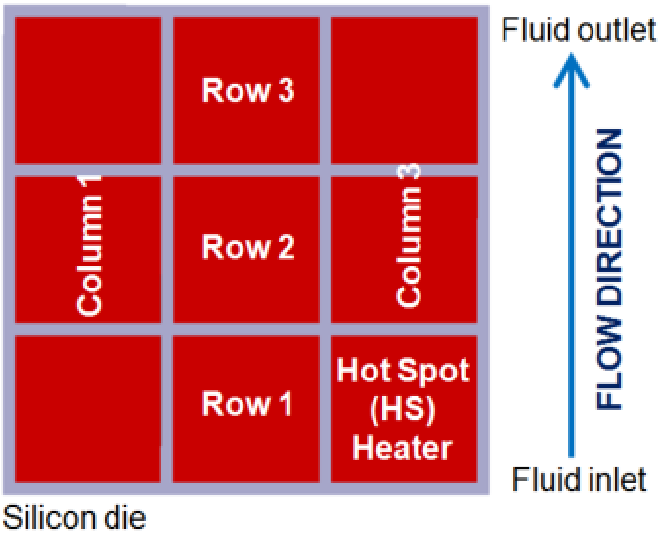

Figure 4.3 front view of single 10×10 mm2 chip with 3x3 hot spot array layout. Microchannels are etched on the back.

In a second phase of the study, results for each of these patterns were simulated for various heat fluxes at 2 W/cm^2 increments, in order to determine the maximum heat flux that can be sustained without exceeding 33% vapor quality at the exit of any channel.

A similar study was conducted for perpendicular-to-flow hot spots, in which all channels were heated, but over only a third of their length. The first row (i.e. closest to the inlet) was activated (Heat Load Pattern 6), then the second (Heat Load Pattern 7), and finally the third (Heat Load Pattern 8). After that the heat load was staggered across HS rows 2,1,3,2 (Heat Load Pattern 9, Figure 4.4f) on layers LV1 through 4 of the stack respectively.

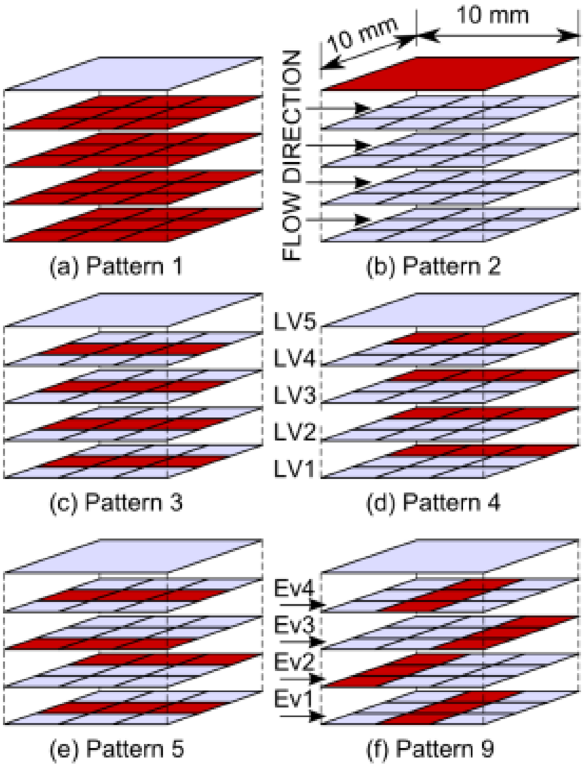

Figure 4.4 Illustrations of the various patterns of active heaters applied to studied chip stack package.

4.5 Results

Uniform heating—All heaters on at the chip level

Results of the simulations show a strong effect of thermal spreading between the layers, which is effective in attenuating non-uniform heating within the chip stack. However, for the nominal full power case (Heat Load Pattern 1, at 50 W/cm^2 per HS and per chip), there is an interesting gradient of temperature through the stack thickness, as shown in Figure 4.5. The plot shows the distribution of temperature through the thickness of the stack (dimension Z, see Figure 3.12b) at several axial locations along the flow direction (i.e. the channel inlet, channel outlet, and center points of each of the three heating elements at 1/6, 1/2, and 5/6 of the channel length respectively), for the middle channels. The vertical lines on the graph delineate the top and bottom of the 100 µm-tall silicon fins which form each evaporator layer. The temperature distribution is uniform laterally (thus not shown). The axial variation on the graph (i.e. difference between the curves) is due to the changes in fluid temperature and in heat transfer coefficient with increasing vapor quality along the channel. The temperature ultimately decreases toward the channel exit due to the pressure drop in the saturated mixture. The gradient of temperature was not anticipated but can easily be explained. For Heat Load Pattern 1, if the chips were thermally insulated from each other, the conditions at each chip would be identical, resulting in identical temperature gradients to the other chips. Despite having all heaters on all chips, stacking the chips with the hot side of one chip bonded to the cold end of the fins on the next necessarily alters the distribution of heat amongst the layers. Since the chips are of small thermal resistance relative to the convective heat transfer resistance at the channels, the heat load of the upper three heated layers (LV2 to LV4) is effectively shared among the four evaporator layers between which they are situated (E1 to E4), and the LV1 heated layer biases the stack towards higher temperatures and heat load at the bottom, as illustrated by Figure 4.5 and Table 4.3.

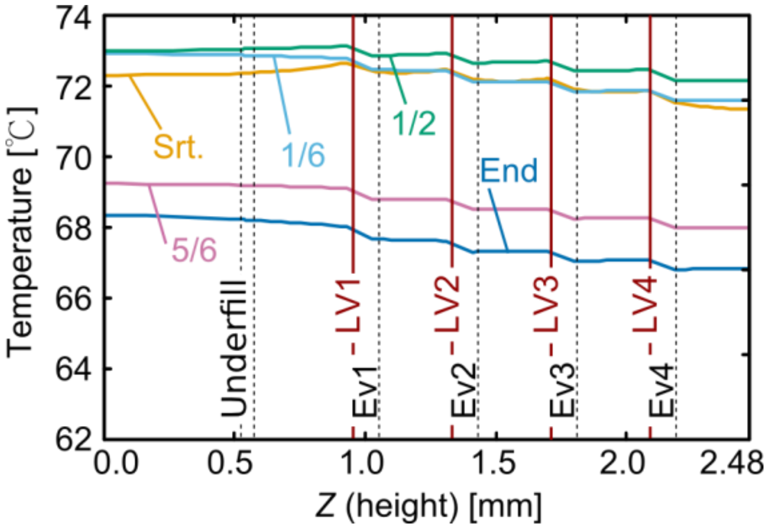

Figure 4.5 Temperature vs. vertical position within the chip stack for Heat Load Pattern 1 at 50 W/cm^2 per chip.

Strong interlayer heat spreading is exhibited when only one heater layer is activated and is, in this context, a favorable aspect for the chip designer. Figure 4.6 and Table 4.4 show results for Heat Load Pattern 2 (all heat at the top of the stack, Figure 4.4b) at 50 W/cm^2 per HS and per chip, which results in the temperature distribution being skewed and heat conduction being directed downwards in the stack. Thus, only 32% of the heat is removed by the top evaporator layer *E4*, with the rest passing through the fins of this evaporator into the rest of the stack below. However, reduction in coolant flow in the most heavily heated channels means that CHF is reduced where the heat flux is highest and that variations of outlet vapor quality are accentuated.

Table 4.3 Results for Heat Load Pattern 1 at 50 W/cm^2 per chip.

Metallization Layer	LV1	LV2	LV3	LV4	LV5
Total Heat (W)	50.0	50.0	50.0	50.0	0.0
Total Heat (%)	25.0	25.0	25.0	25.0	0.0
Max Junc. Temp (°C)	74.3	74.2	74.0	73.8	73.4

Evaporator	Ev1	Ev2	Ev3	Ev4
Max. Wall Temp (°C)	74.3	74.2	74.0	73.8
Max. Vapor Quality (%)	33.6	32.4	31.4	30.3
Total Heat Removed (%)	25.6	25.2	24.8	24.4
Total Mass Flow (%)	24.2	24.7	25.3	25.9
Max Frac. of CHF (%)	26.7	25.5	24.4	23.3

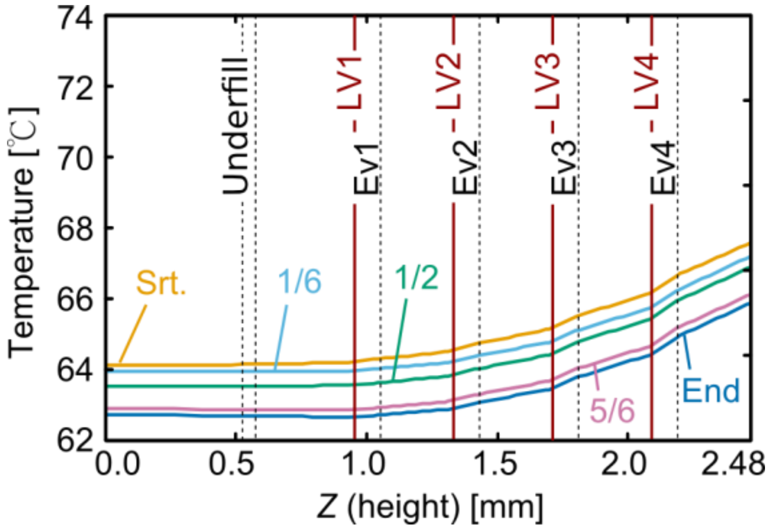

Figure 4.6 Temperature vs. vertical position within the chip stack for Heat load Pattern 2 at 50 W/cm^2 per chip.

Parallel-to-Flow (Column) Hot Spots

The study of parallel-to-flow hot spots (activation of a column of heaters in the flow direction, see Figure 4.3) reveals strong effects of the HS placement on the mass flow distribution width-wise through the evaporator and substantial benefits in distributing hot spots in different locations on different chips in the stack. Figure 4.7 shows the mass flux distribution across all channels for each layer, which results from shutting down the left and right portions of each chip and leaving the center third of each chip active (Heat Load Pattern 3, Figure 4.4c). A depression of mass flow is apparent in the center. As a result, the maximum safe heat flux is reduced compared to the case where all heaters were active (Heat Load Pattern 1). Figure 4.7 shows results for a heat flux of 38 W/cm^2 per HS. The maximum outlet vapor quality is 32.5% and comparable to the fully active chip at 50 W/cm^2. Moving this column of heat from the center to the left of the chip (Heat Load Pattern 4, Figure 4.4d) results in fewer lateral spreading, and further reduces the allowable heat flux.

Table 4.4 Results for Heat Load Pattern 2 at 50 W/cm^2 per chip.

Metallization Layer	LV1	LV2	LV3	LV4	LV5
Total Heat (W)	0.0	0.0	0.0	0.0	50.0
Total Heat (%)	0.0	0.0	0.0	0.0	100.0
Max Junc. Temp (°C)	64.2	64.5	65.1	66.2	67.6

Evaporator	Ev1	Ev2	Ev3	Ev4
Max. Wall Temp (°C)	64.2	64.5	65.1	66.2
Max. Vapor Quality (%)	7.1	7.8	9.1	11.8
Total Heat Removed (%)	20.7	22.3	25.8	31.3
Total Mass Flow (%)	27.1	26.2	24.8	22.0
Max Frac. of CHF (%)	19.6	21.4	25.5	33.5

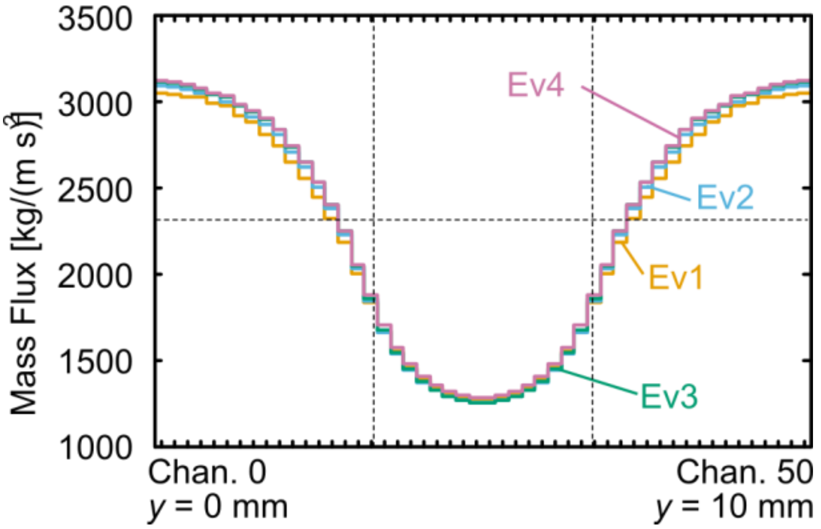

Figure 4.7 Mass flux by channel across each evaporator; 10×10 mm^2 chip; Heat Load Pattern 3 at 38 W/cm^2; T_{SAT} = 60°C.

Figure 4.8 shows the mass flow distribution for this pattern at 24 W/cm^2, which results in a maximum outlet vapor quality of 31.9%. At heat fluxes above 44 W/cm^2 per HS, the left-most channel is predicted to completely dry out (i.e. achieve quality of one). This is extremely significant to the chip designer, since it suggests that a chip properly designed to handle 50 W/cm^2 on all heaters, with a large margin of safety, would start overheating if two thirds of the chip are shut down leaving only the left side active, in the flow direction. The acceptable heat flux (with less than 33% outlet quality) is thus reduced by 52% relative to the baseline case.

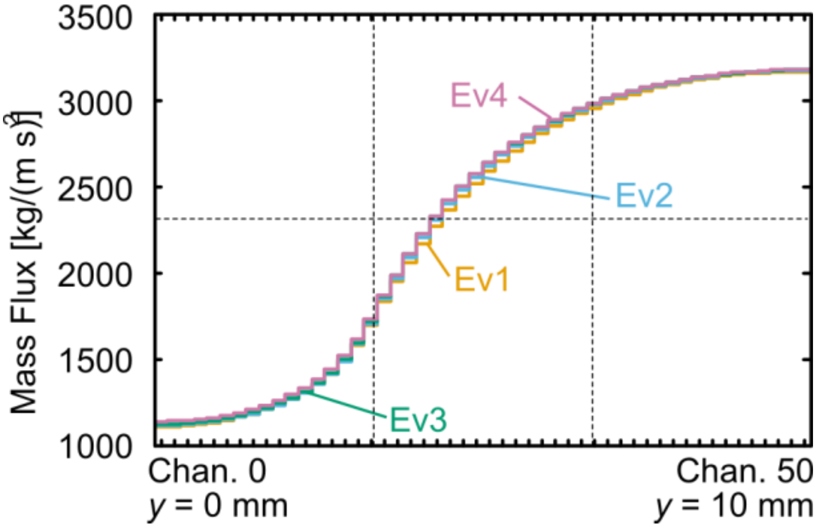

Figure 4.8 Mass flux by channel across each evaporator; 10×10 mm^2 chip; Heat Load Pattern 4 at 24 W/cm^2; T_{SAT} = 60°C.

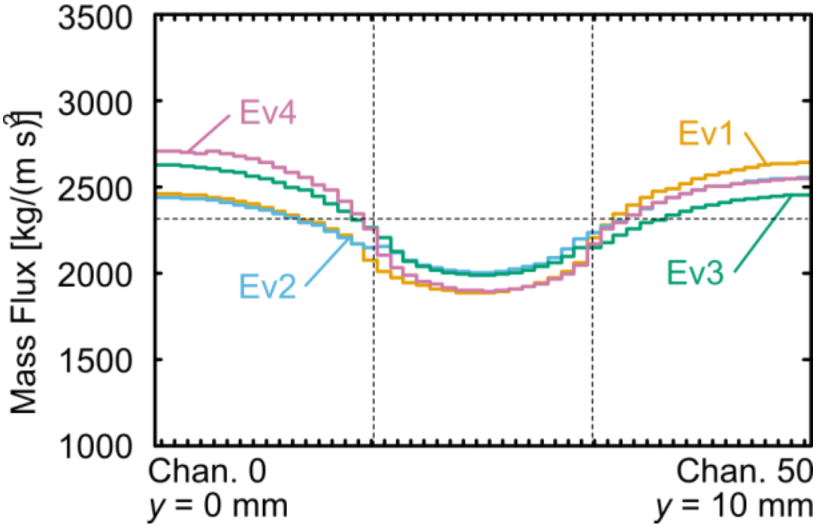

Figure 4.9 Mass flux by channel across each evaporator; 10×10 mm^2 chip; Heat Load Pattern 5 at 50 W/cm^2; T_{SAT} = 60°C.

Staggering the hot spots on different columns in the direction of the flow, for different layers, results in a more uniform mass flow distribution. Such results (Heat Load Pattern 5, Figure 4.4e) are shown on Figure 4.9. Since it is not possible to evenly distribute the load on the three heater columns over the four chips (LV1 to 4), there is still double the total heat load on the center channels compared to the sides, which is the reason for the apparent depression of mass flow in the center channels on each layer. At 50 W/cm^2 in the staggered pattern, the maximum outlet vapor quality is only 17.6%. Heat flux can be increased to 82 W/cm^2 per HS for a maximum outlet vapor quality of 33%. Notably, the flow distribution shown on Figure 4.10 is only slightly different than the one seen on Figure 4.9, indicating that this increase in heat flux for the same heating pattern has a relatively small effect on the mass flow distribution.

The heat transfer coefficients, heat fluxes, and pressure drops are depicted in Figures 4.11 and 4.12, corresponding to the middle channel (channel 25 out 50) for the same simulation case as the one presented on Figure 4.10 (Heat Load Pattern 5, 82 W/cm^2 per HS). The overall trend of the heat transfer coefficient (Figure 4.11) is a result of the two-phase flow development with increasing vapor quality along the channel. The heat transfer coefficients are low at the very beginning of the channel, where the fluid arrives as a single-phase saturated liquid. The heat transfer coefficient then rises dramatically with the beginning of the isolated bubble regime. Between 2 mm and 3 mm along the channel the thickness of the films surrounding the bubbles has thinned such that intermittent dry zones are formed at the tail of the bubbles, and the heat transfer coefficient falls off sharply (although CHF is not reached since the wall is rewetted by the next liquid slug). Beyond 3 mm, the flow enters the annular regime and the heat transfer coefficient increases as the annular film gets thinner.

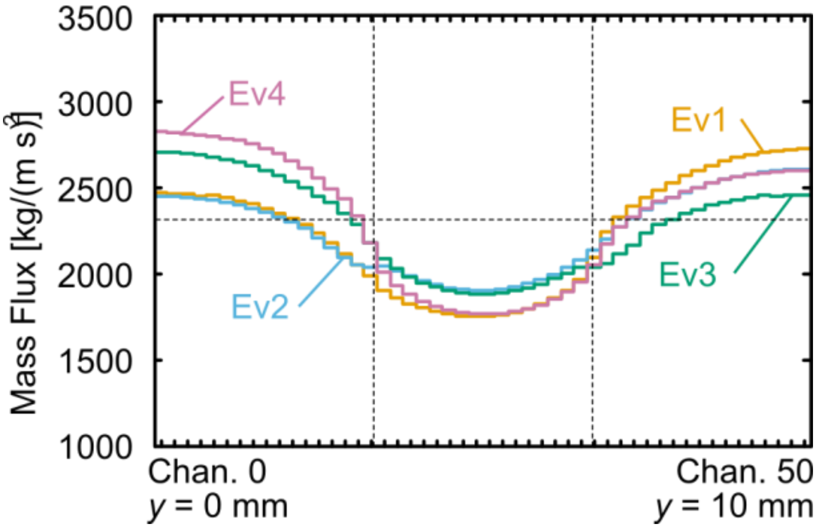

Figure 4.10 Mass flux by channel across each evaporator; 10×10 mm^2 chip; Heat Load Pattern 5 at 82 W/cm^2; T_{SAT} = 60°C.

Heat is concentrated within the zones of high heat transfer coefficient, and as illustrated in Figure 4.11, the heat flux follows the trend established by the heat transfer coefficient. In Figure 4.11, evaporators E1 and E4 show higher heat transfer on the center channel than E2 and E3 since, for Heat Load Pattern 5 (Figure 4.4e), these are nearest to the heaters which are activated in the center section. The higher heat flux is responsible for the higher maximum heat transfer coefficient in nucleate boiling. The higher heat flux and lower mass flow rate are jointly responsible for the higher vapor quality and earlier transition to annular flow. Additionally, since the total channel wall area (400 µm single channel perimeter × 10 mm channel length × 50 channels) for one evaporator layer is twice the chip footprint area (10×10 mm2), a HS heat flux of 82 W/cm2 nominally corresponds to a channel wall heat flux of 41 W/cm2. Actual average heat fluxes on the middle channel are lower than this due to lateral and vertical spreading into unheated zones.

The numbers for thermal resistance, over the total 10 mm × 10 mm area of the chip stack, put the relative contributions into perspective. The total thermal resistance for conduction from the top to bottom of the four heated chip layers is 0.135 K/W. Of this 0.012 K/W is contributed by the 280 µm thick base of each chip, 0.017 K/W is contributed by the conduction through the fins of each evaporator, and 0.004 K/W is contributed by the solder connection at the bottom of each evaporator to the next chip. By comparison, selecting a heat transfer coefficient of 35000 W/m2K (from Figure 4.13) as representative, the thermal resistance to convection is 0.286 K/W. Thus, the resistance to heat convection into a single micro evaporator is roughly twice that of the entire chip stack. Therefore, the two-phase heat transfer process is the most important component to accurately model 3D chip stacks with interlayer cooling.

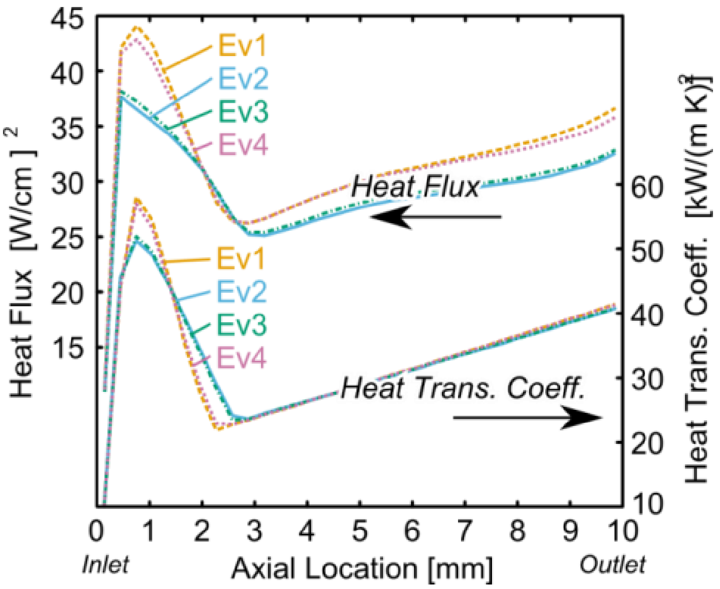

Figure 4.11 Heat flux and heat transfer coefficient versus axial position along the center channel. Heat Load Pattern 5 at 82 W/cm^2; T_{SAT} = 60°C.

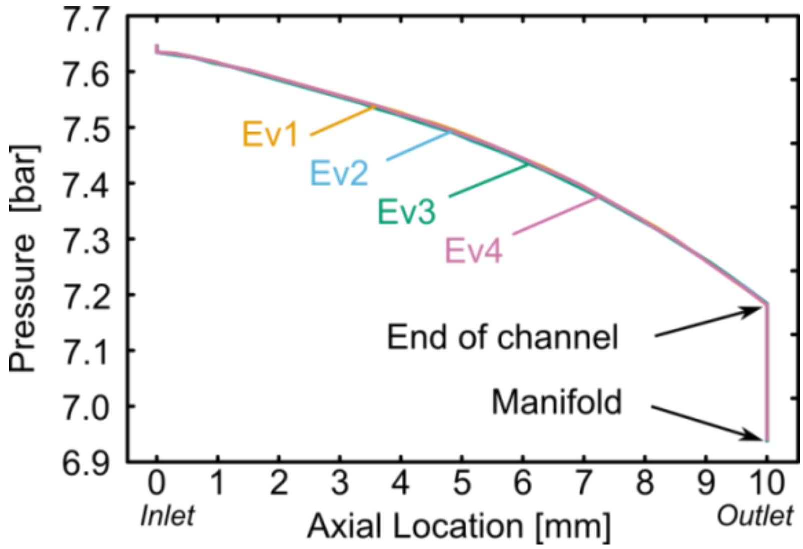

Figure 4.12 Fluid pressure along the center channel, Heat Load Pattern 5 at 82 W/cm^2; T_{SAT} = 60°C.

Given that the manifold inlet pressures have been constrained to be equal, pressure profiles along the channels are essentially indistinguishable, as shown in Figure 4.12. The pressure drop associated with the flow of single phase liquid from the inlet manifold to the entrance of the channels is small, but the one associated with the two-phase flow mixture exiting the manifold is significant. Unfortunately, these results could not be compared to the interlayer pressure drop data presented in § 3.2.5, mainly due to the fabrication imperfections that disturbed the experimental results.

Table 4.5 summarizes the strong advantage of the staggered configuration of hot spots on the various chips. The allowable heat flux, within acceptable bounds of outlet vapor quality, is increased more than three-fold relative to the left-side only pattern (Heat Load Pattern 4, Figure 4.4d), even though the total active heated area is the same within the stack.

Table 4.5 Summary of results for parallel-to-flow hot spots.

Heat Load Pattern	HS Location	Heat Flux per HS [W/cm^2]	Max. Junction Temp. [°C]	Fraction of CHF (%)	Max. Vapor Quality (%)
3	Mid. (Col. 2)	38	70.1	25.6	32.5
4	Left (Col. 1)	24	69.1	26.5	31.9
5	Col. 2,1,3,2	50	67.7	26.7	17.6
		82	71.8	28.0	33.0

Perpendicular to Flow (Row) Hot Spots

The study of the placement of perpendicular-to-flow hot spots, occupying a full row of the heater array across the width of the chip (see Figure 4.3), is summarized in Table 4.6 and shows that staggering hot spots reduces peak temperatures.

Table 4.6 Summary of results for perpendicular-to-flow hot spots.

Heat Load Pattern	HS Location	Heat Flux per HS [W/cm^2]	Max. Junction Temp. [°C]	Fraction of CHF (%)	Max. Vapor Quality (%)
6	First (Row 1)	50.0	71.8	25.8%	12.2
7	Mid. (Row 2)	50.0	70.5	25.4%	11.7
8	Last (Row 3)	50.0	74.0	25.5%	11.4
9	Rows 2,1,3,2	50.0	67.2	25.6%	11.7

In these cases, the heat load is always uniform across the width of the evaporator, so there is no lateral flow imbalance, since all the channels experience the same heat load. Outlet vapor qualities are also small and pose little concern, since only a third of each channel is heated. For Heat Load Patterns 6, 7, and 8 the positioning of hot spots is the same on each layer within the stack (see Table 4.6) and thus there is only a small flow imbalance between the evaporator layers. This means that in this perpendicular configuration, actually staggering the hot spots very slightly *increases* the flow imbalance, evidenced in the reported vapor quality numbers in Table 4.6 for Heat Load Pattern 9 (Figure 4.4f), compared to the previous three patterns. However, the peak heat flux incident on the channel wall is considerably reduced, resulting in a reduction in peak junction temperature for the staggered case.

Effect of Saturation Temperature

Repeating the same pattern and intensity of heat shown on Figure 4.8 (Heat Load Pattern 4 at 24 W/cm^2 per HS), but this time with the fluid inlet saturation temperature reduced to 30°C, slightly increases the flow imbalance while also decreasing the maximum outlet vapor quality. This mass flow distribution is shown on Figure 4.13. Table 4.7 compares the new results to the ones previously presented at 60°C on Figure 4.8. The flow imbalance is increased due to the lower refrigerant vapor density at 30°C and thus larger volumetric generation of vapor (i.e. 153 mm^3 J^{-1} at 30°C versus 82 mm^3 J^{-1}). However, this happened at lower outlet vapor qualities due to the higher latent heat of vaporization. The stepwise jumps in the right portion of Figure 4.13 are due to the laminar-turbulent transition in the liquid flow used in the Lockhart-Martinelli portion of the Cioncolini model [45]. These are evident at 30°C and not at 60°C due to the differences in liquid viscosity (see Table 4.7).

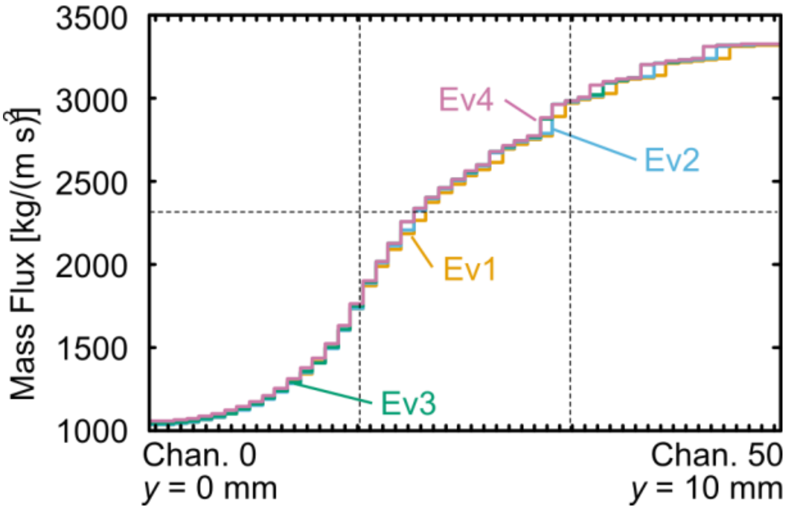

Figure 4.13 Mass flux by channel across each evaporator; 10×10 mm^2 chip; Heat Load Pattern 4 at 24 W/cm^2; T_{SAT} = 30°C.

General Discussion

The strong stack conductance due to the low chip thermal resistances compared to the convection from solid to fluid promotes good heat load sharing amongst the evaporator layers. The implication is that in multi-evaporator scenarios with hot spots, there may exist an optimum heat transfer coefficient relative to the conductance of the surrounding layers, which is sufficiently large to allow the conveyance of heat from the wall to the microchannel, but not so large that the channel closest to the hot spot absorbs an excessive share of the heat load causing channel dryout or excessive outlet vapor quality. Additionally, strong intra-stack conductance relative to convection from the fins was observed to result in the step-like temperature profile through the thickness of the chip, shown on Figure 4.5, which is not a favorable effect for temperature uniformity. Notably, under uniform and non uniform heat loads, both of these aspects would discourage the use of large aspect ratio fins, which increase the effect of convection while decreasing interlayer conductance.

A further issue is that the thermal consequence of dryout and CHF may require substantial rethinking in the context of such microevaporator designs. In the traditional context of single layer (2D) heat flux-controlled microevaporators, these are considered do-not-exceed limits. Thus there has in the past been little incentive to study post-dryout heat transfer or consider it as a viable regime for operation. In the context of the multi-evaporator chip stack this concept is considerably altered, since excursions of the channel wall temperature are limited by the effect of conduction to adjacent layers.

Table 4.7 Comparison of results for Heat Load Pattern 4 at 24 W/cm^2 per HS, for two different fluid inlet temperatures. The junction temperatures are only about 9-10 K above the saturation temperatures in both cases, illustrating the effectiveness of the interlayer cooling approach.

Inlet Fluid Sat. Temperature	60°C	30°C
Max. Outlet Quality (%)	31.9	27.1
Max. Junction Temp. (°C)	69.1	39.6
Total Pressure Drop (bar)	0.33	0.52

4.6 Conclusions

A real-life fabricated 3D chip stack module with integrated cooling has been presented along with its corresponding simulation results, showing the sensitivity of the two-phase flow to the arrangement of hot spots among the layers. The model combines a finite difference solution to the 3D heat conduction in the solid materials with heat transfer and pressure drop in embedded microchannels, using existing, experimentally validated correlations and models.

The strong intra-stack conductance compared to the convection from solid to fluid was well illustrated in the case where only the top most chip in the stack (LV5) was heated, which resulted in only 32% of the heat removed by the closest evaporator (*E4*), with the rest passing through the fins into the rest of the stack below.

The importance of intra-stack heat spreading and the need for a holistic design of all thermal loads and all evaporators are illustrated by contrasting heat flux required in each of the following cases to obtain the same maximum outlet quality of 33%:

- 50 W/cm^2 applied uniformly to each of the four heaters (Heat Load Pattern 1), for a total of 200 W to the package.
- 38 W/cm^2 applied to only the center third laterally (Pattern 3) for a total of 50.7 W to the package.
- 24 W/cm^2 applied to one lateral third of the chip (Pattern 4) for a total of 32.0 W.
- 82 W/cm^2 staggered such that two chips are active in the center third and one on each lateral edge (Pattern 5), for a total of 109.3 W.

Note that the above results show that, in contrast with single phase cooling, shutting down the heat flux on two thirds of the chip reduces the maximum heat flux allowable into the remaining portion due to flow imbalance. Each of the later three cases have the same number of hot spots covering the same shapes and area, so the improvement in allowable heat flux is attributable solely to the effect on the flow in all evaporators of the HS placement on each layer.

For hot spots spanning the width of the chip rather than length, staggering the position is less advantageous. Staggering hot spots along the direction of flow (Pattern 9) increases flow imbalance and slightly increases maximum outlet vapor qualities compared to placing all hot spots in the same sector along the direction of flow (Patterns 6, 7, 8). However, spreading the heat over a large portion of the chip still results in a junction temperature reduction.

Chapter 5 Conclusions and outlook

5.1 Thesis contributions and impact

This thesis was part of a multidisciplinary project called CMOS Advanced Interlayer Cooling (CMOSAIC), funded by the Swiss National Science Foundation. The goal of this project as previously stated was the development of the first ever worldwide prototype 3D IC thermal package with TSVs and single- and two-phase liquid cooling capabilities, as well as the definition of design and manufacturing guidelines for similar future devices. This work in particular was responsible for the design, manufacturing, assembly and fluidic testing of the first ever 3D stack of chips with high aspect ratio TSVs and integrated two-phase cooling capabilities. Various aspects of the work in this thesis have been the result of collaborative efforts between the industry (IBM Research, Zürich) and other academic research groups at EPFL and ETH (the LTCM, LSM and ESL laboratories at EPFL and the LTNT laboratory at ETH).

5.1.1 Solder bonding technology – novel structures

A new concept for the integration of intra chip stack fluidic cooling was presented, namely die-embedded microchannels for single- and two-phase thermal management, using a patterned thin-layer eutectic solder bonding technique for the stack assembly. **Results showed the successful fabrication of 5-layer chip stacks with embedded microchannels and high aspect ratio TSVs**. Optical inspections demonstrated the proper bond line formation and direct current (DC) daisy-chain electrical tests indicated the successful combination of TSVs with thin-layer solder interconnects. Mechanical shear tests on die-on-die bonded samples showed the strength of the patterned thin-layer solder bond (16MPa). An added solder ring-pad component to seal the electrically active pad from any conductive liquid coolant was also investigated and reflow tests on such geometries showed the appearance of a balling effect along the solder ring line. This balling was found to be mitigated when the ring aspect ratio (deposited solder height to ring width ratio) was kept below the experimentally observed critical value of 0.65.

Keeping in mind the thermal stress relief within IC packages, an innovative approach for electrical chip to substrate and chip to chip interconnects was proposed. The coexistence of solder balls and rails on a chip was discussed, supporting power delivery and heat removal for high-performance flip-chip-on-board and 3D stack applications. The rail shaped solder joints are also compatible with the current floorplans of microprocessors with voltages arranged in lines. After reflow, solder rails compared to balls sometimes resulted in a much larger maximal solder width relative to their pads. Therefore, a staggered array arrangement was proposed to minimize shorting risk. In addition, a solder height engineering strategy utilizing modulated pad shapes was discussed to yield equal solder heights for balls and rails present on the same device. However, improper rail design was found to lead to two instability types: 1) Balling and 2) Asymmetric Solder Accumulation. The first was the result of a solder height to width ratio of larger than approximately 0.6 considering long rail lines. The second occured due to fabrication imperfections. The initial non-symmetric pad / solder shape can cause the accumulation of solder at one rail end (typically the end with the larger area) after reflow. The stability of Bow Tie Rails against Asymmetric Solder Accumulation was investigated to provide design rules for a robust rail design. Accordingly, a solder shape phase diagram indicating the parameters of the three identified phases was compiled. Experimental investigations of reflown solder shapes were complemented with numerical results using a surface energy minimization tool called Surface Evolver. A prediction quality of better than 9% was identified indicating the applicability of the tool to perform solder shape design. The solver was also capable to predict the mentioned instabilities, rendering the tool even more valuable. Finally, a thermal interface resistance benchmark of ball and rail-like interconnects is performed in a bulk thermal tester. The rail interface with a solder fill factor of 57% yielded a 7 times reduced interface resistance.

5.1.2 3D integrated chip stack with embedded cooling structures - fabrication, assembly and fluidic testing

A first-of-a-kind three-dimensional stack of five silicon chips with high aspect ratio TSVs and chip backside-embedded microchannels for integrated interlayer two-phase flow cooling was designed, fabricated, assembled and successfully tested with pressurized refrigerant R236fa at 3.3 bar absolute pressure, for the first time. The chip stack survived the initial pressurization tests up to 4 bar absolute pressure, thus allowing the pursuit of two-phase pressure drop measurements. These experiments showed unexpected refrigerant flashing inside the inlet manifold with 10°C of inlet subcooling, as well as high pressure drops. Probable explanations are the fabrication defects on the silicon microchannels: it was observed that some of the channels were simply clogged, that their width was inferior to the desired 100µm and that their inlet orifices did not have the same cavity depth. All these factors decrease the flow cross-section even more, possibly causing the early flashing and high pressure drop measurements. Regarding heat transfer tests however, after prolonged exposure to high pressure, several die-to-die solder interconnects on each one of the five chips started failing, rendering the initially planned subsequential heat transfer tests unfortunately impossible, given the scarce amount of TSV wafers on which to work on. Nevertheless, this novel chip stack survived for a certain period first-of-a-kind high pressure fluidic tests.

5.1.3 Modeling of three-dimensional heat and mass transfer in multi-cavity systems

A novel mechanistic modeling method was presented and used to determine the ideal heat load placement, from a thermal point of view, within a 3D chip stack with interlayer cooling. This was done by solving three-dimensional heat spreading and fluid flow. Simulation results showed a strong effect of thermal spreading between the dies, since these are of small thermal resistance compared to the convective heat transfer coefficient at the channels, which is effective in attenuating non-uniform heating within the chip stack. A staggered hot spot configuration along the flow direction was found to yield the highest heat flux (82 W/cm^2) for the same fixed outlet vapor quality (33%).

5.2 Looking into the Future

To intelligently build upon the findings of this thesis, the following directions, defined by topic, are proposed as a to-do list here for the future scientist(s).

Solder sealing rings

To advance the full integration of electrical, structural and liquid functions in 3D stacks, all functions need to be demonstrated. Leak tests could determine the proper functionality of the proposed sealing method, for instance by direct-current (DC) electrical measurements between the central active pad and the sealing ring in presence of water.

Solder rails

The measured interface thermal resistances showed the improvement offered by such solder shapes in relieving thermal stress between two silicon dies. However this is only one side of the characterization. To qualify the proposed solder rails for high-performance applications, additional experiments need to be performed to determine their electromigration yield current and their thermo-mechanical compatibility for joints between chip and laminate. Additionally, there is still room for improvement regarding the electrodeposition process of different solder shapes on a single wafer. This will always be a complex process to master due its difficult repeatability, but efforts need to be made to improve the galvanic bath’s keep-up by better controlling the electrolyte’s chemical content and natural decay over time, and by ensuring a better agitation within the bath (adapted to the size of the wafer) during plating for an enhanced deposition uniformity across the surface.

3D module: chip stack with high aspect ratio TSVs and integrated cooling capabilities

Regarding the assembled 3D module, a better optimization of the TSV filling process is needed so that it can be used without a great amount of modifications for different TSV floorplans (and sizes) across the wafer. Also, the solder lines sealing the sides of the chip should not go all the way from one edge of the chip to the other, so that they can survive the wafer dicing process following their fabrication. Ensuring this happens will allow a better overall attachment between the dies, and remove the need to “seal” the sides of the chip stack with an elastic epoxy that might have caused die-to-die interconnects to detach due to the prolonged exposure to two-phase flow high pressure. Finally, two-phase heat transfer data within the 3D chip stack module need to be acquired in order to start validating the newly proposed 3D heat and fluid flow thermal model.

Flow boiling of refrigerants in 2D silicon pin fins cavity

A more detailed experimental investigation should be considered from the following points of view regarding the silicon pin fin test section presented in §3.1: high speed camera imaging for the observation of flow development and the various flow patterns for flow boiling of refrigerants in pin fins structures and 2) complementary IR imaging as well as pressure drop measurements for an extended range of flow rates and base heat fluxes to construct a heat transfer coefficient database that will be used to update (or create new) microscale heat transfer and pressure drop models so far mainly adapted to microchannels. In the author’s opinion, the quality of the experimental campaign should parallel the one offered by Szczukiewicz et al. [40] for similarly-sized silicon microchannels. Finally, the next step for pin fins structures is their inclusion within a three-dimensional package design, which would impose similar challenges as the ones discussed in chapter 2 (see §2.1, Figure 2.2).

Modeling of three-dimensional flow boiling of refrigerants in 3D chip stacks

The proposed model in Chapter 4, in addition to allowing a parametric study of heat load placement within a multi-cavity multi-microchannel chip stack, should be also be utilized to optimize the design of the multiple evaporators within the stack (cross-section, length, size of inlet orifices etc.) vis-à-vis certain pre-defined heat loads. Finally, the model should be enhanced in a way that allows its user to choose between different types of heat transfer geometries, such as pin fins.

Appendix A

CMOSAIC Package Assembly Process

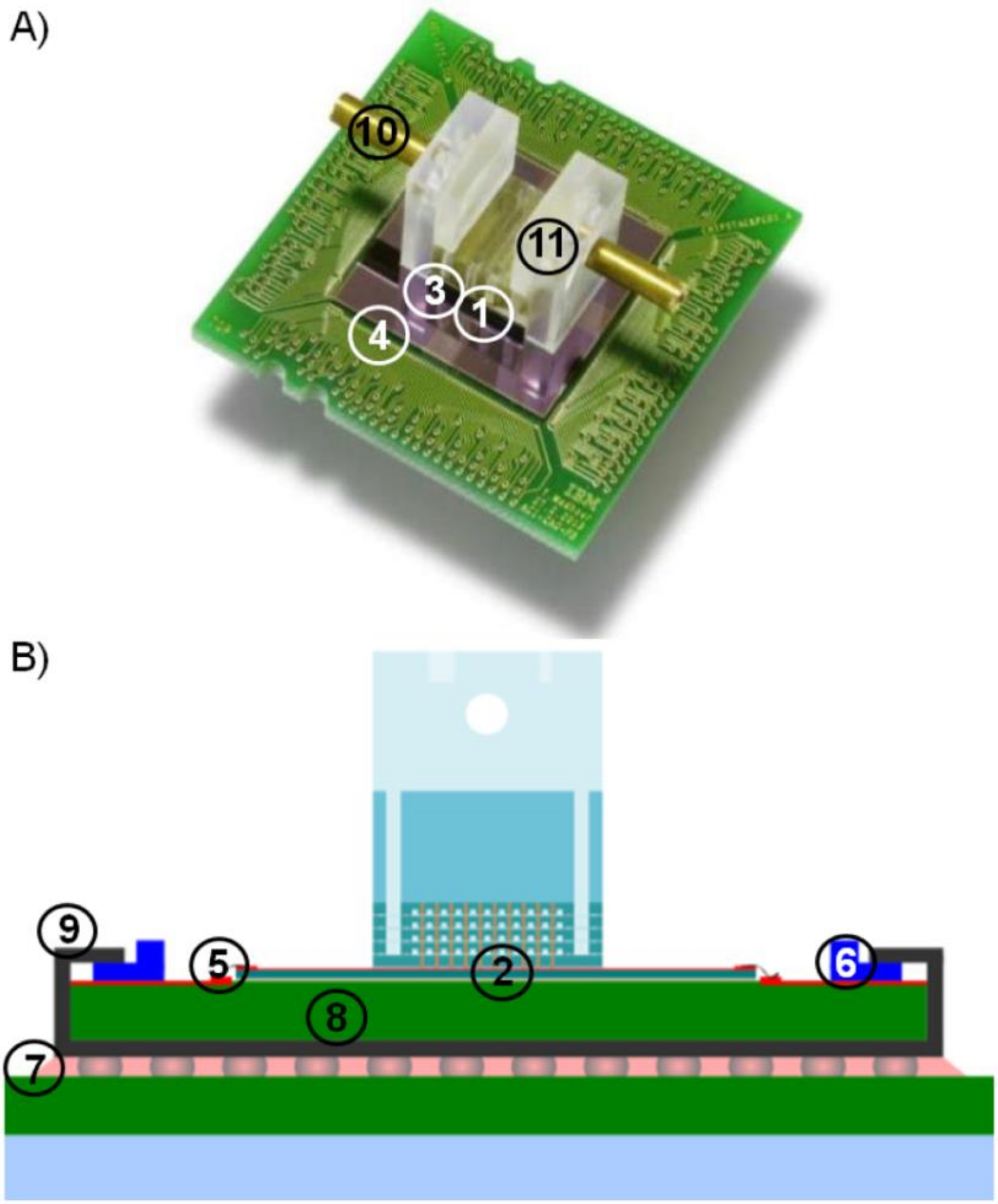

Figure A. 1 A) Photo of real-life built demonstrator of a 3D chip stack module with integrated cooling capabilities. B) 2D schematic side view of package (flow direction against the image). The numbers correspond to the processes on the assembly line order described below.

1. Chip stack flip chip bonding with Silicon interposer chip
2. Underfilling between level 1 and interposer
    - U300-2 EpoTek underfill
3. Glue smearing on side of the stack for optimal sealing and add. mechanical support
    - EpoTek H70E-4
4. Stack gluing to PCB1 – EpoTek H70E-4
    - EpoTek H70E-4 – Electrically insulating and thermally conductive
5. Wire-bonding PCB1 to interposer chip
    - Wedge-wedge Aluminum wire bond (25um-thick wires)
    - Glob top for wire bonding
6. Gluing of PCB1 clamping frame (stainless steel) to PCB1
    - Alignment marks on PCB1 for manual alignment
    - EpoTek H70E-4 (low CTE, electrically insulating)
7. Solder bonding LGA-to-BGA socket to PCB2
    - Foxconn socket F
    - With flux FW259 and solder paste
8. Insertion of stack on PCB1 package inside Foxconn socket F
9. Close and clamp socket
10. Insertion and gluing of initial tubing on manifold (Macor) parts
    - Thermocouples connectors
    - Pressure sensors connectors
11. Gluing of Macor manifold around stack
    - order: top, inlet/outlet cavities, inlet/outlet covers
    - EpoTek H70E-4

Foxconn LGA/BGA socket F (1207) [94]

The socket used to link the two PCBs of the CMOSAIC 3D chip stack module described in Chapter 3.2 is the Foxconn AMD Socket F that carries 1207 pins. In the case of the CMOSAIC design, only 288 pins on the edge of the socket are used: 4 layers x 9 heaters/ layer x 8 connections/ heater = 288 needed connections. Figure A.2 and A.3 show the socket's functioning, design and outline.

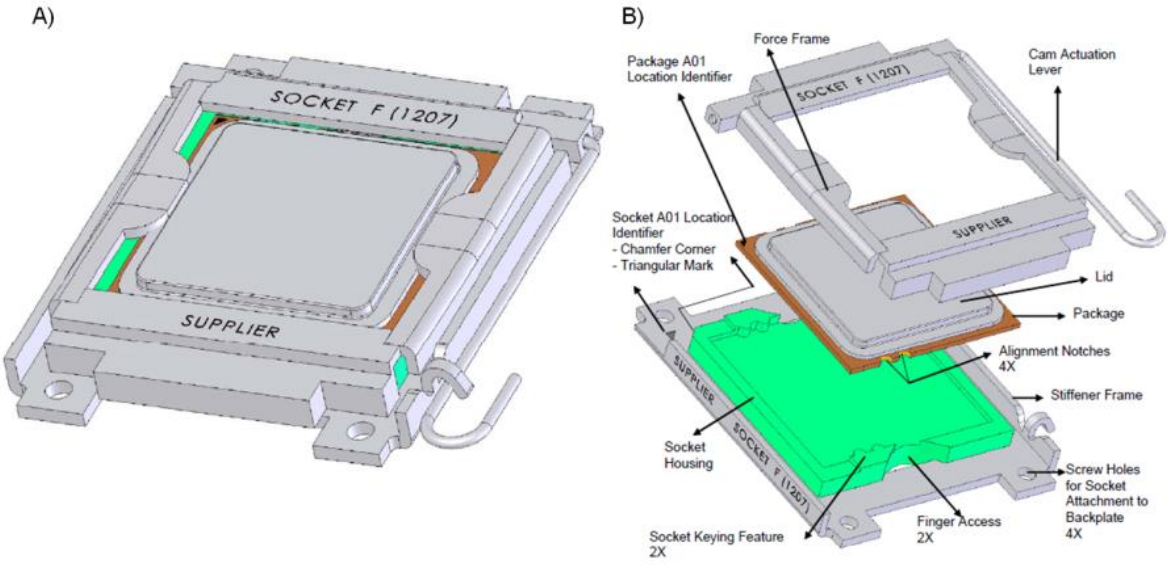
A)
SOCKET F (1207)
SUPPLIER
B)
Force Frame
Package A01
Location Identifier
Cam Actuation
Lever
SOCKET F (1207)
SUPPLIER
Socket A01 Location
Identifier
- Chamfer Corner
- Triangular Mark
Lid
Package
Alignment Notches
4X
Stiffener Frame
Socket
Housing
Screw Holes
for Socket
Attachment to
Backplate
4X
SUPPLIER
SOCKET F (1207)
Socket Keying Feature
2X
Finger Access
2X

Figure A. 2 A) A 3D view of socket F. B) 3D view of its assembly components. The "package" here is generic. It corresponds to the PCB1 with the attached interposer chip and 3D stack (see §3.2.2) in the CMOSAIC module. The "lid" here would correspond to the PCB1's clamping frame described in §3.2.2.

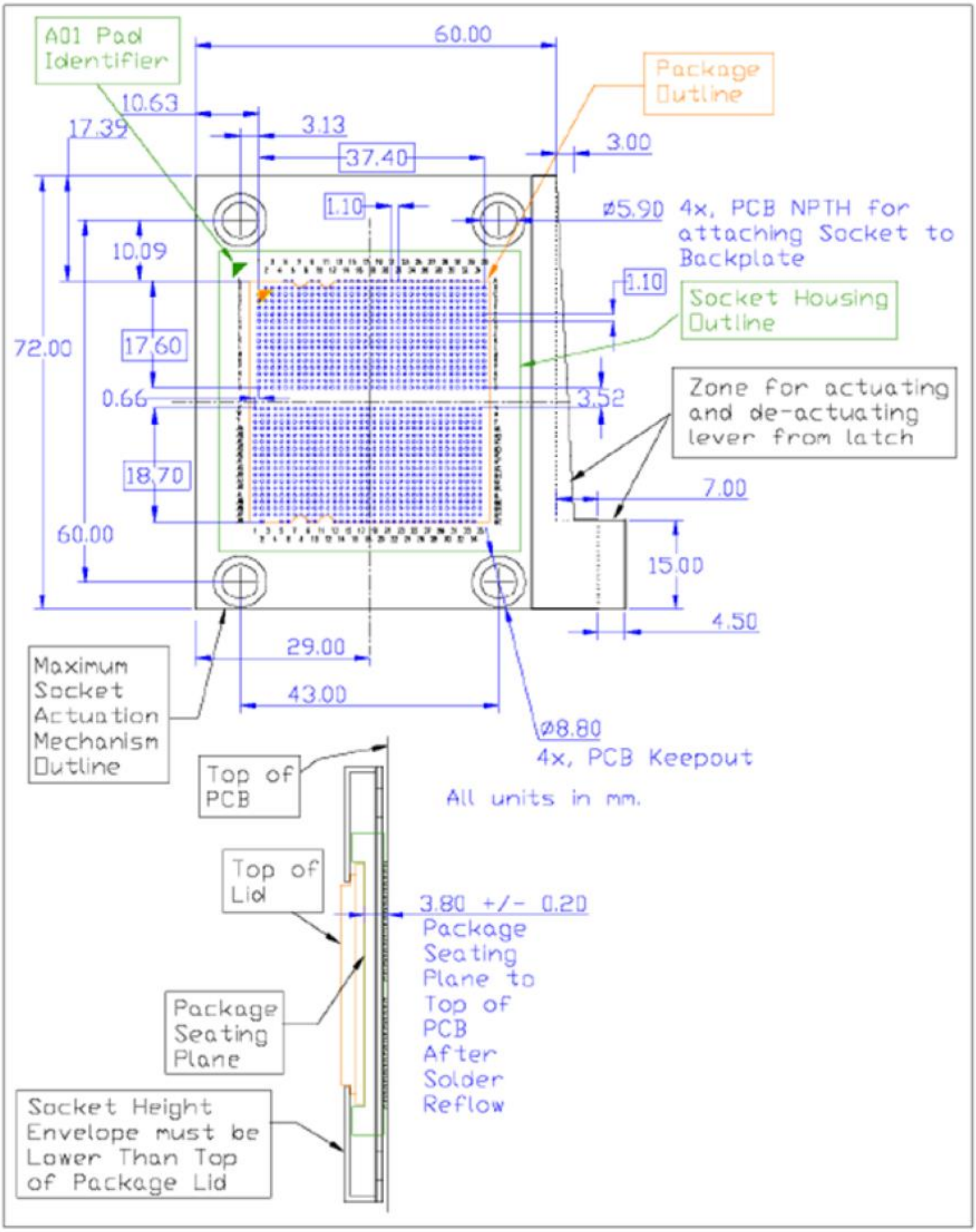
A01 Pad Identifier
60.00
Package Outline
10.63
17.39
3.13
37.40
3.00
1.10
Ø5.90 4x, PCB NPTH for attaching Socket to Backplate
10.09
1.10
Socket Housing Outline
72.00
17.60
0.66
3.52
Zone for actuating and de-actuating lever from latch
18.70
7.00
60.00
15.00
4.50
29.00
43.00
Maximum Socket Actuation Mechanism Outline
Ø8.80
4x, PCB Keepout
Top of PCB
All units in mm.
Top of Lid
3.80 +/- 0.20
Package Seating Plane to Top of PCB After Solder Reflow
Package Seating Plane
Socket Height Envelope must be Lower Than Top of Package Lid

Figure A. 3 Socket F (1207) outline.

Hot spot meander heater CFD modeling

The meander hot spot heaters whose design is presented in §3.2.2 required CFD modeling of their temperature response to the electrical excitation (Joule heating modeling), in order to assess if their design was appropriate by looking at the heat spreading along the meanders. ANSYS software was used to derive the following results, which showed a maximum ΔT of 1.7 [°C] across the heater's surface, making the design of the meander acceptable.

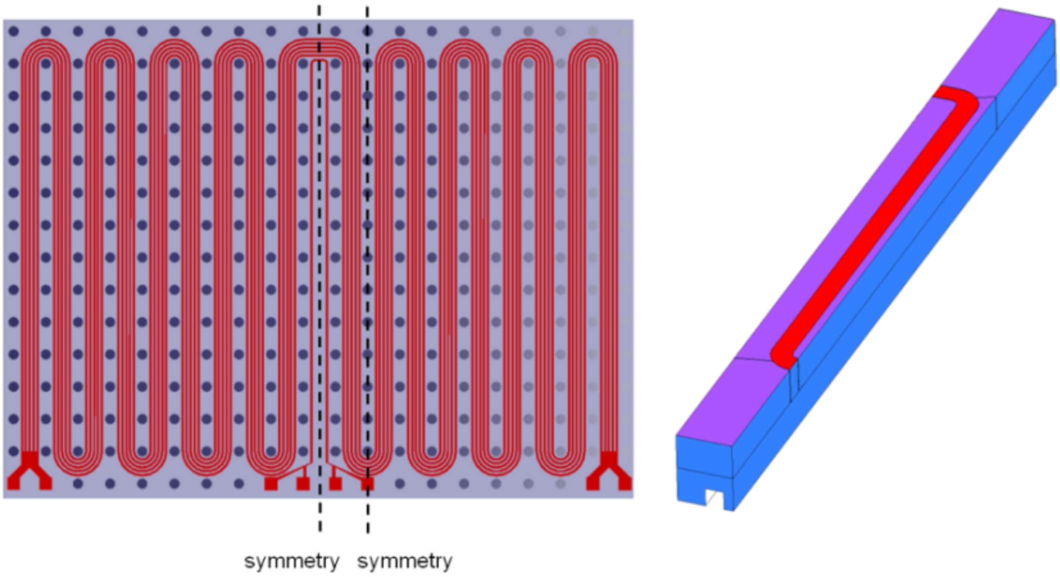
symmetry
symmetry

Figure A. 4 Modeling domain definition through symmetry.

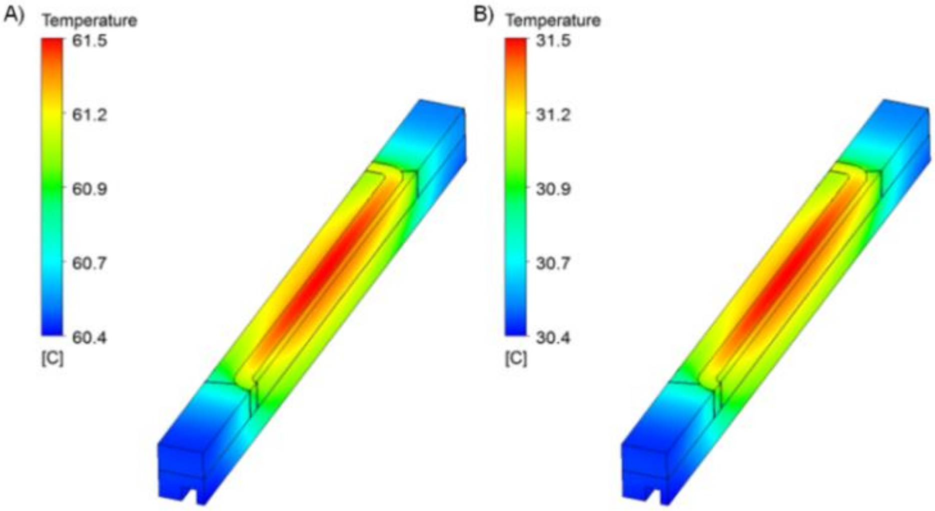
A)
Temperature
61.5
61.2
60.9
60.7
60.4
[C]
B)
Temperature
31.5
31.2
30.9
30.7
30.4
[C]

Figure A. 5 Model results for a high heat transfer coefficient setting (50 kW/m^{2}K). A) Refrigerant temperature at 60°C. B) Refrigerant temperature at 30°C.

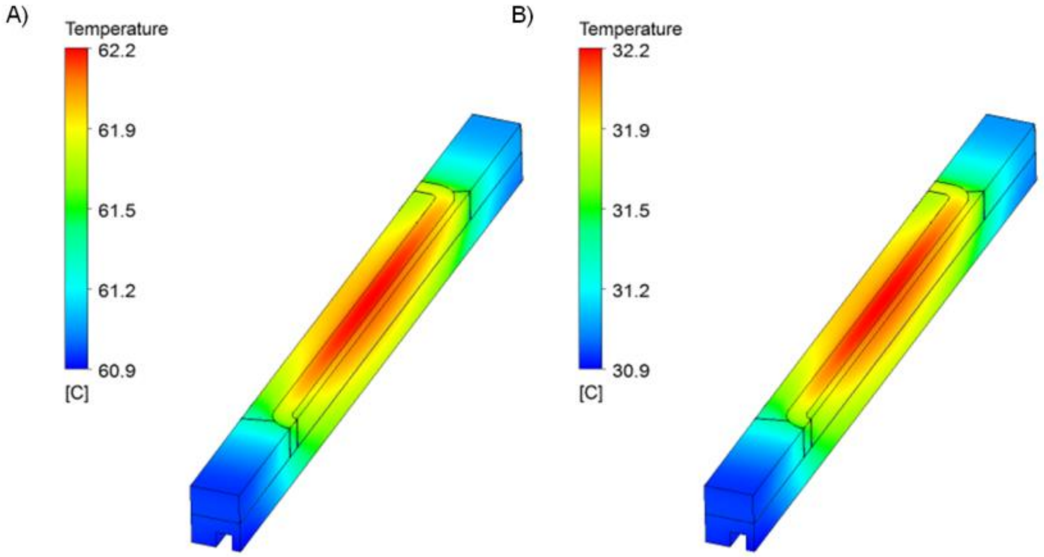
A)
Temperature
62.2
61.9
61.5
61.2
60.9
[C]
B)
Temperature
32.2
31.9
31.5
31.2
30.9
[C]

Figure A. 6 Model results for a middle-range heat transfer coefficient setting (30 kW/m^{2}K). A) Refrigerant temperature at 60°C. B) Refrigerant temperature at 30°C.

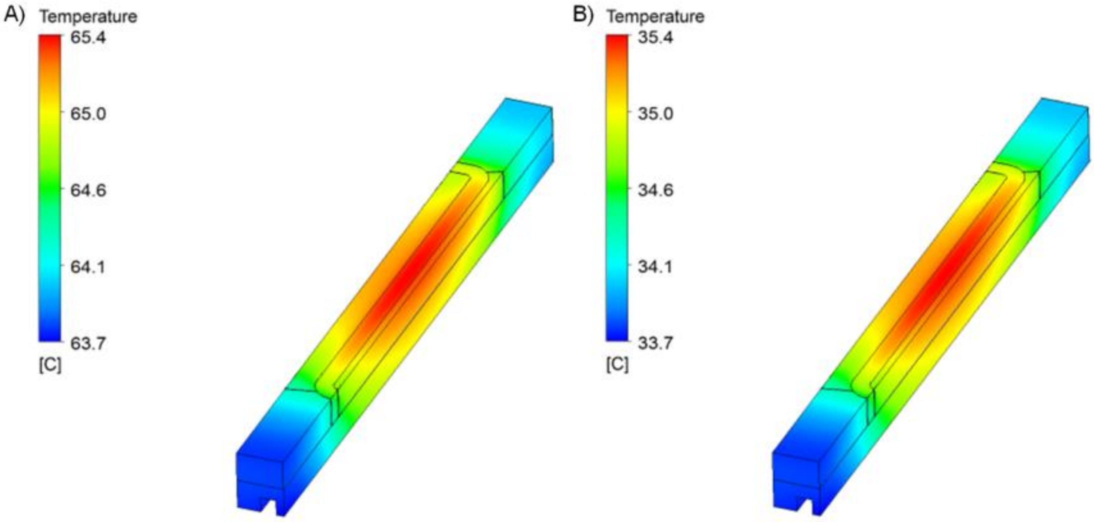
A)
Temperature
65.4
65.0
64.6
64.1
63.7
[C]
B)
Temperature
35.4
35.0
34.6
34.1
33.7
[C]

Figure A. 7 Model results for a very low heat transfer coefficient setting (10 kW/m^{2}K). A) Refrigerant temperature at 60°C. B) Refrigerant temperature at 30°C.

Appendix B

The following presents the InfraRed images resulting from the 2D pin fins test vehicle presented in §3.1. Each image corresponds to an increasingly different background heat flux as defined in §3.1. The orientation of the flow and of the image is indicated on each figure. The indicated pixel numbers define the area of interest, where the background heater is (horizontal and vertical limits).

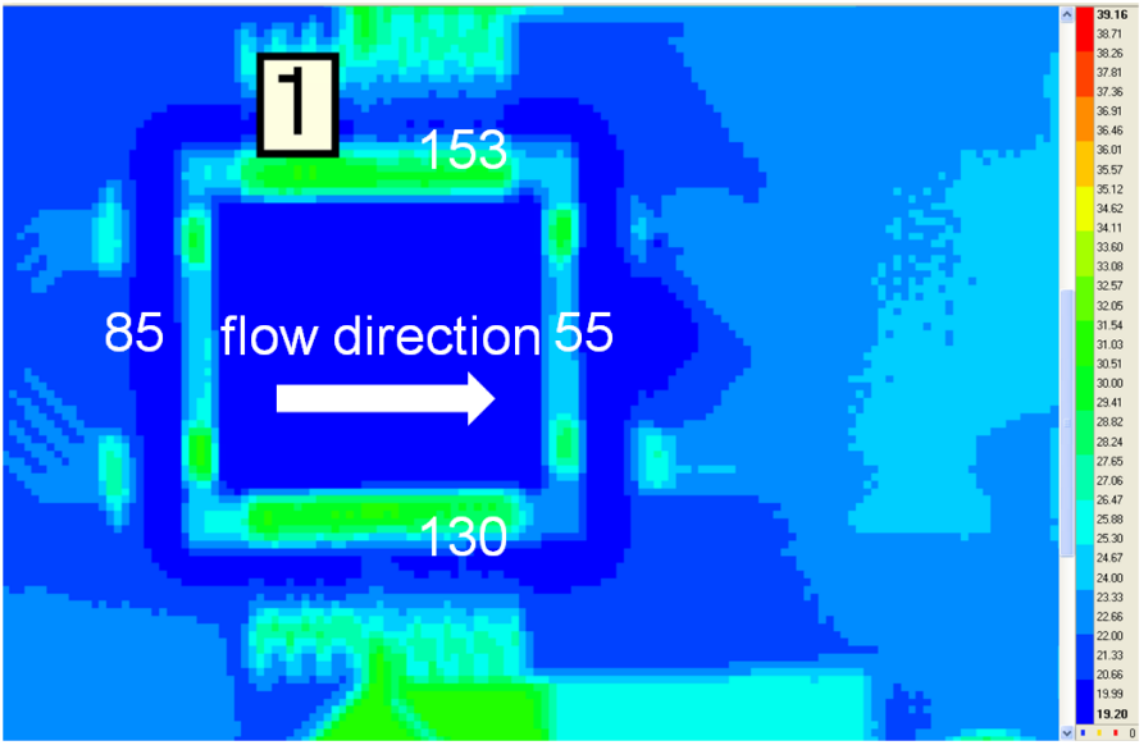

Figure B. 1 Temperature response for q_b = 1.5 W/cm^2, and a flow rate of 11.5kg/hr for flow boiling of R1234ze.

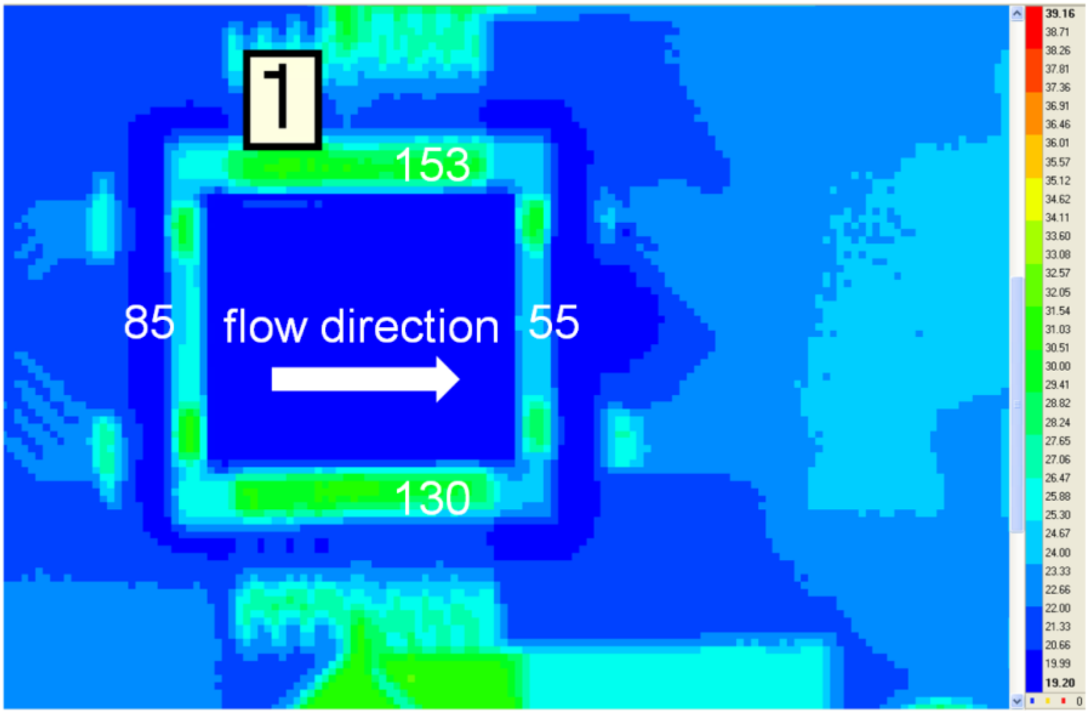

Figure B. 2 Temperature response for q_b = 6 W/cm^2, and a flow rate of 11.5kg/hr for flow boiling of R1234ze.

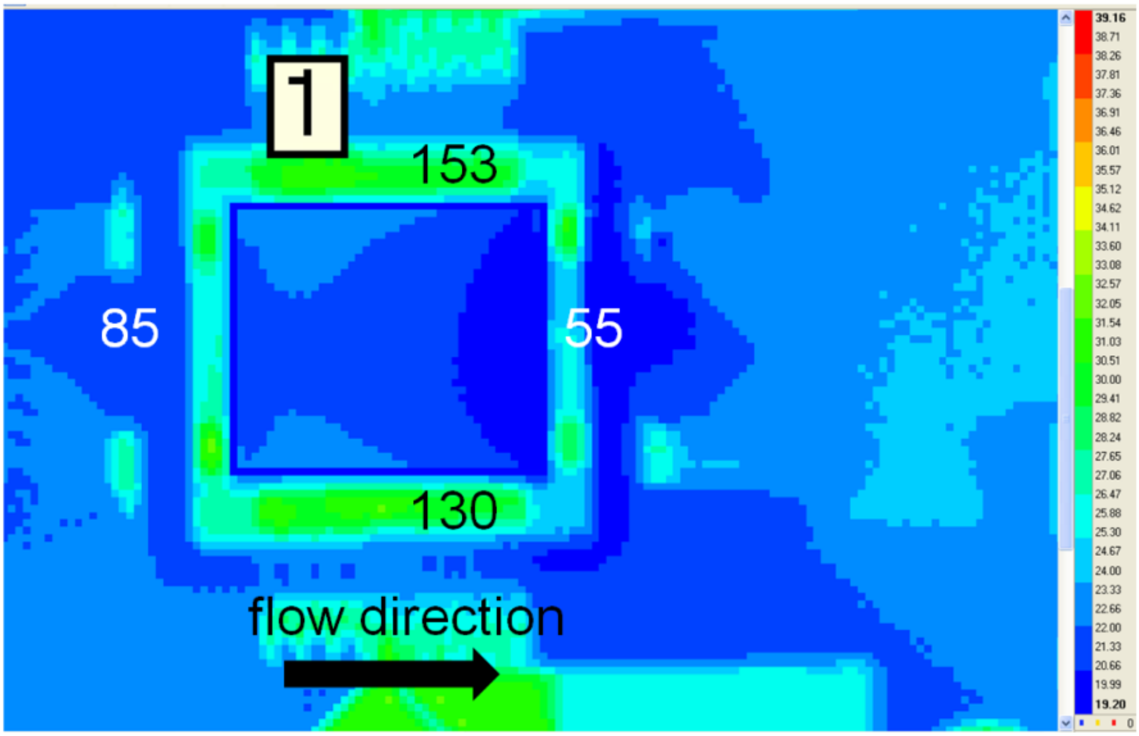

Figure B. 3 Temperature response for q_b = 13.2 W/cm^2, and a flow rate of 11.5kg/hr for flow boiling of R1234ze.

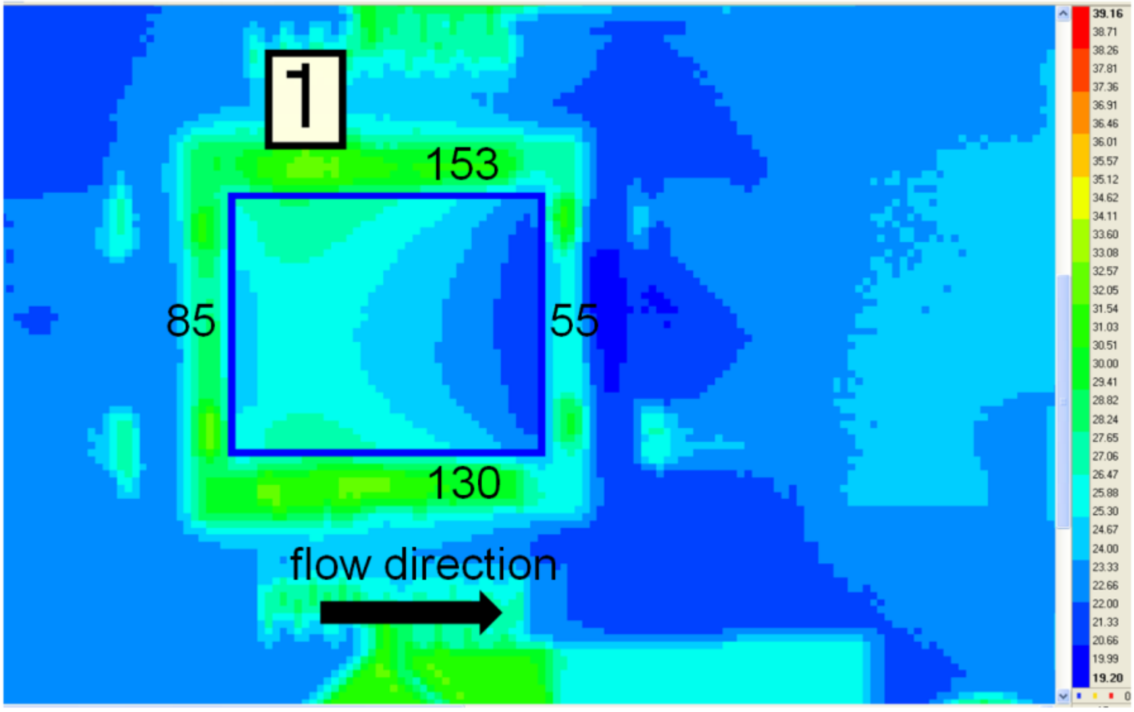

Figure B. 4 Temperature response for q_b = 23.9 W/cm^2, and a flow rate of 11.5kg/hr for flow boiling of R1234ze.

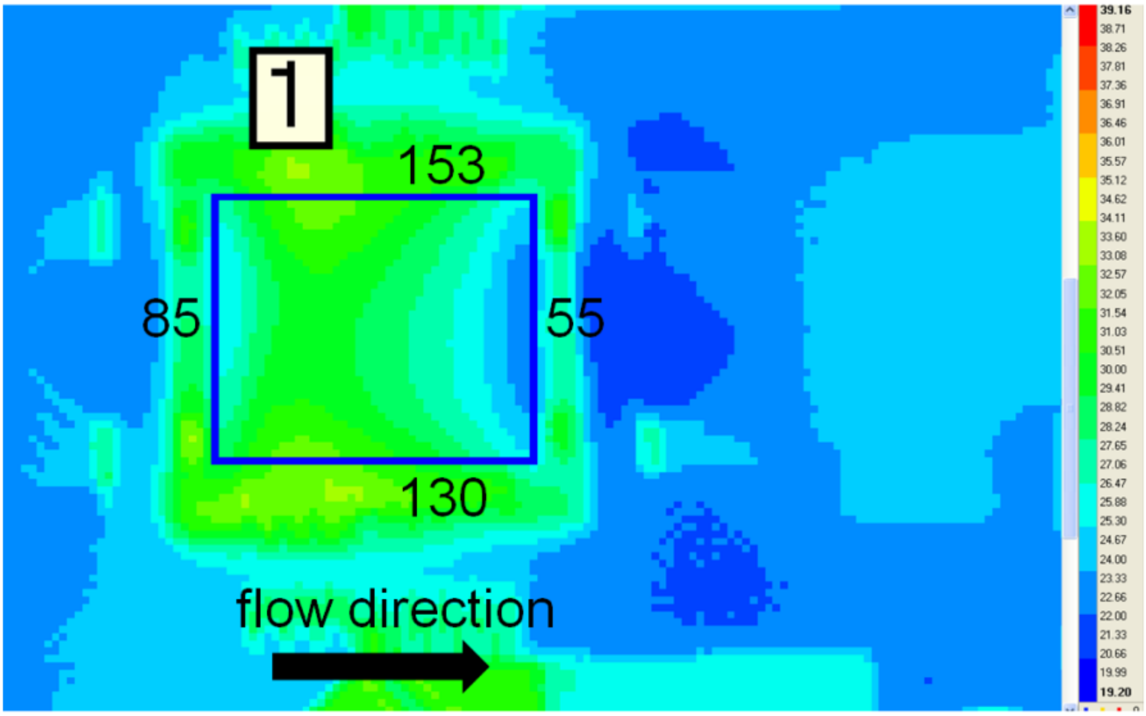

Figure B. 5 Temperature response for q_b = 36.9 W/cm^2, and a flow rate of 11.5kg/hr for flow boiling of R1234ze.

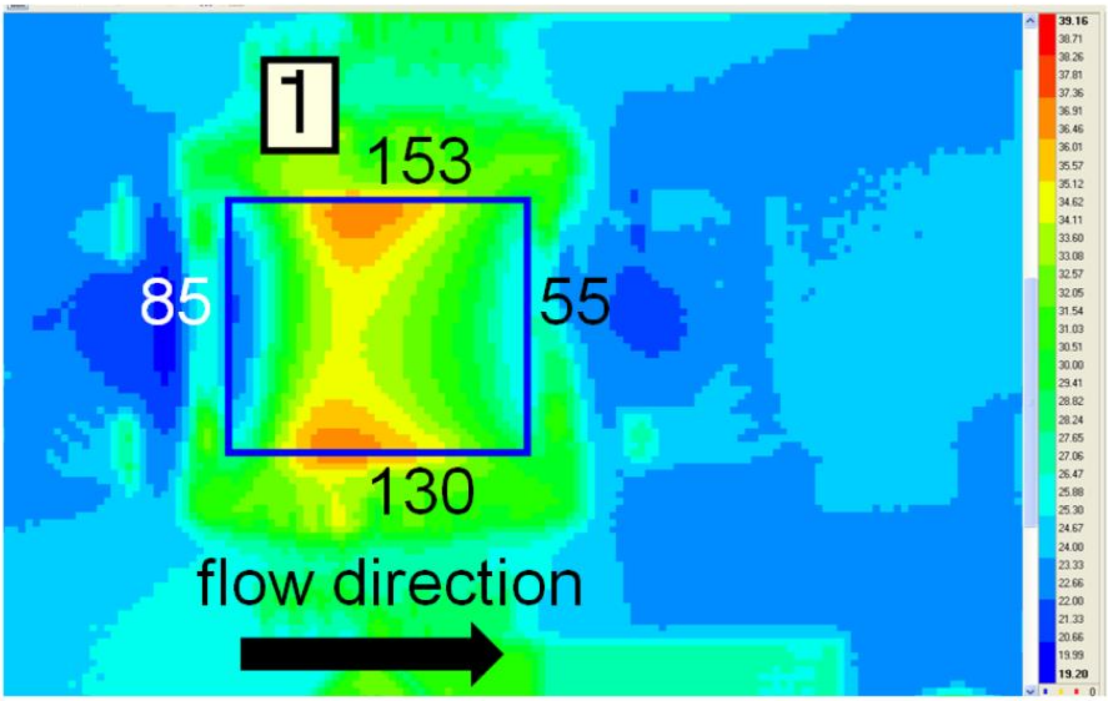

Figure B. 6 Temperature response for q_b = 53.1 W/cm^2, and a flow rate of 11.5kg/hr for flow boiling of R1234ze.

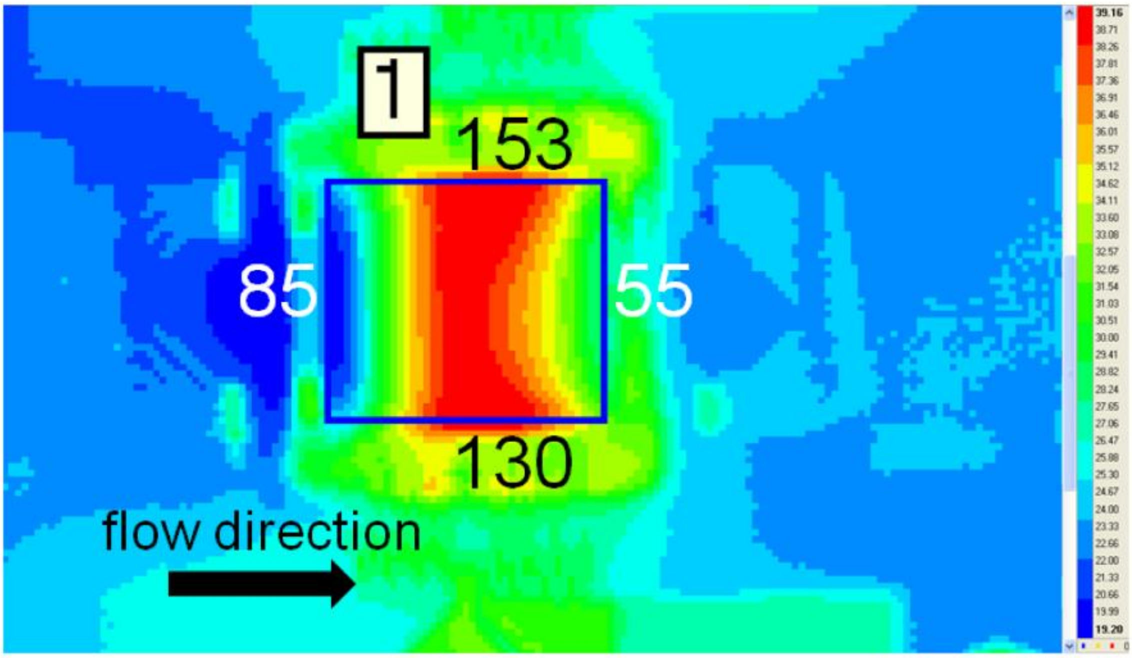

Figure B. 7 Temperature response for q_b = 66.6 W/cm^2, and a flow rate of 11.5kg/hr for flow boiling of R1234ze.

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List of scientific publications

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Journal Publications:

Y. Madhour, J. Olivier, E. Costa-Patry, S. Paredes, B. Michel, and J.R. Thome, “Flow boiling of R134a in a multi-microchannel heat sink with hotspot heaters for energy-efficient microelectronic CPU cooling applications”, IEEE Transactions on Components, Packaging and Manufacturing Technologies, vol. 1(6), pp. 873–883, 2011.

Y. Madhour, B.P. D'Entremont, J.B. Marcinichen, B. Michel, J.R. Thome, "Modeling of two-phase evaporative heat transfer in three-dimensional multicavity high performance microprocessor chip stacks," *Journal of Electronic Packaging,* vol. 136, no. Special Issue Thermodynamics of MEMS, pp. 0.21006.1-0.21006.10, 2014. Winner of BEST PAPER AWARD.

Conference Publications:

Y. Madhour, J. Olivier, E.C. Patry, S. Paredes, B. Michel, and J.R. Thome, “Two-phase flow boiling of R134a in a multi-microchannel heat sink for microprocessor cooling”, THERMINIC Conference Proceedings 2010, Barcelona, Spain.

Y. Madhour, S. Zimmermann, J. Olivier, J.R. Thome, B. Michel and D. Poulikakos, “Cooling of next generation computer chips: parametric study for single- and two-phase cooling”, THERMINIC Conference Proceedings 2011, Paris, France.

Y. Madhour, T. Brunschwiler, Mario El-Kazzi, Bruno Michel, and John Richard Thome, “Patterned die-to-die thin film bonding for 3D chip stacks with integrated microfluidic cooling”, International Conference on Electronic Packaging Technology and High Density Packaging, ICEPT-HDP Proceedings 2012, Guilin, China. Winner of OUTSTANDING PAPER AWARD.

T. Brunschwiler, **Y. Madhour**, T. Tick, G. Schlottig, S. Oggioni, “Investigation of Novel Solder Patterns for Power Delivery and Heat Removal Support”, Electronic Components Technology Conference, ECTC Proceedings 2013, Las Vegas, USA.

A. Sridhar, **Y. Madhour**, D. Atienza, Thomas Brunschwiler, John Richard Thome, “STEAM: a fast compact thermal model for two-phase cooling of integrated circuits”, International Conference on Computer-Aided Design, ICCAD Proceedings 2013, San Jose, USA.

Y. Madhour, M. Zervas, G. Schlottig, T. Brunschwiler, Y. Leblebici, J. R. Thome, B. Michel, “Integration of Intra Chip Stack Fluidic Cooling using Thin-Layer Solder Bonding”, IEEE International 3D Systems Integration Conference, 3DIC Conference Proceedings 2013, San Francisco, USA.

S. Paredes, **Y. Madhour**, G. Schlottig, C. L. Ong, T. Brunschwiler, “Wafer level bonding for embedded cooling approaches”, *Invited Keynote Paper*, 226th Meeting of the ElectroChemical Society, Cancun, Mexico, October 2014.

Curriculum Vitae

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WORK EXPERIENCE

IBM Research, Zurich (January 2010-June 2014)
Science and Technology Department, Advanced Micro Integration Group
Doctoral Candidate, EPFL LTCM (Laboratory of Heat and Mass Transfer)

- PhD Thesis: “3D integrated architectures for microelectronic two-phase flow cooling applications”. Developed a novel prototype of 3D computer chips that allow integrated dielectric evaporative cooling, using commercial refrigerants.
- Established extensive knowledge of electronic and thermal packaging technologies.
- Engineering and research skills in two-phase heat transfer systems as well as in MEMS microfabrication technologies.
- Published several articles in international journals as well as presented research findings at international conferences.
- Awarded the “**Outstanding Paper Award**” at the International Conference on Electronic Packaging Technologies and High Density Packaging, ICEPT HDP 2012, in Guilin, China.
- Supervised Bachelor & Master thesis students.

Swiss Institute of Technology, Lausanne (EPFL), (August 2007 – December 2008)
Laboratory of Heat and Mass Transfer
Research assistant

- Led a project for the development of a new two-phase air-water facility for measurements of twisted-tape insert-induced pressure drop.

Swiss Institute of Technology, Lausanne (EPFL), (August 2007 – January 2008)
EPFL Space Center, Swisscube project
Intern and research assistant

- Successfully implemented Phase C of the thermal modeling for Swisscube, the first satellite entirely built in Switzerland, in collaboration with the European Space Agency.
- Responsible for the validation of the first thermal experimental data.

Swiss Institute of Technology, Lausanne (EPFL), (September 2007 – December 2008)
Laboratory of Applied Mechanics and Reliability Analysis
Teaching assistant

- Co-supervised exercise sessions for Bachelor-level students.

EDUCATION

Swiss Institute of Technology, Lausanne (EPFL), (2007 – 2009)

Master of Science in Mechanical Engineering (average grade: 5.1)

- Thesis topic: Experimental investigation of two-phase flow boiling of R134a in a multi-microchannel heat sink for microelectronic CPU cooling applications.
- First-Of-A-Kind project in CPU cooling, successfully executed at IBM Research, Zurich, Switzerland.
- Activities and Societies: Class Representative. Responsible for the communication between students and professors as well as the department head. Attended monthly board meetings and voted for the hiring of new teaching staff.

Swiss Institute of Technology, Lausanne (EPFL), (2007 - 2009)

Minor in Technology Management and Entrepreneurship

- Minor program - 30 ECTS (& equivalents) in Business topics, in parallel to MSc. degree.
- Obtained intermediate knowledge in Finance & Accounting, Business Strategy, Project Management, and Technology Foresight & Entrepreneurship.

Swiss Institute of Technology, Lausanne (EPFL), (2004 – 2007)

Bachelor of Science in Mechanical Engineering

- Bachelor thesis: Integration of a turbo jet on an unmanned air vehicle (“SmartFish” drone).
- Focus on Energy topics (Advanced Energetics, Photovoltaics, Fuel cells, Turbomachines).
- Activities and Societies: Class Representative.

TECHNICAL SKILLS

Software – MS Office, LaTeX, Matlab, Inkscape, CATIA, LabView, COMSOL, L-Edit.
Experimental – MEMS, Thermal & Electronic Packaging, Heat Transfer, Two-Phase Flows.

LANGUAGE SKILLS

English (fluent), French (native), Arabic (native), German (proficient).

INTERESTS & EXTRA-CURRICULAR ACTIVITIES

- Film and theater play writing and directing
- Vice-president role for “Streetconcept”, an association promoting local artists and organizing cultural events in Western Switzerland.
- Founder and president of the IBM Zurich Research Laboratory Movie Club between June 2013 and June 2014.

REFERENCES

Available on demand.