PLL-based high-speed demodulation of FM signals for real-time AFM applications

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***Abstract*—In this paper we present a new architecture for PLL-based high-speed demodulation of frequency-modulated AFM signals. In our approach, we use single-sideband frequency upconversion to translate the AFM signal from the position sensitive detector to a fixed intermediate frequency of 10 MHz. In this way, we fully benefit from the excellent noise performance of PLL-based FM demodulators still avoiding the intrinsic bandwidth limitation of such systems. Furthermore, the system becomes independent of the cantilever's resonance frequency. To investigate if the additional noise introduced by the single-sideband upconverter degrades the system noise figure we present a model of the AM-to-FM noise conversion in the PLL phase detector. Using this model, we can predict an upper corner frequency for the demodulation bandwidth above which the converted noise from the single-sideband upconverter becomes the dominant noise source and therefore begins to deteriorate the overall system performance. The approach is validated by measured data obtained with a PCB-based prototype implementing the proposed demodulator architecture.**

I. Introduction

Recently, atomic force microscopy (AFM) has gained significant attention in the field of life science as a tool for studying biological structures at the cellular and subcellular level. In contrast to conventional AFM applications in material science where imaging time is of minor importance, in biological AFM applications people are often interested in high temporal resolutions in order to study biological processes with relatively fast time scales such as the dynamic behavior of proteins. Since it has been shown that the minimum detectable force gradient in amplitude modulated (AM) AFM is proportional to $1/\sqrt{Q}$, where Q is the quality factor of the utilized cantilever, high-resolution AM AFM intrinsically requires the use of high-Q cantilevers. However, the frequency response of the cantilever motion with respect to amplitude variations is limited by the same quality factor resulting in an inevitable resolution-bandwidth tradeoff in AM AFM. In frequency modulated (FM) AFM this resolution-bandwidth tradeoff does not exist because the cantilever can respond instantaneously, i.e. without bandwidth limitations, to perturbations in its oscillation frequency [1] and [2] and the theoretically achievable bandwidth in this operating mode is eventually only limited by the cantilever resonant frequency itself. Therefore, in order to fully benefit from this large theoretically achievable bandwidth there is need for high-speed FM demodulators which can provide both the excellent noise performance required in AFM applications and demodulate signals with modulation bandwidths as large as the cantilever resonant frequency.

To account for both of these contradicting design goals, we propose the use of a single-sideband (SSB) upconverter in combination with a subsequent phase-locked loop (PLL) based FM demodulator. Thanks to their closed-loop structure, PLL-based FM demodulators show the best noise performance of all available FM demodulator architectures [3]. However, their demodulation bandwidth is limited to a value between one fifth and one tenth of their input carrier frequency [3]. Therefore, a standalone PLL-based FM demodulator cannot be used when attempting to fully exploit the available signal bandwidth provided by the cantilever. To overcome this problem, we use an SSB upconverter which translates the center frequency of the AFM signal from the cantilever resonant frequency to an intermediate frequency (IF) of 10 MHz without introducing a frequency component at the so-called image frequency which could perturb the lock-in process of the subsequent PLL. In this way, we can select a PLL bandwidth of 1 MHz and it becomes possible for cantilevers with resonance frequencies below 1 MHz to fully exploit their intrinsic bandwidth for high-resolution AFM with high frame rates.

The paper is organized as follows: In section II, we present a detailed overview of the proposed FM demodulator architecture. Section III then deals with the problem of AM-to-FM noise conversion in the PLL phase detector (PD) and we present an analytical model which allows the prediction of the maximally achievable demodulation bandwidth without SNR degradation due to the additional AM noise introduced by the SSB modulator. We then present the details of a PCB-based prototype of the proposed architecture in section IV and show measured results obtained with this prototype in section V. We conclude the paper with a short summary and a brief outlook on future work in section VI.

II. System overview

The architecture of the proposed highspeed FM demodulator is shown in Fig. 1. According to the figure, the AFM

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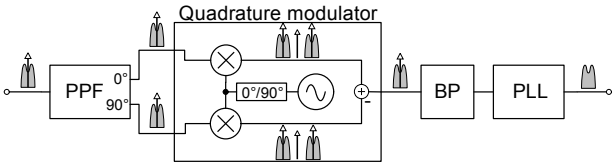

Fig. 1. Illustration of the proposed system architecture.

signal coming from the position sensitive detector is fed into a polyphase filter which generates the quadrature signals required for the subsequent SSB upconversion. The SSB upconversion itself is then performed by means of a quadrature modulator which contains two mixers driven by quadrature LO signals. By adding or subtracting the outputs of the two mixers, the lower sideband (LSB) and the upper sideband (USB) can be selected, respectively. In order to limit the amount of integrated AM noise at the PLL input, the quadrature modulator is followed by a bandpass filter centered around the IF frequency. The output of the bandpass filter then drives the input of the PLL-based FM demodulator.

III. PLL NOISE MODEL

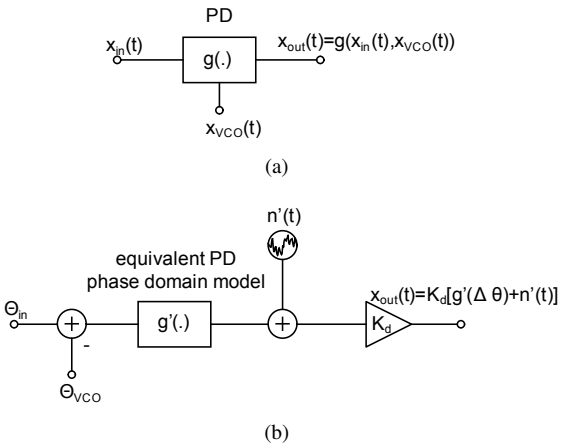

Fig. 2. (a) PD with noisy inputs and (b) equivalent PD phase domain model which transforms the noise at the PD input into an equivalent phase noise process $n'(t)$ at the PD output.

An ideal FM demodulator is insensitive to AM noise in its input signal. However, any real FM demodulator converts a fraction of the amplitude noise at its input into frequency noise and, therefore, care has to be taken in the design process that the addition of the SSB modulator, which can significantly increase the amplitude noise level at the PLL input, does not degrade the overall system noise figure. Since in a PLL-based FM demodulator the AM-to-FM noise conversion takes place in the phase detector, in this section, we will present an analytical model which predicts the contribution of the various noise sources inside the PLL-based demodulator to the PLL's input referred frequency noise including the contribution from amplitude noise at the PD input. To this end, we replace the PD with its input signal $x_{\rm in}(t) = A_{\rm in}\,\sin(\omega_0\,t+\theta_{\rm in})+n(t) = \tilde{A}_{\rm in}(t)\,\sin(\omega_0\,t+\theta_{\rm in}+\theta_{\rm n}(t))$ perturbed by both amplitude noise and phase noise using the equivalent circuit depicted in Fig. 2(b) by a phase domain model with a noise free input and a transformed noise process $n'(t)$ [4]. In the figure, $g(\cdot)$ is the nonlinear phase transfer characteristic of the employed phase detector, the prime symbol indicates transformed quantities and K_d is the equivalent conversion gain of the phase detector. Applying the procedure outlined in [4] to a phase frequency detector (PFD), we obtain for the transformed quantities:

$$g'\left(\Delta\theta\right) = 4\sum_{\nu=1}^{\infty}(-1)^{\nu+1}\frac{\mu_\nu}{\nu}\,\sin\left(\nu\,\Delta\theta\right) \tag{1a}$$

$$\mu_\nu = E\left[\cos\left(\nu\,\theta_n\right)\right] = \frac{1}{2}\sqrt{\pi\,\mathrm{CNR}}\exp\left(-\frac{\mathrm{CNR}}{2}\right)\left[I_{\frac{\nu-1}{2}}\left(\frac{\mathrm{CNR}}{2}\right)+I_{\frac{\nu+1}{2}}\left(\frac{\mathrm{CNR}}{2}\right)\right] \tag{1b}$$

$$\mathrm{CNR} = \frac{\tilde{A}_{\rm in}^2}{2\,\sigma_n^2} \tag{1c}$$

$$S_{N'N'}(j\omega) = \frac{\sigma_{n'}^2}{B_{n'}} \tag{1d}$$

$$\sigma_{n'}^2 = E\left[g^2(\theta_n)\right] = \int_{-\pi}^{\pi}\theta_n^2\,p(\theta_n)\mathrm{d}\theta_n = \frac{\pi^3}{3}+4\sum_{\nu=1}^{\infty}(-1)^{\nu}\frac{\mu_\nu}{\nu^2} \tag{1e}$$

$$B_{n'} \approx B_n\left[1+0.35\,\exp\left(-\mathrm{CNR}\left[1-\frac{\pi}{4}\right]\right)\right], \tag{1f}$$

where μ_ν is the so-called signal suppression factor [4], $I_\nu(\cdot)$ is the modified Bessel function of order ν, CNR is the input carrier to noise ratio, σ_n is the variance of the additive input amplitude noise process $n(t)$, σ_n' is the variance of the transformed noise process $n'(t)$, $B_{n'}$ is the equivalent noise bandwidth of $n'(t)$ and $S_{N'N'}(j\omega)$ is the power spectral density of $n'(t)$. The equivalent phase detector model of Fig. 2(b) can be incorporated into the standard phase domain PLL model according to Fig. 3 where all noisy components are replaced by additive equivalent noise sources [3] and [5]. Assuming moderate fluctuations due to noise, the nonlinear PD transfer characteristic can be linearized around its operating point using the equivalent gain K_d' [4] or [5]. For the PFD employed here K_d' is given by:

$$K_d' = \left.\frac{\mathrm{d}g'(\Delta\theta)}{\mathrm{d}\Delta\theta}\right|_{\Delta\theta=0} = 4\sum_{\nu=1}^{\infty}(-1)^{\nu+1}\mu_\nu. \tag{2}$$

Using this model, we have performed numerical simulations in MATLAB to compute the contribution to the input referred frequency noise of each noise source. For our simulations we have used the loop filter topology shown in Fig. 4 which we also implemented in the PCB-based prototype discussed in section IV, whose transfer function $F(s)$ is given by:

$$K_d\,F(s) = \frac{I_{\rm CP}}{2\,\pi}\,\frac{b-1}{b}\,\frac{R_3}{R_3+R_4}\,\frac{1+s\,\tau_1}{\left(1+\frac{s\,\tau_1}{b}\right)s\,C_1}\,\frac{1}{1+s\,\tau_{\rm out}}, \tag{3}$$

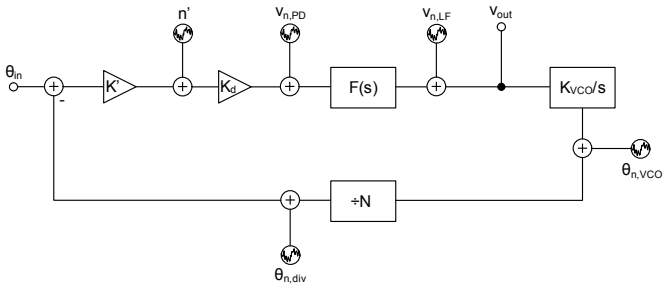

Fig. 3. PLL model incorporating the linearized PD model of Fig. 2(b) and additive noise sources for all remaining noise contributors.

where I_{CP} is the charge pump current, $b = 1 + C_1/C_2$, $\tau_1 = R_1\,C_1$ and $\tau_{\mathrm{out}} = R_2\,C_3$. Simulation results of the input referred frequency noise spectral density for three different input amplitude noise levels are shown in Fig. 5. The model parameters used for the simulation are listed in the figure caption. In the figure, we see that for low frequencies the input referred frequency noise is dominated by the VCO noise and that a corner frequency exists at which the transformed amplitude noise becomes the dominant noise source and after which the total input referred frequency noise increases with a slope of 20 dB/dec.

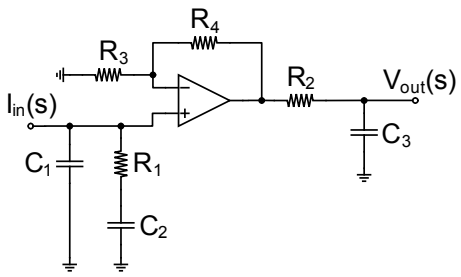

Fig. 4. Schematic of the utilized loop filter topology. Capacitors C_1 and C_2 and resistor R_1 transform the current from the PFD charge pump combination into a voltage and the remaining circuitry provides a further pole which can incorporate the large load capacitance of the discrete VCO.

IV. PCB-BASED PROTOTYPE

In order to validate the proposed demodulator architecture experimentally, we have designed and fabricated a PCB-based prototype with discrete off-the-shelf electronics. The annotated layout of this prototype illustrating the different building blocks is shown in Fig. 6. In order to be compatible with standard AFMs, the prototype design incorporates an input stage which adjusts the signal amplitudes coming from the position sensitive detector to the levels required for the on-board signal processing. The polyphase filter (PPF) generates the quadrature signals required for the single-sideband modulation. It consists of 8 stages to achieve the required minimum image rejection ratio (IRR) of about 26 dB (corresponding to a noise figure of 0.01 dB due to noise coming from the unwanted sideband) over its bandwidth from 1 kHz to 3 MHz. With this PPF bandwidth, the system can work with cantilevers with

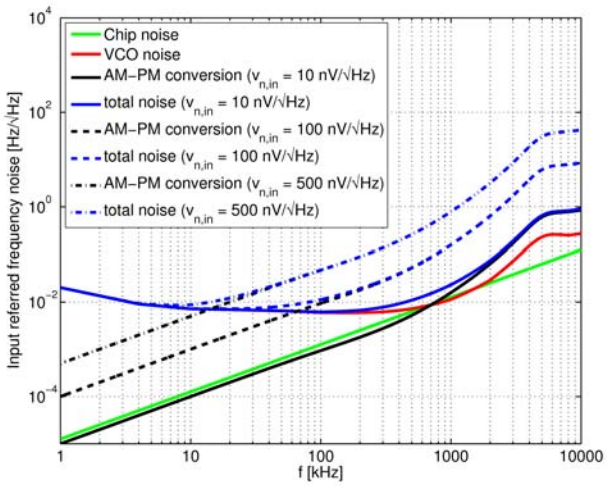

Fig. 5. Simulation results for the input referred frequency noise of the PLL-based FM demodulator for three different levels of AM noise at the PLL input. The remaining simulation parameters correspond to the PCB based prototype described in section IV and are given by: $C_1 = 11\,\mathrm{pF}$, $C_2 = 876\,\mathrm{pF}$, $C_3 = 1.233\,\mathrm{nF}$, $R_1 = 1.47\,\mathrm{k\Omega}$, $R_2 = 12\,\Omega$, $R_3 = 1\,\mathrm{k\Omega}$, $R_4 = 220\,\Omega$, VCO: Minicircuits ROS-70-119+, PLL chip: Analog Devices ADF4002, charge pump current $I_{\mathrm{CP}} = 5\,\mathrm{mA}$.

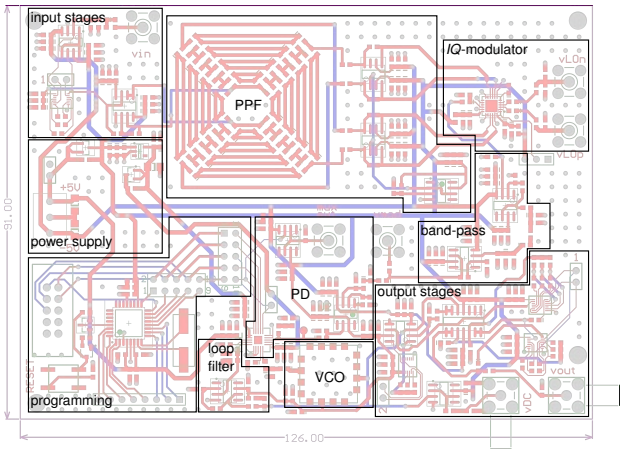

Fig. 6. Annotated layout of the fabricated PCB-based FM demodulator prototype.

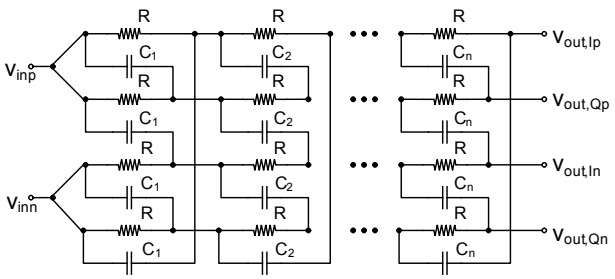

Fig. 7. Schematic of the passive polyphase filter generating the quadrature signals for the SSB modulator.

resonance frequencies between about 10 kHz and 1.5 MHz and signal bandwidths close to the corresponding cantilever resonance frequency. Although the IRR could be improved by a nonuniform placement of the PPF poles and zeros by about 1.5 dB [6] this improvement is not significant and even further diminished by the tolerances of standard discrete components. Therefore, in the presented prototype the pole and zero locations are logarithmically distributed between 1 kHz and 3 MHz. The SSB modulator (LTC5598, Linear Technology) which upconverts the AFM signal to the intermediate frequency $f_{\mathrm{IF}} = 10\,\mathrm{MHz}$ is followed by a passive bandpass filter which removes out of band noise and interferences. The LO signal required for the upconversion at a frequency of $f_{\mathrm{LO}} = f_{\mathrm{IF}} + f_{\mathrm{res}}$, where f_{res} is the resonance frequency of the cantilever, i.e. the center frequency of the AFM signal, is generated by an external signal source generator. The PLL-based FM demodulator (PLL-chip: ADF4002, Analog Devices, VCO: ROS-70-119+, Minicircuits) is designed for a demodulation bandwidth of 1 MHz and followed by tunable output stages with variable gain and bandwidth settings (gain settings: 11, 51, 101, corner frequencies of 4th order Butterworth filters: 10 kHz, 250 kHz, 1.2 MHz) which allow the demodulator to be adjusted for different cantilever resonance frequencies and scan rates. In addition to the signal processing electronics, the PCB also contains the electronics for a stable and low-noise supply voltage generation and a microcontroller to program the ADF4002 through its SPI interface at power-up.

V. Measurements

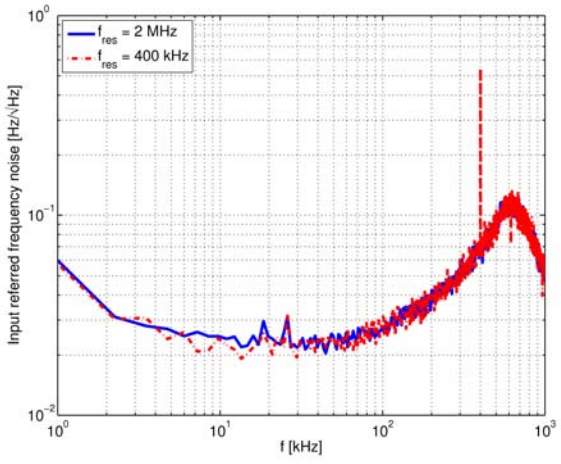

Fig. 8. Measured input referred frequency noise floor of the PCB-based prototype for input center frequencies of 400 kHz and 2 MHz, respectively.

The measured input referred frequency noise of the prototype described in the previous section is shown for the two different center frequencies of 400 kHz and 2 MHz in Fig. 8. The spectrum was obtained by measuring the output referred voltage noise of the PLL and dividing this voltage noise floor by the measured PLL closed-loop sensitivity of 140 μV/Hz. From the figure we see that the noise is identical for the two different input center frequencies. The spurious tone in the spectrum measured with an input center frequency of 400 kHz originates in the LO leakage of the LTC5598 modulator chip. It is due to an imperfect matching of the common mode levels of the modulator's baseband inputs and will be suppressed in future prototype generations by a trimming of these input common mode levels. Overall, the measured frequency noise spectrum matches well (within a factor of 2.5) with the model presented in section III. For lower frequencies, it is dominated by the VCO noise and the converted amplitude noise starts to dominate at a corner frequency of about 100 kHz. The integrated frequency noise in a 400 kHz bandwidth is about 19 Hz.

VI. Conclusion and Outlook

In this paper, we have presented a new architecture for high-speed PLL-based FM demodulation for real-time AFM applications incorporating an SSB modulator to allow the PLL to operate at a higher center frequency and thereby remove its intrinsic bandwidth limitation. We have identified the AM noise additionally introduced by the SSB modulator which is converted into frequency noise in the PLL PD as the limiting factor for the achievable detection bandwidth of the system. The model of this AM-to-FM conversion presented in section III allows to quantify this limitation and account for it during the design phase. In section V, we have presented measured results of a PCB-based prototype of the proposed system which both validates the PLL model of section III and provides a proof of principle that the proposed detector architecture can indeed increase the PLL bandwidth without deteriorating the system noise figure over a certain frequency band. With its integrated frequency noise of about 19 Hz in a frequency bandwidth of 400 kHz, it can safely demodulate AFM signals originating from a cantilever with a resonant frequency of 400 kHz and the corresponding maximum scan rate. However, due to the positive slope of the frequency noise floor originating from the transformed AM noise, the presented prototype cannot demodulate frequencies much higher than 400 kHz. Therefore, we are currently working on an improved prototype with a lower AM noise floor which will allow to work with even higher cantilever resonant frequencies and the corresponding increased demodulation bandwidths.

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