Development of a Versatile low-power 24 GHz Phased Array Front-End in 90 nm CMOS technology

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***Abstract*— This paper deals with the development of a four-channel low-power Phased Array Front-End (PhA-FE) at 24 GHz, targeting both low-power radar sensors and battery powered transceiver applications. Typically, PhA-FEs are power hungry architectures due to multiple parallel RF channels in the FE and complex algorithms for beam steering or high bit-rate demodulation in the digital part. In contrast, we target in this paper applications where both beam steering algorithms and data demodulation are relatively simple and hence achievable with low-power digital signal processing. More specifically, we report on four significant building blocks of the architecture, a Low Noise Amplifier (LNA), a Vector Modulator Phase Shifter (VMPS), a Quadrature Voltage Controlled Oscillator (QVCO) and an Analogue to Digital Converter (ADC) that have been designed the first three in 90nm and the last in 180nm CMOS technology. The LNA shows 24.4 dB gain, 3.4 dB NF and -24.4 dBm input P1dB. The single quadrant VMPS has more than 90° of phase control range and shows less than 0.7 dB of gain variation over phase shifting. The QVCO which consumes less than 32 mW, buffer included, has a tuning range of 8%. The 6bit 20 MS/s ADC consumes 1.8 mW.**

I. Introduction

The widespread use of wireless sensors and portable equipment with wireless connectivity capability demands transceivers and wireless sensors capable of operating at low-power and in environments where many wireless systems generate interference. Sensor networks are often used for environment monitoring and therefore scanning is desirable to improve spatial resolution and sensor range. Two typical examples are traffic monitoring systems based on Doppler radar sensors [1] and radar based surveillance of persons [2].

Similarly, transceivers operating in free bands require increasing bit-rates mainly for sending good quality video. Currently, the standard platform for sending video is 802.11g. However there exists a gap in bit-rate between narrow-band low-power transceivers, capable of sending data up to 2 Mbps, and WLAN transceivers capable of reaching 54 Mbps but consuming more than 500 mW [3].

Both, PhA-FE for scanning systems and medium-bit-rate transceiver are power hungry system due to multiple RF channels and for beam steering or high bit-rate demodulation in the digital part. Under some conditions including low spatial resolution scanning, low speed scanning and low bandwidth efficiency, the implementation of low-power PhA-FEs for radar sensors and medium-bit-rate transceivers (few tens of Mbps) is possible. Exploiting the 200 MHz of bandwidth (BW) offered by the 24 GHz ISM band and the good performance at these frequencies allowed by scaled CMOS technology [4], we propose a low-power, four-channel PhA-FE architecture capable of operating both in radar and transceiver mode.

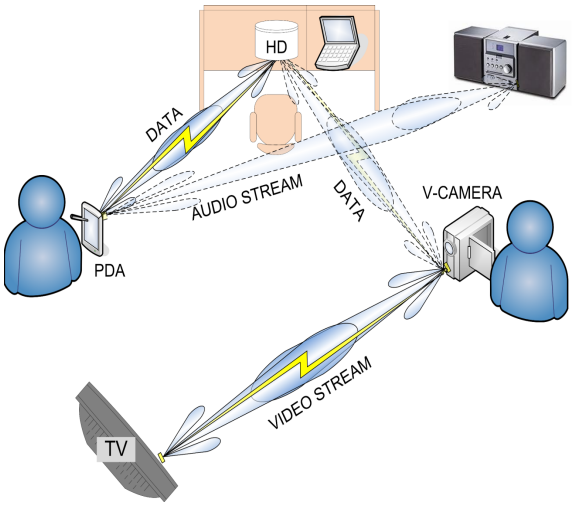

Fig. 1. Medium-bit-rate transceiver for point-to-point links. Beam steering is used for interference mitigation and direct link optimization.

The advantages of beam steering for radar systems are clear, just thinking of the possibility of adjusting the antenna pointing after deployment or slow-scanning the environment for detecting persons. The advantages are less obvious for transceivers; for this reason we discuss the application depicted in Fig. 1 which shows links between different sources of large quantities of data, such as video cameras and PDAs, with typical sinks such as displays, sound playback systems and storage systems. For real-time playback of good quality compressed video (ex. HD-DVD 480p) each link requires more than 10 Mbps. The proposed PhA-FE offers the following benefits: (a) the RF power is focused to the sink with a consequent increasing in signal-to-noise ratio at the receiver; (b) low-power consumption, compared with WLAN due to the simple modulation used (M-PSK), larger bandwidth available and less data overhead for point-to-point links (i.e ten channels with 8-PSK modulated signals), (c) simple medium access

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control based on frequency and space division multiple access. The latter is achievable thanks to the array directivity and the relatively high losses encountered by mm-waves in their paths and going through objects.

The paper is organized as follows: in section II we propose the PhA-FE architecture, and in section III we describe four significant building blocks of the architecture, namely a LNA, a VMPS, a QVCO and an ADC designed the first three in 90nm and the last in 180nm CMOS technology. Finally conclusions and a comparison with the state of the art are provided.

II. Transceiver Architecture

Figure 2 shows the proposed four-channel PhA-FE architecture capable of operating in frequency modulated radar (FMCW), Doppler radar and transceiver modes. Exploiting a direct conversion receiver and a direct modulation transmitter it does not require selective filters for image rejection. The unique filter is a low-pass filter in the zero-IF section of the receiver. Channel phase shifting is implemented by shifting the local oscillator (LO), which gives several advantages: (a) the same phase shifters can be shared in the receiver and transmitter path; (b) each LNA needs less gain, consuming less power; and (c) each complex mixer handles a quarter of the total received power resulting in a relaxed linearity requirement. Phase shifters are used for steering the antenna beam and, in transceiver mode, also for modulating in phase the transmitted RF signal, implementing an M-PSK modulation. Frequency modulation is also possible through the PLL to generate a frequency ramp in FMCW radar mode. The operating mode can alternate between transceiver and radar controlling the state of the switches in the LO phased paths together with some power supply switches for each PA and LNA (not shown in Fig. 1). Finally both I and Q paths of the IF section are composed of a voltage gain controlled amplifier (VGA), a low-pass filter with adjustable cut-off frequency to accommodate different BWs and a 6-bit 20 MS/s ADC. The IF BW starts from 20KHz in doppler radar mode and reaches 5MHz (10MHz double-side) in transceiver mode.

III. Building Blocks

At the moment the four blocks outlined in Fig. 2 are under development for a first tape-out focused on model calibration with a view to the overall front-end integration. Post-layout simulations in Spectre are provided; moreover, for the ADC, measurements are available based on a previous similar implementation in 180nm CMOS technology.

A. LNA

The designed LNA is illustrated in Fig. 3 and is based on three cascode stages. The upper MOSFETs (M2,M4,M6) are low voltage threshold type allowing the same overdrive of the lower MOSFETs (0.5 mV). Bias current has been determined for an output P1dB of 0 dBm. MOSFET lengths have been fixed for a current density of about $150\mu A/\mu m$ which represents a good operating point for gain and noise figure in a low-power design in CMOS technology. No inductor degeneration

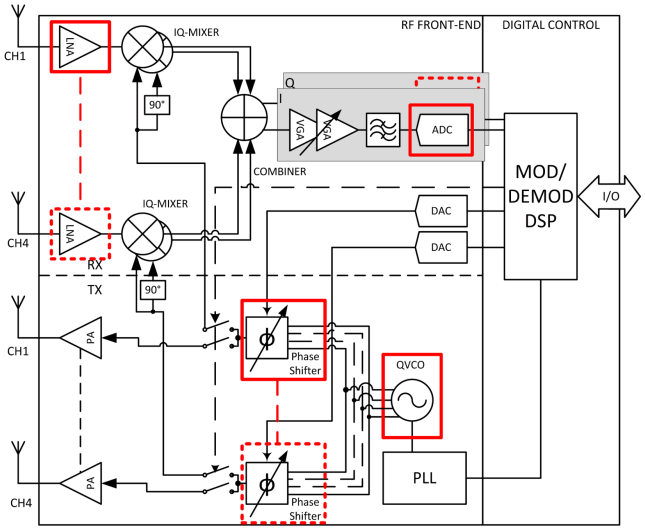


Fig. 2. Block diagram of the PhA-FE for low-power transceivers and radar sensors. Developed building blocks are outlined in red.

has been used in order to achieve the maximum gain this being the scarcest resource at 24 GHz. Fig. 4 shows post-layout

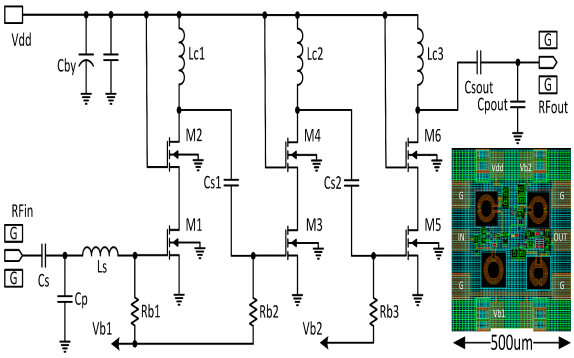


Fig. 3. Three stage 24 GHz cascode LNA.

simulation results including pad effects. The peak power gain is about 24.4 dB at 25 GHz taking into account the frequency downshift in real implementation, the minimum noise figure is 3.4 dB, and the input return loss is better than -10 dB over 1 GHz of band. At an overall consumption of 17.3 mW the input-referred P1dB is -24.4 dBm.

B. VMPS

The designed single quadrant VMPS is shown in Fig. 5. Each variable gain amplifier is based on a cascode in which there are two upper MOSFETs (M2, M3): one connected to the resonant load and the other connected to the power supply. The amplifier gain is controlled by steering the current between these two MOSFETs; maximum gain is obtained when M2 is biased for the same current as M1, and M3 is switched off, and vice versa. In this configuration the input impedance remains constant over the amplifier gain, contributing to the phase accuracy of the phase shifter. The two VGAs are

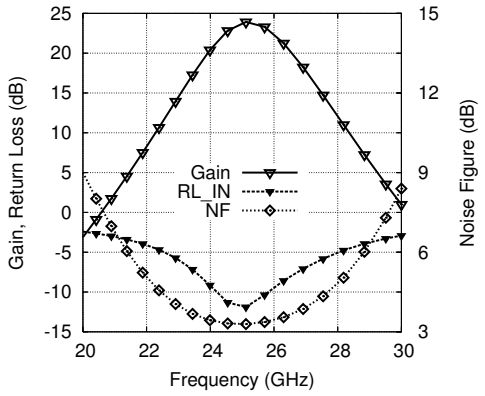


Fig. 4. Simulated gain, noise figure and input return loss of the three stage LNA.

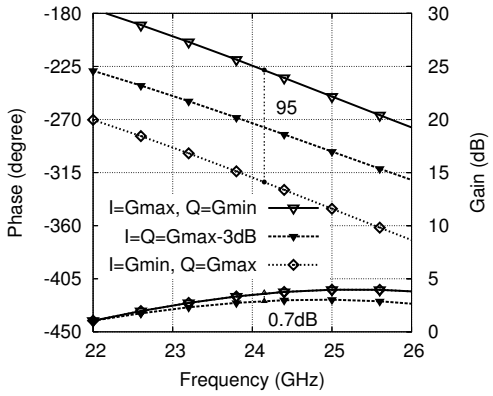


Fig. 6. Phase and gain responses of the single quadrant VMPS.

combined in current on the same load (Lo, Cos, Cop), so that the output current is the weighted combination of two quadrature currents. The ideal phase shifter that generates the IQ components has been inserted only for simulation purposes, and in fact in the final implementation the quadrature components will be generated by the QVCO. Figure 6 shows

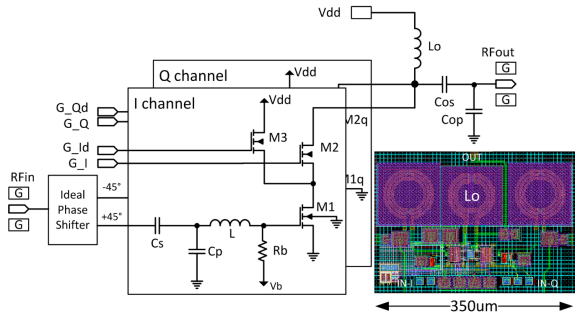
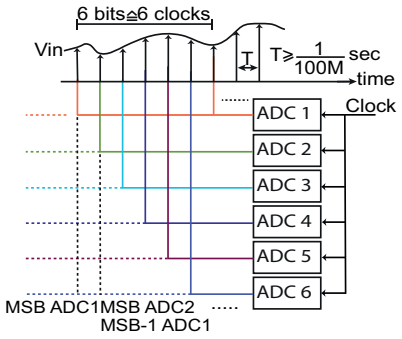


Fig. 5. Single quadrant VMPS schematic; the ideal phase shifter has been inserted for simulation purposes only.

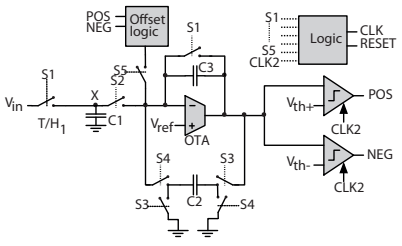
the phase response and the overall gain of the VMPS. Due to small layout asymmetries, for compactness, the phase control range is more than $90°$, the gain is $3.4\,\text{dB}$, and the gain accuracy is better than $0.7\,\text{dB}$ over the phase shift. The single quadrant VMPS consumes $7.4\,\text{mW}$ for an output P1dB of $-6\,\text{dBm}$; extending the circuit to $360°$ of regulation entails doubling the power ($14.8\,\text{mW}$).

C. ADC

The ADC block diagram is shown in Fig. 7(a). Each ADC cell, consists of a redundant signed digit (RSD) ADC and some logic. The schematic of each ADC cell is shown in Fig. 7(b). In this architecture, the number of cells and the sampling rate determine the number of bit and the Nyquist sampling rate, respectively. Thanks to the time interleaving architecture, the circuit preceding the ADC sees only one cell at a time and thus sees a constant capacitive load equal to C1. For the same reason, the track-and-hold stage of one ADC cell is not loaded by the track-and-hold stage of the other ADC cells and it subsides the mismatching problem in the circuit. For a given sampling frequency, the logic in each cell sets the pulse duration automatically to the right value so that the ADC can work with different sampling rates up to $100\,\text{MS/s}$ given the design of the operational transconductance amplifier (OTA) and comparators. A previous implementation of a $4\,\text{GS/s}$ 6-bit ADC in 180nm, designed with the same algorithm and technique, showed the following measured results: $0.9\,\text{GHz}$ of input bandwidth, 5.7 effective number of bit, $28\,\text{mW}$ of power consumption and $0.15\,mm^2$ of occupied area. With 20 cells and an interleaving time of $250\,\text{ps}$, the ADC was able to sample 5ns pulse-based UWB signals. The new $20\,\text{MS/s}$ 6-bit ADC has the same input BW and it shows a power consumption of 1.8mW using 6 cells.



(a) Block Diagram



(b) Single Cell schematic

Fig. 7. The 20 MS/s 6-bit RSD ADC: (a) block diagram and (b) single cell schematic.

D. QVCO

The QVCO generates four outputs simultaneously, which have 90° phase difference from each other. In QVCO schematic design, the coupling transistor architecture is commonly used (Fig. 8). The QVCO is built upon two identical differential VCO cores, in which the cross-coupled transistor architecture are used. The quadrature coupling transistors are inserted for mutual connection; they have the same parameters as the cross-coupled transistor pair (tot. width $= 3.2\mu m$). At the 26 GHz expected frequency, the relative phases and amplitude are layout sensitive. Nevertheless, simulation results show a phase imbalance of less than 2° and an amplitude imbalance of 1.2 dB. Other results are reported in Table I.

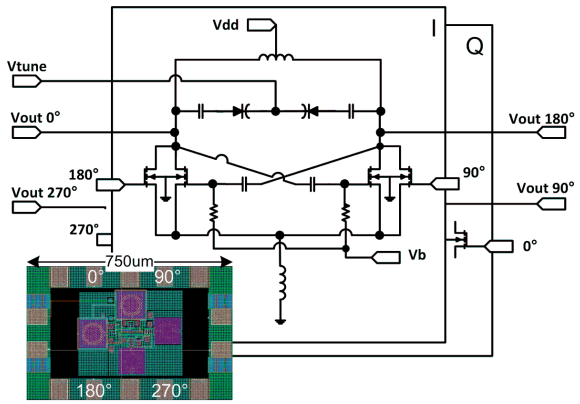


Fig. 8. Schematic of the 24 GHz QVCO. Two identical cross coupled VCOs are coupled in quadrature.

IV. Conclusions

The architecture of a four-channel low-power PhA-FE at 24 GHz capable of implementing both low-power radar sensors and medium-bit-rate transceivers has been proposed, targeting low-power applications. Four significant building blocks, namely a LNA, a VMPS, a QVCO and an ADC have been designed the first three in 90nm and the last in 180nm CMOS technology. Their performance is compared with the state of the art in Table I. As can be seen good RF performances are achieved together with low-power consumption, hence they are suitable to fill the gap between narrowband low-power and WLAN transceivers.

V. Acknowledgments

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TABLE I
Building Blocks performance and comparison with state of the art

LNA	Unit	This work	[5]	[6]	
Tech	nm	90	130	90	
Freq.	GHz	24	24	30	
Gain	dB	24.4	13-16	15	
NF	dB	3.4	6-7.5	3.4	
Power	mW	17.3[d]	15	4	
VMPS	**Unit**	**This work**	**[5]**	**[7]**	
Tech	nm	90	130	130	
Freq.	GHz	24	24	15-26	
Gain	dB	3	0	-3	
ΔG	dB	0.7	0.5	6.3	
O-P1dB	dB	-6.3		>-1.8	
Power	mW	7.4[a,d]	16.5	11.7	
ADC	**Unit**	**This work**	**[10]**	**[11]**	**[12]**
Type		RSD	SAR	Pipe	Pipe
Tech	nm	180	90	180	90
Resolution	bits	6	9	10	10
Conv. rate	MS/s	20	50	50	100
Power	mW	1.8[e]	0.7	9.9	4.5
QVCO	**Unit**	**This work**	**[8]**	**[9]**	
Tech	nm	90	130	130	
Freq.	GHz	26	10	20	
Topology		cc [b]	cc [b]	cc [b]	
Tuning range	%	8	15	10.2	
Out Voltage	mVpp	200		50	
Power	mW	30[d]	14.4[c]	32	

a Power for single quadrant VMPS; double for 360°.
b Cross-coupled.
c Unbuffered output: high impedance output.
d Vdd=1.2V for 90nm tech.
e Vdd=1.8V for 180nm tech.

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