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Review and Classification of Gain Cell eDRAM Implementations

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***Abstract*—With the increasing requirement of a high-density, high-performance, low-power alternative to traditional SRAM, Gain Cell (GC) embedded DRAMs have gained a renewed interest in recent years. Several industrial and academic publications have presented GC memory implementations for various target applications, including high-performance processor caches, wireless communication memories, and biomedical system storage. In this paper, we review and compare the recent publications, examining the design requirements and the implementation techniques that lead to achievement of the required design metrics of these applications.**

I. Introduction

Embedded memories consume a dominant part of the overall area of ASICs and Systems-on-Chip (SoCs), and according to the 2011 International Technology Roadmap for Semiconductors (ITRS) [1] this trend will continue into the foreseeable future. Power dissipation has become the main performance limiter in modern microprocessors, and larger cache memories significantly improve micro-architectural performance and utilization of multi-core systems with only a modest increase in power [2,3]. In state-of-the-art processors, the die area devoted to cache memories is approximately 50%; however, memories occupy significant portions of lower performance systems and components, as well. The standby power of ultra-low power systems, such as biomedical implants and wireless sensor networks, is also often dominated by their embedded memories that continue to leak during long periods of system standby.

The traditional choice of embedded memories has been the 6T SRAM, as it provides high-speed read and write performance with robust static data retention. However, growing memory capacities have led to significant efforts to replace the relatively large SRAM bitcell with a smaller alternative. Concurrent read/write access is an effective method for achieving high memory bandwidth [4], but two-ported SRAMs require additional transistors to implement the unit cells, resulting in even larger area demands. In addition, the off-transistor leakage currents of SRAM cells have become one of the major power consuming components in VLSI systems, especially in standby mode. To combat power consumption, one of the most effective solutions has been found to be lowering the system supply voltage (V_{DD}). However, depleted read and write margins, coupled with increasing process variations, limit the minimum operating voltage of SRAM arrays. Hence, an appropriate candidate for the replacement of SRAM would need to provide high density, low power, and low-voltage operation, while retaining compatibility with standard logic fabrication processes [5].

Embedded DRAMs (eDRAMs) have long been a candidate for replacement of mainstream SRAMs in nanoscale CMOS due to their small cell size and non-ratioed circuit operation. However, the conventional 1-transistor, 1-capacitor (1T-1C) eDRAM requires costly process adders, and provides limited voltage downscaling, while requiring frequent power consuming refresh operations [6–8]. A partial solution to these drawbacks is provided by logic compatible gain-cell (GC) eDRAMs [7]. While the concept of gain cells dates back to the early 1970's, they fell into oblivion due to the predominant development of dedicated process technologies for stand-alone SRAM and DRAM chips. Only during the last decade have GC memories been discovered again as a potential alternative to SRAM due to their potential for higher density, lower power consumption, higher reliability, and 2-port functionality in advanced nodes and at low voltages. Since 2005, around 20 publications from industry and academia show innovative GC designs and array architectures, mostly aiming at replacing SRAM as high-speed caches in high-end processors. A few recent publications design and optimize GC memories for use in wireless communications systems or other fault-tolerant systems, while other work has verified the feasibility of low-voltage operation, making GC arrays good candidates for biomedical systems. [2,3,5,8–21].

Gain cells are dynamic memory bitcells comprised of 2–3 standard logic transistors and optionally an additional MOSCAP or diode. The additional devices (as compared to their 1T counterparts) are used to both increase the in-cell storage capacitance, as well as amplify the readout charge flow as compared to the stored charge level, thus providing the name "gain" cells [12]. The reduced device count results in a much higher bitcell density, as compared to a standard SRAM, while the decoupled read port provides both a non-destructive read operation and two-ported functionality. Neither read nor write operations suffer from the ratioed contention between devices in a 6T SRAM, resulting in increased margins and enabling voltage scaling [15,19]. Finally, leakage power is highly reduced, as fewer devices suffer from Drain Induced Barrier Lowering (DIBL), and scaled supply voltages reduce other leakage components.

Despite these favorable features, gain cells suffer from a number of drawbacks. The primary concern is the small internal storage capacitor that results in short retention times, requiring power-hungry refresh operations. In addition, the depleted storage voltages following a long retention period result in poor read performance. These characteristics are highly dependant on process-voltage-temperature (PVT) variations, thereby requiring careful margin distribution, cell tracking, and reference voltage control [2].

In this paper, we examine the various gain cell implementation options and consider the resulting trade-offs. We review the methods for contending with the drawbacks and improving the performance of the circuits. As a result, we will discuss

the compatibility of the existing designs to various target applications according to energy-efficiency aspects of these implementations.

II. Categorization of Gain Cell Arrays

From the large number of recent publications on GC memories, it is possible to identify three main categories of target applications: 1) high-end processors requiring large embedded cache memories; 2) fault-tolerant systems including channel decoders for wireless communications; and 3) low-voltage low-power biomedical systems.

A. Gain Cells for High-end processors

The vast majority of recent research on GC memories is dedicated to large embedded cache memories for microprocessors [2,3,5,9,11–14,16,22,23]. In fact, GC memories are considered to be an interesting alternative to SRAM, which has been the dominant solution for cache memories for decades. This is due to GC eDRAM's higher density, increased speed, and potentially lower leakage power. Besides the obvious advantage of high integration density, the main design goal for GC memories in this application category are high speed operation and high memory bandwith, especially for industrial players like IBM [13] and Intel [5,22], and recently also for academia [3,23]. A smaller number of research groups specify low power consumption as their primary design goal [2,14]. A recent study shows that GC memories can potentially consume less data retention power (i.e., the sum of leakage power and refresh power) than SRAM arrays (leakage power only) [3].

B. General Systems-on-Chip

Several authors are not very specific about their target applications [7,10,24], as they only mention general SoCs. However, they follow the same trend as the aforementioned processor community by proposing GC memories as a replacement for the mainstream 6T SRAM solution. For these SoC applications, the main drivers are the potential for higher density and lower power consumption than SRAM.

C. Gain Cells for Wireless Communications Systems

A small number of recently presented GC memory designs are fundamentally different from the aforementioned work, as they are specifically built and optimized for systems which require only short retention times, and, in some cases, are tolerant to a small number of hardware defects (read failures) [25]. The refresh-free GC memory used in a recently published low-density parity check (LDPC) decoder is periodically updated with new data, and therefore requires a retention time of only 20 ns [20]. Besides safely skipping power-hungry refresh cycles and designing for low retention times, the work in [8,21] also exploits the fact that wireless communications systems and other fault-tolerant systems are inherently resilient to a small number of hardware defects. In fact, by proposing memories based on multilevel GCs, the storage density of GC memories is further increased at the price of a small number of read failures which do not significantly impede the system performance [8,21].

D. Gain Cells for Biomedical Systems

While the previously described target applications require relatively high memory bandwidth, several recent GC memory publications target low-voltage low-power biomedical applications. A GC memory implemented in a mature low-leakage

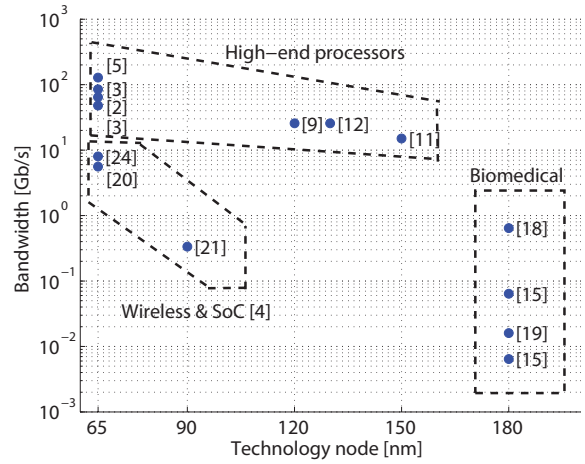


Fig. 1. Bandwidth vs. technology node of several previously published studies.

180 nm CMOS process achieves low retention power through voltage scaling well below the the nominal supply voltage [15]. The positive impact of supply voltage scaling on retention time for given access statistics and a given write bitline control scheme is demonstrated in [18], proposing near-threshold (NVT) operation for longer retention times and therefore lower retention power. A recent study [19] shows that the supply voltage of GC arrays can even be scaled down to the subthreshold (sub-V_{T}) domain, while still guaranteeing robust operation and high memory availibility for read and write operations.

E. Comparison of State-of-the-Art Implementations

Fig. 1 shows the bandwidth and the technology node of state-of-the-art GC memory implementations, highlighted according to target application categories. References appearing multiple times correspond to different operating modes or operating points of the same design. A more than four orders-of-magnitude difference in the achieved memory bandwidth among the various implementations. GC memories designed as cache memory for processors achieve around 10 Gb/s if implemented in older technologies and over 100 Gb/s if implemented in a more advanced 65 nm node. Most memories designed for wireless communications systems or generally for SoCs still achieve bandwidths between 1 and 10 Gb/s. Only the high-density multilevel GC array has a lower bandwidth due to a slow successive approximation multilevel read operation [21]. GC memories targeted towards biomedical systems are preferably implemented in a mature, reliable 180 nm CMOS node and achieve sufficiently high bandwidths between 10 Mb/s and several 100 Mb/s at NVT or sub-V_{T} supply voltages.

Fig. 2 plots the retention power (*i.e.*, the sum of refresh power and leakage power) of previously reported GC memories versus their retention time. For energy-constrained biomedical systems, long retention times of 1–10 ms are a key design goal in order to achieve low retention power of between 600 fW/bit and 10 pW/bit. The memory banks of the LDPC decoder have a nominal retention time of 1.6 µ [20], which is around four orders-of-magnitude lower than that of the arrays targeted at biomedical systems. Even though the reported power consumption of 5 µW/bit corresponds to active

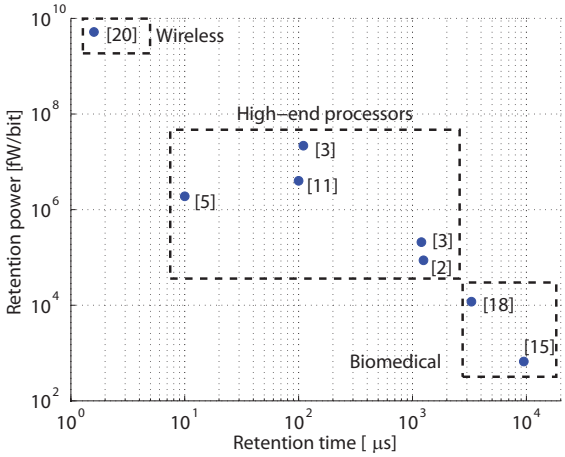


Fig. 2. Retention Power vs. Retention Time for several previously published studies.

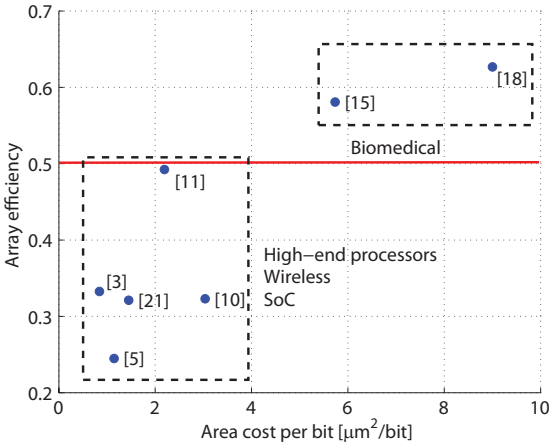


Fig. 3. Array efficiency vs. Area Cost Per Bit for several previously published studies.

power [20], it is fair to compare it to the retention power of other implementations, as data would anyway need to be refreshed at the same rate as new data is written. Interestingly, the power consumption per bit of this refresh-free eDRAM is almost seven orders-of-magnitude higher than the retention power per bit of the most efficient eDRAM implementation for biomedical systems. The retention time and retention power of GC memories for processors are in between the values for the wireless and biomedical application domains. Overall, of course, it is clearly visible that enhancing the retention time is an efficient way to lower the retention power.

The area cost per bit (ACPB) is defined as the silicon area of the entire memory macro (including peripheral circuits), divided by the storage capacity. As opposed to the simple bitcell size metric, ACPB accounts for the area overhead of peripheral circuits and is a more suitable metric to compare different memory implementations. Moreover, we define the array efficiency as the bitcell size divided by the ACPB to normalize this metric independent of technology node. Fig. 3 shows the comparably higher ACPB of biomedical GC memories due to the use of a mature 180 nm CMOS node. However, despite their small storage capacity requirements, these implementations achieve a high array efficiency of over 0.5, by using small yet slow peripherals [15]. On the other hand, none of the GC memories targeted toward processors, wireless communications, or SoC applications achieves an array efficiency as high as 0.5, meaning that over half of the area of the macrocell is occupied by peripheral circuits.

III. Circuit Techniques for Target Applications

In the previous section, we examined the recently proposed GC arrays and analyzed their target systems and applications. A primary conclusion was that gain cells have been shown to be an attractive alternative to traditional SRAM arrays for large caches, ultra-low power systems, and wireless communication systems. In this section, we will take a closer look at the circuits used in these proposals, and analyze the compatibility of these techniques with their target metrics.

A. Gain-Cell Topologies

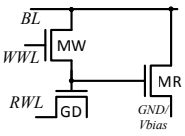
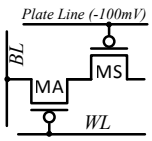
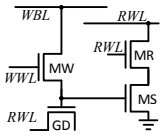
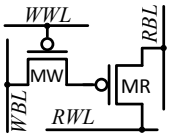
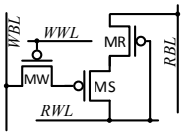
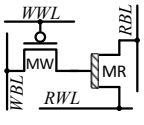
An extensive comparison between recent GC topologies is presented in Table I. The common feature for all these circuits is their reduced device count, as compared to traditional SRAM circuits. The highest device count appears in [13], comprising three transistors and a gated diode, with all other proposals made up of two [3,5,11,15,18,19,22] or three [2,8–10,12,14,20,21,24] transistors. The obvious implication of the transistor count is the bitcell size; however, the choice of the topology is application dependent, as well. The simple structure of the 2T topologies usually includes a write transistor (MW) and a read transistor (MR). MW connects the write bit line (WBL) to the storage node when the write word line (WWL) is asserted, and MR amplifies the stored signal by driving a current through the read bit line (RBL) when the read word line (RWL) is asserted. The 2T structure results in coupling effects between the control lines and storage node, which can affect the data and degrade performance. Therefore, a third device is often added, primarily to decouple RBL from the storage node and reduce RBL leakage. This option enables the designer to trade off density for enhanced performance, robustness, and/or retention time. This trade-off is quite apparent in the cache designs, as the larger capacity systems [3,5,11] prefer the 2T topology at the cost of additional hardware to retain performance. The *Boosted 3T* topology of [2] actually utilizes the coupling effect to extend the retention time by connecting MR to RWL rather than ground, thereby negating some of the positive voltage step inherent to the PMOS MW configurations. An interesting choice of the 2T topology was used in [19] even though the target application was a small array for ultra-low power biomedical sensors. In this case, the stacked readout path of the 3T topology proved to be too slow under sub-V_{T} biases.

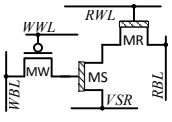
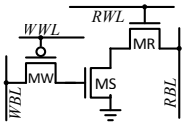
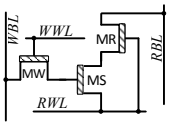
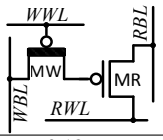
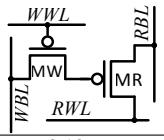
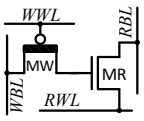
One of the basic considerations that differentiate between high-performance and low-power systems is the refresh power. Whereas high-performance systems may employ a destructive read operation with write-back, low-power systems ensure a non-destructive read and try to maintain high retention times to minimize refresh power. This is apparent in the "Main Design Metric" row of Table I, showing orders-of-magnitude difference in retention time between the two target categories.

B. Device Choices

The majority of today's CMOS process technologies provide several device choices, manipulating different oxide

TABLE I
DRIVER OPERATING MODES

Category	High Performance Processor Caches					
Publication	**[9,12,24]**	**[11]**	**[13]**	**[5,22]**	**[2,14]**	**[3]**
Bitcell						
Tech. Node	0.12 µm, 0.13 µm, 65 nm PTM	0.15 µm	90 nm	65 nm	65 nm	65 nm
Techniques	Gated Diode, Footer Power Gating, Foot Driver	Multi-Level Bitlines, Hybrid open bitline architecture	Gated Diode Sense Amplifier	RBL Clamping, Pipelined Architecture	Boosted 3T, PVT tracking read reference feedback, Regulated WBL	Half Swing WBL, Stepped WWL
Main Design Metric	400 MHz, 70 µs retention, 100 kb	400 MHz, 100 µs retention, 1 Mb	up to 2 GHz, 110 µs retention, 40 kb	2 GHz, 10 µs retention, 2 Mb	500 MHz, up to 1.25 ms ret., 64 kb	667 MHz, 110 µs ret., 192 kb

Category	General SoC		Wireless	Low Power Biomedical Systems		
Publication	**[10]**	**[8,21]**	**[20]**	**[15]**	**[18]**	**[19]**
Bitcell						
Tech. Node	90 nm	90 nm	65 nm	0.18 µm	0.18 µm	0.18 µm
Techniques	Forced Feedback, Write Echo Refresh	Multi Level Bitcell, PVT Replica Column	Refresh Free, Sequential Decoding	I/O Write Transistor, Low Area Sense Buffer	Low Area Sense Buffer	Hybrid Cell with I/O MW, Sense Buffer
Main Design Metric	V_{DD} =0.5 V, 180 µA ref. power, 5 MHz	2–50 µs retention, 1.45 µm^2/bit density	32× 1 kb arrays, 700 MHz, 170 ns retention	V_{DD}=0.75 V, up to 306 ms ret., 0.1–1 MHz, 662 fW/bit ret. power	V_{DD}=0.75 V, 3.3 ms retention, 11.9 pW/bit ret. power	V_{DD} =400 mV, over 40 ms ret., 500 kHz

thicknesses and channel implants to create several threshold (V_{T}) and voltage tolerance options. Careful choice of the appropriate device (PMOS/NMOS, standard/high/low V_{T}) can provide orders-of-magnitude improvement in GC performance, as apparent in Table I. PMOS devices suffer from lower drive strength than their NMOS counterparts, but have substantially lower sub-V_{T} and gate leakage. Since the majority of GC implementations are read access limited, PMOS devices are used in the vast majority of the proposed circuits. For most of the common process technologies, the primary cause of storage node charge loss is sub-V_{T} leakage through MW, and therefore the ultra-low power implementations [15,19] employ a high-V_{T} or I/O PMOS to substantially extend retention time. Gate leakage is a substantial contributor in thin oxide nodes, and so the all-PMOS 2T configuration [5] balances the sub-V_{T} and gate leakages out of and in to the storage node to improve retention time. The decoder system of [20] requires high performance with very short retention times, and therefore an all NMOS low-V_{T} circuit is used. Low-V_{T} devices are used in the readout path of several other publications [3,10], to improve read performance without a large static power penalty, as the voltage drop over the read node is minimal during write and standby cycles.

An important effect caused by device choice selection is the storage node coupling and charge injection. WWL access significantly modifies the initial level of the storage node, depending on several factors. A PMOS write transistor passes a *weak* $'1'$, and an NMOS passes a *weak* $'0'$; therefore an underdrive (PMOS) or boosted (NMOS) access voltage of WWL is necessary to pass a full level to the storage node. However, the larger the WWL swing is, the larger the step in the direction of the deassertion at the storage node. A PMOS MW, for example, is cut-off by the rising edge of WWL, resulting in both capacitive coupling and charge injection to the storage node. Therefore, the initial $'0'$ value will always be significantly higher than ground for a PMOS MW, and the initial $'1'$ value will be significantly lower than V_{DD} for an NMOS device. This limits the storage node range and degrades both the readout overdrive, as well as the retention time. Using a same-type device for MR of a 2T cell induces an additional step in the same direction during read access, further impeding the performance. A hybrid cell, mixing NMOS and PMOS devices [3,8,10,19,21], can be used to combat these effects at the expense of in-bit well separation.

C. Circuit Techniques

In addition to the choice of a circuit topology and device options, several circuit techniques have been demonstrated to further improve system performance according to the target application. One simple and efficient technique is the employment of a sense buffer in place of a standard sense amplifier (SA) in low-power systems [15,18,19]. This implementation requires a larger RBL swing, trading off speed for area and PVT sensitivity. The area trade-off is apparent in Fig. 3 as [15] shows exceptionally high area efficiency. Several

other SA configurations have been demonstrated to deal with various design challenges. The authors of [11] proposed a *force feedback SA* to enable operation at voltages as low as 0.5 V. Chun, *et al.* [3] overcome the problem of small RBL voltage swing by using a current mode SA featuring a cross-coupled PMOS latch and pseudo-PMOS diode pairs. Other SA designs used include p-type gated diodes [9,12,13], offset compensating amps [11], single-ended thyristors [20], and standard latches [5]. The most complex sensing scheme is used for Multi-Level Bitcells in [8,21]. To decipher the four data levels, a successive approximation SA is used.

Several publications [10,15,18,19] discharge WBL during non-write operations to extend retention time that is worse for a stored $'0'$ than a $'1'$ with a PMOS WM. A *Write Echo Refresh* technique was employed by Ichihashi, *et al.* [10], to further reduce the WBL=$'1'$ disturbance. In this technique, the number of $'1'$ write-back operations during refresh are counted and oppositely biased to combat the disturbance. The authors of [2] recognized that the steady state level of a $'1'$ and $'0'$ is common, so they monitor this level and use it as the WBL voltage for writing a $'1'$. This minimizes the $'0'$ level disturbance without impeding the worst-case $'1'$ level. For the system proposed in [3], WBL switching speed is the performance bottleneck, and therefore a half-swing WBL is employed, improving the write speed and reducing the write power.

An issue that is rarely discussed in 2T bitcell implementations is the voltage saturation of RBL during readout. Depending on the implementation of MR, readout is achieved by either charging (NMOS) or discharging (PMOS) RBL. However, once RBL crosses a threshold (depending on the current ratio of the selected bitcell and the number of off unselected cells), a steady state is reached. This phenomena not only limits the swing available for RBL sensing, but also causes static current dissipation that is present throughout the entire read operation. This is one of the phenomena considered in the analysis of [18] resulting in an optimal choice of V_{DD} for a low-power GC. Somasekhar, *et al.* [5] combat the self clamping of RBL by explicitly clamping its voltage under with designated devices.

IV. Conclusion

In this paper, we reviewed and compared the recently proposed GC memories, categorizing them according to target applications and overviewing the characteristics that make them appropriate for these applications. A closer look into the circuit design of these arrays provided further insight into the methods used to achieve the required design metrics through the use of different bitcell topologies, device options, technology nodes, and peripheral implementations. To summarize briefly, the following best practice guidelines should be followed when designing GC arrays for future applications:

- High-V_{T} write access transistors for long retention times and low refresh power, in conjunction with area-efficient sense buffers for high array efficiency are most suitable to meet the storage requirements of biomedical systems.
- High-speed applications should use sensitive sense amplifiers to overcome small voltage differences, and should consider the use of LVT readout transistors for improved read access.
- Frequently updating wireless communication systems can trade-off high-speed access for limited retention time to achieve improved bandwidth.

Acknowledgment

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