

A Switched Capacitor Fully Differential Correlated Double Sampling Circuit for CMOS Image Sensors

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Abstract—Complementary metal oxide semiconductor (CMOS) image sensors are more compatible than charge coupled devices (CCDs) for lab-on-a-chip platforms due to their inherited advantages. However, without the noise reduction circuits, CMOS technology wouldn't be able to compete with CCDs. Today, correlated double sampling circuits (CCDs) are used in all CMOS imagers in order to remove the reset noise and the fixed pattern noise. However, these circuits immensely decrease the fill factor of the image sensors because of their large area and their requirement of extra circuitries in order to convert their single ended outputs to differential outputs. In this paper, we propose a CDS architecture convenient for CMOS imagers that uses switched capacitor fully differential configuration which reduces the noise in the same way as the conventional CDS architectures while decreasing the area and increasing the fill factor.

I. INTRODUCTION

Integrated lab-on-chip platforms attract many interest in particular for biomedical applications especially due to their low cost, portability and effectiveness by their application based designs [1], [2]. They have a wide range of investigation in today's fast evolving research atmosphere. Lab-on-chip platforms may also be easily integrated with image detection systems. However, these type of biomedical applications have immense noise, area and sensitivity constraints and require special effort on noise reduction circuitries.

Image detection systems use different image detecting methods. Among these methods, fluorescence detection systems are most popular ones especially in molecular biology and biochemistry [3], [4]. For example, in the literature, it was shown that toll-like receptors 2 (TLR2) and 4 (TLR4) which play central role in the immune system and are expressed on the surface of immune-component cells such as monocytes [5], vary in amount according to the given dairy food [6]. These proteins recognize foreign substances and activate intracellular signaling cascades to induce gene expression. The dependence of the amount of the TLR2 to the given food has been validated on macrophages by examining the TLR2 expression at different times after the Lipopolysaccharide (LPS) induction. However, this experiment requires the usage of large and expensive experiments in a laboratory environment and is not suitable for simple and fast nutrition analysis. As opposed, a lab-on-a-chip platform dedicated only to nutrition analysis would easily differentiate the food samples according to the variance in toll-like receptors. Hence, it is our aim to build a fluorescence detection system by use of a CMOS technology

and finalize the system with a highly application dedicated lab-on-a-chip platform.

Due to the inherited advantages of CMOS technology over CCDs i.e low power consumption, lower voltage operation, on-chip functionality, lower cost and high integration capability, CMOS technology becomes a better candidate for lab-on-chip platforms despite its lower noise performance [7], [8]. However, in order to overcome the noise limitation of CMOS technology, it is important to have a detailed work on the noise generation in CMOS imagers as well as on possible noise reduction circuits before taking any further step in image sensor design which needs high dynamic range, high sensitivity as well as low area and power consumption for the mentioned lab-on-a-chip platform.

Hence, within the scope of this paper, it is our intention to introduce a convenient noise reduction circuitry for lab-on-a-chip platforms -fully differential switched capacitor CDS technique-, that is more effective in terms of area and fill factor, that gives real fully differential output which can be directly connected to an Analog to Digital Converter (ADC) stage and avoids the usage of extra circuitries for single ended to fully differential conversion which introduces additional noise and reduces the fill factor. The organization of this paper will be as follows: in sectionII, noise sources in CMOS image sensors will be investigated, in section III, current circuit strategies based on correlated double sampling circuits, to reduce fixed pattern noise in different active pixel sensors will be shown, in section IV, a switched capacitor fully differential correlated double sampling circuitry will be proposed together with an improved version with offset compensation and in the last section, the simulation results of the proposed architectures will be shown.

II. IMAGE SENSOR IMPLEMENTATIONS WITH DIFFERENT CDS ARCHITECTURES

Active pixel sensors have become very popular in mid-nineties and still maintain its value since there is an huge research interest on noise reduction in CMOS imagers. Pixel offset noise and reset noise in CMOS active pixel sensors are canceled with a technique called Correlated Double Sampling (CDS) which removes the noise by differencing sampled values taken from the same pixel before and after integration. Typically, each column in every image sensor has a CDS circuitry, which reduces the fill factor significantly, at the same time initiate additional noise depending on the CDS

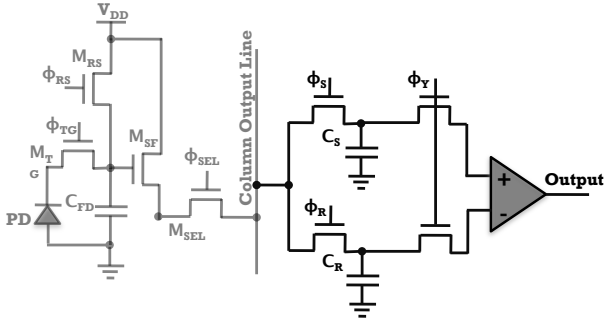


Fig. 1: Traditional Representation of CDS Circuitry with 4T APS

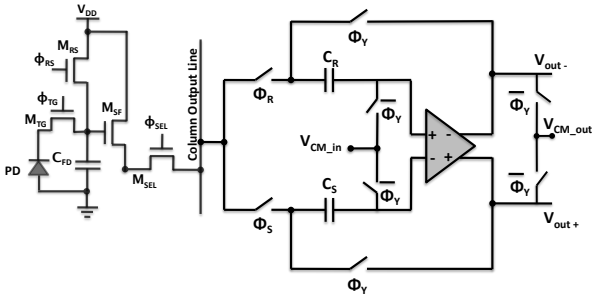


Fig. 2: Proposed Fully Differential CDS Architecture - CDS1

architecture. Traditionally, CDS consists of sample and hold capacitors, C_S and C_H together with Sample and Hold (S/H) switches ϕ_S and ϕ_R and additionally the differencing switch ϕ_Y and differencing single ended amplifier as seen in Fig. 1. In most of the single ended pixels, CDS differencing operation is performed by two buffers as in [9]. This method provides a pseudo-differential output and has the necessity to be converted to a fully differential signal by means of a fully differential amplifier. The extra pseudo-differential to fully differential conversion circuitry gives the flexibility to increase the gain with the capacitance ratios by almost doubling the CDS area in each column as a tradeoff. Another method that is mentioned in [10] is to use an unity gain configured switched capacitor single ended amplifier instead of two buffers, and in the following stage as in the traditional method, to convert from single ended to fully differential by means of a unity-gain or gain configured fully differential amplifier.

Thus, both of the implementations suffer from the loss of area with their requirement of extra single ended to fully differential conversion circuits. In addition, the first method complicates the timing diagram due to the extra switches required for a switched capacitor offset compensated fully differential amplifier in addition to the S/H and differencing switches of the CDS itself.

III. PROPOSED CDS CIRCUITRY

With the problems addressed in the previous section and with the questions in mind appearing as why we are bothered by the single ended output and how to reduce the area cost

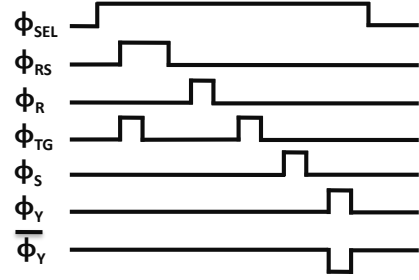


Fig. 3: Timing Diagram of the Proposed CDS Architecture

of CDS, we ended up designing a CDS circuit providing a real differential output from the differencing operation. By this method, we avoid the usage of extra differential conversion circuitry and relatively reduce the area of CDS. In Fig. 2, the unity gain switched capacitor fully differential amplifier is shown as an alternative CDS circuitry with the timing diagram in Fig. 3. To the best of our knowledge, apart from the fully differential transimpedance amplifier (TIA) CDS circuits in differential pixels [3], fully differential CDS architectures haven't been proposed by the designers except in [11], where the differencing operation of the CDS is done only through the positive input node of the op-amp and the negative input node is always kept connected to the common-mode voltage. However, this design complicates the timing operation as well as extremely increases the number of switches. As opposed, the architecture we propose in Fig. 2 offers a very simple solution with an easy clocking scheme. The amplifier basically operates as a unity gain buffer [12] with additional two sampling switches as ϕ_S and ϕ_R in order to charge the pixel value before and after integration. In this architecture, first at ϕ_{RS} pixel is reset through M_{RS} transistor. After the reset operation, when ϕ_R is high, pixel reset value is charged on the capacitor with the loss of offset and the capacitor value becomes $V_{reset} + V_{os}/2$. Later, when ϕ_{TG} becomes high and with the light incident on the photodiode, photodiode current starts discharging the reset voltage value. At the end of the integration phase, ϕ_S becomes active and the pixel value after integration is sampled on the capacitor at the negative input of the amplifier and the capacitor is charged to $V_{sig} - V_{os}/2$. Finally, at ϕ_Y phase, pixel value after integration is subtracted from the pixel value before the integration and final value is found as $V_{reset} - V_{sig} - V_{os}$. There are a few problems that should be addressed about this CDS architecture. First of all, this architecture requires the op-amp output to be reseted at each clock cycle, which decreases the effective timing of the op-amp by half and makes the slew rate and settling time requirements of the op-amp difficult [12]. However, although this is an important concern for sample and hold circuits, analog memories or delay stages that unity gain buffers are widely used, it is not an issue for this application since the timing intervals are already determined in the pixel section, and a final differencing clock ϕ_Y is indispensable. However, there are two other problems that should be more carefully analyzed; gain compensation and

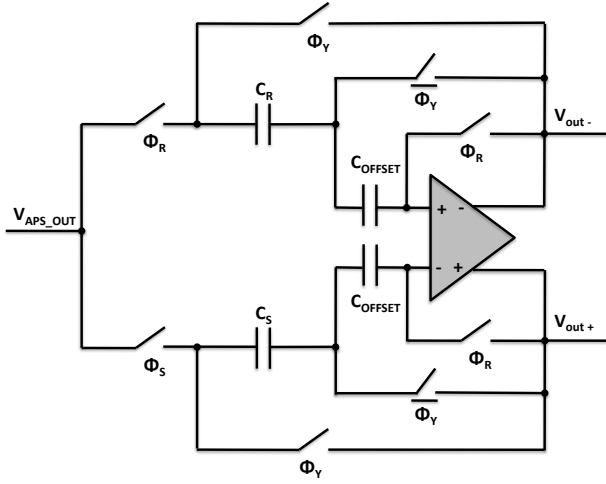


Fig. 4: Improved Fully Differential CDS Architecture with Offset Compensation - CDS2

offset compensation. The unity gain buffer architecture neither provides gain compensation nor offset compensation where latter is more important since the amplifier offset introduces column FPN to the image sensor. Because of this reason, the proposed architecture is improved to an offset compensated scheme as in Fig. 4. The offset compensated architecture has the same timing diagram as the first proposed architecture. It has two additional capacitors to charge the offset of the amplifier to the capacitors during the $\overline{\phi_Y}$ phase and during the ϕ_Y phase, offset that is charged on the offset capacitors are subtracted from the pixel voltage before and after integration. In this architecture, during ϕ_R phase, not only the reset voltage of the pixel is charged on the C_R capacitor, but also differential outputs are connected to the differential inputs in order to set the initial values to the amplifier inputs and to avoid floating inputs due to the offset capacitors connected to the differential inputs. Illustration of the switch settings of the improved CDS architecture at different phases is shown in Fig. 5 which explains the offset compensation and charge distribution in a better way. Gain compensation is left out of the scope of this paper. However, if required the design can be evolved to a gain and offset compensated architecture as explained in [12].

IV. SIMULATION RESULTS

In this chapter, simulation results of the two proposed fully differential switched capacitor CDS architectures will be shown. The main concern of these simulations is the noise generated by these CDS architectures itself. In the first simulation in Fig. 6, the transient behaviors of the the proposed architecture is shown. As seen by the figure, when the ϕ_Y switch is active, the differential outputs are generated. In Fig. 7, the output noises $\text{dB}(V^2/Hz)$ of the two CDS architectures are compared. The dashed line corresponds to the output noise of the architecture without offset compensation and the straight line corresponds to the one with offset compensation. Since the output noise simulation excludes the dc offset, here we see an increase in the output by the offset compensation architecture,

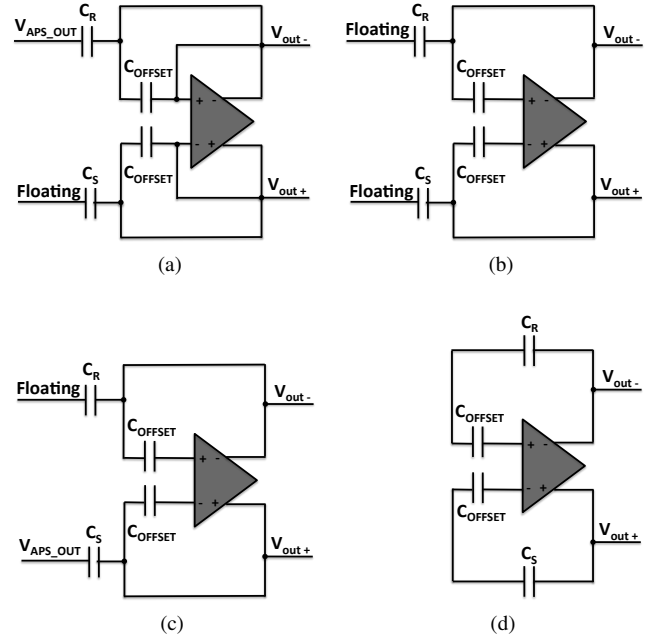


Fig. 5: Improved CDS Clocking Sequence:

- ϕ_R is ON, pixel reset value is charged on C_R and initial values are set at the op-amp input terminals.
- ϕ_R and ϕ_S are both OFF, offset is charged on C_{offset} .
- ϕ_S is ON, pixel voltage after integration is charged on C_S .
- ϕ_Y is ON, pixel value after integration is subtracted from the pixel reset value together with amplifier offset.

due to the increased number of components. The second simulation in Fig. 8 shows the comparison of the simulated SNR results versus the input signal amplitude of the two CDS architectures. Here what is meant by the input signal amplitude is the voltage drop from the initial reset value after the integration period which means that input signal level is expected to be low for low illumination and high for high illumination. When simulating SNR, the reset input is kept constant as in the real case and the input signal which is the voltage drop due to the illumination is varied. The improvement by the offset compensation can now be clearly seen. When the input signal is 500mV, the highest SNR is reached which is 74.12dB for the CDS architecture without offset compensation and 81.79dB for the architecture with offset Compensation. The importance of the offset compensation is even more clear when the input signal is at its minimum. When the signal is 1mV SNR achieved by the first architecture is 22.23dB while it is 32.4dB for the latter. When doing these simulations, the input frequency is set as 137Hz while the sampling frequency is 2.5kHz.

V. CONCLUSION

CMOS image sensors for biological researches especially for fluorescence detection systems have been an interest through many years now. Noise reduction circuits are indispensable blocks in CMOS image sensors. These circuits

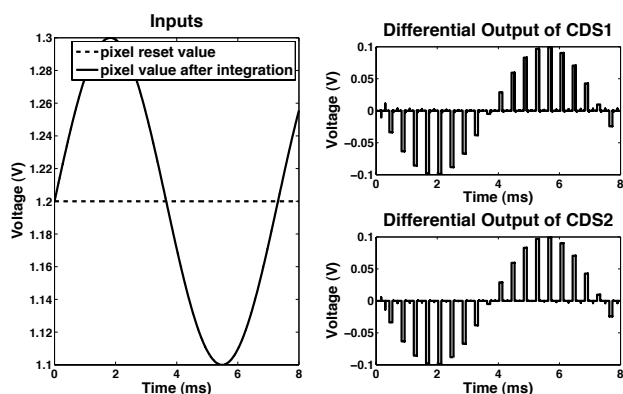


Fig. 6: Transient Behaviors of the Two CDS Architectures

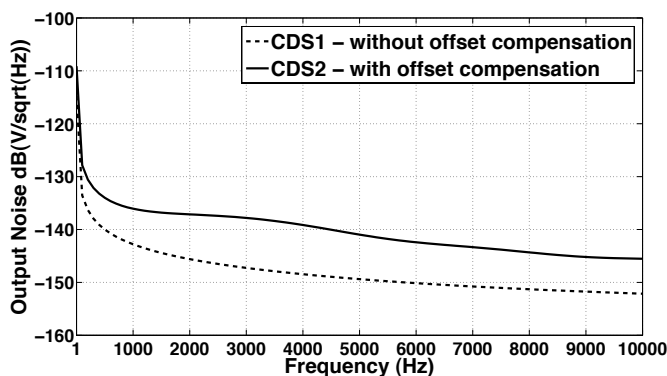


Fig. 7: Output Noise Comparison of the two architectures - Unity Gain Buffer vs Unity Gain Buffer with Offset Compensation

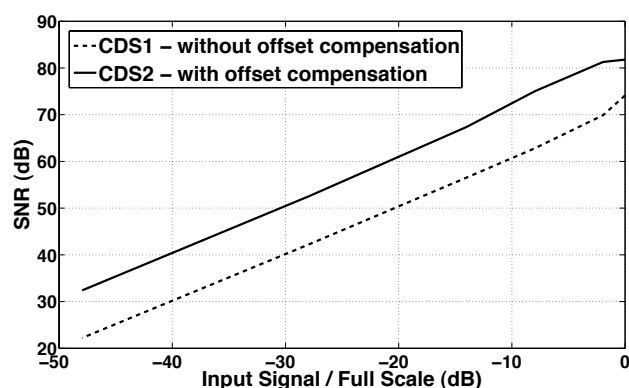


Fig. 8: SNR Comparison of the Two Architectures

occupy large area and reduce immensely the fill factor of the image sensors. Although typically these circuits are simply constructed by 4 switches, 2 capacitors and 2 buffers, they generate pseudo-differential outputs and they need to be converted to fully differential signals before their outputs are connected to the following Analog to Digital converter stages. For this operation, assuming having no gain or offset compensation, 2 capacitors and a fully differential OTA with reasonable gain are required. In this paper, we proposed two CDS architectures both merging the two mentioned blocks of CDS; traditional CDS and pseudo differential to fully differential converter. The proposed architectures not only generate a direct differential output from the CDS, but also promise area reduction by half. First proposed architecture is a basic unity gain buffer and the second one is the improved version of this with offset compensation. The latter of two shows a better SNR performance with increase of 10dB at the lowest signal value in where the offset is most effective.

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