Modeling methodology of high-voltage substrate minority and majority carrier injections

Fabrizio Lo Conte, Jean-Michel Sallese, Maher Kayal
Electronic Laboratory (e-lab.epfl.ch)
EPFL, 1015 Lausanne, Switzerland - fabrizio.loconte@epfl.ch

***Abstract*—This paper presents a modeling methodology for substrate current coupling mechanisms. An enhanced model of the diode ensuring continuity of minority carriers is used to build an equivalent schematic, accounting for minority and majority carrier propagation in the substrate. For the first time a typical H-bridge structure is simulated with the proposed methodology. The parasitic current injected in the substrate by a high-voltage structure is simulated in a circuit-level simulator as well as with a finite elements method. Both are compared to measurements and show a very good agreement. The simulation resources needed by the proposed equivalent schematics are thus greatly reduced in regard to the finite element approach, offering an efficient tool for substrate modeling in smart power IC's.**

I. INTRODUCTION

A new trend in integrated electronics is to concentrate different types of electronic functions on the same substrate, going from sensitive analog circuits to dense and fast digital functions. Moreover, in advanced applications, where actuation of external parts is required, it is common to have high-voltage and high-power circuits integrated in the ASIC.

This kind of technology is called Smart Power IC. The driving capabilities are typically in the order of 40V and can reach several amperes. These integrated circuits are commonly used in consumer electronics (printers, scanners, etc.) as well as in automotive and avionics applications [1].

Typically these technologies are integrated on standard low-voltage CMOS technologies (such as 0.18µm) with some additional steps to implement high-voltage transistors. Electrical isolation between these high-voltage elements can be obtained in different ways, such as self-isolation, trench-dielectric-isolation and junction isolation [1].

In junction isolation topology, isolation is obtained by the reverse biasing of PN junctions, where the P-type part is the substrate and the N-type part is the drain or source of high-voltage NMOS or PMOS transistors, respectively. When inductive or capacitive loads are switched, these junctions can be direct-biased and will inject electrons and holes directly into the substrate. Those electrons and holes will be further coupled by other junctions integrated in the same substrate [1-4].

This electrical coupling noise can severely disturb low voltage analog circuits located in the surrounding area, and may also deeply affect the functionality of digital parts. Such parasitic signals represent the major cause of failure and provoke the need for expensive circuit redesign [1, 3].

Today, this parasitic coupling is modeled using standard bipolar transistors or thyristors models. Typically the coupling between 2 NMOS drains is modeled by a lateral NPN transistor [1-4], where the emitter and collector of the bipolar transistor represents the N-type diffusion of the NMOS drain, and where the P-type base of the lateral bipolar transistor represents the substrate. A cross-section of the high-voltage transistor is shown in Figure 1. The extraction of the parameters for parasitic transistors is highly dependent upon the layout and the coupling effects should be accounted for in a 3-dimensional way [2]. In a classical H-bridge structure, at least four high-voltage transistors are used, leading to a very complex equivalent bipolar schematic with transistor parameters depending on the biasing. Moreover, imposing a bipolar 'meshing' may not be valid in this case.

This lack of design methodology prohibits an efficient design strategy and fails to give clear predictions of electrical perturbations in high voltage integrated circuits.

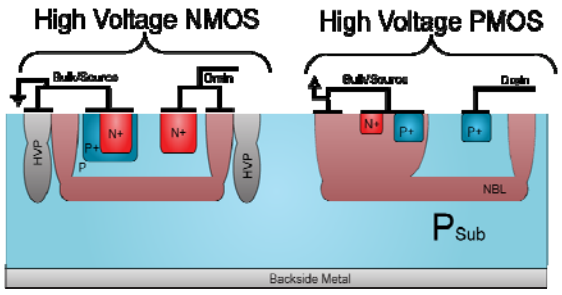

Figure 1. Cross Section of a Smart Power IC LDMOS with bipolar identification and the equivalent diode schematic

A new modeling approach was proposed in [5,6] using an enhanced diode model. The adopted concept consists of providing additional terminals to the diode in order to keep minority carrier continuity at the interconnections. PN junctions are now the elements to be identified, instead of parasitic bipolar transistors. In addition, parameter extraction of the equivalent diode network is greatly simplified: parameters used in the model of the PN junction are mapped to technological and geometrical parameters of the layout.

In this paper we demonstrate that the parasitic substrate current can be modeled by an equivalent schematic of the substrate, followed by a systematic detection of individual PN junctions. This is a major improvement with respect to the tedious and arbitrary process of substrate bipolar

978-1-4244-6661-0/10/$26.00 ©2010 IEEE

transistors identification. The results obtained with this approach are compared to finite element simulations and to the measurements done on an integrated 40V H-Bridge structure.

II. Compact Model

The substrate equivalent schematic is obtained by interconnecting enhanced PN junctions that account for minority carrier continuity at the boundaries. Minority carrier concentration and gradient are outputted as voltage and current respectively, through an additional terminal. Therefore, minority carriers are not fully recombined at the contact between two diodes, allowing bipolar effect to take place as illustrated in Figure 2.

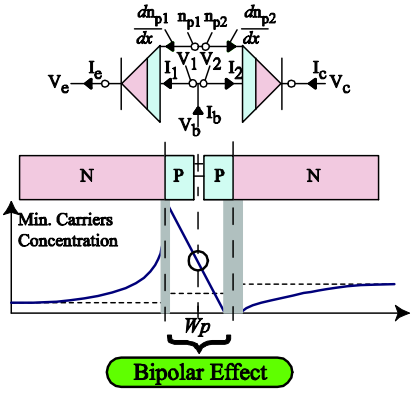

Figure 2. Equivalent bipolar schematic using enhanced diode model.

The parameters used by the enhanced diode model are listed in Table 1. The layout-dependent parameters are extracted from the dimensions of the junction, i.e. the size of the high-voltage NMOS transistor. The additional parameters are technology-dependent and therefore should be extracted from integrated test structures or directly from the components present in the design kit.

Table 1
Diode Parameters

Type	Parameter Name	Origin
Layout	N-Length	Schematic
	P-Length	Floor-Plan
	Width	Schematic
Technology	N doping	
	P doping	
	Tau_0	
	Tau_n	
	μ_p	

III. Integrated H-Bridge Structure

Figure 3 shows the integrated structure of a full 40V H-bridge having an ON resistance of 1Ω. Transistors N1, N2, P1 and P2 are classical driving transistors. Diode D1 and D2 are additional free-wheeling diodes used to limit the reverse biasing of the transistor when inductive loads are switched off. The additional transistors N3 and N4 are used during the test to inject or collect charges flowing in the substrate.

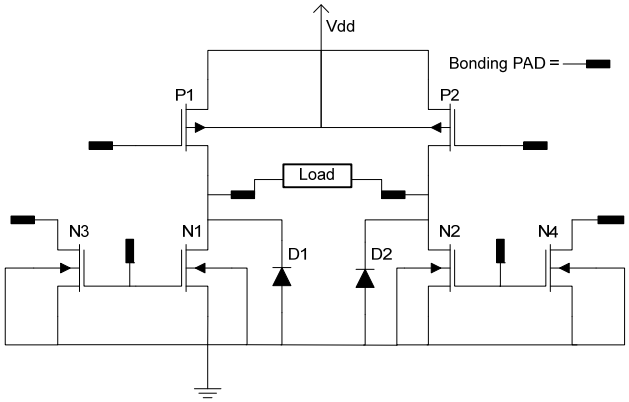

Figure 3. Integrated H-Bridge schematics.

The active dimension of the H-bridge is 760µm width and 700µm height. The placements of the transistors are shown in Figure 4. The two additional NMOS transistors are located in the center of the bridge, which is surrounded by a typical 9µm isolation structure, composed of a deep P diffusion connected to the ground.

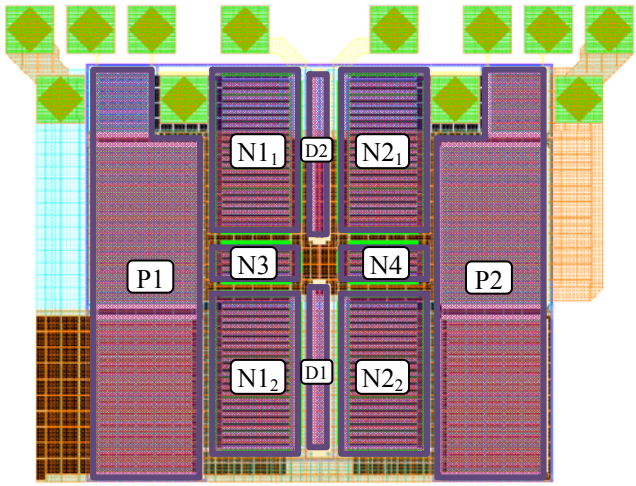

Figure 4. Integrated H-Bridge layout.

IV. Finite Element Analysys

In order to optimize the performance and the surface occupied by a transistor, it is essential to layout the transistor in a folded way; this means that the transistor is decomposed in many fingers that are connected together in a parallel.

Figure 5a shows a cross-section of a folded NMOS transistor. It is composed of three fingers that share drain and source terminals.

Simulating such a structure in a finite element simulator is very difficult; thus the structure needs to be simplified in order to reduce its complexity and to preserve carrier injection and collection in the substrate. The discrepancy in the latter is predominantly the result of the N-type buried layer (NBL) [2]. Moreover the current flowing in the drain to bulk diode is already taken into account in the transistor model. We keep only the NBL diffusion as illustrated in figure 5b.

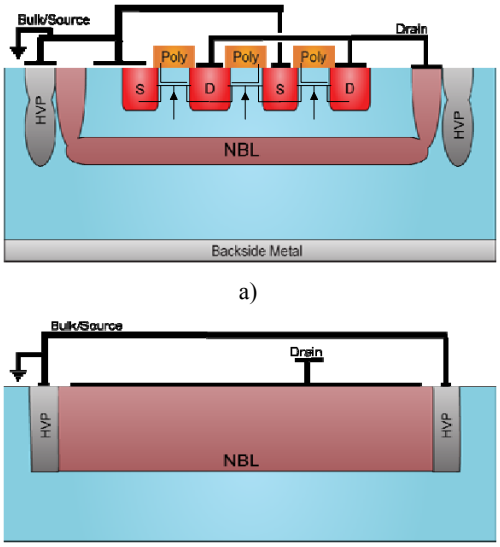

Figure 5. a) Cross-view of an NMOS folded layout, b) simplified structure

The PMOS transistor is different from the NMOS transistor, as shown in Figure 1. In this case, the NBL is connected to the bulk, i.e. the supply voltage.

In addition to the geometrical parameters extracted from the layout, some additional technological parameters are necessary to simulate the structure. These are summarized in Table 2.

Table 2
TECHNOLOGY PARAMETERS

Parameter Name	Value	unit
NBL doping	$8.5e^{18}$	cm^{-3}
HV-P doping	$6.1e^{15}$	cm^{-3}
Substrate doping	$9e^{14}$	cm^{-3}
Junction depth	5	µm
τ_p	$2e^{-6}$	second
τ_n	$5e^{-6}$	second
μ_p	470	$cm^2/V{\cdot}s$
μ_n	1417	$cm^2/V{\cdot}s$

In most cases all these technological parameters are confidential. Therefore, we set them to typical values [2, 7, 8] commonly encountered in high-voltage technology.

In the simulation shown in Figure 6 , transistor N4 is biased 0.5V below the substrate voltage, thus injecting a current in the substrate. Other transistors are biased to a positive voltage, thus coupling the injected charge.

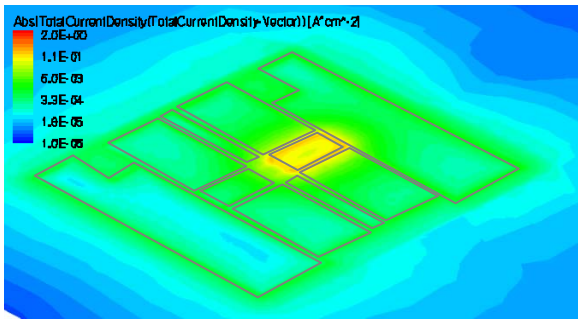

Figure 6. Current density, 10µm below the surface.

The currents coupled by each transistor are shown in Table 3.

Table 3
COUPLED CURRENT

Transistor name	Finite Elements		Measurements	
	Absolute value	Attenuation [dB]	Absolute value	Attenuation [dB]
N1	819nA	-25.26	896nA	-24.48
N2	7.13µA	-6.46	8.45µA	-4.99
N3	162nA	-39.33	244nA	-35.78
N4	–15µA	---	–15µA	---
Vdd	2.02µA	-17.41	2.24µA	-16.51
Gnd	4.85uA	-9.81	---	---

The drain voltage of transistor N4 during measurements was 0.528V

For a fair comparison between measurements and simulations, the injected current was matched to the one obtained from simulations. The results agree, confirming that the technological parameters and the transistor simplification were estimated correctly.

V. EQUIVALENT SCHEMATIC

In a second step, an equivalent schematic was implemented by further interconnecting the enhanced diode components to map the layout. Next the effects arising from the third dimension were obtained by adding a second layer inside the substrate. Additional components were used to model the vertical interconnections.

Figure 7 shows the equivalent schematics used to model the substrate around the transistors $N2_2$-P2-N4. It is composed of two parts. The top-layer models the first 5µm depth of the substrate. The bottom-layer accounts for the depth extending from 5µm to 15µm.

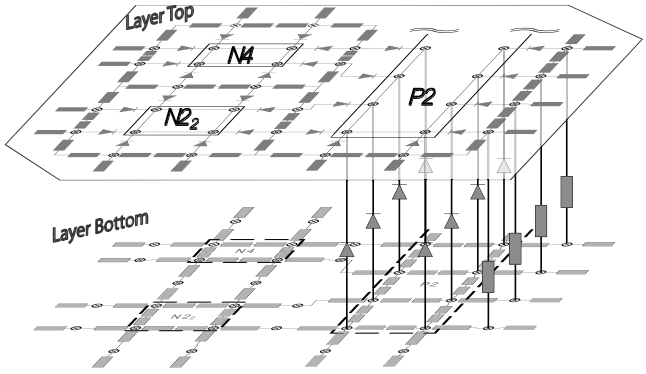

Figure 7. Equivalent schematic for $N2_2$-P2-N4 substrate region. (for readabily purpose some vertical elements are hidden)

All geometrical parameters were extracted from the layout of the H-bridge. The technological parameters are the same as those used for the finite element simulation.

Finally, the full equivalent schematic of the H-bridge and the surrounding substrate was implemented in a SPICE-like simulator. The N4 junction was biased 0.5V below the substrate potential. The results are presented in Table 4.

Table 4
COUPLED CURRENT

Transistor name	Schematic		Measurements	
	Absolute value	Attenuation [dB]	Absolute value	Attenuation [dB]
N1	80.5nA	-35.02	295nA	-24.59
N2	1.59μA	-9.12	2.79μA	-5.06
N3	22.3nA	-46.15	80nA	-35.9
N4	–4.56μA	----	–5μA	---
Vdd	672nA	-16.6	740μA	-16.6
Gnd	---	---	---	---

The drain voltage of transistor N4 during measurements was 0.498V

The parasitic coupled current obtained agrees with the measurements. The error must be analyzed, keeping in mind that this approach is devoted to parasitic substrate simulation, which does not need to be accurate within a few percent. The main difference between finite elements and schematic simulations is the injected current from a junction biased at -0.5V. This mismatch comes from the exponential characteristic of the diode that makes a significant difference in the injected current for a very small voltage difference.

The computational resources needed for these simulations are presented in Table 5, confirming that the SPICE-like simulation is a very good compromise between accuracy and CPU time.

Table 5
SIMULATION RESOURCES

Type	Finite Elements	SPICE Schematics
CPU Time	9h	10s
Memory	2.2GB	30MB

A complete functional simulation accounting for substrate coupled current can be done during the design of the circuit.

VI. CONCLUSION

This paper presents a general SPICE-compatible modeling methodology to simulate parasitic currents in IC's substrate that are responsible for circuit malfunction or run away, because of latching.

The equivalent schematic is based on an enhanced compact model of the diode, accounting for minority carriers at the component boundary. Classical technological parameters were used as input parameters and their values were validated through finite element simulations. The results obtained by the finite element method and the equivalent schematic agree with the measurement of an integrated high-voltage H-bridge. The simulation resources needed for the proposed modeling methodology are greatly reduced compared to the ones used by the finite element simulator.

This marks the first time that a systematic procedural modeling methodology has been used to build an equivalent schematic of substrate current propagation. It accounts for minority and majority carriers and allows a direct co-simulation of an H-bridge structure that fully includes parasitic substrate current.

ACKNOWLEDGMENT

This work has been supported by the Swiss National Funding Science Foundation, project 200021-125321/1.

The authors thank Advanced Silicon, Lausanne, for the technical and technological support provided during the development of the test circuit.

REFERENCES

[1] B. Murari, F. Bertotti, G. Vignola, *Smart Power ICs 2nd Edition*, pp. 218-220, Springer-Verlag, Berlin, 2002.

[2] M. Schenkel, *Substrate Current Effects in Smart Power ICs*, Hartung-Gorre-Verlag, 2003, ISBN 3-89649-848-7.

[3] Ronald R.Troutman, *Latchup in CMOS Technology The problem and its Cure,* Kluwer Academic Publishers second Printing, 1995.

[4] R. J. Widlar, *Controlling substrate currents in junction-isolated ICs*, IEEE J. Solid-State Circuits, vol. 26, pp. 1090–1097, Aug. 1991.

[5] Lo Conte, F.; Sallese, J.-M.; Pastre, M.; Krummenacher, F.; Kayal, M.; "Global Modeling Strategy of Parasitic Coupled Currents Induced by Minority-Carrier Propagation in Semiconductor Substrates," *Electron Devices, IEEE Transactions on*, vol.57, no.1, pp.263-272, Jan. 2010.

[6] Lo Conte, F.; Sallese, J.-M.; Pastre, M.; Krummenacher, F.; Kayal, M.; "Global 2D modeling of minority and majority substrate coupled currents," *Solid State Device Research Conference, 2009. ESSDERC '09. Proceedings of the European*, vol., no., pp.153-156, 14-18 Sept. 2009.

[7] Ikeda et al., "MOS/Bipolar device with stepped buried layer under active regions (Patent style)," U.S. Patent 4 799 098, January 17, 1989.

[8] G. Masetti, M. Severi, and S. Solmi, "*Modeling of Carrier Mobility Against Carrier Concentration in Arsenic-, Phosphorus- and Boron-Doped Silicon*" IEEE Trans. Electron Devices, vol. ED-30, no. 7, pp. 764-769, 1983.