

Subthreshold Current-Mode $\Delta\Sigma$ Quantizer with 3-Decade Scalable Sampling Rate and pA Resolution for Bio-Medical Applications

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Abstract—A current-mode $\Delta\Sigma$ analog-to-digital data converter (ADC) for biomedical readout front-end systems is being presented. The core of this circuit is a current-controlled ring oscillator (CCO) whose oscillation frequency is proportional to the input current signal. To shape the quantization noise and improve the resolution, the CCO has been used as an integrator in $\Delta\Sigma$ configuration. Experimental results show that the proposed ADC can reach to 54 dB signal-to-noise ratio while the sampling frequency is 45.5 kHz and consuming 800 nW power (with an oversampling ratio of 64). The sampling frequency of this ADC can be adjusted from 700 Hz to 540 kHz with a scalable power dissipation, corresponding to 17.5 pW/Hz sampling frequency.

I. INTRODUCTION

Current-mode analog-to-digital data converters (ADCs) are critical components in biomedical and other similar sensory systems [1]. The main goal in this work is to convert the detected input current directly to digital signal just after the sensor. In this way, it is possible to simplify the overall system, reduce the sensitivity to noise, and do the further analysis on data in digital domain. This requires high-precision and low-power current-mode data converters, which are able to detect signals in the range of few tens of pico-Amperes.

The core of the topology that is being proposed in this work is a current-controlled oscillator (CCO) in which the output oscillation frequency is proportional to the input current. Hence, the output frequency is representative of the input detected current, without implementing a transimpedance amplifier (TIA) that is generally used in such systems. Since the digital levels are very low, however, it is essential to have a high resolution quantizer. To convert the oscillation frequency to digital data with a high precision, the ring oscillator has been used in a $\Delta\Sigma$ configuration in order to shape the quantization noise [2].

The other important issue is the system energy consumption. To reduce the power dissipation and make it suitable for ultra-low power applications, the circuit needs to operate in subthreshold regime. However, operating in subthreshold regime imposes many limitations on circuit performance, and some effects such as oscillator jitter, or device mismatch become very important. Therefore, a very careful system level analysis is required to study the performance of the system in presence of different sources of nonideality. The rest of this

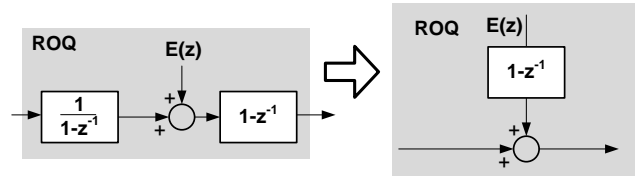


Fig. 1. Behavioral model for a ring oscillator based quantizer.

article concentrates on two important issues: system analysis and circuit implementation.

II. RING OSCILLATOR BASED $\Delta\Sigma$ QUANTIZER

Ring oscillator based $\Delta\Sigma$ ($R\Delta\Sigma$) modulators have recently become very attractive for implementing high-speed and high-resolution analog-to-digital converters [2]-[4]. In this structure, the ring oscillator acts as the loop integrator and quantizer, simultaneously. Ring oscillator quantizer behaves as a multi-bit quantizer that can improve the system resolution. Also, this type of quantizer benefits from an inherent dynamic element matching (DEM) property that results in a more linear specification [3]. These properties make this topology very suitable for different applications. In this work, we are employing this topology for high-resolution and ultra-low power applications.

Figure 1 shows the behavioral model for a ring oscillator based quantizer (ROQ). As illustrated in this figure, the ring oscillator acts as an integrator in phase domain. To measure the input signal, the oscillation frequency is compared to a reference clock frequency. This could be done using a counter [2], or a differentiator as explained in [4]. In this step, quantization noise, $E(z)$, appears due to the comparison process. The quantization noise generated in each comparison step will be considered in the next conversion step, and hence the circuit acts as a first order $\Delta\Sigma$ modulator [2]. Any source of error such as: reference clock jitter, ring oscillator jitter, and also delay mismatch among different delay elements inside the ring oscillator can corrupt the quantization noise, and hence reduce the resolution of the quantizer. In the next Section, the behavior of the quantizer in presence of these nonideality effects will be studied.

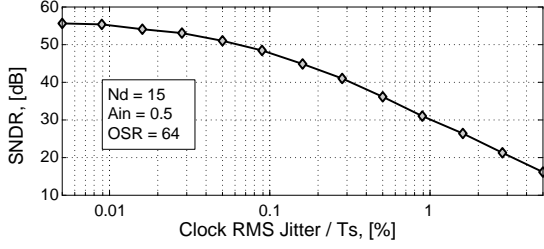


Fig. 2. The effect of sampling clock jitter on SNDR based on behavioral modeling for a first order $R\Delta\Sigma$ modulator (or equivalently ROQ).

III. ANALYSIS

In this Section, the main nonideality effects in a $R\Sigma\Delta$ modulator will be very briefly studied.

A. Sampling Clock Jitter

Sampling clock jitter is one of the main sources of error in $R\Sigma\Delta$ modulators. Sampling clock period (T_s) acts as the voltage reference in conventional ADCs [5]. Therefore, any variation on T_s will affect the output linearity. In a real case where sampling clock contains jitter, clock period can be indicated by a random number with average value of \bar{T}_s and variance of σ_{T_s} . Therefore, $T_s = \bar{T}_s + \Delta T_s$, where average value of ΔT_s is zero and its variance is σ_{T_s} .

Fig. 2 shows the effect of clock jitter on circuit dynamic range. In this figure, the RMS value of the jitter is normalized to the clock period. As the sampling clock frequency in this design is very low, the effect of sampling clock jitter can be neglected.

B. Oscillator Jitter

The jitter on edges of the ring oscillator changes its instantaneous oscillation frequency. This jitter changes the nominal delay of a delay cell to:

$$t_{d(i)} = \bar{t}_d + \Delta t_{d(i)} + \partial t_{d(i)} \quad (1)$$

where $\Delta t_{d(i)}$ represents the delay mismatch component among different delay elements, and timing uncertainty has been stated by $\partial t_{d(i)}$ which has a average value of zero and variance of σ_{t_d} . Assuming that there are N complete transitions during one T_s , the timing jitter will be accumulated over N transition, and hence the last transition inside the time interval of T_s will be displaced. This displacement (d) depends on the value of $\partial t_{d(i)}$ and the number of transitions, N . Assuming normal distribution for ring oscillator jitter [6], the variance of d is:

$$\sigma_d \approx \partial t_{d(i)} \cdot \sqrt{N}. \quad (2)$$

and worst case happens when $N = N_d$ (N_d is the number of delay stages in the ring oscillator). Meanwhile, as the number of delay elements increases, the oscillator jitter effect becomes more pronounced. Although the oscillation frequency in this design is very low, however since the relative jitter amplitude is considerable especially in subthreshold operating regime, this effect should be very carefully considered in the design.

C. Delay Mismatch

In an ideal case, all the elements inside the ring oscillator exhibit the same amount of delay. Therefore, the reference sampling clock is counted by equally spaced pulses. In a real implementation, there is always some mismatch among the circuit elements, and hence among the delay values which makes the time to digital converter nonlinear. This nonlinearity can directly affect the dynamic range (DR) at the output of quantizer.

The effect of delay mismatch in $R\Sigma\Delta$ modulators is partially similar to the effect of resistor mismatch in a resistor string based analog-to-digital converter. In this type of converters, the resistor mismatch can cause nonlinearity at the output of ADC [5]. The difference in $R\Sigma\Delta$, however, is that the delay elements are continuously changing their placement in the queue. This effect is due to this fact that the delay element that does the first transition in each conversion step depends on the oscillator phase in the previous step. The continuous change of the starting point in delay line can provide a first order averaging over the nonlinearity of the quantizer (or DEM).

Fig. 3 illustrates a simple ring oscillator based quantizer. The input signal is in current domain and if necessary, a capacitance can be used to remove the DC component of the signal as it is required in many bio-electronic interface systems. In this design, subthreshold source-coupled logic (STSCCL) circuit topology [7] has been used to implement the delay elements which is very convenient for implementing ultra-low power circuits. Using this circuit configuration, the delay of each element in a ring oscillator can be represented by random numbers of $t_{d(i)}$, $i = 1, \dots, N_d$ with an average value of:

$$\bar{t}_d = \ln 2 \times V_{SW} C_L / I_{SS} \quad (3)$$

and variance of σ_{t_d} . Also, in a ring oscillator, the sum of the delay values should be equal to $T_{osc}/2$, or:

$$\sum_{i=1}^{N_d} t_{d(i)} = 1/(2f_{osc}) = N_d \bar{t}_d. \quad (4)$$

In other words, assuming $t_{d(i)} = \bar{t}_d + \Delta t_{d(i)}$, then: $\sum_{i=1}^{N_d} \Delta t_{d(i)} = 0$.

D. Performance Analysis

In a ROQ, in each conversion step, the reference clock period is divided to an integer number of $N[n]$ and a residue $q[n] < 1$ by the ring oscillator. Indeed, the reference clock period is divided by the first N transitions of ring oscillator and there will be a residue time smaller than the delay of stage $N + 1$. Hence:

$$T_s[n] = \sum_{i=1}^N t_{d(i)}[n] + q[n] \times t_{d(N+1)}. \quad (5)$$

Replacing the different sources of nonideality in (5) results in:

$$\bar{T}_s[n] = N \cdot \bar{t}_d[n] + R_t[n] \quad (6)$$

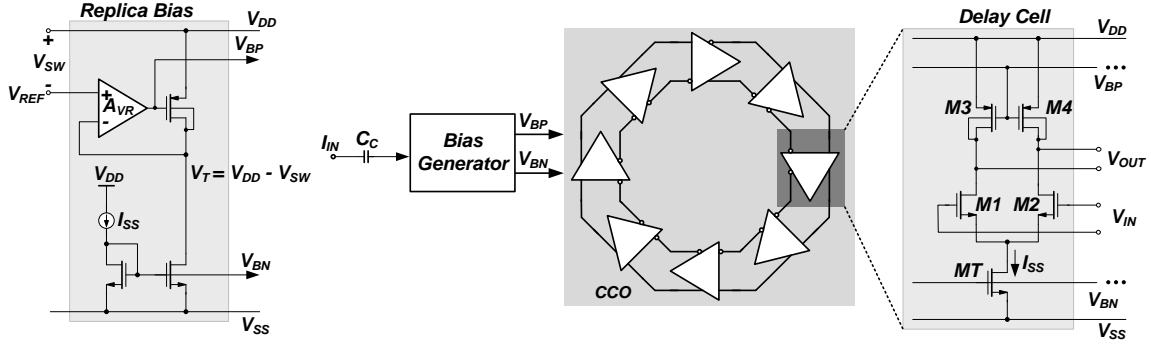


Fig. 3. Proposed ring oscillator based quantizer uses subthreshold source-coupled logic (STSCL) circuit as delay element. Replica bias (RB) circuit is used to generate the appropriate bias voltages for NMOS tail bias and PMOS load devices [7].

where R_t represents the residual time or quantization error in time domain and can be calculated by:

$$R_t[n] = \sum_{i=1}^N \Delta t_{d(i)} + \sum_{i=1}^N \partial t_{d(i)} + q[n] \cdot t_{d(N+1)} - \Delta T_s \approx Q[n] \cdot \bar{t}_d[n]. \quad (7)$$

It can be seen that the total quantization noise Q depends on the input signal level through N . The first term in right hand of (7) is zero when $N = N_d$ which happens when the input signal is close to its maximum value. In this special case, the effect of delay mismatch is negligible. However, as the number of transitions decreases by reducing the input signal level, the mismatch effect will become more pronounced. The second term in (7), as represented in (2), is proportional to the time interval that the jitter will be accumulated which has an RMS value of $\partial t_d \sqrt{N}$. Therefore, this effect is more pronounced when N is larger or equivalently, input signal has larger values.

Regarding (7), in presence of non-ideality effects, the quantization noise power will be increased by this factor:

$$\alpha[N] = 1 + \left(\sum_{i=1}^{(N+1)} \frac{\Delta t_d}{\bar{t}_d} + \sum_{i=1}^N \frac{\partial t_d}{\bar{t}_d} - \frac{\Delta T_s}{\bar{t}_d} \right) \quad (8)$$

IV. CIRCUIT IMPLEMENTATION

In this Section, design of a current-mode ROQ based on system requirements extracted in Section III, will be discussed. As will be seen, the current-mode topology provides the possibility to achieve a very wide sampling frequency range with a scalable power consumption and 8-bit target resolution.

The ring oscillator is the most important component in a $R\Sigma\Delta$ topology. As explained in Section III, oscillator jitter and delay mismatch are the main design concerns that can affect the modulator performance. In the following, the design of ring oscillator with acceptable level of jitter and delay mismatch will be addressed.

1) *Delay Matching*: The maximum acceptable mismatch on gate delay puts a lower limit on area of devices inside the delay element. Using (3), the delay mismatch of STSCL elements can be calculated by:

$$\left(\frac{\Delta t_d}{\bar{t}_d} \right)^2 \approx \left(\frac{\Delta V_{SW}}{V_{SW}} \right)^2 + \left(\frac{\Delta I_{SS}}{I_{SS}} \right)^2 + \left(\frac{\Delta C_L}{C_L} \right)^2. \quad (9)$$

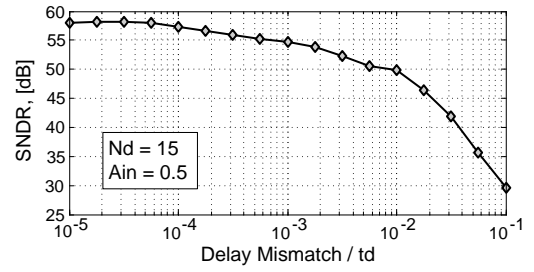


Fig. 4. Effect of delay mismatch on first order quantizer based on behavioral modeling.

Variation on V_{SW} depends on matching of PMOS load devices in delay elements (M3, M4, and MPR in Fig. 3). It also depends on matching between the tail bias current of the delay elements (I_{SS}). The last term in (9) depends on the total capacitive load at the output of each delay element. This capacitance comes partially from interconnect parasitic capacitance, and partially from parasitic capacitance of NMOS and PMOS transistors. Therefore, a fully symmetric layout in addition to large MOS devices are required to guarantee having a good matching on load capacitance. Thus, it is possible to relate the delay mismatch with the size of circuit components. Fig. 4 shows the effect of delay mismatch on circuit SNDR.

2) *Oscillator Jitter*: As shown in [6], the standard deviation of jitter in an oscillator after ΔT seconds is

$$\sigma_j = \kappa \sqrt{\Delta T} \quad (10)$$

where κ is a proportionality constant determined by the circuit parameters. It is shown that [8]:

$$\kappa \geq \sqrt{\frac{8}{3\eta}} \cdot \sqrt{N_d \cdot \frac{kT}{P} \cdot \left(\frac{V_{DD}}{V_{char}} + \frac{V_{DD}}{R_L I_{SS}} \right)} \quad (11)$$

where k is Boltzmann's constant, T is the junction temperature, N_d is the number of delay elements, P is the total oscillator power consumption, and $\eta \approx t_d/t_r$ is a function of rise time and delay in each delay element. Meanwhile, V_{char} is the characteristic voltage of the device [8]. Assuming that

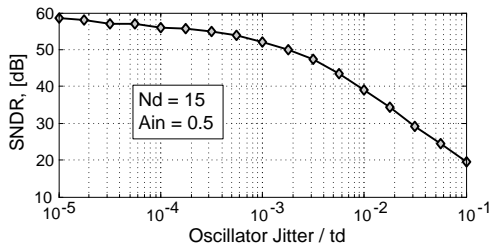


Fig. 5. Effect of oscillator jitter on first order quantizer SNDR based on behavioral modeling.

$V_{char} \approx 4U_T$ for subthreshold devices, and $V_{SW} \approx 8U_T$, then:

$$\kappa > \sqrt{q/(\eta I_{SS})} \quad (12)$$

where q is the unit electron charge in Coulomb. It can be seen that the only way to reduce the jitter is to increase the tail bias current of the ring oscillator. To have a RMS jitter value not more than $\sigma_{j,Max}$, tail bias current of each delay cell should be larger than:

$$I_{SS} > \sqrt{2 \ln 2 q V_{SW} C_L N_d \eta t_d} / \sigma_{j,Max} \quad (13)$$

In $R\Delta\Sigma$ topology, in each conversion step, the first transition occurs after t_d seconds with jitter variation of $\kappa \cdot \sqrt{t_d}$. The following transitions occur at $i \times t_d, i = 2, \dots, N$ with standard variation of $\kappa \cdot \sqrt{i \cdot t_d}$. Therefore, the maximum jitter value will happen when $N = N_d$ which is equal to

$$\sigma_{j,Max} \leq \kappa \sqrt{T_s} \quad (14)$$

V. EXPERIMENTAL RESULTS

Fig. 6(a) shows the photomicrograph of the test chip fabricated in CMOS 90 nm technology. To be able to perform the measurements at very low currents levels (100 pA to 100 nA), a linear and programmable current divider has been used in front of the circuit. An external sinusoidal current source with maximum amplitude of $1 \mu A$ is applied to the programmable current divider circuit and output current can be programmed using two external digital signals.

As it is illustrated in Fig. 6(b), SNDR of the ring oscillator quantizer remains relatively constant over sampling frequencies ranging from 700 Hz (100 pA full scale current) to 540 kHz (100 nA full scale current). The measured dynamic range is less than the expected value mainly due to the flicker noise of the current divider front end circuit.

The test chip also includes an array of oscillators to study the delay mismatch. Experimental data shows that the delay mismatch is well below 1% for the designed oscillators which means the size of delay cells and also logic cells can be reduced slightly.

To be able to operate in such low bias current levels with scalable power dissipation, STSCL topology has been used for implementing both the delay elements and also the logic circuit. Since in this type of circuits, the power dissipation is linearly proportional to the operating frequency, as shown in

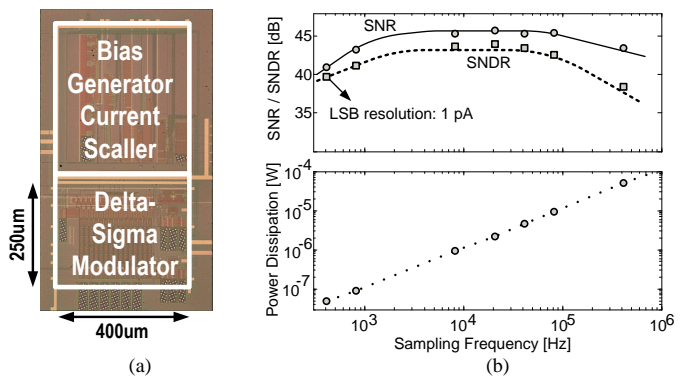


Fig. 6. (a) Chip photomicrograph fabricated in a conventional 90 nm CMOS technology. (b) SNDR and power dissipation versus sampling frequency based on experimental results.

Fig. 6(b), the power dissipation of the entire quantizer circuit is also linearly proportional to the sampling frequency.

These experimental results have been achieved for an open-loop first-order $\Delta\Sigma$ modulator. Using ROCs in higher order $\Delta\Sigma$ loops will result in much higher dynamic range values.

VI. CONCLUSIONS

Design and analysis of a current-mode ring oscillator based quantizer has been presented. The sensitivity of this type of circuits to different sources of nonideality, especially to the sampling clock jitter, oscillator jitter, and mismatch has been analyzed and explored based on behavioral modeling. To demonstrate the performance of ring oscillator based quantizers, an analog-to-digital converter has been implemented in conventional CMOS 90 nm technology. Experimental results show that this circuit can be used over a wide sampling frequencies (700 Hz to 540 kHz) with pico-Ampere range resolution and 12.5 nW minimum power consumption.

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