DESIGN AND FABRICATION OF SUSPENDED-GATE MOSFETS FOR MEMS RESONATOR, SWITCH AND MEMORY APPLICATIONS

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Abstract

Wireless communication systems and handset devices are showing a rapid growth in consumer and military applications. Applications using wireless communication standards such as personal connectivity devices (Bluetooth), mobile systems (GSM, UMTS, WCDMA) and wireless sensor network are the opportunities and challenges for the semi-conductor industry. The trend towards size and weight reduction, low power consumption and increased functionalities induces major technological issues. Today, the wireless circuit size is limited by the use of lots of external or "off-chip" components. Among them, quartz crystal, used as the time reference in any wireless systems, is the bottleneck of the miniaturization. Microelectromechanical systems (MEMS) is an emerging technology which has the capability of replacing the quartz. Based on similar technology than the Integrated Circuit (IC), MEMS are referred as electrostatically, thermally or piezoelectrically actuated mechanical structures.

In this thesis, a new MEMS device based on the hybridization of a mechanical vibrating structure and a solid-sate MOS transistor has been developed. The Resonant Suspended-Gate MOSFET (RSG-MOSFET) device combines both advantages of a high mechanical quality factor and the transistor intrinsic gain. The physical mechanisms behind the actuation and the behavior of this device were deeply investigated and a quasi-static model was developed and validated, based on measured characteristics. Furthermore, the dynamic model of the RSG-MOSFET was created, taking into account the non-linear mechanical vibrations of the gate and the EKV model, used for MOSFET modeling.

Two fabrication processes were successfully developed to demonstrate the proof of concept of such a device and to optimize the performances respectively. Aluminum-silicon (Al-Si1%) and pure silicon-based RSG-MOSFETs were successfully fabricated. DC and AC characterizations on both devices enabled to understand, extract and evaluate the mechanical and MOSFET effects. A specifically developed RF characterization methodology was used to measure the linear and non-linear behaviors of the resonator and to evaluate the influence of each polarization voltages on the signal response. RSG-MOSFET with resonant frequencies ranging from 5MHz to 90MHz and quality factor up to 1200 were measured.
Since MEMS resonator quality factor is strongly degraded by air damping, a 0-level thin film vacuum packaging (10^{-7} mBar) process was developed, compatible with both AlSi-based and silicon-based RSG-MOSFET. The technology has the unique advantage of being done on already released structure and the room temperature process makes it suitable for above-IC integration.
In parallel, a front-end compatible process was defined and major build blocks were developed in industrial environment at STMicroelectronics. This technology is based on the

Silicon-On-Nothing technology, originally developed for advanced transistor, and therefore making the MEMS resonator process compatible with CMOS co-integration.

DC characterizations of SG-MOSFET had shown interesting performances of this device for current switch and memory applications. Mechanical contact of the gate with the MOSFET channel induces a current switching slope greater than 0.8mV/decade, much better than the theoretical MOSFET limit of 60mV/decade. Maximum switch isolations of -37dB at 2 GHz and -27dB at 10GHz were measured on these devices.
A novel MEMS-memory has been demonstrated, based on the direct charge injection to the storage media by the mechanical contact of the metal gate. Charge injection and retention mechanisms were investigated based on measured devices. Cycling study of up to 10^5 cycles were performed without noticing major degradations of the electrical behavior neither mechanical fatigue of the suspended gate. The measured retention time places this memory in between the DRAM and the FLASH memories. A scaling study has shown integration and compatibilities capabilities with existing CMOS.

Keywords:
Suspended-Gate MOSFET, MEMS resonator, MOSFET detection, dynamic mechanical modeling, surface micromachining process, vacuum packaging, front-end process, MEMS switch, MEMS memory, Verilog-A code, MEMS-based oscillator.

Version abrégée

Depuis les années 1990, les systèmes de communication et les appareils sans fil connaissent une croissance fulgurante dans les applications grand public et militaires.
Les différentes applications utilisant les standards de communications sans fil destinées à la communication personnelle (Bluetooth), aux réseaux de communication mobile (GSM, UMTS, WCDMA) et aux réseaux locaux (WLAN) présentent des opportunités de développement et des challenges importants pour l'industrie des semi-conducteurs.
La tendance actuelle de réduction de taille et de poids des appareils sans fil, ainsi que la diminution de leur consommation d'énergie et l'augmentation du nombre de fonctionnalités posent des problèmes majeurs au niveau technologique. La taille des circuits de communication est aujourd'hui limitée par l'utilisation d'un certain nombre de composants « off-chip » ou externes. Parmi ceux-ci : le quartz. Cet élément central de toute la chaîne de réception et transmission du signal ne peut être intégré sur une puce en silicium.
Mais les technologies microsystèmes émergentes ou "Microelectromechanical Systems (MEMS)" ont récemment démontré la faisabilité d'une intégration monolithique d'un composant ayant des performances similaires à celles du quartz, par l'utilisation de technologies issues de la micro-électronique.

Ce mémoire présente ainsi le développement et la réalisation d'un tel élément: un nouveau composant MEMS, basé sur l'hybridation d'une structure mécanique et d'un transistor MOS, et destiné à être utilisé comme base de temps. Le transistor à grille résonante suspendue (RSG-MOSFET) ainsi développé combine à la fois les performances mécaniques en termes de facteur de qualité et le gain intrinsèque du transistor. Les mécanismes physiques de l'actionnement de cette structure ainsi que son comportement ont été approfondis, et un modèle quasi-statique du composant à été développé et validé sur des caractéristiques de mesures. De plus, un modèle dynamique du RSG-MOSFET, basé sur les vibrations non-linéaires de la structure mécanique et sur le modèle de transistor EKV créé à l'EPFL, a été développé dans un langage compatible avec un design de circuit.

Afin de valider ce concept d'hybridation et d'en optimiser les performances mécaniques et électriques, deux procédés de fabrication ont été successivement développés. Des transistors à grille suspendue en alliage d'aluminium et de silicium (Al-Si1%), et en silicium pur, ont été fabriqués. Des caractérisations DC et AC sur ces dispositifs ont permis d'extraire, d'évaluer et de dissocier les différents effets purement mécaniques des effets provenant du semi-conducteur. Une méthodologie de caractérisation à été développée dans ce sens et à permis de mettre en avant les effets non-linéaires sur ces dispositifs résonants ainsi que l'influence des paramètres de polarisation sur la réponse du résonateur. Des RSG-MOSFET ayant des

fréquences de résonance comprises entre 5MHz et 90MHz ont été mesurées avec des facteurs de qualité atteignant 1200.
Étant sensibles à l'amortissement dans l'air, les résonateurs électromécaniques doivent fonctionner sous vide pour atteindre des facteurs de qualité élevés. Un procédé de fabrication en film mince permettant d'encapsuler sous vide (à 10^{-7} mBar) une structure libérée a été développé et réalisé sur un RSG-MOSFET, doté d'une grille en AlSi. Cette technologie utilise un procédé à température ambiante, permettant ainsi une intégration « above-IC », ou sur le circuit intégré, sans en endommager les performances.
En parallèle, un autre développement technologique permettant l'intégration « front-end », ou en début de chaîne, à été défini. Les principaux blocs technologiques ont été développés à cet effet dans un environnement industriel, chez STMicroelectronics. Ce procédé est basé sur l'utilisation de la technologie SON (Silicon-On-Nothing), initialement développé pour les générations de transistors avancées, permettant ainsi d'effectuer une intégration monolithique entre le MEMS et le circuit.

Par ailleurs, des caractérisations DC sur des SG-MOSFET ayant de faibles constantes de rigidité ont permis de démontrer des performances intéressantes de ce composant pour des applications de commutateur de courant DC et de mémoires MEMS. Le contact mécanique entre la grille suspendue et le canal du semi-conducteur permet d'obtenir des pentes de commutation supérieures à 0.8mV/décade, surpassant la valeur limite théorique de la pente sous-seuil de 60mV/décade d'un transistor MOS. Des isolations de -37dB à 2 GHz et de -27dB à 10GHz ont été mesurées sur ces dispositifs.
Une nouvelle mémoire MEMS à été démontrée, basée sur l'injection directe de charges par le contact mécanique entre la grille et le diélectrique de stockage. Les mécanismes d'injection et de rétention de charges ont été étudiés sur la base de mesures. Une étude de cyclage sur 10^5 cycles a permis de montrer une bonne fiabilité mécanique et électrique des mémoires. La mesure du temps de rétention de la cellule mémoire la place entre la DRAM et la FLASH, et une étude approfondie sur la miniaturisation de cette cellule a permis de mettre en avant ses possibilités d'intégration et de compatibilité avec les technologies CMOS existantes.

Mots clefs:
Transistor à grille suspendue. SG-MOSFET, résonateur MEMS, détection MOSFET, modélisation mécanique dynamique, procédé de fabrication par micro-usinage de surface, encapsulation sous vide, procédé front-end, commutateur MEMS, mémoire MEMS, oscillateur MEMS, code Verilog-A, base de temps.

Introduction

For the past 30 years, Micro-Electro-Mechanical Systems (MEMS) have been developed in Universities and research laboratories, but their introduction into the consumer market started only recently. The strong development of the semiconductor industry during that period has enabled the miniaturization of electro-mechanical moving structures down to the micro-meter size[1]. MEMS devices are fabricated with the same technology as transistors and can offer additional functionalities such as mechanical sensors or/and actuators.

MEMS sensors are today found in the automotive market, for example in the form of accelerometers for shock detection in the control unit of the air-bag. MEMS-based pressure and gas sensors are also a mature market and some other volume applications are emerging as gyroscopes. In the medical field, MEMS bio-sensors are growing quickly due to increasing demands in miniaturized lab-on-a-chip components.
Further major applications of MEMS actuators are inkjet printers and micro projection display (DLP[2]).

The other MEMS application field is for actuators and among them volatile and non-volatile memories which are investigated due to their capability for high density and low power consumption. This emerging technology is planned to compete with advanced CMOS technologies (Complementary Oxide Semiconductor) for the non-volatile market but also offers alternatives for low power embedded memory. Recent market studies[3] shows that

[1] One micro-meter = 10^{-6} meter

[2] Digital Light Processor, from Texas Instruments. Array of MEMS micro-mirrors for projection display

[3] Prismark market review, 2006

communication systems field is likely to be the next key applications for the so-called Radio Frequency MEMS (RF MEMS). Nearly a billon of mobile phone handset are shipped every year, with size, cost and autonomy being the major criteria, there is strong competition in finding a technology that could fulfill these requirements. Actual mobile systems are using multiple components bonded on a Printed Circuit Board (PCB). To further miniaturize wireless systems, external components such as filters and time reference blocks must be integrated on-circuit or on-module. Ultimately, a single chip will handle signal reception and transmission. Such a vision is shown in Fig. 1.

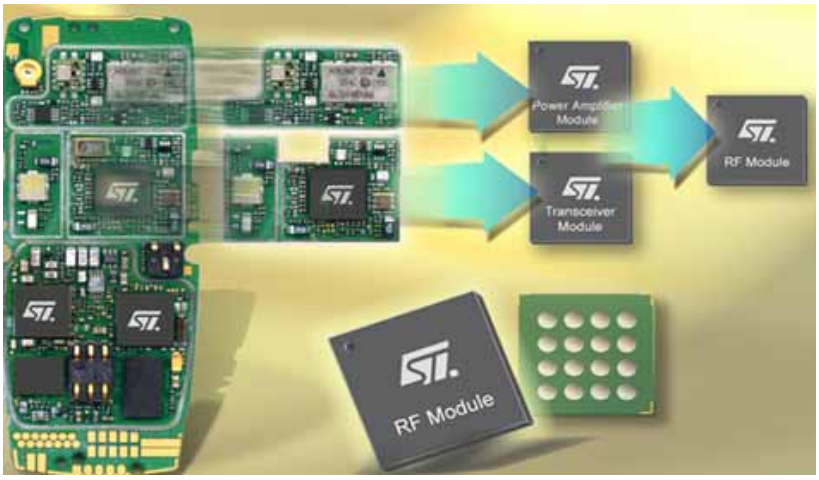


Fig. 1 Schematic of the trend towards single chip module

The use of a single transceiver chip generates free space on the circuit board, which could be used to integrate other modules in the cell phone. These new modules could be additionally dedicated to short range communications which enable direct interaction of the cell phone with the surrounding environment, also known as the concept of “ambient intelligence”. This concept is based on the fact that the user can access and interrogate different sensors around his environment though the cell phone interface. These sensors can provide general information such as humidity, pressure and temperature levels but can also be more users specific. An example application could be the monitoring of the elderly people, detecting the fall by using a MEMS accelerometer, sending the information to the cell phone which can react by calling the family or the doctor.

MOTIVATION AND SCOPE OF THE THESIS

The starting point of this thesis was to develop a MEMS resonator for time reference application. Then, considering actual limitation of these vibrating structures in terms of signal amplification, the RGT (Resonant Gate Transistor) architecture [2] using a suspended-gate vibrating over a FET channel was chosen. A device miniaturization improvement over this first structure was done by combining the actuation and the detection part in a single device. Based on this approach, a model for this complex resonator was developed. Fabrication processes were created to validate this conceptual architecture and to optimize performances.

This work has been done in the frame of the integrated MIMOSA European project “Microsystems Platform for Mobile Services and Applications” (IST-2002-507045).

Further investigations of the quasi-static operation enable to use this device as switch and memory.

ORGANISATION OF THIS THESIS

The first chapter of this dissertation discusses state-of-the art RF MEMS technologies and devices for communication systems application. In particular, MEMS resonators for time reference and filtering applications are analyzed. The expected figures of merits needed for such applications for each communication standard are given. This chapter introduces the resonator challenges for high frequency operation and mechanical displacement detection. Among these challenges, the limitation of the capacitive detection of high frequency mechanical displacement is compared to the use of the MOSFET detection. Compact resonant suspended-gate MOSFET (SG-MOSFET) architecture is proposed and is further developed in this thesis.

The modeling aspect of a resonant SG-MOSFET based on the combination of analytical mechanical and electrical equations is examined in Chapter II. A static model of a MOSFET having a mobile suspended-gate was developed. It is based on the mechanical force-stiffness relationship of an anchored-gate under electrostatic actuation, and on a continuous MOSFET expression from weak to strong inversion. Further dynamic model of the resonant SG-MOSFET is presented with a circuit design-compatible coding language (Verilog-A). This model includes the non-linear displacement of the vibrating gate and uses the EKV[4] model to accurately describe the MOSFET behavior in all operating regimes.

Novel SG-MOSFET fabrication processes for metal and silicon gate are described in Chapter III. To achieve high performances, the SG-MOSFET must be encapsulated in a vacuum packaging. A 0-level thin film packaging was developed and the dimensioning of the cavity for mechanical stability is presented. A front-end CMOS compatible process is presented, using the SON[5] technology, and critical fabrication blocks were validated.

Chapter IV presents the measurement results for the metal and silicon-based Resonant Suspended-gate MOSFET. The differences between capacitive and MOSFET detection on oscillator circuit design are investigated, showing a clear advantage of the RSG-MOSFET for circuit design.

The unique mechanical and electrical characteristics of the SG-MOSFET makes it suitable for switch applications, as presented in Chapter V, for which a 0.71mV/dec subthreshold swing is measured. A novel MEMS memory, based on the combination of mechanical and electrical hysteresis of the SG-MOSFET is also investigated. The charge injection and retention mechanisms of this memory are explored. An original memory addressing scheme based on a unique property of the device and the scalability issues is studied.

[4] Enz, Krummenacher, Vittoz. Charge-based analytical model for MOSFET transistors

[5] Silicon On Nothing. Technology based on selective epitaxy and etching of SiGe material for advanced MOSFET fabrication

Chapter I

MEMS for communication systems, state-of-the art and challenges

Communication systems and among them wireless systems are taking an increasing place in our environment. Semiconductor industries are the technology drivers in that field. From the first transistor in 1947, the advance of technology and tools has allowed a sufficient miniaturization to create complex circuit able to send and receive data remotely. Transmitters and receivers are based on circuit architecture using integrated transistors but also external components assembled on a printed circuit board. To further miniaturize the receiver/transmitter device, different technologies were developed to embed on-chip or on-module devices having the same performances as the external components. These new technologies are at present in the R&D phase and approach industrialization.

Electrostatic and thin film piezoelectric MEMS are two CMOS-compatible technologies, aimed at replacing quartz oscillators and ceramic filters for on-chip integration. The basic piezoelectric and electrostatic actuation principles are described in this chapter. These technologies are the best candidates for on-chip time reference applications in terms of specifications and challenges. The MEMS flexural and bulk vibration modes resonators, related to different resonator geometries are expressed. Characteristics, technology and performances of state-of-the-art electromechanical and piezoelectric resonators are presented and compared. Trends in resonator technology, material, geometry and integration can therefore be extracted. Specifications for filter, VCO and reference oscillator applications are presented.

Based on the analysis of state-of-the-art MEMS resonators, an original approach for the detection of the mechanical displacement is introduced, based on MOSFET detection as compared to classical capacitive detection. The interest for such detection is then evaluated.

I.A. MEMS-based wireless circuit architectures: why?

The trend for multi-band wireless device to connect any worldwide network pushes the circuit designers to develop innovative architecture including tunable components. Moreover, due to the reduction of size and power consumption, novel architecture such as sensor networks are currently under development [3]. This architecture is based upon the short range communication between sensor nodes and a base station which could be the cell phone to monitor various factors such as home thermal isolation or storage condition in a warehouse.

In order to integrate all of these components in a single wireless device, the transceiver circuit should therefore connect to high performance components to satisfy various operating frequencies and stringent requirements between each communication channel. Part of the today's solution comes from the use of high quality factor components that cannot be fabricated on-chip together with the CMOS technology. RF MEMS devices, such as high quality factor inductors [4] or variable capacitors [5], offer interesting alternative solutions to external components. RF MEMS switches were also developed for circuit re-configuration microwave circuit and phase shifter, for which they offer significant advantages in term of isolation and insertion loss over existing components. But the two major areas where RF MEMS can offer disruptive solutions are the time reference signal and the filtering applications.

I.A.1. Time reference components

"Historically, navigation has been a principal motivator to search for better clocks. Even in ancient times, one could measure latitude by observing the stars' positions. However, to determine longitude, the problem became one of timing. Since the earth makes one revolution in 24 hours, one can determine longitude from the time difference between local time (which was determined from the sun's position) and the time at the Greenwich meridian (which was determined by a clock)" [6, 7]: Longitude in degrees = (360 degrees/24 hours) x t in hours.

Time reference devices, also called reference oscillators, are today implemented in various applications and among them wireless communication systems and electronic watches are dominant markets. These two applications are using however different frequencies defined either by technological means or by standardization. Wireless systems, and specifically 2G (GSM) and 3G (UMTS) systems, are using multiple frequency bands to transmit and receive data, depending on the network and localization. Therefore complex circuits with multiple frequency references are required. In wireless products, the time reference is used to synchronize the mobile device with the base station from which the signal is propagating. Time reference components can either be used in high frequency wireless communications (from 900MHz to 2.4GHz, depending on the standard and application) or low frequency application like watches (32.768 kHz). More generally, time reference devices are also found in most consumer electronic products, including computers.

I.A.2. Quartz oscillator

The typical device used in clock reference is the quartz crystal. It is a piezoelectric material, characterized by the fact that applying a voltage on its opposite sides induces a mechanical displacement. The quartz is a mineral which is physically cut and packaged to insure reliability. Depending on the edge cut of the crystal, various natural resonant frequencies can be achieved. Quartz characteristic are a resonant frequency limited to 50-to-100MHz and a very high quality factor (Q greater than 100 000). Quality factor is a value that represents the ratio between the energy stored in the component and the energy lost when actuated at its resonant frequency per cycle of operation. Depending on the quartz cut, the frequency stability over temperature is in the range of 10ppm (part per million) to 50ppm for a XO (Crystal Oscillator) and can be reduced to 1ppm for a TCXO (Temperature Controlled Crystal Oscillator) and even down to 0.001ppm for an Oven Controlled XO. The quartz oscillator is today the most reliable time reference that could fit into mobile wireless devices but also one of the few components that is still not integrated in circuit.

An oscillator is based on a circuit loop, integrating a resonator and a sustaining amplifier. The frequency precision of oscillation depends on the quality factor of the resonator used as a sharp filter, and increase with a higher Q. In a quartz oscillator, the quartz plays the role of the high Q filter. An interesting rule of thumb is that multiplying the operating frequency of an oscillator by a factor n, using frequency multiplier circuit, divides by a factor n the quality factor at that frequency. An interesting way to compare quartz crystal and integrated resonators is therefore the F_{res}xQ factor, which will be calculated for every state-of-the-art resonator in Table I.

I.A.3. MEMS-based integrated oscillator

The next miniaturization step is the development of integrated time reference component into the circuit to replace the external quartz. Electrostatic and piezoelectric MEMS resonators were demonstrated to be suitable for on-chip integration [8, 9]. These integrations could be done in-IC (Integrated Circuit) [8] or above-IC [9]. Few demonstrations of MEMS-based oscillators were demonstrated based on these two technologies [10, 11], showing very interesting performances in terms of integration (320x320µm^2 for the electrostatic MEMS-based oscillator and 640x650µm^2 for the piezoelectric oscillator) and power consumption (480µW and 12.7mW respectively). The performances are however very disparate mainly due to the resonator type investigated on the next section.
For wireless communication systems, the goal is to develop a structure with a high resonant frequency combined with a high quality factor.

I.B. Resonator architectures

I.B.1. Piezoelectric resonators (Bulk Acoustic Wave - BAW)

Considering a piezoelectric layer embedded in two conductive electrodes: by application of an alternative voltage, acoustic waves propagate and reflect between the two electrodes, creating mechanical displacement in the plane perpendicular to the electrodes. Mechanical

displacement is maximal for a thickness of the material equal to half of the wavelength of the resonant frequency. In embedded applications, other piezoelectric materials than quartz have been studied. Materials that can be deposited in thin layers at temperature compatible with standard CMOS fabrication, as aluminum-nitride (AlN) were developed. Typical characteristics of resonators made of thin film piezoelectric layers are their high resonance frequency comprised between 500MHz and 10GHz with a quality factor up to 1500 [12]. The quality factor in that device is limited by the fact that acoustic waves not only propagate perpendicularly to the electrodes but also laterally, which limits the amount of energy given to the dominant mode. Waves are also not perfectly reflected by the electrodes and then are eventually transmitted to the substrate where this energy is lost. Two approaches have been developed to lower the energy loss in the substrate by isolating it from the resonator by either using an air-gap as in Film Bulk Acoustic Resonators (FBAR) [13] or by using a Bragg reflector as Solidly Mounted Resonators (SMR) [14] to maximize the reflected energy (Fig. 2).

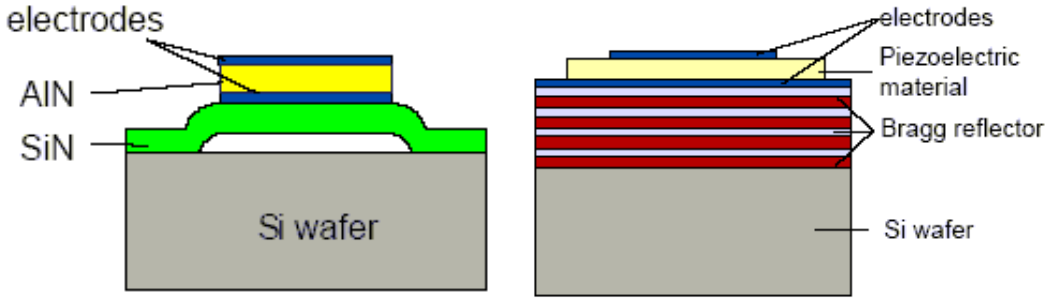


Fig. 2 Cross section of thin films FBAR and BAW SMR resonators

I.B.2. Electrostatic resonators

Another interesting way to build resonators is to reduce the size of a macro vibrating mechanical structure to integrate it on the same silicon substrate as the CMOS circuit. Electrostatic MEMS resonator behavior is similar to tuning fork that resonates at its resonant frequency under an excitation. The natural pulsation frequency of MEMS resonator is function of its mass and stiffness as $\omega = 2\pi f = \sqrt{k/m}$. It increases when dimensions are scaled down, and a frequency up to 1.5GHz [15] has been demonstrated. A key advantage of MEMS resonators is that the resonant frequency of the structure is photolithographically defined, therefore allowing multiple frequencies on the same chip.

Electrostatic actuation comes from the force created between two movable conductive plates facing each other and polarized with different voltages, producing an attractive force. In the case of an electrostatic MEMS resonator, the actuation electrode is fixed and only the suspended conductive structure is moving. The force between the two conductors as function of the energy stored in two capacitors can be written as

$$F_{elec} = \frac{1}{2}\Delta(CV^2) = \frac{1}{2}\frac{\varepsilon_0 S V^2}{(d_0 - y)^2} \quad (1)$$

Where d_0 is the initial gap between the two plates, S is the area faced by the two conductive parts, and y the vertical displacement of the structure under actuation. The mobile structure is actuated at its resonance frequency by applying an AC voltage. The force between the two plates is defined by the sum of a DC and the AC voltage. Equation 1 can then be rewritten as:

$$F_{elec} = \frac{1}{2}\frac{\varepsilon_0 S}{(d_0 - x)^2}(V_{dc}^2 + 2V_{dc}V_{ac}\sin\omega t + V_{ac}^2\sin^2\omega t) \quad (2)$$

This equation highlights the fact that the DC and AC signal creates a resonance at the natural frequency of the resonator but also at twice its frequency.

I.B.2.a. Flexural mode architectures

Flexural mode mechanical resonators can be single or double clamped beam, resonating in-plane or out-of-plane at their intrinsic resonant frequency, which depends on the beam material and dimensions. This vibration mode is typically used for low-to-medium frequency applications (typically from 10kHz to 100MHz), as high frequency can only be achieved by scaling down the beam in order to increase the rigidity, which has a negative impact on the power handling capability of the resonator. An example of a two ports lateral Clamped-Clamped beam (CC-beam) resonator is presented in Fig. 3, where the beam is excited under an electrostatic potential created between the electrode and the polarized resonator.

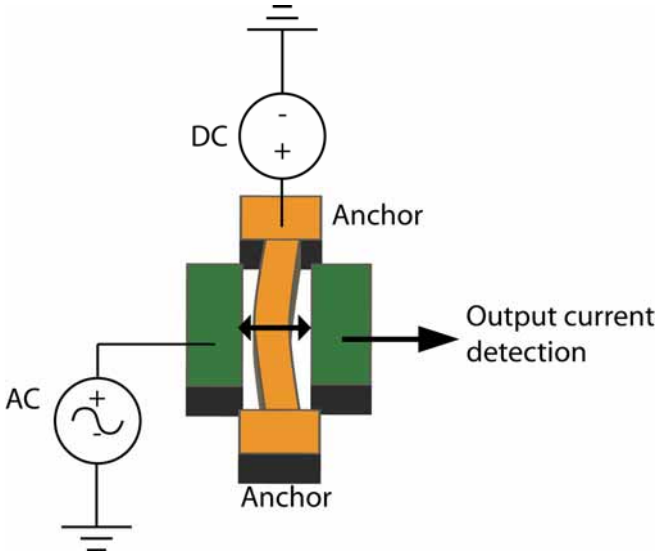


Fig. 3 Schematic of a lateral flexural Clamped-Clamped beam resonator

For CC-beam resonator geometry with a fixed beam thickness, the range of achievable resonant frequency by varying the beam length and width is shown in Fig. 4. Flexural vibration mode is characterized by a relatively large beam displacement (up to 1/3 of the gap) at the resonant frequency compared to the bulk mode resonators.

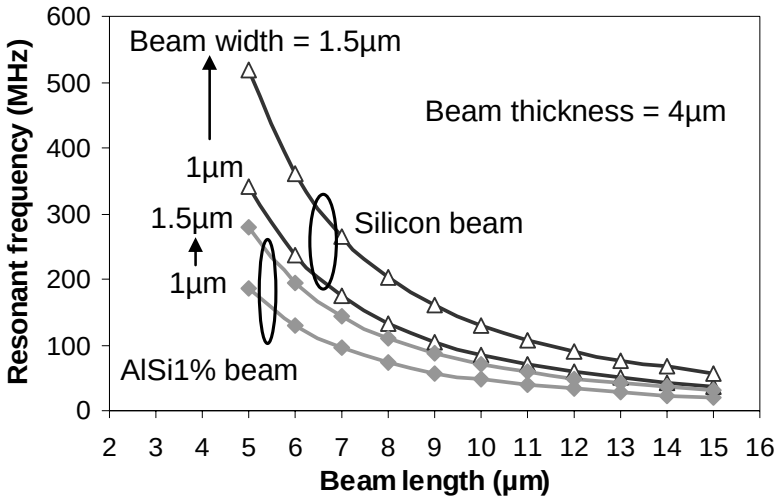


Fig. 4 Resonant frequency versus the length of a AlSi and Si-based Clamped-Clamped beam resonator

I.B.2.b. Bulk or Lamé mode

The bulk vibration mode uses the wave propagation inside the resonator to make it resonate. The advantage of this structure is the high resonant frequency achievable, up to the gigahertz range [16], while keeping a sufficiently large mass in order to store a maximum of energy, and therefore exhibiting a high quality factor. The bulk vibration mode induces however lower displacement than the flexural mode which makes difficult the detection of displacement at high frequency. An example of a disk bulk mode actuation is presented in Fig. 5, where the disk is anchored on two vibration nodes, characterized by the fact that the displacement tends to be negligible at these nodes. The resonator is actuated under the electrostatic field created by two opposite electrodes subjected to the same AC potential, while the conductive resonator is polarized by a DC voltage. The Lamé mode obtained with this excitation is characterized by the conservation of the resonator volume, and therefore presents minimal thermo-elastic dissipation.

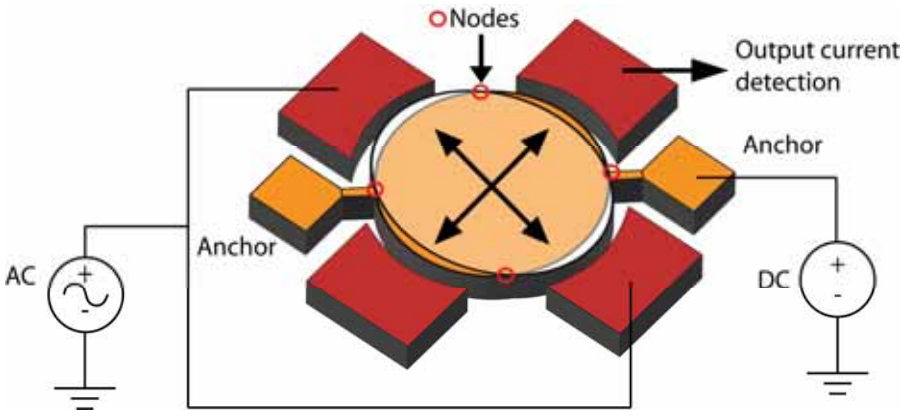


Fig. 5 Schematic of a Bulk Lamé mode disk resonator

The disk vibration of Fig. 5 is characterized by the fact that opposite actuation contracts both side of the resonator while the two other sides are expanding simultaneously. According to

that geometry and for a fixed disk thickness, the range of achievable resonant frequency by varying the disk radius and the resonator material is shown in Fig. 6.

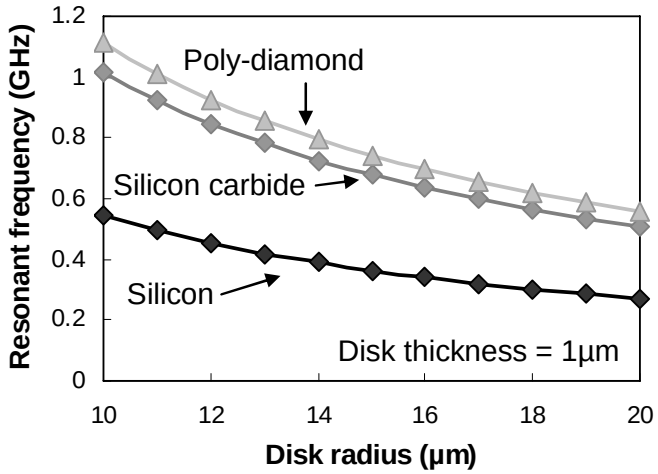


Fig. 6 Resonant frequency of a disk resonator for different radius and different materials: Si, SiC and poly-diamond [17]

I.B.2.c. Coupled resonator architecture

MEMS resonators are characterized by a high quality factor compared to LC tank (Inductance - Capacitance) resonators and BAW resonators. This associated signal transmission is therefore characterized by a narrow band around the resonant frequency, which is interesting to minimize the insertion loss for filtering application. However, compared to the requirements for communication standards, single electromechanical resonators used as filter exhibit a too narrow bandwidth, restricting them for this application. Therefore specific architectures have been developed in order to increase the transmission bandwidth. For this purpose, coupling flexural beams architecture [18] and coupling bulk-mode disk architecture [19] have been demonstrated. The bandwidth of coupled beam resonator is increased by a factor of 40 compared to a single resonator [20]. Wideband filtering is obtained by coupling two identical resonators with a beam. The coupling beam, placed at vibrating nodes, acts as an added stiffness of the second resonator. The resonant peak of the second resonator is therefore shifted to a higher value and the total bandwidth is the sum of each resonator response, as shown in Fig. 7.

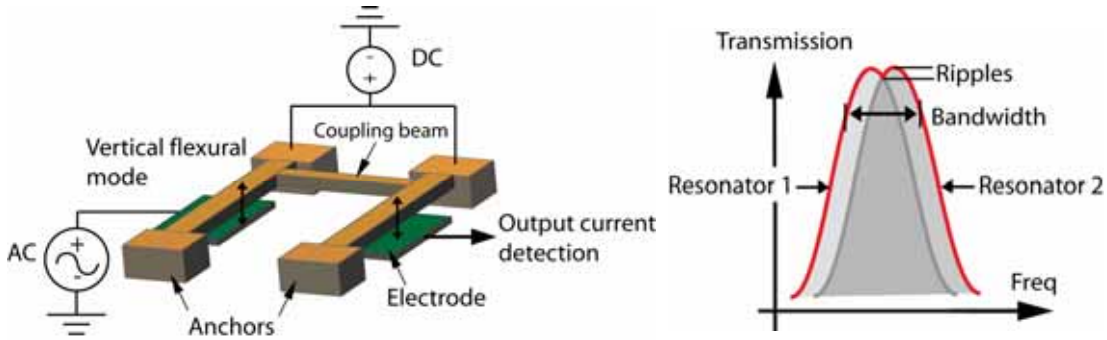


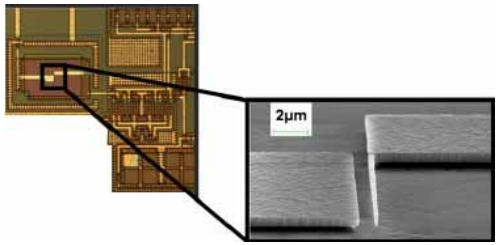
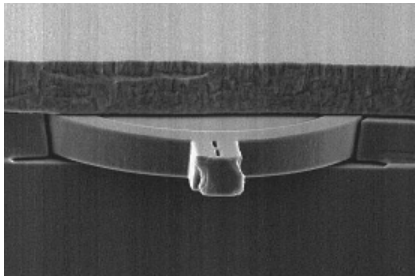
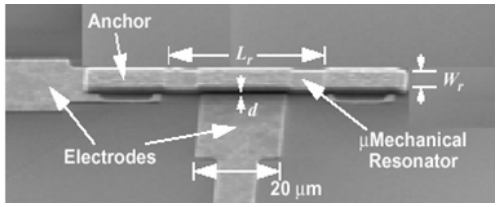
Fig. 7 Coupling beam geometry to increase the bandwidth at the resonant frequency of two vertical flexural mode resonators with similar dimensions

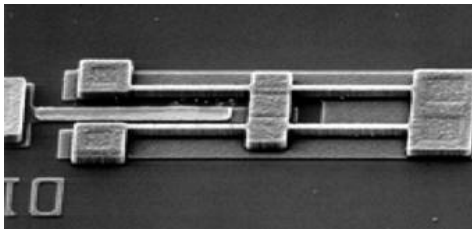
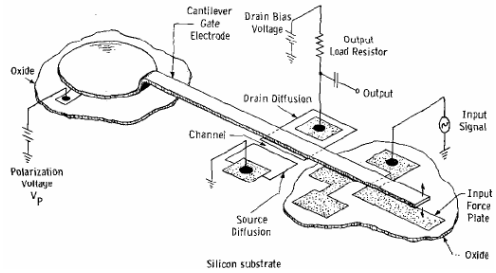
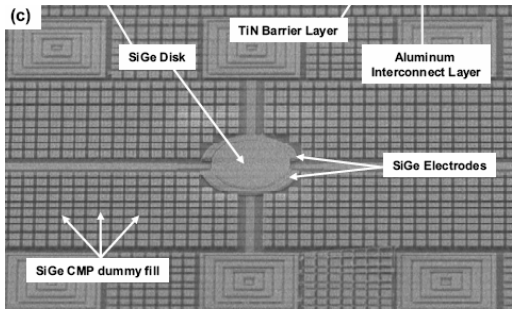
I.C. Electrostatic and piezoelectric resonators state-of-the-art, characteristics and performances

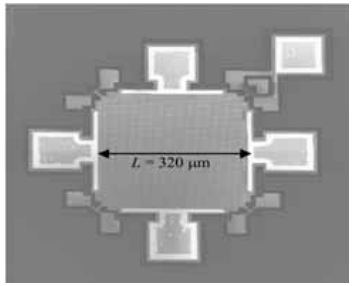
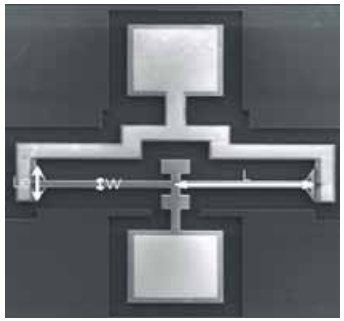
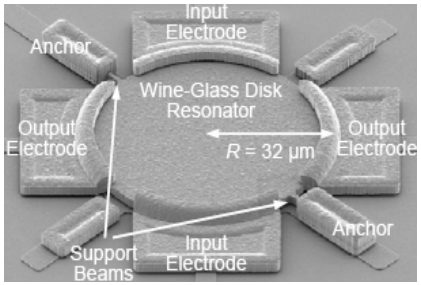
The following section exposes the state-of-the-art resonators technologies and performances (resonant frequency, quality factor, motional resistance). The table is ordered by considering first the flexural mode resonators, arranged according to the increased F*Q factor. The bulk mode resonators follow the same order and in the last part of the table, piezoelectric and quartz resonators performances are introduced. Note that the F_{res}xQ factor is a tool for comparison but other characteristics such as IC-integration and vibration detection methods should also be taken into account. The following abbreviations are used in the table:

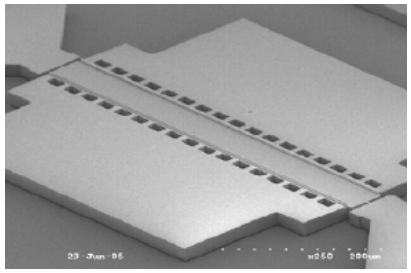
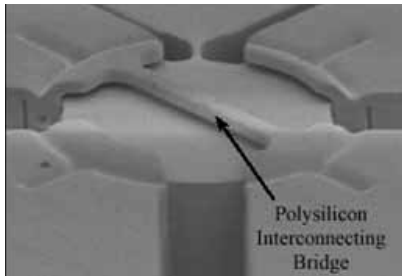
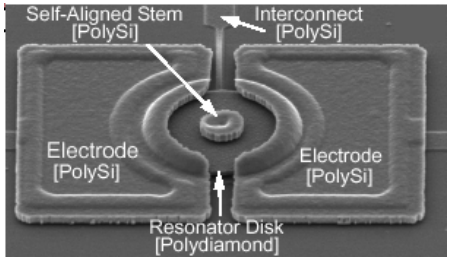
F_R	resonant frequency	Q	Quality factor	ρ	Density
V_p	DC bias	PN	Phase noise	BW	Band width
E	Young modulus	FFC	Far-From-Carrier	ω	Pulsation
υ	Poisson coefficient	R_m	Motional resistance		

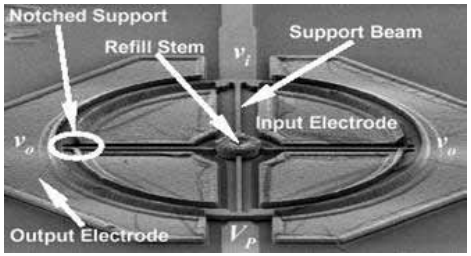
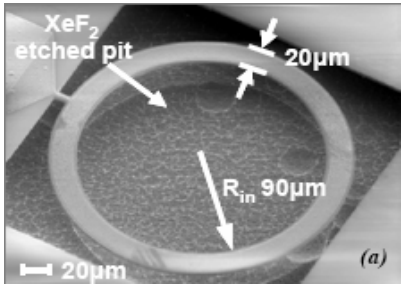
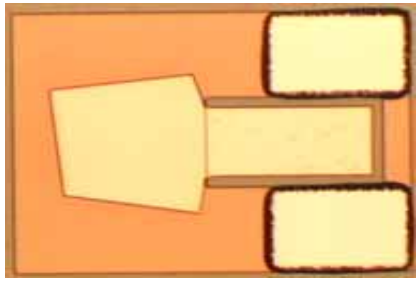
Table I. Technologies and performances of state-of-the art flexural and bulk-mode electrostatic resonators and piezoelectric resonators.

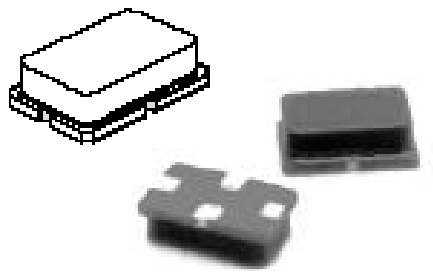
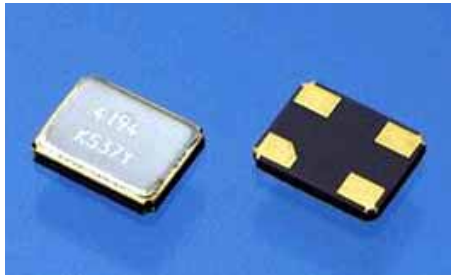
Resonator	Mode	SEM View	Techno & Comments	Performances
In-plane cantilever [8] Capacitive detection	Flexural mode	 Dim: L = 14.4µm,W = 260nm h=600nm, gap=200nm	**in-IC integration** Si resonator	**F(GHz)*Q =12** Res.: F_R = 1.49MHz Q = 8000 (vacuum) V_p = 2V Chip size = 7.5x7.5mm^2
DETF (Double-end tuning fork) [21] Capacitive detection	Flexural mode	 Dim: 220x8µm, h=20µm, gap=1µm	DRIE Silicon epitaxy Epipoly packaging technology Technology in production	**F(GHz)*Q =13** Res.: F_R = 1.3MHz Q = 10 000 (vacuum) V_p = 10V
Out plane CC-Beam resonator and filter [22] Capacitive detection	Flexural mode	 Dim: 40.8*8µm, h=2µm, gap=0.1µm	Surface micromach. Si substrate polySi resonator	**F(GHz)*Q = 68** Res.: F_R = 8.5 MHz, Q = 8 000 (vacuum) TCF = - 16.7 ppm/°C R_m = 8.46kΩ Osc.: 10MHz, PN = -120dBc/Hz far from carrier Filters: Mechanical coupling 2.4MHz, BW = 41kHz, Rejection 35dB, Insertion Loss<2dB

Resonator	Mode	SEM View	Techno & Material	Performances
Out plane FF-Beam [23] Capacitive detection	Flexural mode	 Dim: 13.1*4µm, h=2µm, gap=0.16µm	Surface micromach. Si substrate polySi resonator	**F(GHz)*Q = 687** Res.: F_R = 92.2MHz Q = 7 450 (vacuum) TCF = -12 ppm/°C R_m=167kΩ V_p=10V Osc.: 70MHz, PN=-130dBc/Hz FFC
Out-of-plane Cantilever [2] MOSFET detection	Flexural mode	 Dim: L = 482µm, h=3.4µm, gap=10µm	Surface micromach. metal resonator (gold)	**F(GHz)*Q =2*10^{-3}** Res.: F_R = 30kHz Q = 67 (air) V_p = 50V
Disk [24] Capacitive detection	Bulk Contour mode	 Dim: R=40µm, h=2µm, gap = 60nm	Surface micromach. SiGe Epitaxy Above-IC	**F(GHz)*Q = 1676** Res.: F_R = 202MHz Q = 8 300(vacuum) V_p = 10V TCF = -46.5ppm/°C

Resonator	Mode	SEM View	Techno & Material	Performances
Plate [25] Capacitive detection	Bulk Square-extensional mode	 Dim: 320x320µm, h=10µm, gap=0.75µm	DRIE SOI substrate Si resonator	**F(GHz)*Q = 1 703** Res.: F_R = 13,1MHz Q = 130 000 R_m = 4.47kΩ V_p = 20-100V Osc.: PN=-150dBc/Hz FFC
FF Beam [26] Capacitive detection	Bulk Longitudinal mode	 Dim: 140x10µm, h=10µm, gap=1.1µm	DRIE SOI substrate Si resonator	**F(GHz)*Q = 2 594** Res.: F_R = 13,1MHz Q = 198 000 (vacuum) Q = 2000 (air) R_m = 290kΩ V_p = 19V Osc.: 13MHz, PN=-130dBc/Hz FFC
Disk [27] Capacitive detection	Bulk Contour mode	 Dim: R=12µm, h=3µm, gap=20nm	Surface micromach. Poly Si resonator Solid SiN gap	**F(GHz)*Q = 5 150** Res.: f_R = 164MHz Q = 31400 (vacuum) R_m = 42.6kΩ V_p = 10V

Resonator	Mode	SEM View	Techno & Material	Performances
In plane CC Beam [28, 29] Capacitive detection	Bulk (SiBAR)	 Dim: 300x30µm (150x15), h=20µm (10), gap=160nm (145)	HARPSS SOI substrate Si resonator	**F(GHz)*Q = 6 013 - 13 217** Res.: F_R = 103MHz Q = 80 000 (vacuum) R_m =5kΩ V_p = 18V Osc.: 103MHz, PN=-108dBc/Hz @1KHz, PN=-135dBc/Hz FFC
Disk [30] Capacitive detection	Bulk Elliptical mode	 Dim: R=29.2µm, h=18µm, gap=160nm	HARPSS [31] SOI substrate Si resonator	**F(GHz)*Q = 7 320** Res.: F_R = 149,3MHz Q = 45 700 (vacuum) Q = 25 900 (air) R_m = 43.3 kΩ V_p = 17V
Disk [32] Capacitive detection	Bulk Radial contour mode	 Dim: R=10µm (24), h=3µm, gap=90nm	RIE Si substrate CVD poly-diamond resonator	**F(GHz)*Q = 17 440** Res.: F_R = 1,51GHz Q = 11 550 (vacuum) Q = 10 100 (air) R_m = 1.2MΩ V_p = 2.5V TCF = -12,1 ppm/°C Osc.: 61.2MHz, PN=-132dBc/Hz FFC

Resonator	Mode	SEM View	Techno & Material	Performances
Ring [33] Capacitive detection	Bulk contour mode	 Dim: R_1=11.8µm, R_2=18.7µm, h=2µm, gap=50nm	Surface micromach. Si substrate polySi resonator	**F(GHz)*Q = 18 000** Res.: F_R = 1,2 GHz Q = 15 000 (vacuum) R_m = 17.1kΩ V_p = 10V
AlN ring [34]	Bulk Contour mode	 Dim: R_1=90µm, R_2=100µm, h_{AlN}=2µm,	AIC process Si substrate AlN resonator	**F(GHz)*Q = 1 370** Res.: F_R=472.7MHz Q = 2900(vacuum) R_m = 84Ω Osc.: 224.1MHz PN=-110dBc/Hz@10kHz Filters: 236.2MHz, BW=647kHz, reject. 26dB, Insertion Loss -7.9dB
SMR BAW resonator [9]	Bulk Acoustic Wave	 Dim: 150x150µm, h_{AlN}=1.7µm	Surface micromach. Si substrate AlN SMR resonator	**F(GHz)*Q= 2 354** Res.: F_R=2.14GHz Q =1 100 (air) R_m = 1Ω TCF = -18 ppm/°C Osc.: 5GHz [11] PN=-140dBc/Hz@600kHz Filters: 2.25GHz, BW=78MHz, Insertion loss -3dB

Resonator	Mode	SEM View	Techno & Material	Performances
SAW [35]	Surface Acoustic Wave	 Dim: 5.74x3.73mm, h=1.16mm	Surface micromach. In Package	**F(GHz)*Q= 787 - 3920** Res.: F_R = 315MHz Q=2 500 (air) R_m=19Ω F_R = 980MHz Q = 4 000 (air) R_m = 20Ω TCF = 0.032ppm/°C Filters: 167MHz, BW=70kHz, Reject. 5dB, insertion loss 8dB
Quartz (Takanashi)	Piezoelectric	 Dim: 3x2.3mm, h=0.8mm	Quartz In Package	**F(GHz)*Q= 5 760** Res.: F_R = 38.4MHz Q = 150 000 R_m = 10kΩ TCF = 0.015ppm/°C
Quartz [36]	Piezoelectric Lamé mode	 Dim: 3.2 x 2.5 x 0.55 mm	Quartz In Package	Res.: F_R = 4MHz R_m = 150-500Ω TCF = +0.1/-0.5 ppm/°C Frequency tolerance = +/- 30ppm

Various performances in terms of quality factor and resonant frequencies were achieved with different technologies. Various materials, such as single-crystal silicon, polysilicon, poly-diamond, AlSi, AlN, Silicon-Germanium and quartz were investigated. The technology options for electromechanical resonators is today very diverse, many coming from university facilities, but the trend for single-crystal silicon resonators can be extracted. The trend towards in-IC or above-IC integration is not yet defined, and comes not only from the technological complexity but also from the cost-per-wafer to integrate horizontally (in-IC) or vertically (above-IC) the resonators. Horizontal integration induces a lower chip density per wafer and vertical integration induces a higher back-end-of-line assembly cost.

Electrostatic MEMS resonators use mainly capacitive displacement detection techniques and one example of MOSFET detection was presented. This last technique necessitates a more complex analytical study and fabrication processes than capacitive MEMS detection, and for this reason was put on a side since its first validation in 1967 [2]. This structure presents however the potential of an intrinsic gain of due to the intrinsic transistor, inducing a much higher output detection current than for capacitive detection and being therefore interesting for circuit integration. This work concentrates on the MOSFET detection aspect of a vibrating flexural Clamped-Clamped beam resonator and its impact on circuit design.

I.D. Applications of MEMS resonators and specifications

In a classical transceiver architecture, external of low performance internal components such as local oscillator, VCO and filters could eventually be replaced by on-chip mechanical devices [37]. Different performance requirements are needed for the cited applications.

I.D.1. Local oscillator

The local oscillator is the reference of the PLL, used to synchronize the signal to the base station. This application is the best suited for MEMS resonators due to its intrinsic high quality factor at frequency possibly, which is much higher than of quartz crystal. MEMS resonators however have to fulfill stringent specifications in terms of resonant frequency accuracy, frequency drift under temperature variations and ageing, as developed in Chap. IV. Other consumer applications which could benefit of an integrated time reference are watches (32.768 kHz), TV (27 MHz) and RFID (13 MHz).

I.D.2. Voltage Control Oscillator (VCO)

VCOs are usually using variable capacitor in fully differential oscillator architecture in order to modify the oscillating frequency. It has been shown previously that the resonant frequency of a CC-beam resonator is directly related to the applied DC and AC voltages used for the electrostatic actuation [38]. A frequency tuning of 6.6% has been measured on a 15MHz resonator [39]. Phase noise response of the VCO could then benefits from the high quality factor of these integrated MEMS as compared to the standard low quality factor LC tank classically used today. Comparison with published FBAR and SAW (Surface Acoustic Wave)-based VCO is presented in Table I. Challenges of MEMS resonators for this application are, in terms of possible tuning range, at high frequency application for which CC-

beam architecture is not appropriate (Fig. 4). Moreover, more investigations on the relationship between the phase noise and the applied DC voltages are needed as source of possible degradation of the VCO's performances [40].

	FBAR VCO	**M650 SAW VCO**	**Published SAW VCO**	**Electromechanical Resonator (Target)**	**Unit**
Power supply	2.4	3.3	3.0	<2.5	V
Current consumption	22 - 39	80	35	<20	mA
Operating frequency	2110	622	2488	2000	MHz
Tuning range	15	0.4	0.5	> 20-30	MHz
Relative tuning range	0.71	0.07	0.02	>1	%
Best phase noise @600kHz	-140.7	-143	-160	-140	dBc/Hz
Quality Factor	400	---	---	1000	-
Physical size	1.49	126	100	0.2	mm^2

Table I. FBAR, SAW and MEMS-based VCO characteristics and target [41]

I.D.3. Filters

High Frequency MEMS-based filters have been demonstrated based on coupled MEMS resonator architecture [18, 42, 43]. The specifications for the wireless standards are listed in Table II.

Filter types	**Standard**	**Central Frequency**	**Bandwidth**	**Channel**
Bandpass	WIMAX	2.3 to 2.7GHz 3.3 to 3.7GHz	1.5 to 10MHz	10kHz
Bandpass	WIFI	2.4 to 2.5GHz 4.9 to 5.9GHz	20 MHz	312.5 kHz
Bandpass	FM	98 MHz	20 MHz	100 kHz
Lowpass	GSM	900kHz	200 kHz	Few 10 MHz
Lowpass	WCDMA	2.1 GHz	60 MHz	2 to 5 MHz

Table II. Filtering specifications

According to the specifications of Table I, Table II and to the state-of-the-art performances described in section C, electromechanical resonators can eventually be suited for filtering application requiring a low bandwidth (WIMAX, FM and eventually WIFI). VCO application is challenging, especially in terms of tunability at high frequency.

I.E. Interest of MOSFET detection for MEMS resonators

Wireless application requires the use of MEMS resonators in the Intermediate and Ultra-High Frequency domains (from 30MHz to 300MHz and from 300MHz to 3GHz respectively). To achieve those frequencies, resonators should be very stiff; this lowers the mechanical displacement for the same applied electrostatic field. According to Fig. 6, high frequency resonators are technologically achievable. The limitation comes from the detection of resonator displacement at resonance. Capacitive detection, classically used for the motional measurement, gives a capacitive current related to the capacitance between the resonator and the electrode. At resonance, displacement induces a maximal capacitance variation, measured as a peak of motional current. For high frequency resonators, with low mechanical displacement, the capacitance measurement suffers from the low capacitance variations, which ultimately can be lower than the detection threshold.

This limitation could however be overcomed, in principle, by using MOSFET detection architecture. The resonator is then considered as a mobile gate resonating over the channel, modulating channel charge and, consequently, the drain current. The original Resonant Gate Transistor (RGT) [2] was the first attempt to use that detection technique for mechanical resonator. The device was composed of a metallic suspended cantilever actuated by an electrode and used as a mobile gate of a MOSFET transistor. Based on the same principle, compact resonator geometry was developed to optimize the actuation and detection aspects and make it suitable for scaled resonators. The actuation and the detection parts are then combined in a single device, as shown in Fig. 8, called Resonant Suspended-Gate MOSFET (RSG-MOSFET) [44]. A particularity of the RSG-MOSFET is that the vibrating (mobile) gate directly modulates the surface potential of the MOS channel and the subsequent inversion charge. DC and AC signals are superposed on the single suspended gate electrode.

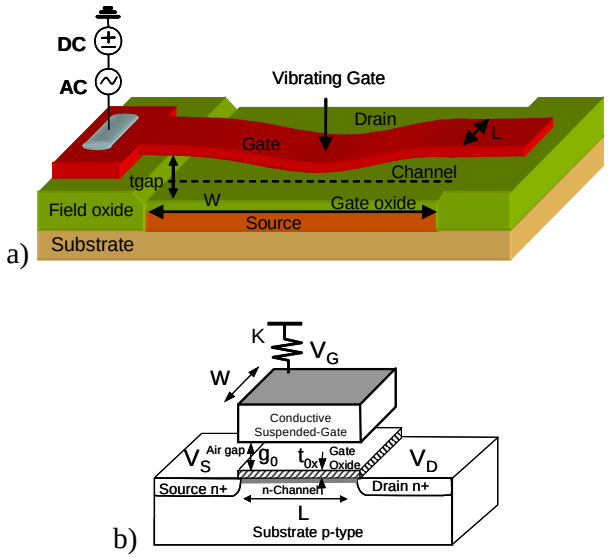


Fig. 8 Schematics of a) a Resonant SG-MOSFET and b) cross section of the SG-MOSFET

The MOSFET detection is then a very interesting solution to detect displacement for high frequency resonators. This architecture is investigated in more details regarding the modeling aspects in Chapter II.

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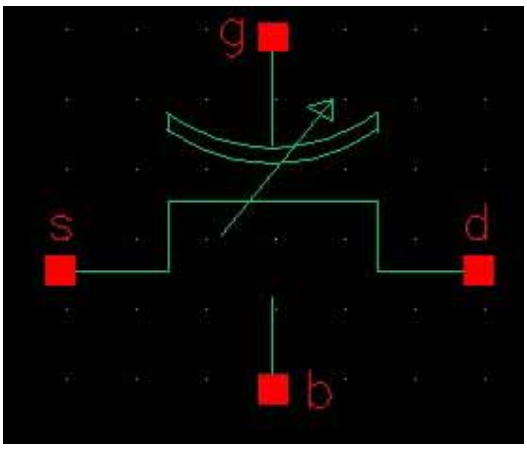
Chapter II

Quasi-static and dynamic modeling of the SG-MOSFET



RSG-MOSFET instance symbol created for Cadence® design kit

Introduction

The SG-MOSFET architecture can be used in quasi-static for MEMS switch and memory applications, and in dynamic for resonator application. The complex device behavior includes the mechanical electrostatic actuation of the suspended-gate and the MOSFET channel operation. The influences of the beam characteristics and MOSFET parameters on the device behavior were investigated in static and dynamic operation.

The mechanical behavior of a beam resonator is deeply study in order to explain and predicts the displacement and the losses mechanisms in the device. The quality factor can be predicted by studying the different sources of loss involved in the silicon and AlSi vibrating structures. Capacitive resonators show mechanical and electrical non-linearities that degrades the transmitted signal. This effect is modeled and the non-linearities mechanisms are investigated.
The equivalent electrical circuits of a flexural capacitive resonator and a RSG-MOSFET were developed and allowed a comparison between the two detection techniques in terms of output signal amplitude. In order to use the model in circuit design, a dedicated Verilog-A code was created, based on the EKV MOSFET model and on analytical description of the mechanical vibration.

II.A. Static modeling of a clamped-clamped SG-MOSFET

II.A.1. Suspended-gate MOSFET electrical modeling

Electrical equivalent circuit of the SG-MOSFET is presented in Fig. 9 where gap, inversion and depletion capacitances (C_{gap}, C_{ox}, C_{dep}, and C_{inv}) are capacitively dividing the applied gate voltage V_G. The electrical MOSFET model includes a continuous expression for the gate-to-channel capacitance (C_{gc}) in weak, moderate and strong inversion, in the linear MOSFET region.

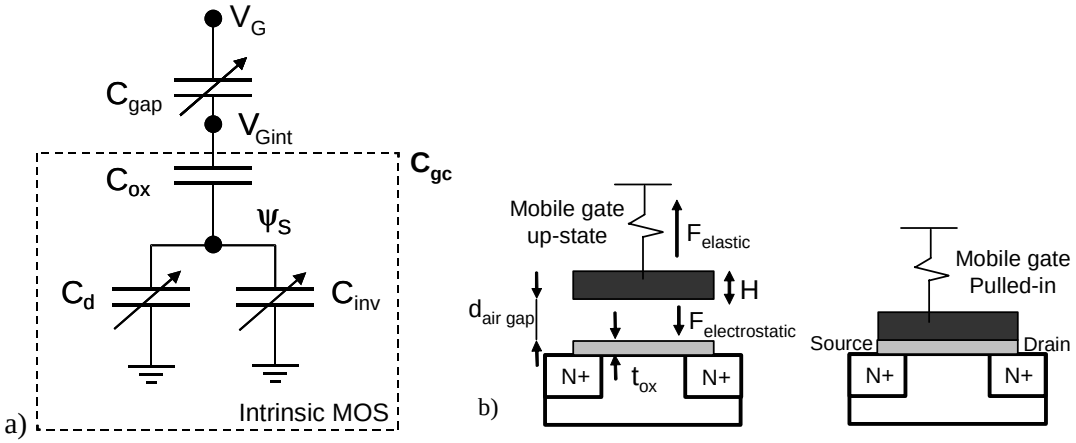


Fig. 9 a) Electrical equivalent circuit of the SG-MOSFET showing the capacitive divider, b) Schematic of the SG-MOSFET in the up-state and down-state

Two modeling approaches are possible for this device considering the parameter sets:

- Applied gate voltage V_G and gate-to-channel capacitance C_{gc}
- Intrinsic gate voltage V_{Gint} and gate oxide capacitance C_{ox} (as a classical MOSFET device).

The last couple was chosen in the model. The relation between the gate voltage V_G and the intrinsic voltage V_{Gint} acting on the MOSFET, is function of the gate to channel capacitance C_{gc} and the air-gap capacitance C_{gap} [44]. The gate voltage is capacitively divided as expressed in equation (II- 1).

$$V_{G\,int} = \frac{V_G}{\left(1 + \frac{C_{gc}}{C_{gap}}\right)} \tag{II- 1}$$

The continuous MOSFET electrical expression of the model is based upon the gate-to-channel capacitance variation according to Fig. 9, where the oxide and depletion capacitances are respectively C_{ox} and C_d:

$$C_{gc}(V_{G\,int}) = \frac{C_{ox} C_{inv}}{C_{ox} + C_{inv} + C_d} \tag{II- 2}$$

The gate-to-channel capacitance equation, valid from weak to strong inversion was developed in [44] and is written as:

$$C_{gc}(V_{G\,\mathrm{int}}) = \frac{\frac{\eta-1}{\eta}\cdot\frac{1}{\sqrt{2}}\cdot\exp\left(\frac{V_{g\,\mathrm{int}}-V_T}{\eta\cdot U_T}\right)}{\frac{\eta-1}{\eta}\cdot\frac{1}{\sqrt{2}}\cdot\exp\left(\frac{V_{g\,\mathrm{int}}-V_T}{\eta\cdot U_T}\right)+1}\cdot C_{ox} \qquad \text{(II- 3)}$$

In this equation, $\eta = 1 + C_d / C_{ox}$ is the subthreshold coefficient and $V_T = V_{FB} + 2\eta\phi_F$ is the threshold voltage. Equations (II- 1) and (II- 4) are combined to evaluate the intrinsic voltage and the gate-to-channel capacitance C_{gc}. The inversion charge Q_{inv} is calculated from the integration of the C_{gc} over the intrinsic voltage.

$$Q_{inv} = \int C_{gc}(V_{g\,\mathrm{int}})dV_{g\,\mathrm{int}} = \ln\left[\frac{1}{2}\frac{(\eta-1)}{\eta}\sqrt{2}\exp\left(\frac{V_{g\,\mathrm{int}}-V_T}{\eta U_T}\right)+1\right]\eta U_T C_{ox} \qquad \text{(II- 4)}$$

The motional drain current, relative to the charge inversion along the channel when the gate resonates is defined from (II- 5), in the linear MOSFET region, as

$$I_d = \mu_n \frac{W}{L}\int_{V_s}^{V_d} -Q_{inv}.dV \qquad \text{(II- 5)}$$

II.A.2. Electro-mechanical modeling

The force-stiffness relationship describes the electrostatic force applied between the gate and the MOSFET channel and governs the beam displacement. The electro-mechanical analysis considers the total energy stored between two conductive plates, which can be written as:

$$U_{tot} = U_{elec} - U_{meca} = \frac{1}{2}C_{gap}V^2 - \frac{ky^2}{2} \qquad \text{(II- 6)}$$

When the gate is at a mechanical equilibrium, the derivative of this equation over the y displacement is null. The gap capacitance is written as:

$$C_{gap} = \frac{\varepsilon_0 S}{d_{gap}} \qquad \text{(II- 7)}$$

In the SG-MOSFET architecture, the voltage drop between the gate and the substrate is directly related the gate-to-channel capacitance and is expressed as $V = V_G - V_{G\,\mathrm{int}}$.

The resulting quadratic equation of the electrostatic force is derived from (II- 6) as:

$$F_{elec} = \frac{1}{2}\frac{\varepsilon_0 S}{y^2}(V_g - V_{g\,\mathrm{int}})^2 = ky \tag{II- 8}$$

where y is the vertical gate displacement, S the electrostatic area and k the gate rigidity.

II.A.2.a. Pull-in and pull-out effects description

When the gate deflected under the electrostatic force, the suspension spring creates a restoring force F_k with a magnitude of $F_k = ky$. At equilibrium, the two forces balances and (II- 8) can be written as:

$$k(d_{gap} - y) = \frac{1}{2}\frac{\varepsilon_0 S}{(d_{gap} - y)^2}(V_g - V_{g\,\mathrm{int}})^2 \tag{II- 9}$$

where d_{gap} is the initial air-gap distance. The rigidity of the structure is calculated from its geometry and dimensions as:

$$\begin{aligned} k_0 &= \frac{192EI}{L_{beam}^3} \\ I &= \frac{W_{beam}H_{beam}^3}{12} + \frac{H_{beam}W_{beam}^3}{12} \end{aligned} \tag{II- 10}$$

where I is the bending moment of inertia of the rectangular shape beam, E is the Young's modulus and H_{beam}, L_{beam} and W_{beam} are respectively the beam thickness, length and width. υ is the Poisson's ratio. The restoring force is a linear function of the displacement and the electrostatic force is an inversely quadratic function, therefore there exists a stable equilibrium point only when:

$$y \le \frac{2}{3}d_{gap} \tag{II- 11}$$

This deflection is obtained for a voltage drop called the pull-in voltage (V_{pi}). This voltage is however different between a metal-metal structure and the SG-MOSFET due to the presence of the voltage divider for the last one. The pull-in voltage for a clamped-clamped metal-metal switch is derived from (II- 9) and (II- 11) as:

$$V_{pi} = \sqrt{\frac{8.k.d_{gap}^3}{27.\varepsilon_0.W_{beam}L_{beam}}} \tag{II- 12}$$

For the SG-MOSFET, however, when V_G increases, the electrostatic force attracts the gate towards the substrate, which depletes the channel. This effect decreases the depletion capacitance and, due to the capacitive divider behavior defined in (II- 1), tends to lower the

voltage drop between the gate and the channel, therefore lowering the electrostatic attraction. The stable and unstable mechanical regions for the metal-metal switch and the SG-MOSFET are shown in Fig. 10.

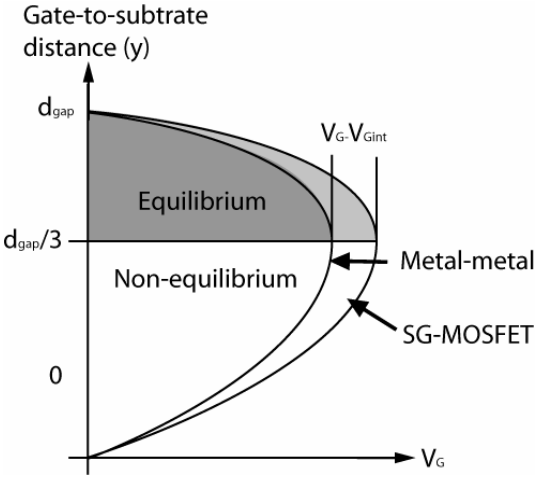


Fig. 10 Mechanical stable and unstable regions for a metal-metal switch and a SG-MOSFET

The SG-MOSFET pull-in voltage V_{pi_MOSFET} deduced from (II- 1) and (II- 10) is therefore greater than for capacitive switches [45]. The pull-in voltage for a clamped-clamped suspended-gate MOSFET is derived as:

$$V_{pi\_SG-MOSFET} = \sqrt{\frac{8k\left(1+\frac{C_{gap}}{C_{gc}}\right)^2 d_{gap}^3}{27\varepsilon_0 W_{beam} L_{beam}}} \qquad \text{(II- 13)}$$

After pull-in, the capacitance is equal to the gate-to-channel capacitance C_{gc}. A comparison of a metal-metal and a SG-MOSFET pull-in voltages for suspended structures of similar dimensions is shown in Fig. 11 with a pull-in voltage difference of ΔV = 1.04V which corresponds to 17.3% variation.

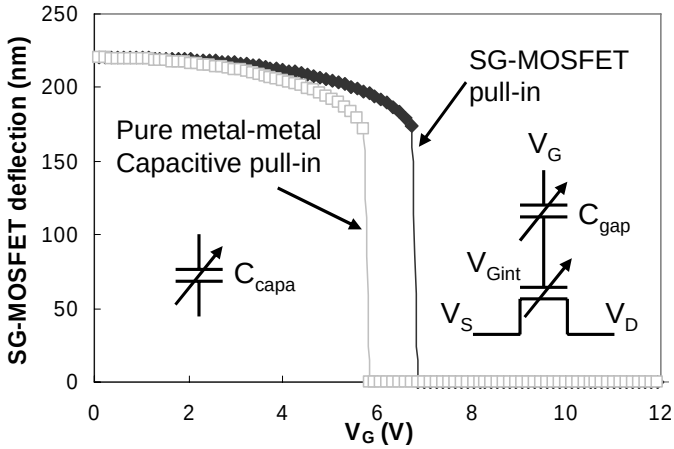


Fig. 11 Comparison of the capacitive and SG-MOSFET pull-in voltage for an AlSi-based CC-beam with length, width, thickness of respectively L_{beam} = 48µm, W_{beam} = 2µm, H_{beam} = 500nm and air-gap of 245nm with a gate oxide of T_{ox} = 10nm

A thicker gate oxide lowers the gate-to-channel capacitance and therefore shifts up the pull-in voltage according to (II- 14). Fig. 12 shows the pull-in shifts for a gate oxide varying from 5nm to 60nm. The induced pull-in voltage shift is ΔV = 0.6V which corresponds to 8.8% variation.

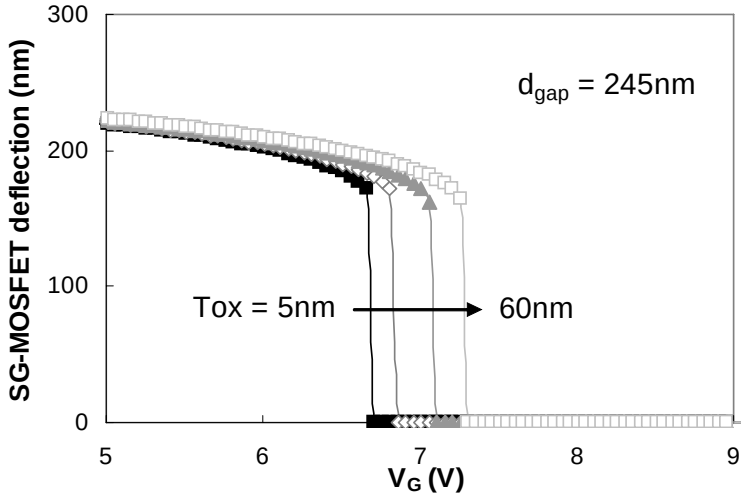


Fig. 12 Comparison of the SG-MOSFET pull-in voltage for various gate oxide thicknesses on a CC-beam with similar dimensions as for Fig. 11

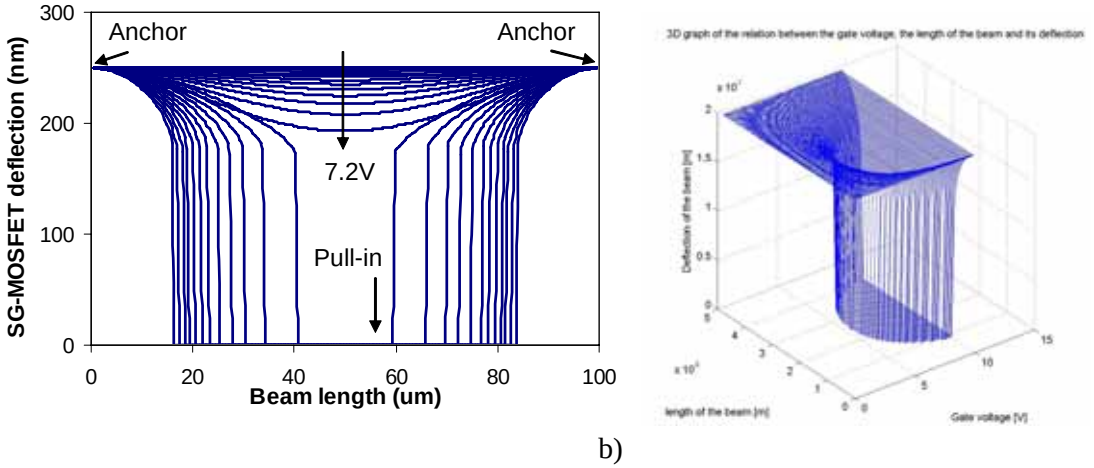
When the gate is collapsed on the substrate, a strong electric field through the gate oxide maintains this stable state. The mechanical release of the beam is only possible if the electrostatic force becomes lowers than the restoring force. This effect occurs at a voltage called pull-out, lower than the pull-in voltage. The voltage shift comes from the fact that the initial stable conditions are different.

II.A.2.b. Beam shape during mechanical deflection

In practice, under electrostatic actuation, the CC-beam bends non-uniformly towards the MOSFET channel. The model was optimized to consider the shape of the deflecting beam, using the equation of beam deflection along its length under a homogeneous load [46]:

$$y(x) = \frac{\lambda}{12EI}\left(\frac{x^4}{2} - L_{beam}x^3 + \frac{L_{beam}^3 x}{2}\right) \qquad \text{(II- 14)}$$

The beam deflection along its length, before and after the pull-in effect is shown in Fig. 13, where the shape of the beam when contacting the substrate is not modeled.



b)

Fig. 13 a) Deflection shape of a fixed-fixed beam under vertical electrostatic actuation, b) 3D deflection view of the beam subjected to an increased gate voltage

II.A.2.c. Total SG-MOSFET drain current

In order to account for the beam deflection shape, the beam length (W of the channel) was divided into parallel X_n sections for which the air-gap capacitance was considered as uniform. For each section, the gate-to-channel capacitance is calculated accordingly to the gap size and the electrostatic field acting in that region. The total output current I_{DS} is then the sum of the drain current of each section as:

$$I_{DS} = \sum_{0}^{n} I_d(X_n) \qquad \text{(II- 15)}$$

Prediction of the electrical parameters (V_{Gint}, g_m, ΔC_{gc}, ΔI_{DS}) of the RSG-MOSFET are carried out from the model. The influence of the gate oxide and beam stiffness variations on SG-MOSFET electrical characteristics are shown in Fig. 14 and Fig. 15. The mechanical pull-in and pull-out effects on the gate-to-channel capacitance and drain current are shown in Fig. 16 and Fig. 17. It is interesting to note that in standard MOSFETs, the drain current in the subthreshold regime increases exponentially with the gate voltage. In the case of the movable gate MOSFET, the increase of V_G induces the air-gap reduction and increases the gate capacitance. The drain current increases super-exponentially in weak inversion when the gate voltage is approaching the pull-in region. This effect is slightly seen in the following simulated curves just before the pull-in effect.

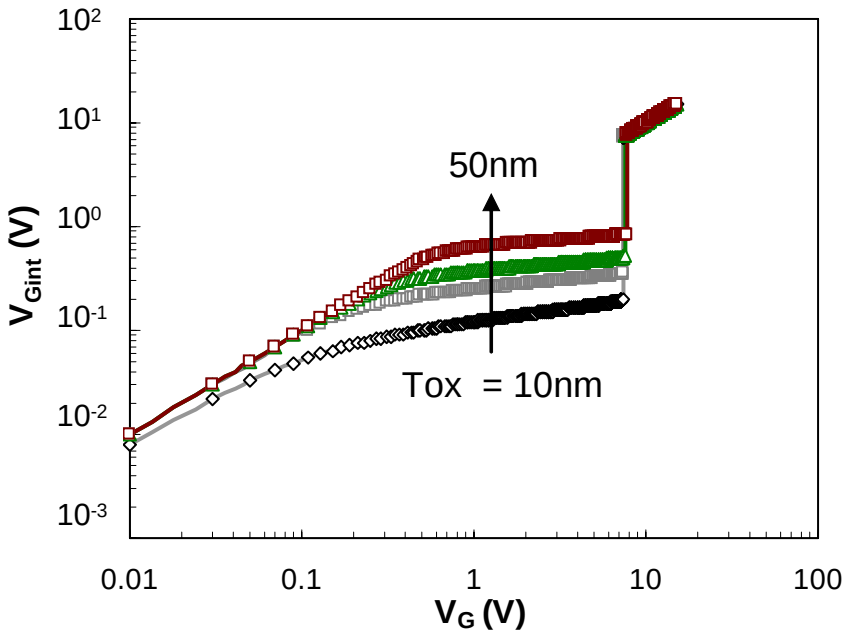


Fig. 14 Simulated intrinsic gate voltage V_{Gint} versus gate voltage V_G for various oxide thicknesses with similar device dimensions of Fig. 11

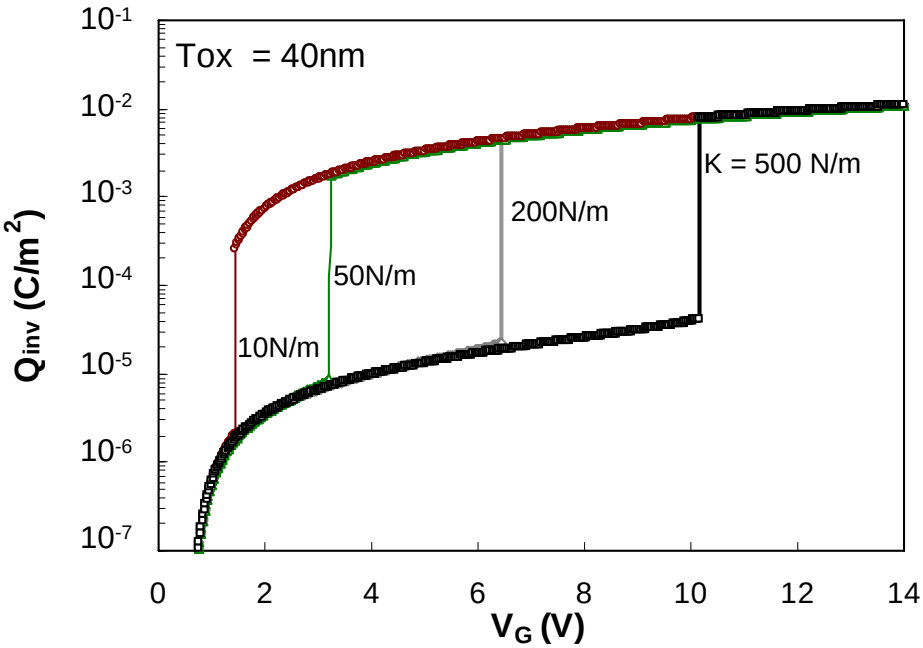


Fig. 15 Simulated inversion charge Q_{inv} versus gate voltage V_G for various beam rigidity considering the same MOSFET active zone.

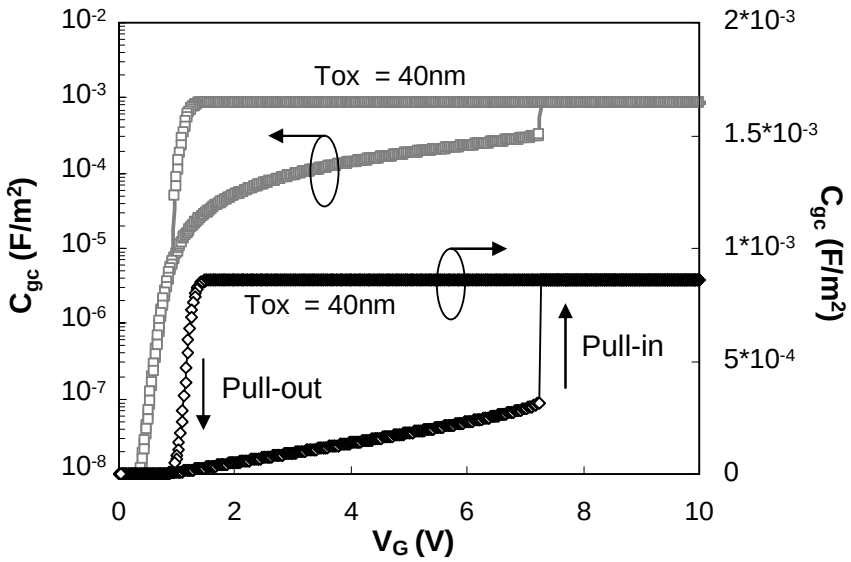


Fig. 16 Simulated gate-to-substrate capacitance C_{gc} versus gate voltage V_G in linear and log scale, showing the pull-in and pull-out effects on the suspended beam with similar dimensions than of Fig. 11

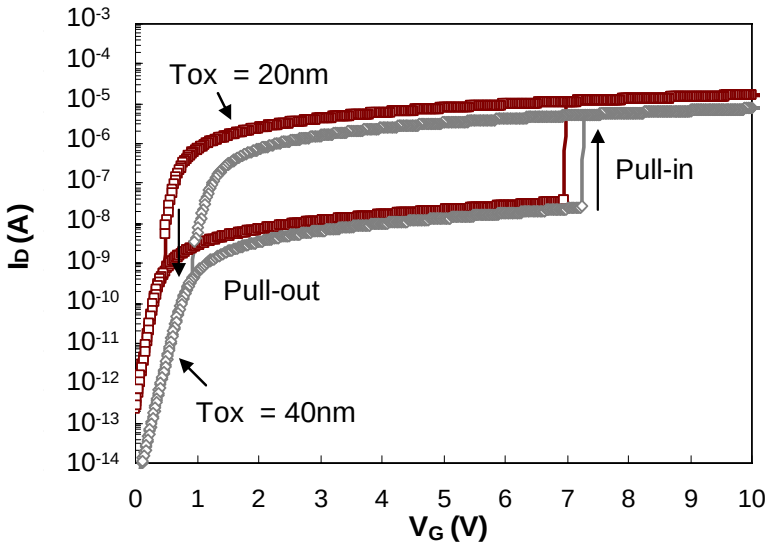


Fig. 17 Simulated drain current I_{DS} versus V_G for various oxide thicknesses, showing the pull-in and pull-out effects on the suspended beam with similar dimensions than of Fig. 11

II.A.3. Model validation

The model was fitted with experimental data reported in [47]. Fig. 18 shows the good agreement obtained between simulated and measured curves for various drain voltages (0.1V to 5V) from weak to strong inversion. The suspended polysilicon gate MOSFET width and length are 15µmx10µm respectively, with an air-gap of 500nm and a W/L channel dimensions of a 7µm/7µm fabricated on a glass substrate. The simulation also shows the effect of pull-in voltage on current characteristics in the case of a small air gap of 100nm (for larger air-gaps, the pull-in effects occur at higher gate voltages, outside of the curve scope).

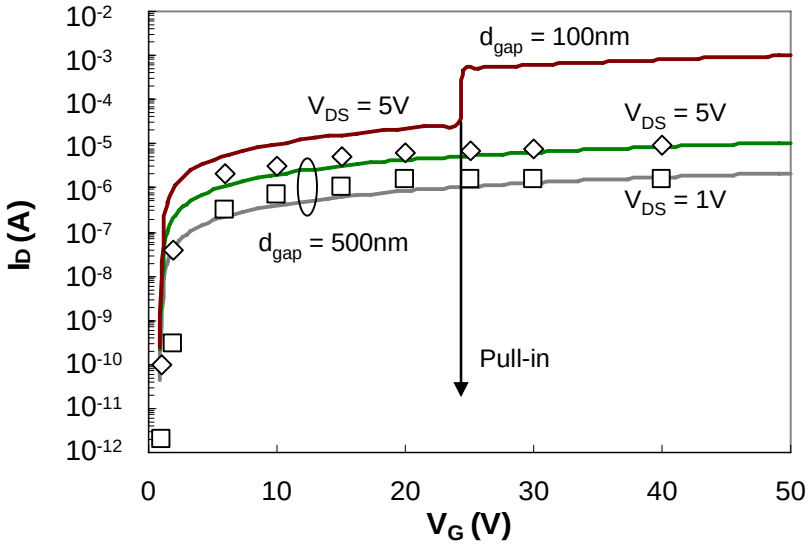


Fig. 18 Comparison between simulations (lines) based on the model and experimental data (dots) from [47] for a fixed-fixed beam structure for various drain-source voltages V_{DS}.

A second model validation was performed on fabricated metallic Suspended Gate-MOSFET and presented in Chapter V to validate the SG-MOSFET switch application.

II.A.4. Electrical air-gap for SG-MOSEFT

Both metal and polysilicon gate have been fabricated with two different processes (see Chapter III). For the SG-MOSFET modeling, especially for pull-in voltages prediction, the notion of electrical air-gap is introduced. It represents the electric field between the gate and the channel, more relevant than physical air-gap. It was shown in [48] that for doped silicon MEMS resonators with an air-gap as small as 200nm, the effective electrostatic gap between electrode and resonator is larger than the air-gap due to doping level at the silicon electrode-air interface. Electrical air-gap should then include poly-depletion in the case of polysilicon gate, and also the gate oxide thickness. Poly-depletion is strongly dependant on the silicon doping level and on the surface electrode potential. The effective gap in that case is the sum of the initial gap d_{gap0} and the depletion zone that could be considered electrically as a dielectric at first approximation. In strong inversion, the equivalent gap thickness (EGT) of the RSG-MOSFET considering the surface channel conduction can be written as:

$$EGT = d_{gap0} + \frac{t_{ox}}{\varepsilon_{rox}} + \frac{\sqrt{\frac{4\varepsilon_{SI}}{qN_G}\Phi_F}}{\varepsilon_{rSI}} \qquad \text{(II- 16)}$$

With d_{gap} the air gap between the electrode and the conductive suspended gate

t_{ox} the gate oxide thickness

ε_{rox} and ε_{rSI} the relative-to-free space oxide and the silicon permittivity

ε_{SI} the silicon permittivity

q the elementary charge and N_G the gate doping level

The Fermi level Φ_F depends on the silicon gate doping level, varying from 0.47eV for 10^{18} at/cm^3 to 0.59eV for 10^{20} at/cm^3 for an n-doped silicon. The EGT is respectively 214nm and 205nm for the previous doping level, with d_{gap} of 200nm and t_{ox} of 20nm. The AlSi work function depends also on the deposition process and on the percentage of silicon in aluminum. The work function can vary from 3.9eV to 4.3eV. For an AlSi suspended gate, however, the depletion zone does not occur and the EGT is reduced to the sum of the gap and the oxide thickness.

II.A.5. Disturbing forces on nano-gap devices - The Casimir effect

Reduction of the air-gap is mandatory to lower the pull-in voltage of SG-MOSFET memory and switches and achieve CMOS compatible voltages. Small gap between the beam and the substrate is mandatory to increase the detection current induced by the motion of the beam, and decrease the resonator motional resistance (see B.2). To achieve high quality factor, MEMS resonators have to be actuated under vacuum, as explained in B.5.2.c. At that scale however, other attractive force than electrostatic force act on the beam and can induce pull-in of the beam towards the substrate. It is therefore mandatory to consider the Casimir force for the SG-MOSFET. Casimir effect explains this phenomenon which is related to the attraction of two uncharged conductive plates facing each other by the only presence of the vacuum. The Casimir effect takes into account the dispersion forces, Van Der Waals forces, molecular attraction and the interaction between atoms and walls [49].

Casimir theory considers that even at perfect vacuum and absolute zero temperature, all fields, especially electromagnetic fields are not perfectly stable but fluctuate around a mean value; this effect is known as vacuum fluctuations. Due to these fluctuations, atoms in an excited state can turn to a ground state by spontaneously emits a photon which energy is transported by the field. Electromagnetic fields have frequency spectrums that are all equivalent in vacuum. However between the two conductive plates, the field at the frequency equal to half of the wavelength of the cavity resonant frequency is perfectly reflected on the plates and is then amplified. At all other frequencies the field is cancelled inside the cavity. This physical effect has been correlated to the “field radiation pressure”, which is the pressure created by electromagnetic field on every surface. As the field is not equal inside and outside the cavity, conductive plates can be push apart or attracted towards each other.
- At the cavity resonant frequency, inner field is stronger than outer field and the related pressure tends to push apart the two plates.
- At all other frequency, inner field is lower than outer field and the related pressure tends to attract the two plates towards each other.

It has been demonstrated in [50] that on balance, attractive radiation pressure is slightly stronger than the repulsive force, which ends up of the contact of the two plates if the pressure becomes larger than the restoring mechanical force. Radiation pressure is strongly dependent to the reflection of wavelength in the two plates. The amount of reflection depends on the plate’s material. Defects and roughness on plate’s surface also disturbs and attenuates the reflection value, then changing the radiation pressure. Expression of the Casimir force considering the distance between two perfectly conductive plates is:

$$F_{Casimir} = -\frac{\pi^2 hc}{480}\frac{S_{plate}}{d_0^4} \qquad \text{(II- 17)}$$

Where S_{plate} is the surface of the plate facing each other, h is the Planck's constant and c the light speed in free space. A coefficient η, comprised between 0 and 1, accounts in equation (II-18) for the non-perfectly conductive material, as doped silicon is introduced to the equation and is as

$$F_{Casimir\_silicon} = \eta F_{Casimir} \qquad \text{(II- 18)}$$

Comparison of the induced beam displacement due to Casimir force and electrostatic force is shown in Fig. 19. Simulations were performed considering a perfectly conductive silicon-based CC-beam and actuation electrode, with a beam length, width and thickness of respectively of 14.1µm, 6 and 1µm. For this device, note that the Casimir force is stronger than the electrostatic force created for a gate voltage of 1V, and the minimum air-gap to maintain the mechanical equilibrium is 8nm. This gap thickness is however close to the technological limits of current processes, especially when considering the surface roughness.

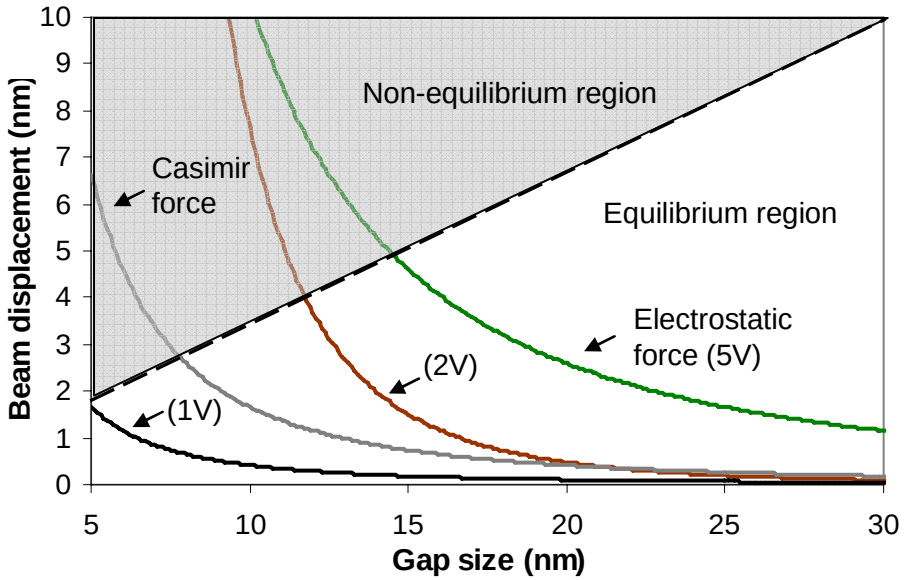


Fig. 19 Effect on Casimir force on the beam displacement of a suspended conductive structure, depending on the air-gap size. Comparison with the electrostatic force induced-displacement for various applied voltages (1, 2, 5V)

For this CC-beam design, air-gap below 10nm becomes critical in terms of self actuation of the beam and therefore has to be avoided.

II.B. Dynamic modeling of the RSG-MOSFET

As described in the previous chapter, a major driven application for MEMS resonators is the WCDMA, which necessitates a 38.4MHz reference device. Therefore the following electro-mechanical studies are related to resonators with dimensions enabling this natural frequency.

II.B.1. Mechanical dynamic behavior and mode shape

Different methods are available to describe the dynamic behavior of a vibrating system [51], with the most used of them are based on:

- Newton's law of motion, considering that the some of forces acting on a moving structure equal its mass times the acceleration
- Energy conservation method, considering that the total energy of a system is unchanged at all time

In order to describe in detail the different forces involved in a vibrating beam and the specificity of mode shapes in fixed-fixed beam, the energy method will be studied. Each following equations represent the different kinetic and potential energies associated with the beam deflection.

The stretching of the beam when bending (Energy per unit length) is:

$$U_{stretch} = \frac{1}{2} EI \left(\frac{\partial^2 y(x)}{\partial x^2} \right)^2 \quad \text{(II- 19)}$$

The axial deflection of the beam (Energy per unit length) is:

$$U_{axial} = \frac{1}{2} T \left(\frac{\partial y(x)}{\partial x} \right)^2 \quad \text{(II- 20)}$$

The external load applied on the beam (Energy per unit length) is:

$$U_{ext} = -P(x) y(x) \quad \text{(II- 21)}$$

The kinetic energy of the mass with a certain velocity, per unit length, is:

$$K_{mass} = \frac{1}{2} \rho A \left(\frac{\partial y(x)}{\partial t} \right)^2 \quad \text{(II- 22)}$$

The friction forces acting on the beam when moving, also called dissipation function is:

$$D = \frac{1}{2} \gamma \left(\frac{\partial y(x)}{\partial t} \right)^2 \quad \text{(II- 23)}$$

Lagrange function is based on the Hamilton principle saying that the integral of the energies along the beam length, which is the difference between the kinetic energy T and potential energy U, is a minimum. The Lagrange function L is:

$$L = \frac{1}{2}\int_0^{L\_beam} \left(K_{mass} - U_{stretch} - U_{axial} - U_{ext} + D\right)dx = \int_0^{L\_beam} L^* dx \qquad \text{(II- 24)}$$

By integrating this function over the time, the Euler-Lagrange equation is defined (II- 26). Differentiation with dots and primes denote the differentiation with respect to time and spatial coordinate respectively.

$$\frac{\partial L^*}{\partial y} - \frac{\partial}{\partial t}\frac{\partial L^*}{\partial \dot{y}} - \frac{\partial}{\partial x}\frac{\partial L^*}{\partial y'} + \frac{\partial^2}{\partial x^2}\frac{\partial L^*}{\partial y''} = 0 \qquad \text{(II- 25)}$$

Considering the external load as the electrostatic force in the case of electrostatic resonators, the equation becomes

$$-\rho A\frac{\partial^2 y}{\partial t^2} = EI\frac{\partial^4 y}{\partial x^4} - T\frac{\partial^2 y}{\partial x^2} - \frac{\varepsilon_0 w V^2}{(d-y)^2} + \gamma\frac{\partial y}{\partial t} \qquad \text{(II- 26)}$$

Simplifications of the wave equation (II- 24) can be done in the case of the flexural vibrating structure, considering that the displacement of the structure is limited in comparison with its length. It is also assumed that the flexural effect is dominant compared to the shear deformations and the effect of the rotary inertia, which eliminates the third term of (II- 27) (Bernoulli assumptions). The general expression of the solution is written as

$$y = A\sin(\lambda_n \frac{y}{L}) + B\cos(\lambda_n \frac{y}{L}) + C\sinh(\lambda_n \frac{y}{L}) + D\cosh(\lambda_n \frac{y}{L}) \qquad \text{(II- 27)}$$

Where A, B, C and D are constants determined by the boundary conditions. Taking the initial condition at each end of a CC-beam (II- 26), the resonant pulsation of the structure is expressed as (II- 31).

$$\begin{aligned} &y(0,t) = 0 \\ &\frac{\partial y(0,t)}{\partial x} = 0 \end{aligned} \qquad \text{(II- 28)}$$

The solution of equation (II- 26) follows the general form:

$$y_0 = y(x)\cos(\omega t + \phi) \qquad \text{(II- 29)}$$

The expression of the resonant frequencies for the n Eigen modes is derived from the equation (II- 27), without considering axial load:

$$\omega_n^2 = \frac{\lambda_n^4}{L^4}\frac{YI}{\rho A} \qquad \text{(II- 30)}$$

where Y is the Young's modulus for a narrow vibrating beams and $Y = E/(1-\upsilon^2)$ for a wide vibrating beam (W_{beam} >> H_{beam}). λ_n corresponds to the value associated with the vibration mode shape number (n) [52]. Solutions of the equation (II- 28) give the values of λ_n corresponding to each mode of vibration. Table III shows the values for a CC-beam up to the 4th mode of vibration related to Fig. 20.

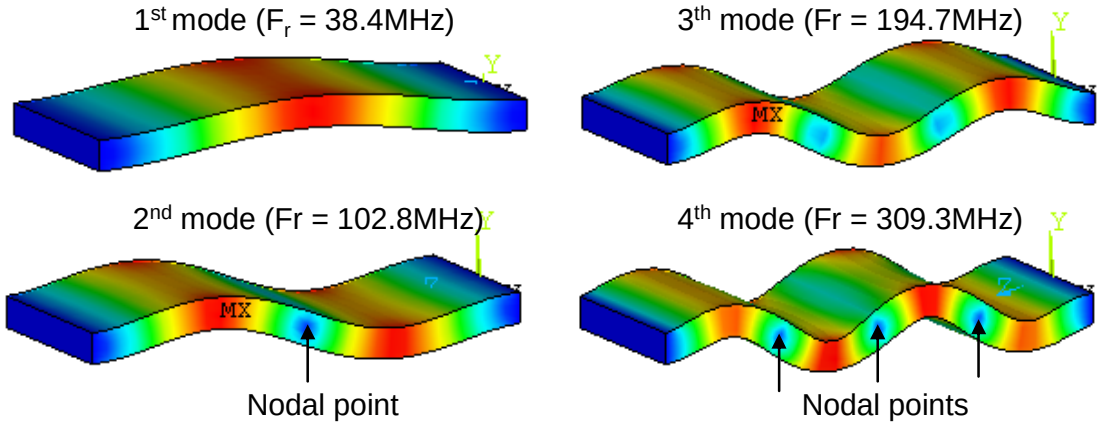


Fig. 20 ANSYS® simulations of vibrating mode shapes on a 15µm long, 1µm thick and 6µm wide polysilicon beam

Geometrie	λ_n values				
	1st mode	2nd mode	3rd mode	4th mode	5th mode
Cantilever	1.8746	4.6928	7.8527	10.9927	14.1335
CC-beam	4.7288	7.8512	10.9928	14.1335	17.2743

Table III. λ_n values related to the vibrating mode shape number for cantilever and CC-beam geometries

II.B.1.a. Nodes on CC-beam

Along a CC-beam length, for a mode shape order greater than one, points along the beam with no displacement are observed (nodal point), see Fig. 20. Nodal points distance from anchors can be calculated from the classical mode shape equation (II- 32) valid for linear amplitude vibrations ([52], [53]), and taking the λ_n values for a CC-beam in Table III.

$$W_{mod\ eshape} = \cosh(\lambda_n \frac{y}{L}) - \cos(\lambda_n \frac{y}{L}) - \alpha_n(\sinh(\lambda_n \frac{y}{L}) - \sin(\lambda_n \frac{y}{L}) \qquad \text{(II- 31)}$$

where $$\alpha_n = \frac{\cosh(\lambda_n) - \cos(\lambda_n)}{\sinh(\lambda_n) - \sin(\lambda_n)} \qquad \text{(II- 32)}$$

For a beam length of 10µm, Table IV defines nodal points for each vibrating modes.

Geometry	Nodal point distance from anchor			
	1st mode	2nd mode	3rd mode	4th mode
CC-beam	No	5µm	3.59µm 6.41µm	2.78µm 5µm 7.22µm

Table IV. Nodal point along the 10µm beam length for each mode shape

High mode shape resonance can be used to achieve higher frequency operation, however the first mode is easier to actuate with a single actuation electrode and allows larger amplitude of displacement which is of benefits to the output current level. For example, considering a uniform cross section of the SG-MOSFET, the resonant frequency of the first vibrating mode, without electro-mechanical coupling [23], is expressed as

$$f_0 = 1.027\sqrt{\frac{E}{\rho}}\frac{H_{beam}}{L_{beam}^2} \qquad \text{(II- 33)}$$

Resonant frequency of a CC-beam in the first mode shape is therefore strongly dependent on the beam dimensions and specifically to its length and thickness. For high frequency resonators, the frequency sensitivity to dimensions, related to the lithographical step, can severely shift the frequency from the expected value. As an example, a variation of 10nm in length on a 6.5µm long and 1µm thick polysilicon beam induces a frequency shift of 800 kHz at 200 MHz (51kHz for a 38.4MHz resonator with similar thickness and 15.1µm length).

II.B.1.b. Effect of stress on the resonant frequency

Stress-induced deposition in thin film also impacts the natural resonant frequency of the resonator. The thin film stress depends exclusively on deposition conditions: gas flow rate, temperature and time (see Chap. III). The global thermal budget during the overall device fabrication process impacts the stress, as well as material doping type and doping level [54]. For CC-beam resonators, in order to control the air-gap between the structure and the substrate, zero-stress or tensile stress is mandatory, whereas compressive stress will induce bucking of the beam.

To model the effect of stress on the resonant frequency, an axial load related to the stress σ and the free vibration operation is considered. The following variable separation and substitution method are used:

$$y(x,t) = \Gamma(x)(A\cos\omega t + B\sin\omega t) \qquad \text{(II- 34)}$$

With $$\Gamma(x) = Ce^{px} \qquad \text{(II- 35)}$$

The equation (II- 26), under damping free and Bernoulli assumptions, and using Laplace transform becomes:

$$p^4 - \frac{\sigma}{YI} p^2 - \rho A \frac{\omega^2}{YI} = 0 \qquad \text{(II- 36)}$$

The new second order auxiliary equation has two distinctive solutions:

$$k_1^2, k_2^2 = \frac{\sigma}{2YI} \pm \sqrt{\frac{\sigma^2}{4Y^2 I^2} + \frac{\rho A \omega^2}{EI}} \qquad \text{(II- 37)}$$

The solution of the differential equation is expressed as:

$$\Gamma(x) = C_1 \cosh(k_1 x) + C_2 \sinh(k_1 x) + C_3 \cos(k_2 x) + C_4 \sin(k_2 x) \qquad \text{(II- 38)}$$

The boundary conditions of the beam are $Y(0, L_{beam}) = 0$ and $\partial^2 Y(0, L_{beam})/\partial x^2 = 0$. Thus the solution must satisfy the equation $\sinh(k_1 L_{beam}) * \sin(k_2 L_{beam}) = 0$, leading to the only possible root: $k_2 L_{beam} = n\pi$ (n is an integer) [53, 55, 56]. The resonant frequency for a thin film having a tensile stress σ can then be written as:

$$\omega_n(\sigma) = \frac{\pi^2}{L_{beam}^2} \sqrt{\frac{YI}{\rho A}} \sqrt{n^4 + \frac{n^2 \sigma L_{beam}^2}{\pi^2 YI}} \qquad \text{(II- 39)}$$

The influence of the stress on resonant frequency is dependent to the vibrating modes and is more important for the first mode. In thin film technology, a stress below 100 MPa is hardly measurable and therefore usually considered as zero stress. However, in terms of resonant frequency accuracy, as shown in Fig. 21, it is shifting the frequency by 450 kHz (1.17%) and up to 2.4 MHz (6.25%) for respectively 100MPa and 500 MPa of tensile stress. The thin film stress should therefore be very well controlled and reproducible to predicatively design resonator with targeted frequencies.

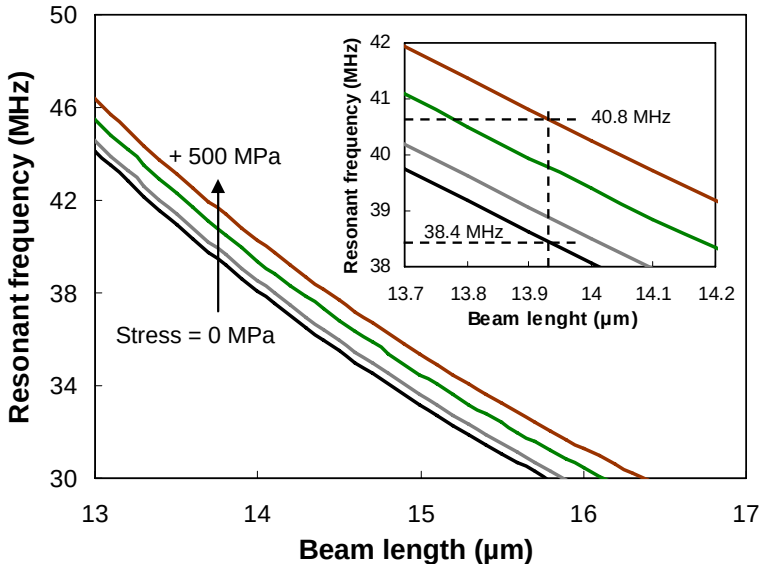


Fig. 21 Simulated resonant frequency shift with tensile stress in the 1µm thick and 6 µm wide silicon resonator

The shift of the resonant frequency is symmetrical for tensile or compressive film stress. However in practice compressive stress induces buckling of the beam and could end up with sticking of the beam to the substrate.

Two conclusions can be drawn with this stress study: stress in the structural layer should be controlled, reproducible, and close to the zero-stress value. Compressive stress has to be avoided because as the beam is buckling up or down, the air-gap distance is not controlled anymore, which has a strong impact on the performances.

II.B.2. General study of non-linearities in a capacitive MEMS resonator

In this part, Newton's approach of dynamic behavior is used for a comprehensive understanding on non-linearities in oscillators. The interest in this section is to look at the impact of non-linearities for the general case of a damped-forced Duffing system. Non-linearities occur in electrostatically actuated MEMS resonators and induce signal distortion in the transmission spectrum. A classical capacitive flexural CC-beam can be modeled more accurately than a standard RLC model by including non-linear terms. These terms are related to a spring whose stiffness varies with displacement and electric field [57]. The non-linear restoring F_k can be expand in series expansion as:

$$F_k(y) = ky + k_1 y^2 + k_2 y^3 + ... + O(y^n) \quad \text{(II- 40)}$$

The damped forced Duffing equation is then expressed up to the third expansion order as:

$$\frac{d^2y}{dt^2} + \frac{\gamma}{m}\frac{dy}{dt} + \frac{k}{m}y + \alpha y^2 + \beta y^3 = \frac{F_\omega}{m}\cos\omega t \quad \text{(II- 41)}$$

Where $\alpha = k_1 / m$ and $\beta = k_2 / m$. Other mechanical non-linear modeling work [51] do not consider the second order term, as it was demonstrated to have no impact on the general non-linear behavior of the resonator. For more clarity however, the full demonstration is done in hereby. To solve equation (II- 41), the Lindstedt's method is used. This technique is looking at the effect of a simple singular perturbation scheme ε to derive the relationship between period and amplitude in the equation [58]. Second and third order of correction can be found analytically by considering an unforced and undamped harmonic oscillator, $y = 0, F = 0$. As the non-linear terms are shifting the resonant frequency, a time constant τ related to the free damping oscillator is set for the shifted frequency.

$$\omega_{shifted}\, t = \tau \quad \text{(II- 42)}$$

Equation (II- 41) is therefore written as:

$$\omega_{shifted}^2 \frac{d^2y}{d\tau^2} + \omega_0^2 y + \varepsilon\alpha y^2 + \varepsilon^2\beta y^3 = 0 \quad \text{(II- 43)}$$

Being non-linear, displacement and $\omega_{shifted}$ can be expanded in power series as:

$$\begin{aligned} \omega_{shifted} &= \omega_0 + \varepsilon\omega_1 + \varepsilon^2\omega_2 + ... + O(\varepsilon^n) \\ y &= y_0 + \varepsilon y_1 + \varepsilon^2 y_2 + ... + O(\varepsilon^n) \end{aligned} \quad \text{(II- 44)}$$

Considering the third expansion order, equation (II- 44) can be written as a set of equations, grouped in powers of ε, where all terms have to be equal to zero in order to satisfy (II- 43).

$$\omega_0^2 \frac{d^2 y_0}{d\tau^2} + \omega_0^2 y_0 = 0 \quad \text{(II- 45)}$$

$$\omega_0^2 \frac{d^2 y_1}{d\tau^2} + \omega_0^2 y_1 + \alpha y_0^2 + 2\omega_0\omega_1 \frac{d^2 y_0}{d\tau^2} = 0 \quad \text{(II- 46)}$$

$$\omega_0^2 \frac{d^2 y_2}{d\tau^2} + \omega_0^2 y_2 + \alpha y_0 y_1 + \beta y_0^3 + (\omega_1^2 + 2\omega_0\omega_2)\frac{d^2 y_0}{d\tau^2} + 2\omega_0\omega_2 \frac{d^2 y_1}{d\tau^2} = 0 \quad \text{(II- 47)}$$

Solution of equation (II- 45) is in the form:

$$y_0 = Y_0 \cos\tau \quad \text{(II- 48)}$$

This solution is introduced into (II- 46), which becomes:

$$\omega_0^2 \frac{d^2 y_1}{d\tau^2} + \omega_0^2 y_1 = 2\omega_0\omega_1 Y_0 \cos\tau - \alpha Y_0^2 \cos^2\tau \quad \text{(II- 49)}$$

The positive term on the right part of the equation will result in a solution where y_1 is growing indefinitely, which is no physical possible as we considered an unforced oscillator. Therefore $2\omega_0\omega_1 Y_0 \cos\tau = 0$, inducing $\omega_1 = 0$.

$$y_1 = \frac{\alpha Y_0^2}{6\omega_0^2}(\cos 2\tau - 3) \quad \text{(II- 50)}$$

The third equation (II- 47) is then combined with (II- 48) and (II- 50)

$$\omega_0^2 \frac{d^2 y_2}{d\tau^2} + \omega_0^2 y_2 = -\left[-\frac{5\alpha^2}{6\omega_0^2}Y_0^3 + \frac{3\beta}{4}Y_0^3 - 2\omega_0\omega_2 Y_0\right]\cos\tau - \left[\frac{\alpha^2}{6\omega_0^2}Y_0^3 + \frac{\beta}{4}Y_0^3\right]\cos 3\tau \quad \text{(II- 51)}$$

To avoid non-physical solution, the term related to the resonance is a zero giving, therefore written as:

$$\omega_2 = \frac{1}{2\omega_0 Y_0}\left[-\frac{5\alpha^2}{6\omega_0^2}Y_0^3 + \frac{3\beta}{4\omega_0}Y_0^3\right] \quad \text{(II- 52)}$$

Considering equation (II- 44), the shift in resonance frequency of a non-linear oscillator in a small oscillations, or damping free assumption [58], is therefore expressed as:

$$\omega_{shifted} = \omega_0 + \kappa Y_0^2 \qquad \text{with} \qquad \kappa = \frac{3\beta}{8\omega_0} - \frac{5\alpha^2}{12\omega_0^3} \quad \text{(II- 53)}$$

According to (II- 53), if β is negative and for any α, the resonant frequency decreases due to the spring softening effect related to the electrical non-linearities. On the other side, the resonant frequency increases for positive β due to the spring hardening effect related to mechanical non-linearities. The resonator displacement amplitude depends upon the quality factor and the beam rigidity. The bifurcation amplitude, defined as the maximal displacement before the non-linearities occur [59], is expressed as:

$$x_b = \sqrt{\frac{\omega_0}{\sqrt{3}Q|\kappa|}} \quad \text{(II- 54)}$$

The maximal beam amplitude at the resonance [60], slightly higher than the bifurcation amplitude is expressed as:

$$x_c = \sqrt{\frac{4\omega_0}{3\sqrt{3}Q|\kappa|}} \quad \text{(II- 55)}$$

Mechanical and electrical non-linearities not only shift the resonant frequency but also induce mechanical and electrical noises [61, 62], which degrades the phase noise in an oscillator system. To avoid these effects while having the maximum detection signal, the resonator should be actuated close to the bifurcation. The biasing voltage should then be defined accordingly.

II.B.3. Mechanical and electrical non-linearities for a CC-beam resonator

In CC-beam architecture, both electrical and mechanical non-linearities can occur, the resulting rigidity expression is function of a mechanical rigidity k_m and an electrical rigidity k_e. The rigidity expression is developed in this part up to the third order term, in order to be consistent with equation (II- 44).

II.B.3.a. Mechanical non-linearities

Mechanical non-linearities correspond to the change of the beam stress due to the elongation, also known as the force-displacement relation. In the case of a CC-beam [57], the non-linear mechanical spring can be approximated as:

$$k_m = k_0\left(1 + \frac{1}{\sqrt{2}H_{beam}^2}y^2\right) \quad \text{(II- 56)}$$

During measurements, mechanical non-linearities are observed on resonators with a very high quality factor, for which the mechanical displacement is important. To dissociate this effect with electrical non-linearities, the biasing polarization should be set to a low value in order to consider the electric field as uniform during the vibration.

II.B.3.b. Electrical non-linearities

Capacitive or electrical non-linearities are derived from the series expansion of (II- 57). The equation was derived up to the second and third order as the most relevant to the non-linear electrostatic coupling. However the second order term has been shown in [63] to be the dominant term.

$$F_{elec} = \frac{1}{2}\frac{\varepsilon_0 A(V_G - V_{G\,\mathrm{int}})^2}{(d-y)^2} = \frac{\varepsilon_0 A(V_G - V_{G\,\mathrm{int}})^2}{d^3}\left(1 + \frac{3}{2d}y + \frac{2}{d^2}y^2 + O(y^3)\right) \quad \text{(II- 57)}$$

This can be related to a negative rigidity of the system as:

$$k_e = k_{e0}\left(1 + k_{e1}y + k_{e2}y^2\right) \quad \text{(II- 58)}$$

$$\text{With} \quad k_{e0} = -\frac{\varepsilon_0 A V_G^2}{d^3}, k_{e1} = \frac{3}{2d},\ k_{e2} = \frac{2}{d^2} \quad \text{(II- 59)}$$

During characterizations, electrical non-linearities are observed when applying a strong DC bias and AC amplitude polarization.

II.B.3.c. Influence of mechanical and electrical non-linearities on the response

The effects of mechanical and electrical non-linearities on the amplitude response are shown in Fig. 22. It is shown that on the frequency spectrum, large displacement amplitude either induces by large electrostatic force or high quality factor create signal distortion. If the amplitude displacement reaches the bifurcation point (x_b), the amplitude-frequency slope becomes infinite. Above that amplitude, in a specific spectrum range, two different amplitudes are possible for the same frequency, resulting in a hysteresis effect. The response is then dependent to the sweep direction and follows the “2” curve (Fig. 22) if the frequency sweep is increasing and the “1” slope is the frequency sweep is decreasing. These effects are shown on measured characteristics in Chapter IV.

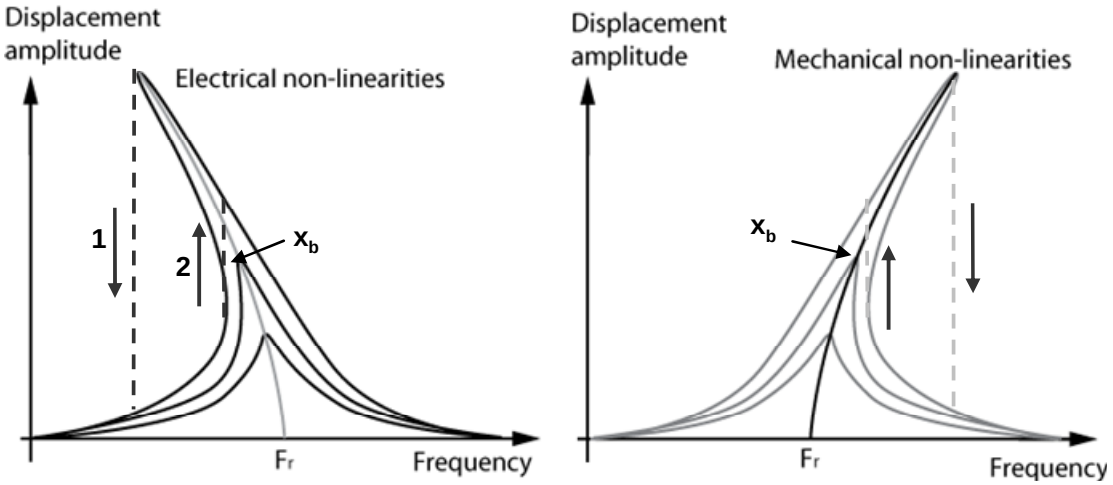


Fig. 22 Schematic of mechanical and electrical non-linearities influence on transmission response

II.B.4. Quality factor

The quality factor is a figure of merit of MEMS resonators and is describes as stored and dissipated energy ratio:

$$Q_{reson} = 2\pi \frac{MaxStoredEnergy}{DissipatedEnergyPerCycle} = 2\pi \frac{W_n}{\Delta W} \quad \text{(II- 60)}$$

Both stored energy and dissipated energy can be optimized to achieve high quality factor.

II.B.4.a. Stored energy in mechanical resonators

The maximum energy stored in an electro-mechanical resonator, before bifurcation is described in [64] and depends of the vibration mode, the resonator mass (density ρ and volume $V_{resonator}$) and the maximum displacement:

$$W_n = \frac{\rho}{8} V_{resonator}\, \omega_n^2 x_{nc}^2 \quad \text{(II- 61)}$$

Fig. 23 presents the relation between the mass of resonators and the quality factor of MEMS resonators reported in the literature. Note that new materials recently appeared for MEMS resonators such as the poly-diamond which has a very high young's modulus, or the poly-SiGe (Silicon-Germanium) used for its low temperature deposition process. The density of these materials differs from the silicon and then modifies the amount of the total energy stored in the resonator. Massive resonators, using extensional (beam [26] and square [25]) or bulk mode (I-bar [65]) resonance can be highlighted from Fig. 23 due to their exceptional quality factor.

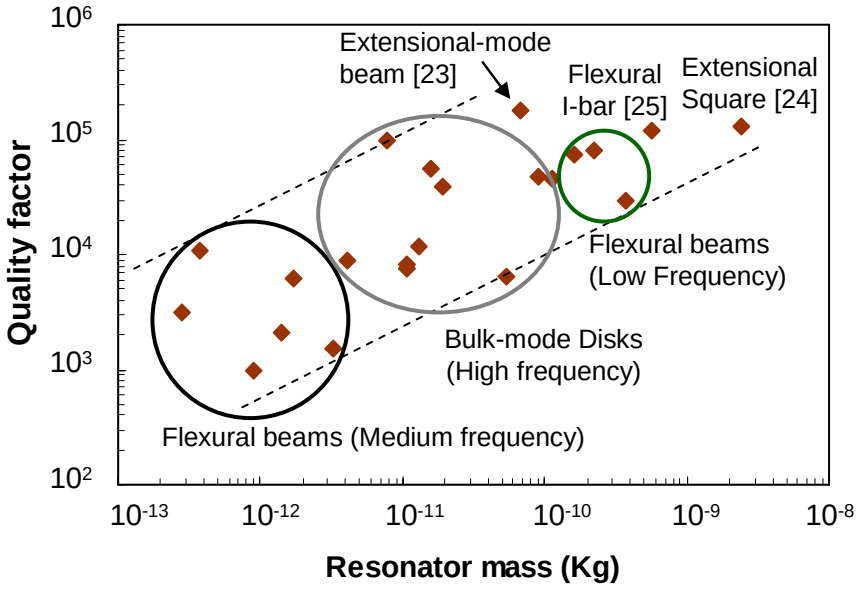


Fig. 23 Graph of the electro-mechanical resonator quality factor relatively to their mass. Medium frequency flexural beams [66, 67], High frequency disks [24, 30, 66], Low frequency flexural beams [1]

This graph disregards resonator anchor geometries and amplitude of displacement, which is greater for flexural beam than for contour-mode resonators. It gives a general trend from which increasing the mass of the vibrating structures, increases the quality factor.

II.B.4.b. Energy dissipation in resonator

Energy dissipations in resonators during vibrations are due to intrinsic structure parameters but also to the environment and are all referred as damping. By looking at the signal transmission through the resonator, the damping induces a lower resonant peak and more insertion losses.

The quality factor can be written as the sum of inversed Q of the thermoelastic, support, coulomb, and gas losses:

$$\frac{1}{Q} = \sum_i \frac{1}{Q_i} = \frac{1}{Q_{thermoelastic}} + \frac{1}{Q_{\sup port}} + \frac{1}{Q_{coulomb}} + \frac{1}{Q_{gas}} \qquad \text{(II- 62)}$$

II.B.4.b.i Structural or thermoelastic damping (TED)

Internal friction during vibration causes energy loss, through heat dissipation, in non-perfectly elastic materials. If the device is considered as a sum of atomic layers, during deformation, layers are subject to different stretching and compression depending on their place, and induce internal friction. The relative motion between particles inside the resonator induces energy dissipation by heating. This loss is more important for resonators with non-perfect atomic structure. For very large structure (macro) it has been shown that there is a phase shift between the applied force and the related displacement [53, 68]. Due to the heat transfer time, loading (heating) and unloading (cooling) cycle follows a hysteretic behavior. In Fig. 24, the hysteresis are represents the total energy loss per cycle.

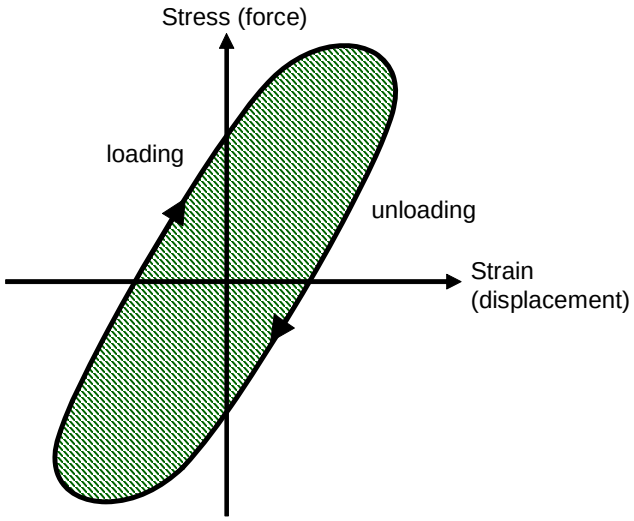


Fig. 24 Hysteretic behavior of the energy dissipation for structural damping due to heat transfer time constant with an elastic material

For micro devices, thermoelastic effect also induces major losses but phase shift effect is neglected due to the small volume for which the heat has enough time to diffuse. However note that this assumption is no valid for high frequency operation above GHz, where intra-crystalline damping occurs. Thermo Elastic Dissipation (TED) has been first modeled by Zener [69] using the Hook's strain-stress relation $\sigma = Y\varepsilon$ in 1D. It describes stress and strain relaxation times (τ_σ and τ_ε) for a material subjects to temperature variations under dynamic operation, and is expressed as

$$\sigma + \tau_\varepsilon \frac{d\sigma}{dt} = Y\left(\varepsilon + \tau_\sigma \frac{d\varepsilon}{dt}\right) \tag{II- 63}$$

A two dimensional model, considering the beam length and thickness, based on the previous relationship has been developed in [69, 70].

$$\frac{1}{Q_{thermoelastic}} = \frac{Y\alpha_T^2 T_0}{C_p \rho}\left[\frac{6}{\varsigma^2} - \frac{6}{\varsigma^3}\frac{\sinh(\varsigma)+\sin(\varsigma)}{\cosh(\varsigma)+\cos(\varsigma)}\right] \tag{II- 64}$$

$$\text{With} \quad \varsigma = H_{beam}\sqrt{\frac{\omega_n \rho C_P}{2\kappa}} \tag{II- 65}$$

where κ is the thermal conductivity (90W/mK for doped silicon and 120W/mK for AlSi1% [48], α_T the thermal expansion coefficient ($2.6\text{x}10^{-6}\text{K}^{-1}$ for silicon and $18\text{x}10^{-6}\text{K}^{-1}$ for AlSi1% at 300°K), C_p the specific heat (713J/kgK for silicon and 938J/kgK for AlSi1%) and Y the Young's modulus considering either thin or wide vibrating beams. Fig. 25 shows the behavior of the thermoelastic loss as function of the operating frequency. The simulation is performed on an AlSi1% and silicon-based flexural resonators both resonating at 38.4MHz but with

different thickness to compensate for their Young's modulus difference (E_{Si} = 160GPa and $E_{AlSi1\%}$ = 49GPa). The beam length and width are respectively 14.1µm and 6µm, whereas the beam thickness is 1µm for the silicon-based structure and 1.65µm for the AlSi1% beam.

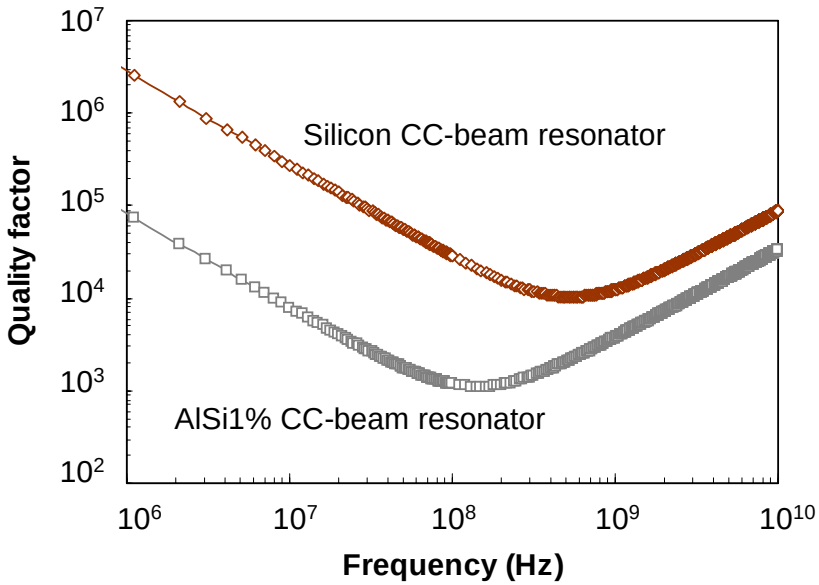


Fig. 25 Simulation of the quality factor limited by the TED for a single crystal doped silicon resonator and AlSi1% resonator at 300°K vibrating at their natural resonant frequencies.

From [71], the frequency for which a minimum Q is reached, for a CC-beam resonator is expressed as:

$$f_{\min Q} = \frac{\kappa\pi}{2\rho C_P H_{beam}^2} \qquad \text{(II- 66)}$$

According to Fig. 25, silicon beam resonator is more suited to achieve high quality factor, and the CC-beam geometry should be limited to medium frequency operation (below 500MHz). The resonator geometry can be optimized to reduce the structural damping by limiting displacement. Structures with less mechanical displacement, such as bulk mode resonators, minimize internal friction and then dissipate less energy than flexural beams counterpart [66].

II.B.4.b.ii Dry friction or Coulomb damping

This damping is related to the fact that friction between two surfaces in contact generates heat losses. For resonator, this heat loss is between the vibrating structure and the surrounding atmosphere. This kind of damping is very small and becomes even negligible by placing the resonator into a vacuum package where particles are rare. The dry friction can be expressed, by using the friction force fN and the amplitude of vibration Y [53]:

$$c_{coulomb} = \frac{4fN}{\pi\omega Y} = Q_{coulomb}^{-1} \qquad \text{(II- 67)}$$

II.B.4.b.iii Gas or viscous damping

Considering a CC-beam with vertical deflection, the effect of gas compression between the resonator and the substrate induces a resistive force opposite to the electrostatic force. The damping force is function of the fluid viscosity, the dimensions of the resonator, the distance between the resonator and the substrate, the frequency of vibration and the velocity of the resonator. Viscous damping has a major impact on quality factor. Two approaches have been developed to model the gas damping:

Viscous flow model - The first one considers the traditional viscous flow model, considering the fluid viscosity in a continuum gas, which is valid in air. In vacuum however the viscous model was derived by considering an effective viscous coefficient instead of a viscosity coefficient in order to model the behavior in rare air. This concept has proven accurate prediction of the quality factor as function of the pressure [72]. This approach however considers that even in very low vacuum, the number of molecules is sufficient to consider that the fluid is viscous, which is physically not truly accurate.

Free molecular model - The other approach is the free molecular model that considers the momentum [73] or energy [74] transfer from the beam to the surrounding air by collisions with molecules. The energy transfer model, which can physically explain the interaction between molecules and the vibrating surface, and considering the effect of nearby actuation electrodes, will be developed.

The number of molecules moving from the environment under the beam boundary area per unit time is expressed in [73] as:

$$N = \frac{1}{2} n_0 v (L_{beam} + W_{beam})(d_0 - y) \qquad \text{(II- 68)}$$

Where n_0 is the concentration of molecules and v the average velocity of the molecules expressed as:

$$v \approx \sqrt{\frac{8RT_0}{\pi M_{mol}}} \qquad \text{(II- 69)}$$

With M_{mol} the molar weight of the gas and R the universal gas constant. The method is to compare the energy of molecules coming under the beam and the energy going out of the beam after collisions with the surface. The difference is due to the energy given by the beam to the molecules. For this we consider:

- The molecule initial velocity in the y direction v_{y0} and the initial velocity in the X-Z direction v_{xz0}
- The time for a molecule to cross the channel between the beam and the substrate: $\Delta t = W_{beam} / v_{xz0}$
- The time needed for one collision in the y direction for a time period, $\Delta C = \Delta t v_{Y0} / 2(d_0 - y)$

Taking the assumption that the molecule gains a speed of 2dy/dt after each collision, the velocity of molecules moving out the beam-to-substrate interface is written as $v_y = v_{Y0} + \Delta C * 2dy/dt$. Then the difference between input molecule kinetic energy $E_{input} = m\left(v_{y0}^2 + v_{xz0}^2\right)/2$ and the output energy is expressed as:

$$\Delta E_{molecule} = \frac{1}{2} m \left[\frac{2W_{beam} v_{y0}^2}{(d_0 - y) v_{xz0}} \frac{dy}{dt} + \left(\frac{W_{beam} v_{x0}}{(d_0 - y) v_{xz0}} \frac{dy}{dt} \right)^2 \right] \quad \text{(II- 70)}$$

Considering a beam excitation following the form $y = Y_0 \cos \omega t$ and combining (II- 69) with (II- 71), the total energy loss for one excitation cycle is expressed as

$$\Delta E_{cycle} = N \frac{1}{\omega} \int_0^{2\pi} \Delta E_{molecule} dt \quad \text{(II- 71)}$$

The resulting quality factor for a rectangular beam and considering that the amplitude of vibration is much smaller than the air gap, combining (II- 71) and (II- 72), is expressed as:

$$Q_{gas} = \frac{2\pi \left(\frac{1}{2} m Y_0^2 \omega^2 \right)}{\Delta E_{cycle}} \quad \text{(II- 72)}$$

$$Q_{gas} = \sqrt{2\pi} \rho_{beam} H_{beam} f_0 \left(\frac{d_0}{W_{beam}} \right) \sqrt{\frac{RT_0}{M_{mol}}} \frac{1}{p}$$

This equation is only valid if there are a small number of molecules in the environment. From equation (II- 70), it can be seen that gas damping is highly related to the frequency of vibration and to the dimensions of the beam and air gap distance. The resulting quality factor for viscous and free molecular energy transfer model on 38.4MHz silicon resonator is shown in Fig. 26.

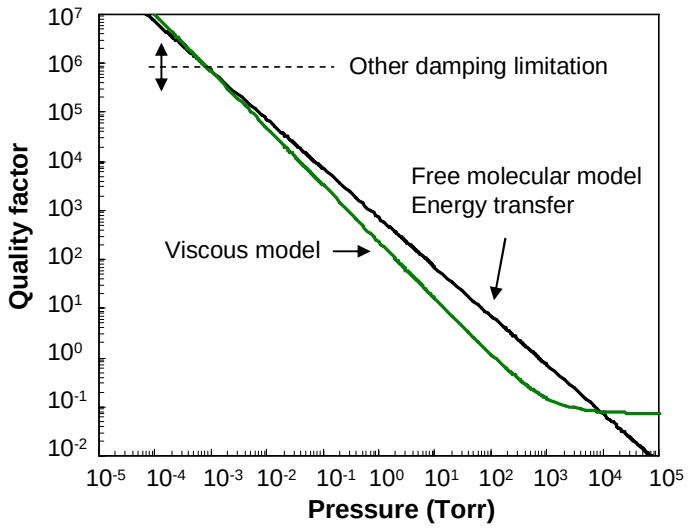


Fig. 26 Simulation of quality factor due to air damping for a 38.4MHz CC-beam silicon resonator (6µm wide, 14.1µm long, 1µm thick) with 50nm air-gap

Viscous model and free molecular model using energy transfer are very similar at very low vacuum. Viscous flow assumption can model the quality factor in the higher pressure region showing the limit for which it becomes constant.

II.B.4.b.iv Support loss damping

Support loss largely impacts the quality factor. It depicts the fact that energy given to the vibrating structure is lost in the fixed anchor. The loss phenomena can be described by the wave propagation theory in the material. Considering a CC-beam anchored at both ends at semi-infinite surfaces made of the same material, the wave propagates the energy generated by the vibration. This energy entering in the anchors is lost for the resonator. To model the effect of support loss, the following assumptions were made, related to the flexural CC-beam architecture:

- When W_{beam} is much larger than H_{beam}, the lateral vibration of the beam is considered as negligible
- At the clamped ends, no displacement occur and the displacement slope is zero
- None of the vibration energy that goes to the anchor reflects and is being re-injected in the beam
- Anchors are considered as semi-infinite plates and their natural frequency of vibration do not impact the beam vibration

The support damping equation for a CC-beam resonator is given in [71], and written as:

$$Q_{anchor} = \varphi_n \left(\frac{L_{beam}}{h_{beam}} \right)^3 \tag{II- 73}$$

where φ_n is the support loss coefficient of the resonator, and values for different vibration modes are gathered in Table V.

Mode 1	Mode 2	Mode 3	Mode 4
0.638	0.223	0.114	0.069

Table V. Support loss coefficient for a CC-beam flexural resonator

It is interesting to note that beam width has no influence on the loss with this resonator architecture, due to the domination of longitudinal wave. The support loss coefficient expression is inversely related to the Poisson's ratio of the structural material but independent of the Young's modulus and amplitude of vibration, if the resonator stays in the linear displacement region. The resulting quality factor for support loss damping on a 38.4MHz silicon resonator and for different vibrating modes, is presented in Fig. 27.

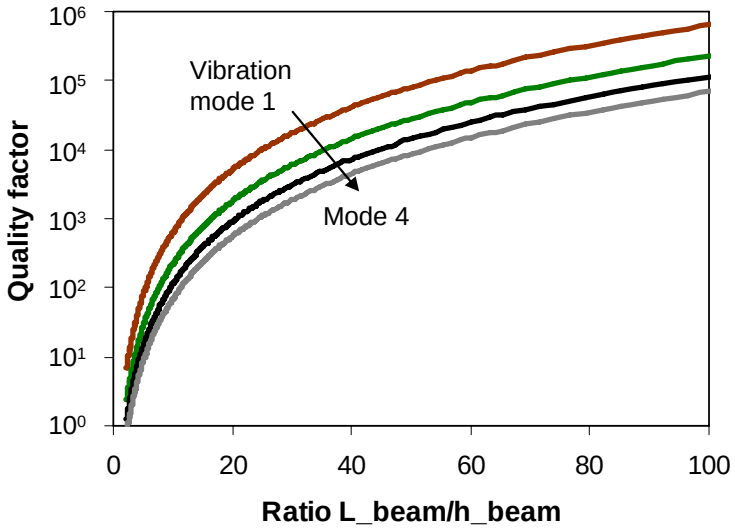


Fig. 27 Quality factor due to anchor loss mechanism for a CC-beam resonator depending on the length-to-beam ratio at 38.4MHz

A method to reduce anchor loss is the use of a free-free beam structure, for which the resonator is anchored at mechanical nodes by thin suspended arms. These arms are vibrating at a quarter wavelength of the resonator to minimize the energy loss and are anchored to the substrate at their ends [23]. The resulting quality factor gain is a factor of 20 as compared to CC-beam at the same frequency.

The previously stated assumption considered a resonator and anchor form with identical material, therefore wave energy going through anchors were lost. However support losses can then be reduced by using different material with different velocity propagation. Such an approach, already used in BAW resonators [12], uses a Bragg reflector composed of stacked layers of different acoustic impedances to reflect part of the energy "lost" toward the resonator. A first attempt to reduce anchor loss on mechanical resonators by using different materials was done on disk resonators [17] made of poly-diamond with a central stem made of polysilicon. The strong difference of acoustic velocity of polysilicon (8000m/s) and poly-diamond (18000m/s) induces a large reflection of incident waves in the central polysilicon beam, limiting the energy propagation in the stem and then increasing the quality factor by a factor of 6 as compared to full polysilicon disk resonator.

II.B.4.b.v Surface loss damping

Contamination at the resonator surface can also cause degradation of the quality factor. Due to absorption and desorption of contaminant molecules at the resonator-gas interface, part of the energy stored in the resonator can therefore be evacuated through these random interface states. Effect of surface losses can be minimized by a passivation heating treatment [75]

II.B.4.b.vi Other source of losses

Other sources of losses have been identified, mainly due to process fabrication. Micro-cracks and roughness on the side of the resonator can appear during resonator patterning [76]. Local high temperature heat treatment insures crystal rearrangement and scalloping reduction [77].

II.B.5. Equivalent electrical circuit model

II.B.5.a. General analysis on pure capacitive resonator

Electrostatic MEMS resonators can be mechanically and electrically modeled by a resonating damped system as shown in Fig. 28, where the analogies between the mechanical rigidity k, the mass m, and the damping μ are respectively the capacitance C_x, the inductance L_x and the resistance R_x [78]. The coupling (gap) capacitance C_{gap} describes the static capacitance between the resonator and the electrode [67].

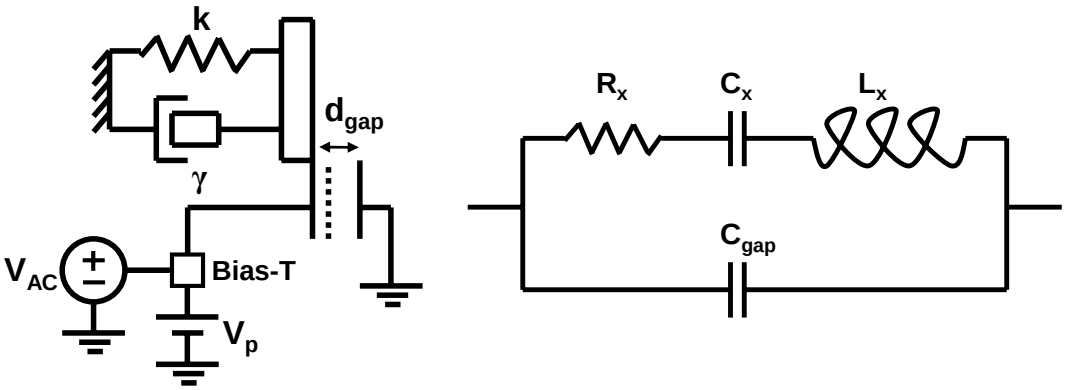


Fig. 28 Schematics of the mechanical and electrical model of an electrostatic resonator

The analogy between electrical and mechanical paramaters can be derived from the transfert function of the dipole (II- 75), where X represents the vibration amplitude.

$$X = \frac{F_{elec} / m_{eff}}{\sqrt{\left(\omega_0^2 - \omega^2\right)^2 + \left(\frac{\omega\omega_0}{Q}\right)^2}} \qquad \text{(II- 74)}$$

The quality factor of the structure is defined as $Q = \omega_0 m / \gamma$ where γ is the damping coefficient. Damping is also described by the factor $c = \gamma / \sqrt{km}$ which is equal to Q^{-1}. In other words, the quality factor represents the number of oscillations of an unforced vibration system before it is completely damped. Considering that the resonator length is composed of multiple elementary blocks, the mechanical displacement of these blocks is different along the beam, due to the anchor boundary conditions. For each of these parts, the kinetic energy should be different, considering that this energy is related to the strain in the material. For a CC-beam, the central deformation at the center of the beam is more important than close to the anchors and therefore kinetic energy is larger at the middle. The notion of effective mass is introduced [52], derived from a ratio of energy ratio and expressed as:

$$m_{eff} = m\frac{Peak\_kinetic\_energy}{\frac{1}{2}v(x)^2} = m\frac{\frac{1}{L_{beam}}\int_0^{L_{beam}}\left[W_{\mathrm{mod}eshape}(x)\right]^2 dx}{\left[W_{\mathrm{mod}eshape}(L_{beam}/2)\right]^2} \qquad \text{(II- 75)}$$

The natural series and parallel resonances frequency of the CC-beam is expressed as:

$$f_S = \frac{1}{2\pi\sqrt{L_X C_X}} \text{ and } f_P = f_S\sqrt{1+\frac{C_X}{C_0}} \qquad \text{(II- 76)}$$

II.B.5.b. Influence of coupling capacitance on signal transmission

The transmitted and reflected signals through the resonator are characterized by a series and a parallel resonance. The series resonant frequency is generated by the resonance of the $R_xL_xC_x$ motional branch. At that frequency f_r, the maximum signal is transmitted and the impedance seen from the output is reduced to the motional resistance R_x. The parallel frequency is generated by the resonance between the coupling capacitance C_0 and the motional branch. In between the two resonances, the impedance of the device is inductive whereas it is capacitive outside the resonances (Fig. 29).

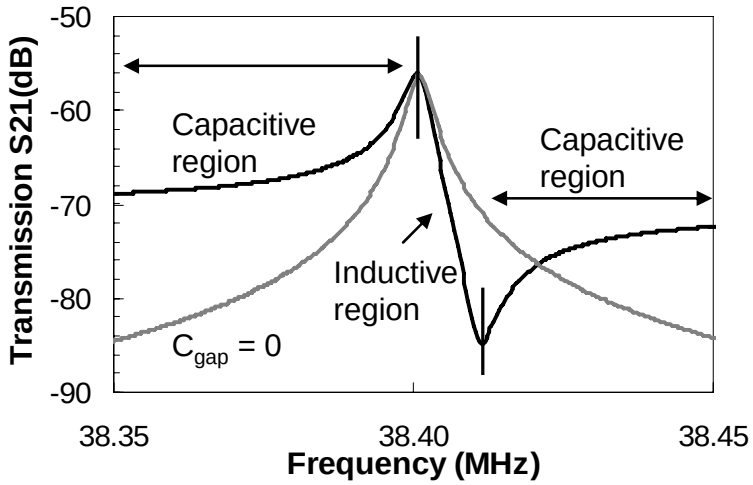


Fig. 29 Simulated transmission of a 38.4 MHz capacitive resonator with 50nm air-gap (black) connected to a 50Ω load, and after removing the direct coupling capacitance C_0 (grey).

II.B.5.c. Influence of coupling capacitance on signal measurement

Typical transmission and phase response at the resonant frequency is shown in Fig. 30 and Fig. 31, where the quality factor clearly influences the signal amplitude. The simulations were done on a 38.4 MHz silicon-based resonator with a beam length, width and thickness of respectively 14.1µm, 6µm and 1µm. The air-gap between the resonator and the actuation electrode is 50nm.

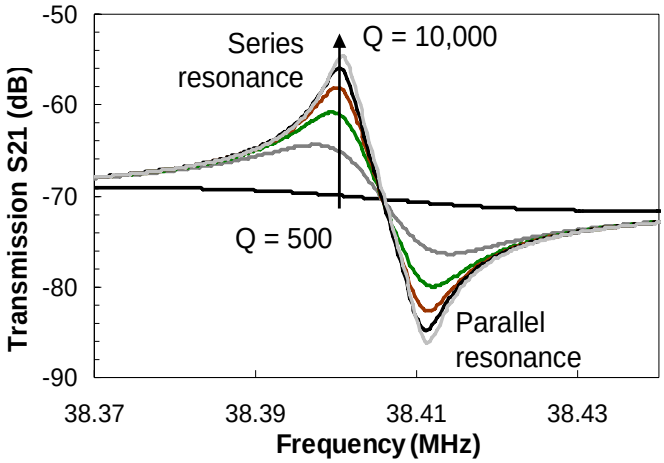


Fig. 30 Transmission response of a 38.4 MHz MEMS resonator using capacitive detection and connected to a 50Ω load. Influence of the quality factor on the amplitude response.

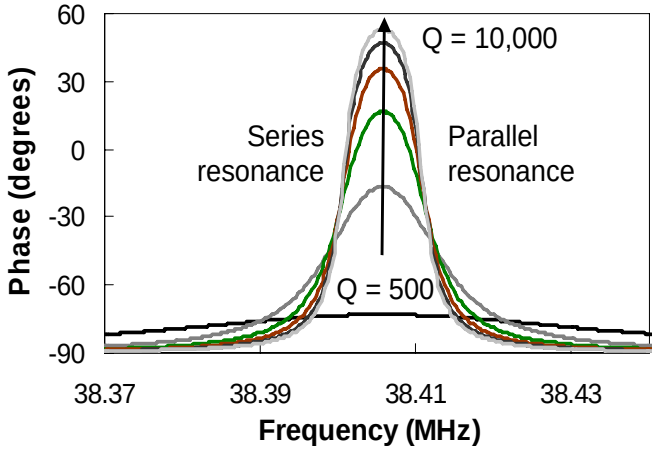


Fig. 31 Phase response of a 38.4 MHz MEMS resonator using capacitive detection and connected to a 50Ω load. Influence of the quality factor on the phase response.

The value of Q can be calculated by dividing either the resonant or anti-resonant frequency by the signal bandwidth at 3dB below the peak, as:

$$Q = \frac{f_r}{\Delta B_{3dB}} \tag{II- 77}$$

Note that outside the resonant frequency bandwidth, damping effect has no influence on the displacement. Therefore, if the resonator is subject to disturbing forces (like environmental or transportation vibrations) with frequencies far below or above the resonant frequency, their impact are negligeable on the resonator response [64]. The electrostatic transduction between the actuation electrode and the vibrating part is related to the quality factor Q as:

$$\mu_0 = \frac{2\pi f_0 m_0}{Q} \text{ and } \eta = \frac{V_p \varepsilon_0 S}{d_0^2} \tag{II- 78}$$

Values of the electrical equivalent circuit are directly derived from the previous relations and are expressed as:

$$R_x = \frac{\mu_o}{\eta^2},\ L_x = \frac{m}{\eta^2} \text{ and } C_x = \frac{\eta^2}{k} \qquad \text{(II- 79)}$$

The motional resistance is strongly dependent on the distance between the resonator and the electrode, to the applied voltage and to the surface of the resonator [79], as expressed in equation (II- 81). In the case of a capacitive transduction and considering small displacement, R_X at resonance can be approximate as:

$$R_x = \frac{k d_0^4}{\omega Q V_p^2 (\varepsilon_0 W_{beam} H_{beam})^2} \qquad \text{(II- 80)}$$

In reference oscillator design, the motional resistance has to be compensated by the gain of an amplifier; therefore resonator design has to be optimized to minimize R_x. Few parameters can be optimized while keeping the same resonant frequency:

- The air-gap d_0 between the beam and the actuation electrode can be reduced. This technique is most efficient technique previously used to lower the motional resistance
- Quality factor Q should be maximized (developed in II.B.1.d)
- Surface S of the resonator should be maximized by either using large structures or a coupled-resonator architecture [80]
- Increase the applied polarization voltage V_p

The transmission response amplitude strongly depends on the motional resistance. The amplitude response is more important for a small air-gap (Fig. 32), which is in line with the reduction of the motional resistance.

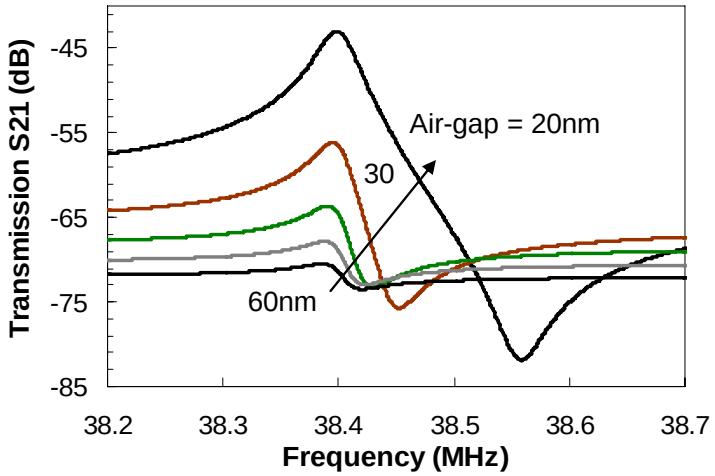


Fig. 32 Simulated transmission amplitude response of a 38.4MHz resonator for various air-gap distance

The motional current of a capacitive transducer is proportional to the modulation of the capacitance between the resonator and the actuation electrode, and depends on the beam displacement. The expression of this current, considering a harmonic displacement of the beam ($y(t) = Ye^{j\omega t}$) is:

$$I_m = -V_P \frac{\partial C_{gap}}{\partial x}\frac{\partial x}{\partial t} = -j\omega\eta Y \qquad \text{(II- 81)}$$

At the mechanical resonance, the maximum displacement is determine by the Hookes' law [64] and is expressed as:

$$Y(\omega_0) = \frac{F_{elec}Q}{k} = \frac{\eta V_G Q}{k}. \qquad \text{(II- 82)}$$

The resulting maximal motional current is:

$$I_m(\omega_0) = \frac{\omega_0 Q V_G \eta^2}{k} \qquad \text{(II- 83)}$$

The electrical equivalent circuit of Fig. 28 is used as input for circuit design. Values of the equivalent circuit are however very different from those of the quartz as shown in Table VI.

	Quartz	MEMS disk resonator [81]	MEMS CC-beam resonator [82]	MEMS comb-drive resonator [83]
R_x	50Ω	25KΩ	17.5KΩ	500KΩ
C_x	0.04pF	4aF	0.3fF	0.5fF
L_x	0.25H	0.23H	0.83H	200kH

Table VI. Typical equivalent circuit values for quartz and MEMS resonator

The strong impact of these values on the circuit design of MEMS-based oscillators is developed in Chap. IV.

II.B.5.d. Resonator with MOSFET detection

The resonator with MOSFET detection has a different small signal electrical equivalent model than for the capacitive detection (Fig. 28). The vibrating gate and the air-gap capacitance can be modeled by a RLC series branch in parallel with the air-gap capacitance, coupled with the small signal MOSFET analysis to account for the transistor gain, as shown in Fig. 33.

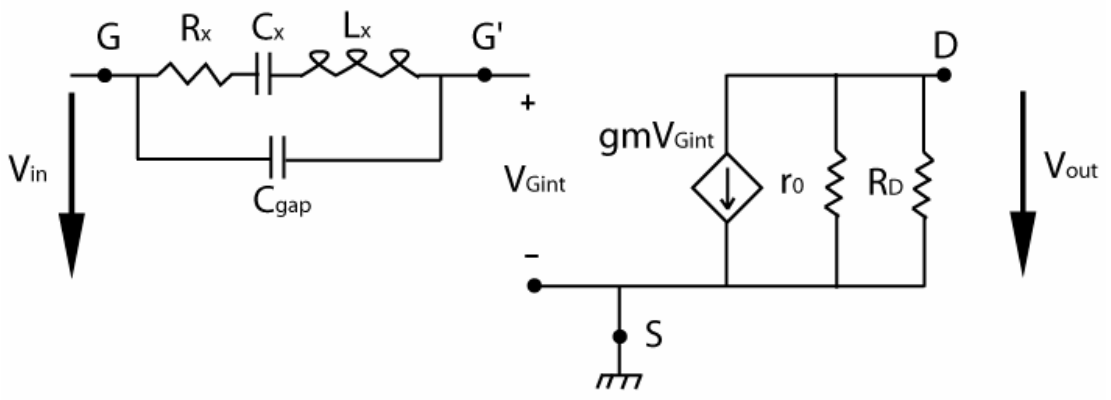


Fig. 33 Small signal equivalent model of a RSG-MOSFET

The transfer function of the small signal equivalent MOSFET, taking into account the drain access resistance R_D is:

$$\frac{V_{out}}{V_{G\,\mathrm{int}}} = -gm(R_D \,//\, r_0) \qquad \text{(II- 84)}$$

For the high frequency response of the equivalent circuit, the gate-to-source C_{GS} and the gate-to-drain C_{GD} capacitances should be added to the model. The total capacitance, according to the Miller's theorem [84], is then written as:

$$C_{eq} = C_{GS} + C_{GD}(1 + gm(R_D \,//\, r_0)) \qquad \text{(II- 85)}$$

This equivalent capacitance together with the input signal-source resistance (50Ω for a network analyzer and an impedance analyzer) creates a low-pass filter. The high-frequency pole is then written as:

$$\omega_{pole} = \frac{1}{C_{eq} R_{input}} \qquad \text{(II- 86)}$$

In the case of the RSG-MOSFET, due to the presence of air-gap between the gate and the channel, the C_{GD} and C_{GS} capacitances are small (in the order of 0.5fF for a resonator with 300nm air-gap and a beam length of 15µm). The filter pole is then much higher than the resonant frequency of the beam and does not cut-off the transmitted signal.

II.B.5.e. Comparison between capacitive and MOSFET detection

The comparison of the two detection techniques was carried out on CC-beam resonators, by varying the beam width (equivalent to a MOS channel length) and systematically calculating the maximal output current, as shown in Fig. 34. Simulations were performed with the previously developed analytical model, taking a silicon-based resonator with width and thickness of respectively 48µm and 500nm. An arbitrary quality factor of 1000 was used for the simulation, but in line with the damping analysis of part B.4. It is clearly shown in Fig. 34 that the drain current increases with the reciprocal of the beam width. In other words, the MOSFET drain current is higher for a shorter channel length, due to the MOS amplification effect. For small surface area, the capacitive output current is smaller than the MOS drain current but increases linearly with larger beam width. A critical value in which we have identical maximum output current for the two techniques occurs in this device architecture for a beam width of around 30µm. As high frequency operation is targeted for MEMS resonators, dimensions of the beam have to be reduced to stiff the resonator and increase the natural resonant frequency. The resonator scaling has therefore a positive influence on the MOSFET detection current.

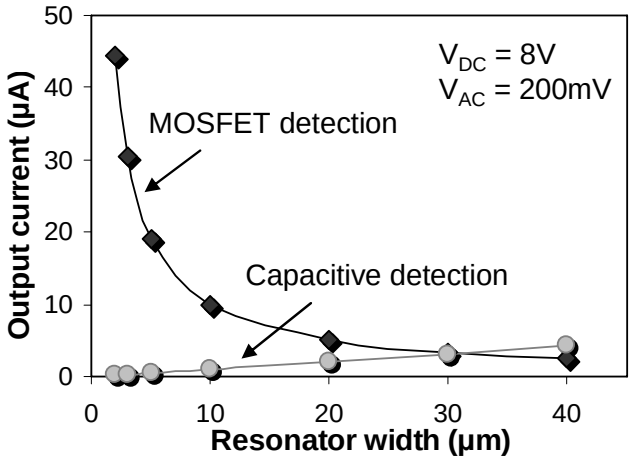


Fig. 34 Comparison of the simulated peak current for capacitive and MOSFET detections at different beam width, for a gate oxide thickness of 10nm and an air-gap size of 200nm

The peak-to-peak current amplitudes for the capacitive and MOSFET resonators are gathered in Table VII. The MOSFET detection shows a more important current variation than capacitive detection when scaling.

Beam width (channel length)	1µm	5µm	10µm	30µm	40µm
Capacitive peak-to-peak current (µA)	0.01	0.06	0.14	0.5	0.68
MOSFET drain peak-to-peak current (µA)	13.7	3.67	1.98	0.7	0.54

Table VII. Peak-to-peak current amplitude for the capacitive resonator and RSG-MOSFET described in Fig. 34

II.C. RSG-MOSFET model for circuit design

Analytical models can only be implemented in standard circuit simulator such as SPECTRE® on CADENCE® or ELDO® by using a specific Verilog-A coding language. Requirements for circuit design are that the device model has to describe all MOSFET operation regions, and includes specific effects as transient current and electron velocity saturation effects.

Dynamic modeling of the RGS-MOSFET was developed based on vibrating equations described in section B.4 and the EKV model for the MOSFET detection [85]. EKV transistor model is valid for all operating regions including weak inversion, moderate inversion, and strong inversion in linear and saturation regions. The model used for DC applications in section A.1 was only valid in linear region. The EKV model uses the intrinsic symmetry observed in a MOSFET transistor and considers the different drain, source and gate voltages referred to the local substrate. It uses the charge description in the material to express the current flow in the device.

The particularity of the EKV model as compared to other model such as SPICE, are:

- Low number of parameters, and most of them are physical
- Continuous expression of current and capacitances

The RSG-MOSFET symbol was created on the Cadence® environment in order to instance it in circuit diagrams (Fig. 35). The different pins are connected to nodes in the Verilog-A codes and voltage and current input/output at each of these nodes are dependent to the analytical expressions of the drain, source, bulk and gate charges. The model was fully functional on SPECTRE® and ELDO® simulators.

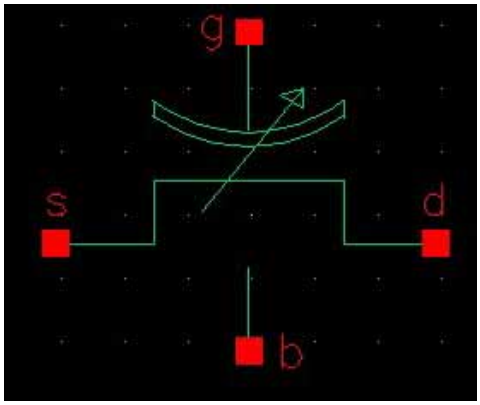


Fig. 35 RSG-MOSFET instance symbol for Cadence®

A second analytical model was developed for capacitive MEMS resonators and used in circuit to design an oscillator. The impact of the capacitive and MOSFET detection for circuit application is developed in Chapter IV.

II.D. Modeling perspectives of the Resonant SG-MOSFET

A static and dynamic model of a CC-beam resonator with MOSFET detection was developed and accounts for electro-mechanical linear and non-linear phenomena occurring in this device. Equivalent small signal electrical circuits were developed for capacitive resonators and RSG-MOSFET. Modeling tradeoffs between the resonant frequency, the output signal amplitude, the motional resistance and the quality factor were explained in this chapter.

The influences of various SG-MOSFET design (airgap, oxide thickness, gate width and length, gate area, beam shape during deflection) and mechanical (stiffness) parameters have been investigated through simulation based on analytical modeling. It might be concluded that by a smart choice of the dimensions, one can design a SG-MOSFET device that operates as switch (pull-in voltage) in a low voltage region (<5V), compatible with integrated circuit voltage supply. In contrast, the design window for a resonator application is different and rather targets higher stiffness (resulting in high pull-in voltages).

It was essentially demonstrated that, when the size of the suspended gate is scaled down, the MOSFET detection (associated to the resonator application) provides a much higher output current than the capacitive detection, which suggests the use of this device architecture for scaled devices (in principle, corresponding to high frequency applications).

The modeling perspectives for quasi-static and dynamic operation are:

Quasi-static modeling: The trends towards miniaturization of resonator and mechanical switch, makes the effect of nanoscale forces in vacuum or air environment more important and sometimes dominating the electrostatic force. Other source of nanoscale effects can be investigated in a next phase, such as adhesion forces when the beam is collapsed on the substrate, or effect of electrostatic fringing field which could modify the gate actuation.

Dynamic modeling: Loss mechanisms in vibrating structures were studied with a more specific focus on the CC-beam architecture, showing that support loss and thermoelastic damping are dominant. Further investigations on loss mechanisms on other resonator architecture, such as disk or lamé mode are currently under investigation in order to achieve the required high frequency operation for MEMS resonators [86]. The effects of mechanical and electrical non-linearities on oscillator amplitude-induced noise and on phase noise in an oscillator loop are also a major research area and represent a bottleneck to introduce MEMS resonators in the market [60, 87].

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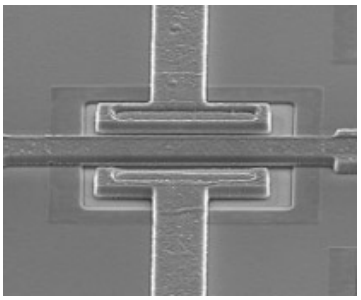
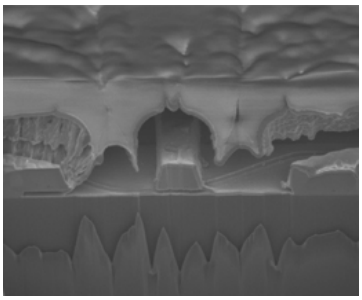
Chapter III

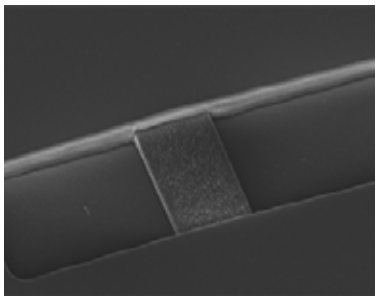
SG-MOSFET fabrication processes



SEM picture of AlSi-based RSG-MOSFET
(Scale: CC-beam of 30x6µm^2)



FIB cross section of an encapsulated RSG-MOSFET with a 0-level thin film packaging
(Scale: 4.5µm thick SiO_2 membrane)



SEM picture of a silicon-based RSG-MOSFET before releasing
(Scale: CC-beam of 15x6µm^2)

Introduction

This chapter describes the different processes developed to fabricate and optimize the SG-MOSFET. A metal-based SG-MOSFET process, derived from a previous technology used for RF-MEMS passives [5], was developed as a test vehicle to demonstrate the SG-MOSFET concept in DC and RF operation. It is a non self-aligned MOSFET process using an AlSi% suspended-gate. Polyimide and polysilicon sacrificial layers were investigated. The process is based on four masks and one Chemical and Mechanical Polishing (CMP) step.

A silicon-based suspended-gate process was developed on Silicon On Insulator (SOI) wafers to optimize the SG-MOSFET performance. The innovative process uses the silicon dioxide of the SOI wafer as sacrificial layer and the gate oxidation is performed on an already released structure. The process is a MOSFET self-aligned and the air-gap between the beam and the channel is controlled by the thickness of the Bulk Oxide (BOX) of the SOI. The process is based on seven masks.

SG-MOSFET resonators, switches and memories must be placed in a vacuumed environment to achieve high performances and to avoid any degradation of the MOSFET. A 0-level vacuum packaging process based on thin film deposition above released resonator was demonstrated [89].The packaging process is compatible with both the suspended metal-gate and the silicon-gate MOSFET processes. The packaging is a two mask process on top of an already suspended SG-MOSFET

In parallel with this process effort at the EPFL, a front-end compatible process was developed for industrial environment and critical technological blocks were demonstrated at STMicroelectronics. The process is very compact and based on one mask and one CMP step after the classical Silicon Trench Isolation (STI) steps used to isolate the transistors from each other.

III.A. Metal-based SG-MOSFET process

III.A.1. Process description

The process is based upon a technology developed for RF MEMS passives [5], compatible with above-IC CMOS integration. From this base, an innovative process was developed to combine MOSFET with MEMS resonators fabrication. Two different sacrificial layers were investigated for two applications: polysilicon layer for MEMS resonators and polyimide layer for MEMS memory. The fabrication process is composed of four masks and includes one CMP (Chemical Mechanical Polishing) step, as shown in Fig. 36.

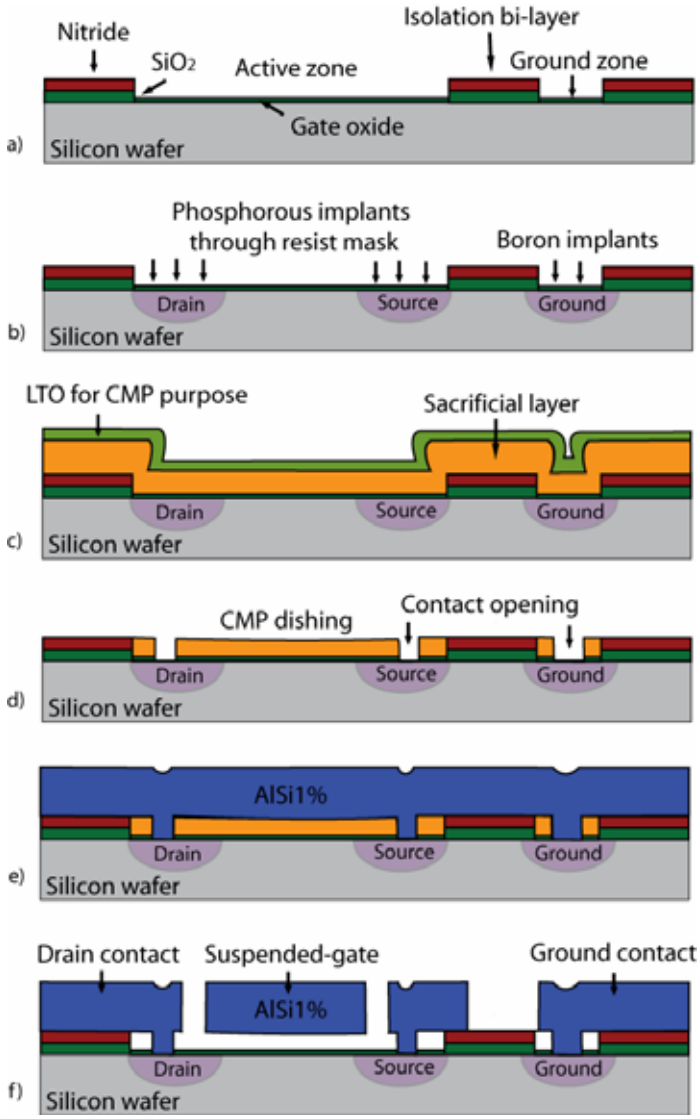


Fig. 36 Schematic of the fabrication process steps of an AlSi-based SG-MOSFET

III.A.1.a. Active zones definition and silicon dry oxidation

A wet oxidation was used to grow a 100nm silicon dioxide layer at a temperature above 900°C, using a Centrotherm® equipment. An hydrox system composed of a torch fed with O_2

and H_2 creates a water vapor which is flown in a furnace and reacts with the silicon to create SiO_2 and volatile hydrogen according to the following formula.

$$Si + 2H_2O \rightarrow SiO_2 + 2H_2 \quad \text{(III- 1)}$$

A silicon nitride layer was deposited by LPCVD (Low Pressure Chemical Vapor Deposition). A dichlorosilane gas is flown in the furnace at temperature above 700°C and mixed with ammonia to react with the silicon according to formula (III- 2). The resulting HCl and H_2 gases are volatile.

$$3SiCl_2H_2 + 4NH_3 \rightarrow Si_3N_4 + 6HCl + 6H_2 \quad \text{(III- 2)}$$

Active zones were then dry etched (Alcatel 601E®) through the SiO_2-Si_3N_4 isolation bi-layer (Fig. 36a). The height of isolation layer will define the air-gap of the suspended-gate, as the structure will be anchored on both sides of this layer. Different splits on isolation layer thickness, from 200nm to 500nm, have been fabricated in order to evaluate the impact of the air-gap on the SG-MOSFET behavior. A thermal gate oxide was grown in the active zones with splits from 20nm to 60nm. The thermal dry oxidation of the silicon created under an oxygen gas flow at temperature above 900°C, according to the equation (III- 3).

$$Si + O_2 \rightarrow SiO_2 \quad \text{(III- 3)}$$

During this process, part of the silicon is consumed at a rate of 0.44 times the total SiO_2 thickness. Compared to PECVD (Plasma Enhanced Chemical Vapor Deposition) SiO_2 deposition, the dry oxidation process is slow but results in a very dense and pure material, with a very low number of contaminants.

III.A.1.b. Source and drain implantation

Source and drain were photolithographically defined and a thick photoresist mask was used to implant through the thin gate oxide. A $2x10^{15}$ at/cm^3 phosphorous dose at 35keV was used to highly uniformly dope the silicon bulk at $1.2x10^{20}$ at/cm^3 on 200nm depth (Fig. 36b). A second masking step was used to implant Boron to define the ground contact. Silicon surface amorphization is avoided by implanting through the thin thermal oxide layer. Diffusion annealing at 900°C during 5 minutes rearranges the atomic structure of the silicon to include the dopant in the mesh and therefore creates sites with excess of electrons (N-type phosphorous doping), or excess of holes (P-type boron doping).

III.A.1.c. Polysilicon sacrificial layer

A critical step on this process is to precisely control the gap between the gate and the channel, which is achieved by controlling the sacrificial thickness and uniformity on the wafer. A 500nm LPCVD polysilicon layer was deposited (Fig. 36c). The polysilicon is deposited by the chemical reaction of a silane gas adsorbed at the wafer surface which then separates to create silicon and hydrogen, as described in formula (III- 4).

$$SiH_4 \rightarrow Si + 2H_2 \quad \text{(III- 4)}$$

Polysilicon material was used as sacrificial layer due its good conformal deposition and etching selectivity over the AlSi and dielectric materials. It has been shown that a high selectivity over the AlSi can be obtained by using pure isotropic chemical SF_6 plasma [90].

III.A.1.d. Polyimide sacrificial layer

A polyimide (PYRALIN PI2610) sacrificial layer was also investigated due to its good etching selectivity to the AlSi and the dielectric layers. The polyimide is usually etched under an oxygen plasma. Polyimide is also resistant to temperature up to 400°C. In order to optimize the sacrificial layer thickness to control the air-gap, polyimide thickness should be in the order of twice the isolation layer thickness. Polyimide is a relatively viscous material, for which thickness of 2µm is achieved with a standard spinning speed of 4000 rpm (rotation per minute) (Fig. 37). Thinning of the polyimide is done by dilution with the Pyralin® T9039 thinner to obtain layers from 200nm to 1µm depending on the dilution ratio, as shown in Fig. 37.

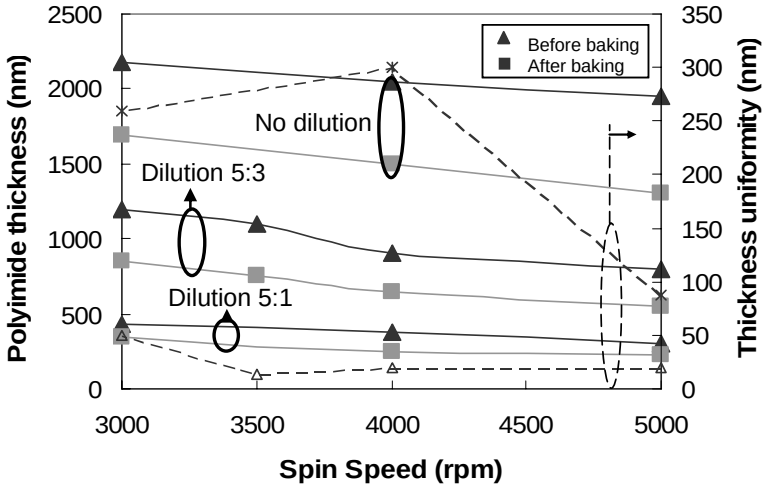


Fig. 37 Polyimide thickness versus spin speed for various dilution ratios (left axis – continuous line) and thickness uniformity over the wafer (right axis - doted line)

Increasing the spinning speed above 4000 rpm has a positive impact on thickness control and uniformity over the wafer. A thickness uniformity of 3.3% is achieved for a spinning speed of 5000 rpm with a dilution ratio of 5:3. Tests were made with a fixed spinning time of 30 seconds. Optimal result for the SG-MOSFET in terms of thickness and uniformity was obtained for a 5:1 dilution ratio. Polymerization of the polyimide under N_2 atmosphere using two curing steps (200°C/1h and 300°C/1h) stabilizes the material while making it harder. Annealing process reduces the total polyimide thickness by one fourth.

III.A.1.e. CMP of polyimide and polysilicon sacrificial layers

Chemical Mechanical Polishing (CMP) step is critical to flatten the sacrificial layer in order to have a flat resonator structure and then limit energy loss through thermo-elastic dissipation due to stress concentration in the non-flat parts of the resonator. The CMP is a mechanical abrasion of the wafer surface combined with a reaction with a chemical substance. The mechanical abrasion is done by putting in contact the wafer, placed on a rotating head, with a large rotating pad wetted in an abrasive chemistry called slurry:

- The chuck and the pad rotating speed are set separately in order to control the mechanical polishing rate as well as the pressure applied from the head to the pad. The controlling parameters are the work pressure (in psi, pound-force per square inch = 6.89kPa), the pad speed and the head speed (in rpm, rotation per minute). The CMP uniformity depends on the density of area to polish and on geometry of the polished parts.
- The slurry is composed of colloidal silica particles of 50nm diameter diluted to 30% concentration with a basic or neutral chemistry. A very basic chemistry composed of ammoniac is used for the polysilicon CMP, which reduces the roughness and facilitate the mechanical abrasion and a neutral chemistry is used for polyimide CMP.

In order to avoid dishing in the sacrificial layer a 200nm of oxide was sputtered at room temperature followed by two steps of CMP (Steag Mecapol E460). A first 3min step using the 7psi/35rpm/30rpm parameters (work pressure/ pad speed/ head speed) were used to eliminate the oxide and remove the active region holes. A second CMP of 2min at low pressure (4psi/35rpm/30rpm) removed non-desired polyimide. This technique allowed a sacrificial layer thickness control of around 5% over the wafer, as seen in Fig. 38.

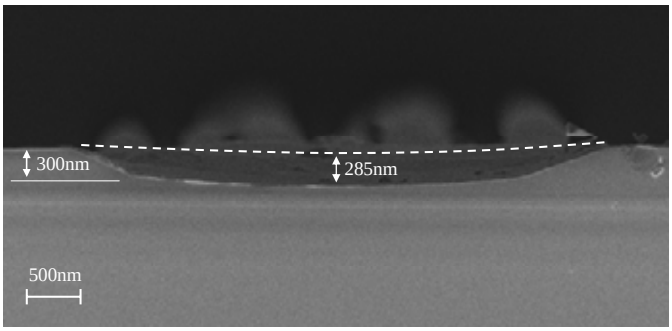


Fig. 38 Cross section of a polysilicon refilled active zone after the CMP steps

III.A.1.f. Contact and structural layer

Polysilicon sacrificial layer: the source and drain contacts were patterned (Alcatel 601E®) through the polysilicon in mixed C_4F_8 and SF_6 plasma [91]. The SF_6 gas produces fluorine radicals which associate with the silicon to create volatile molecules, according to equation (III- 5)

$$Si + 4F \rightarrow SiF_4 \qquad \text{(III- 5)}$$

In parallel, the C_4F_8 dissociates and creates a passivation layer on the silicon by a polymerization process (polymeric fluorocarbon C_nF_k [92]). The passivation is directly etched on the bottom of the cavity by the ions bombardment but stays on the sidewalls and prevents the silicon lateral etch. The thermal gate oxide is etched with a C_4F_8 plasma (Fig. 36d) which reacts with the SiO_2 to create volatile molecules (SiF_4, SiF_2, CO_x, COF_2) and fluorocarbon polymers, which are also used to limit lateral etching, even if the SiO2 etching is naturally anisotropic due to the need of ions.

Polyimide sacrificial layer: the source and drain were patterned by an anisotropic oxygen plasma etching (TEPLA 300®), due to the polarization of the substrate holder that directs the

flow of ions perpendicularly to the substrate. The gate oxide etching is done by an anisotropic C_4F_8 plasma etching to open the contacts through the 20-to-40nm thermal oxide and therefore access the doped silicon.

III.A.1.g. Metal-gate layer

The suspended-gate is made of an aluminum-silicon film alloy (AlSi 1%). The 1.8µm thick structural layer is deposited by sputtering (Pfeiffer vacuum Spider-600®) under high vacuum with a 20 kHz, 2000 W pulsed-DC conditions (Fig. 36e). Pattern of the metallic layer was done with chlorine-based plasma (STS Multiplex ICP®) at an etching rate of 500nm/min selectively stopping on the silicon nitride film (Fig. 36f). During the plasma, the chlorine reacts with the aluminum to create $AlCl_3$ volatile molecule [93]. The AlSi etching recipe used in this process shows a higher selectivity over the silicon nitride than for the silicon dioxide, which explains the use of a nitride-based top isolation layer. In terms of isolation however, SiO_2 has a lower dielectric constant (ε_{ox} = 3.9) than Si_3N_4 ($\varepsilon_{nitride}$ = 7.5) which justifies the use of the SiO_2-Si_3N_4 isolation bi-layer.
AlSi1% material was chosen to lower the contact resistance between the Al-based metal layer and the doped silicon. Indeed, using pure aluminum in contact with the doped silicon, the silicon diffuses in the Al, therefore allowing the aluminum to rearrange in the former silicon regions. Due to the presence of non-uniform native oxide at the silicon surface, the diffusion is random and begins where oxide is thinner. If the silicon diffusion length is larger than the p-n junction depth, the junction is short-circuited. The silicon diffusion in aluminum is saturated at 1% of silicon; therefore AlSi1% deposition is suited to avoid silicon diffusion and lowers the contact resistance. According to the previous statement, the use of AlSi4% for the metal gate should be only motivated by its larger tensile stress.

III.A.1.h. Releasing step

Polyimide sacrificial layer: the etching uses oxygen plasma fully selective with AlSi layer and thermal oxide but introduce large number of defects in the gate oxide. The polyimide etching was done with a 2.45 GHz, 400W oxygen plasma (TEPLA 300®). The etch rate is strongly dependant to the chamber temperature and can vary from 200nm/min to 1µm/min (at 100°C).

Polysilicon sacrificial layer: the etching uses a pure isotropic SF_6 plasma with an etch rate of 5µm/min. By Comparison with the process used for anisotropic polysilicon etch (A.1.f), the polymerization is avoided by the absence of C_4F_8 gas. The unwanted etch of the gate oxide is limited to 2nm/min. The PolySi:SiO_2 selectivity of this process is therefore 2500:1.

A released RSG-MOSFET structure, fabricated with a polysilicon sacrificial layer, is presented in Fig. 39a, showing a 220nm air-gap over a 40nm gap oxide (Fig. 39b).

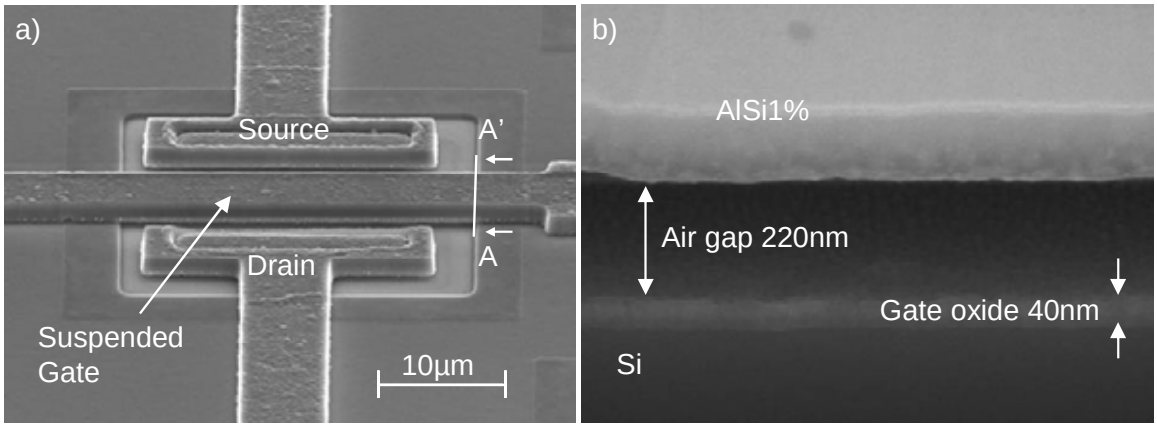


Fig. 39 a) SEM picture of a released CC-beam SG-MOSFET fabricated with a polysilicon sacrificial layer, b) FIB cross section along the AA' line

III.A.2. Structural layer stress investigation

III.A.2.a. Stress measurement technique

Stress on thin films was investigated based on wafer curvature and Guckel ring structure [94]. Wafer curvature measurement is done by scanning the surface with a laser beam and the light reflection intensity or phase is measured (TENCOR FLX 2900). Silicon wafers are pre-stress by depositing a 2µm thick oxide using a wet oxidation process. Wafer curvature is measured before and after the AlSi thin film deposition. Due to the change in curvature after deposition, the intrinsic stress of the film can be deduced, using the Stonley's formula (III- 6). This equation yields a reasonable estimation of the stress in the thin film, considering the film thickness t_f much smaller than the substrate thickness t_s.

$$\sigma_f = \frac{E_s}{6(1-\upsilon_s)} \frac{t_s^2}{t_f} \left(\frac{1}{R_{sf}} - \frac{1}{R_s} \right) \qquad \text{(III- 6)}$$

where E_s and υ_s are respectively the substrate Young's modulus and Poisson's ratio, R_s and R_{sf} the measured curvature radii before and after film deposition. The accuracy of the film stress measurement is about 10%. A better accuracy can be obtained for small radius of curvature equivalent to highly stressed thin film.

III.A.2.b. Residual stress and characteristic on Al-based film

In order to control the resonator-to-channel air-gap, suspended-gate has to show a tensile stress. Various room temperature sputtered Al-based material have been investigated to evaluate the impact of silicon concentration on film stress: Al, AlSi1%, AlSi4%. Fig. 40 shows that the three different films exhibit a tensile stress varying from 68MPa to 99MPa after an annealing.

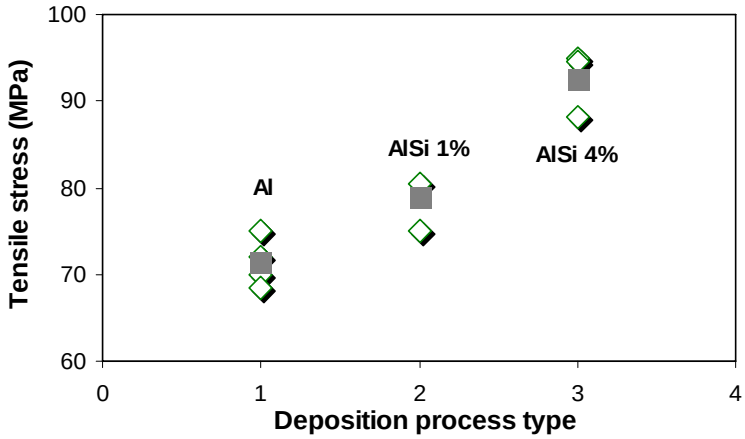


Fig. 40 Stress measurement of different thin films after annealing at 440°C (diamond-shaped points are related to wafers measurement, squares are the mean stress values)

Annealing process is needed to reduce contact resistance between the metal and the doped silicon region. Annealing is done at 440°C under gas composed of 5-10% of hydrogen and 90-95% of nitrogen. Nitrogen is used to avoid reaction between oxygen and the metal which creates aluminum oxide, and hydrogen is employed to remove defects on surface, specially pending silicon links at the SiO_2/Si interface. Pulsed and DC processes were used for Al and AlSi4% films deposition.

III.A.2.c. Temperature effect

Semiconductor components are subject to temperature variation during their life cycle. Temperature cycle has been tested on Al, AlSi1% and AlSi4% films previously annealed at 440°C. Similar stress measurement was done as previously, and temperature swept from room temperature to 440°C.

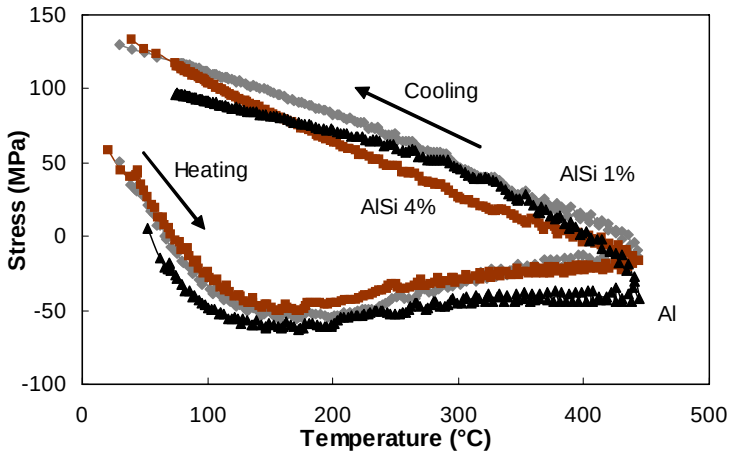


Fig. 41 Stress variation of 2µm thick AlSi 1%, AlSi 4% and Al over a 30°C to 440°C temperature cycle

Various phenomena have to be considered to explain the hysteretic behavior of Fig. 41. Wafer curvature depends on Al-based thermal expansion but also on silicon and SiO_2 expansions.

Thermal expansion coefficients of each material are respectively 20ppm/K for the aluminum, 3ppm/K for silicon and 0.5ppm/K for the silicon dioxide. When heating up the sample, Al-based material is the first film to relax due to its high thermal expansion (from 20° to 150°C). At higher temperature, the thermal expansion of successively silicon substrate and silicon dioxide dominates. When cooling down, re-crystallization of the Al-based material occurs and the initial stress is shifted up. The temperature cycling under oxygen atmosphere causes at high temperature the insertion of oxygen molecules in the aluminum. Oxidized aluminum films exhibit a significant higher tensile stress than pure Al-based films. During re-crystallization, oxidized film shows hillocks on the top of the aluminum, increasing also its roughness as seen in Fig. 42.

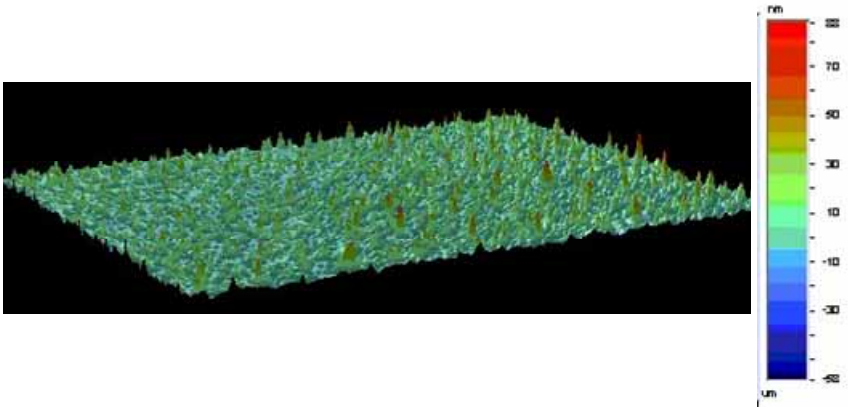


Fig. 42 Optical profiler measurement of the surface roughness on AlSi 1% film after re-crystallization, hillocks are visible on optical profiler and roughness is +/- 30nm

As stated previously, thermal expansion coefficient of the Al-based material is much higher than those of silicon and oxide, and stress variation on a full wafer at a temperature range from 20°C to 150°C can be considered arising from the Al-based material only. The temperature cycling on the AlSi1% film is shown in Fig. 43 and presents a hysteretic behavior between the heating and the cooling phase.

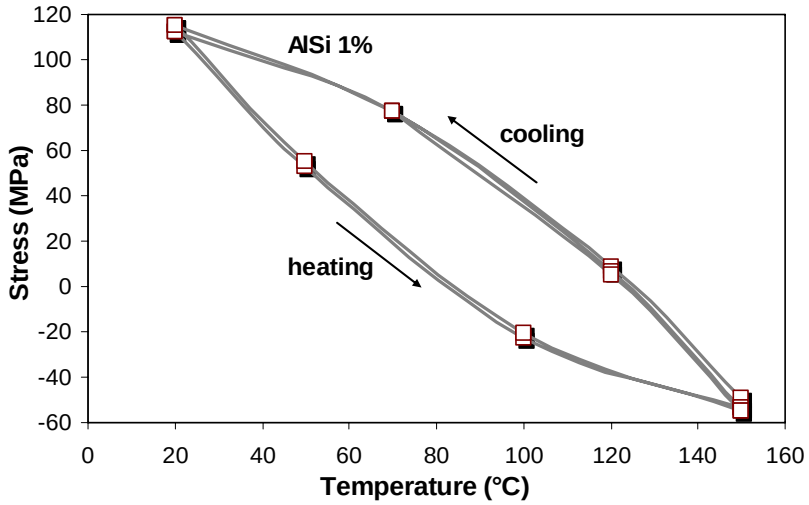


Fig. 43 AlSi1% temperature cycles from 20°C to 150°C showing a hysteretic stress behavior

The temperature dependence of the thin film stress has a strong impact on the resonance frequency. A simulated frequency variation on a 100MHz CC-beam resonator is shown in Fig. 44, with a maximum shift of 1900ppm at 150°C.

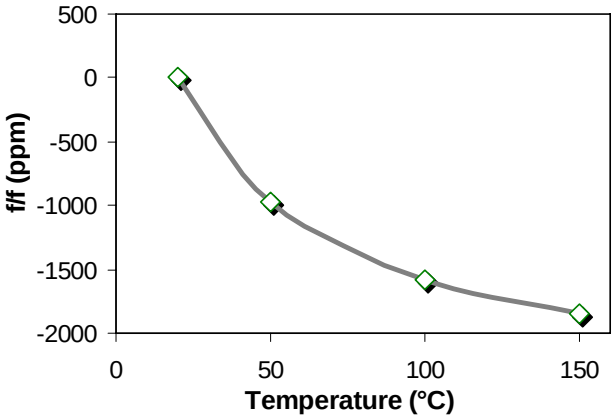


Fig. 44 Simulation resonant frequency shift of a 100MHz AlSi1% resonator under a temperature variation range from 20° to 150°C (Beam length = 10µm, thickness = 2µm and width = 4µm)

III.A.2.d. Stress measurement from devices

On chip test structures were designed to measure either compressive or tensile stress on the structural layer. According to wafer curvature measurement, a tensile stress was expected in the AlSi film and Guckel rings [94] were fabricated to measure this stress. As shown in Fig. 45, tensile stress tends to stretch the rings towards the anchors, inducing compressive moment on the central part. Stress value can be calculated from the ring dimensions for which buckling of the central part occurs.

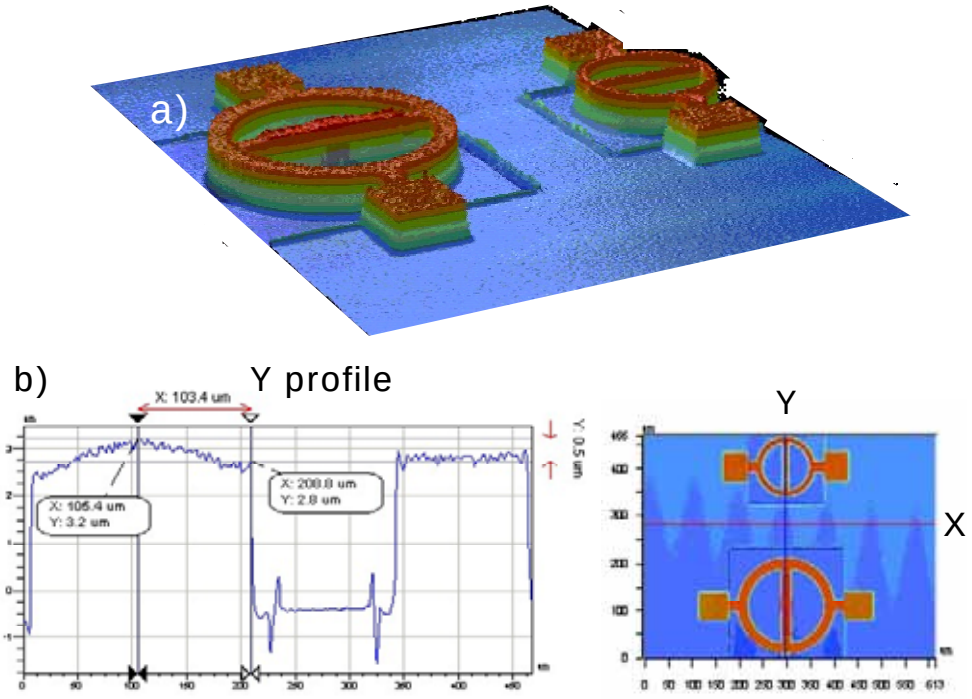


Fig. 45 a) Optical profiler picture of two Guckel rings of 180µm and 120µm long central beam, b) dimension profile along the Y direction

Stress value of the film can be derived from the maximum displacement of the central beam of the ring (see Appendix A). The accuracy of this technique depends on the ability to find the closest set of rings for which small variation of beam length induces buckling, which is in this case for a ring size between the two structures. The profile of the central beams presented in Fig. 45b, shows that the bucking occurs only for the larger ring. According to the value of this critical ring, a film stress of 150MPa was calculated. Considering the fact that the optimal ring for which the beam begins to buckle should be placed between the two rings of Fig. 45, the calculated stress value is in good agreement with the 80MPa tensile stress measured on the wafer curvature (Fig. 40).

III.A.2.e. Stress gradient measurement

The total stress in a material is the sum of the mean residual stress and the stress gradient and can be written as:

$$\sigma_T = \sigma_0 + \sigma_G(y) \tag{III- 7}$$

The stress gradient can be extracted from the deflection amplitude of different suspended cantilevers. When the structure is released, the stress σ_0 is relaxed and only the stress gradient acts on the beam. The bending moment due to the stress gradient is written as:

$$M = \int_{-H_{beam}/2}^{H_{beam}/2} W_{beam} y \sigma_G(y) dy \tag{III- 8}$$

A linear stress gradient can be approximated and the resulting stress is defined as:

$$\sigma_G(y) = yE\gamma \tag{III- 9}$$

where γ is the linear stress gradient. Combining (III- 8) with (III- 9), γ can be written as:

$$\gamma = \frac{12M}{EW_{beam}H_{beam}^3} = \frac{M}{EI} \tag{III- 10}$$

where I is the moment of inertia of a rectangular beam. The moment of inertia at the endpoint of a cantilever is expressed as (III- 11) and the stress gradient is calculated from the displacement amplitude.

$$\Delta\gamma = \frac{ML_{beam}^2}{2EI} = \frac{\gamma L_{beam}^2}{2} \tag{III- 11}$$

The displacement at the edge of the cantilever is measures with an optical profiler (Veeco Wyko NT1100), as shown in Fig. 46.

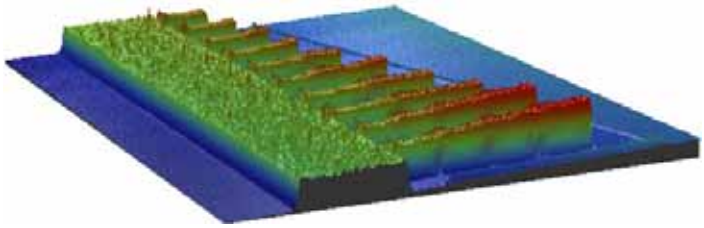


Fig. 46 Optical profiler picture of 2µm thick and 20µm wide AlSi1% cantilevers with length ranging from 50µm to 200µm, after a 380°C annealing

The stress gradient is extracted from the fit of the tip deflection versus the cantilever length curve in Fig. 47.

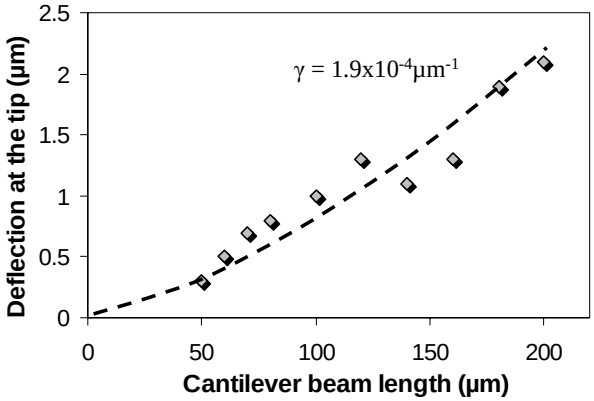


Fig. 47 Measured deflection of the tip of cantilever presented in Fig. 46

III.A.2.f. Young's modulus extraction

Young's modulus extraction is essential to design resonators and switches. Typical value for the thin aluminum film is 70GPa. The value for the AlSi1% alloy can simply be obtained by actuating the suspended structure:

- Young's modulus is extracted from the DC characterization of a low rigidity beam up to the pull-in voltage. To avoid any influence of the channel potential, a suspended AlSi CC-beam above defined air-gap d_{gap} and a second metal electrode was used for the experiment. The pull-in voltage equation can be then reversed to extract the Young's modulus as:

$$E = \frac{27\varepsilon_0}{192I}(V_{PI})^2 \frac{W_{beam}L_{beam}^4}{8d_{gap}^3} \qquad \text{(III- 12)}$$

In the case where the air-gap is unknown, the mechanical structure can be actuated at its natural frequency; the Young's modulus is extracted from the resonant frequency developed in Chapter II.B.1 for a CC-beam vibrating at its first vibration mode:

$$E = \rho\left(\frac{fL_{beam}^2}{1.03H_{beam}}\right)^2 \qquad \text{(III- 13)}$$

Both techniques were used and a resulting AlSi1% Young's modulus of 48GPa was extracted.

III.A.2.g. Summary of sputtered Al-Si1% properties

Mechanical and electrical of sputtered Al-Si1% is presented in Table VIII, where the electrical resistivity was extracted in [95].

Characteristics	Sputtered AlSi1%
Poisson's ratio	0.35
Young's modulus (GPa)	48
Mean stress (MPa)	80-150 tensile
Stress gradient (μm^{-1})	$1.9x10^{-4}$
Electrical resistivity (Ω.m)	$3.3x10^{-8}$

Table VIII. Summary of sputtered AlSi1% thin film properties

III.A.3. Conclusion and limitations of the metal gate SG-MOSFET process

A suspended metal-gate over MOSFET process has been successfully developed to achieve the fabrication of the first reported functional SG-MOSFET device. Two sacrificial layers were studied using polysilicon or polyimide. A CMP step was optimized for the two sacrificial layers. The processes used to release these two layers impact the SG-MOSFET devices behavior and determines the possible application; resonator for the polysilicon layer and memory for the polyimide layer (see Chap. IV and V). The stress on different Al-based thin films and the influence of temperature on the metal-gate behavior were investigated.

However, in order to increase the performances of the SG-MOSFET, material choice and dimensions control have to be improved:
- Mechanical characteristic of Al-based beam compared to silicon is less attractive for vibrating structures due to its low Young's modulus (E = 48GPa for AlSi 1% and 160GPa for silicon thin films). For a MEMS resonator application, in order to compensate the lower rigidity compared to silicon beam, the thickness of the AlSi beam has to be greater or the beam length smaller to achieve the same resonant frequency.

- The air-gap dimension is defined by a CMP step which results in a non-uniform thickness along the suspended-gate due to the dishing effect.

- Al-based materials have a high temperature coefficient, which induces a strong change in Young's modulus and therefore a large frequency drift with temperature variation.

- Non self-aligned MOSFET process results in strong dependency of the transistor source and drain access resistances to the alignment step.

III.B. Silicon resonator process

A new silicon gate process has been developed, overcoming the issues of the metal-gate process in terms of air-gap control and self-aligned process. Moreover, as expressed in chap II, silicon gate is more suitable to achieve high quality factor by improving thermo-elastic damping. The process composed of seven masks without the need of CMP is presented in Fig. 48.

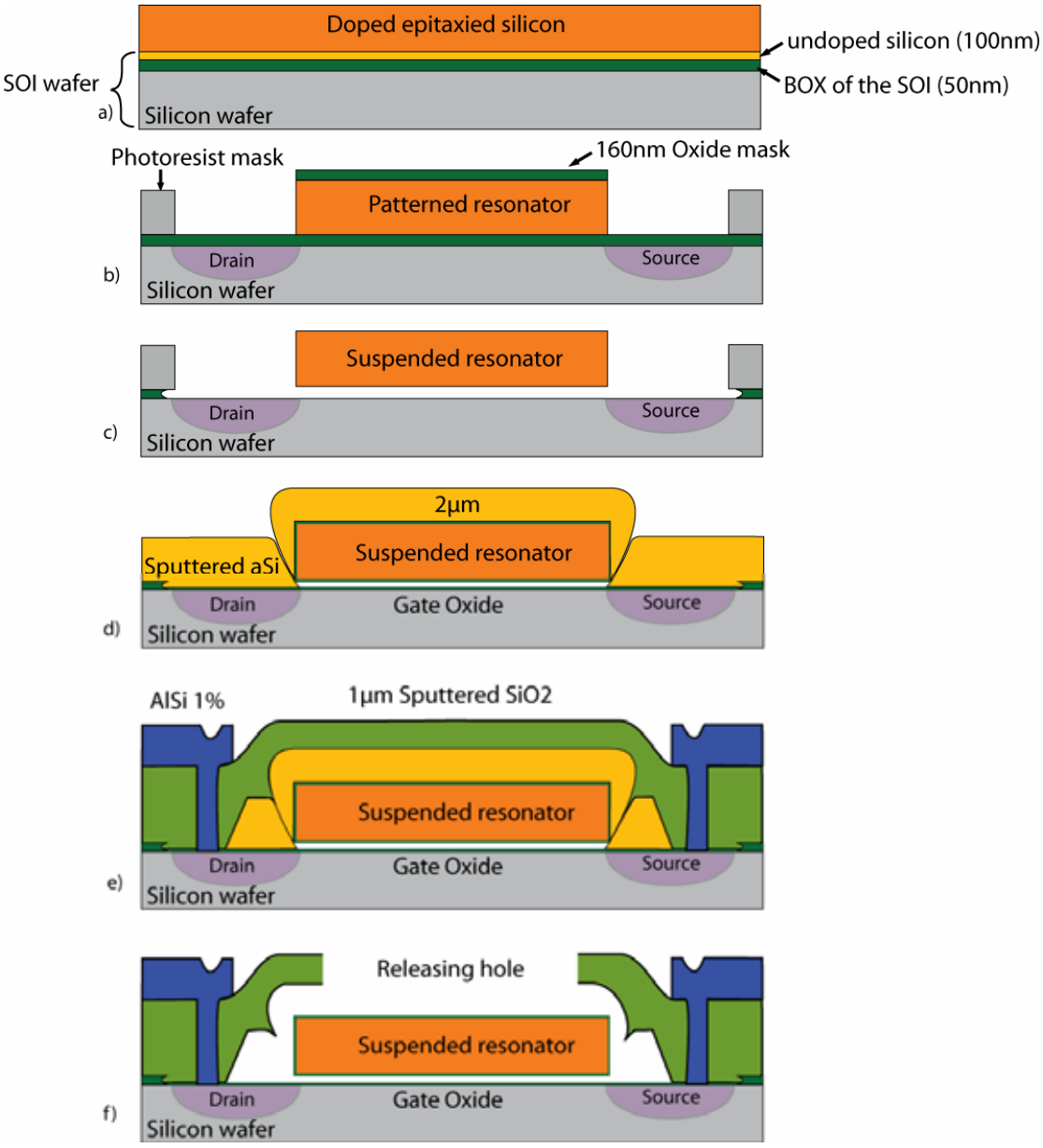


Fig. 48 Schematic of the fabrication process steps of a silicon SG-MOSFET for MEMS resonator application

III.B.1. Wafer pre-processing

In order to have a very good gap control, SOI wafer with 50nm of Buried OXide (BOX) and 100nm of undoped silicon were used. 900nm thick intrinsically phosphorous doped silicon was epitaxied at 3-4x10^{19} at/cm^3 in order to have a uniform doping profile over the overall thickness (Fig. 48a). Uniform doping cannot be achieved with doping implantation due to the high energy needed for deep implantation, and $POCl_3$ doping has a limited control over the implantation depth. A Low temperature 160nm silicon dioxide layer was deposited to serve as mask layer for resonators patterning. In order to dope the initial 100nm silicon layer of the SOI wafer, an optimized 5 minutes 950°C annealing was simulated and realized. For this step, the thin SiO_2 mask also plays a role of dopant barrier to avoid amorphization of the silicon surface due to dopant desorption during annealing. The silicon was patterned using a mixed SF_6 and C_4F_8 gases (Fig. 48b), as described in Chapter III A.1.f.

III.B.2. Sacrificial layer etching

Specific wet etching processes were tested to etch the sacrificial SiO_2 and suspend the resonator over the 50nm air-gap. Sticking of resonator beam on the substrate during wet release has been shown to be critical for small air-gaps due to surface contact created by water capillarity [18].

III.B.2.a. HF vapor etching

HF vapor etching technique consists of using the evaporation of a HF bath under a heated mechanically clamped wafer in order to etch the oxide sacrificial layer [96, 97]. A key advantage of this technique is that sticking of the suspended structure is avoided due to the absence of HF in liquid phase. However this technique does not allow using photoresist as mask material as it absorbs the HF and etches the protected zones faster than the opened zone.

III.B.2.b. BHF etching combined with CPD

A more complex but stable and reproducible solution has been developed combining buffered HF (BHF) oxide etching and using a Critical Point Dryer (CPD, Tousimis Automegasamdri 915B®) to avoid sticking of the structure (Fig. 48c). After sacrificial oxide etching in a BHF, composed of NH4F (40%) and HF (49%) mixed with a 7:1 HF dilution ratio, the wafer is put successively in deionized water and in ethyl alcohol. Due to higher hydrophilic properties, alcohol replaces water under the released structures. The CPD chamber is then filled out with liquid CO_2, replacing the alcohol by successive purge and fill processes. The alcohol is almost twice as dense as the liquid CO_2; therefore, the alcohol migrates towards the lower elevation where the purge hole extracts it, while the incoming liquid CO_2 stays on the top part. The CPD equipment is designed to reach the supercritical point of the liquid CO_2, at a pressure of 1072psi (pound-force per square inch = 6.89kPa) and a temperature of 31°C where liquid is directly transformed into gas, then avoiding sticking issues. The result of this process on a silicon-based SG-MOSFET is shown in Fig. 49, where the 50nm air-gap is perfectly released without any sticking issue.

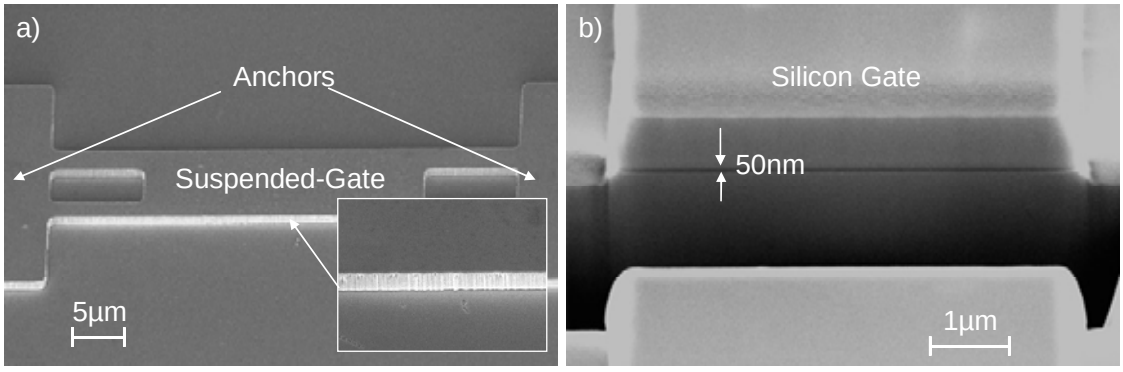


Fig. 49 SEM pictures of a) a suspended-gate after oxide etching with the combined BHF with CPD process, b) FIB cross section of the gate showing the 50nm air gap along the 6µm wide beam

III.B.3. Effect of gate oxidation on resonance frequency

In order to make the MOSFET gate oxide, a dry oxidation was performed on the suspended structure. Splits of dry oxide have been performed without showing any stress issues on the suspended-beam. This oxidation consumes part of the silicon and therefore has a slight impact on the final Equivalent Gap Thickness (EGT, see Chap. II). The resonance frequency of the resonator is also affected due to the different Young's modulus between the SiO_2 and the Si. Based on FEM analysis using ISE®, oxidation thickness was found according to the doping type and concentration. FEM analysis using ANSYS® has been performed and Table IX shows the strong impact of the oxide thickness on the gate resonant frequency.

Oxide thickness	0	6.6 nm	29nm
Resonant freq (MHz)	38.4	38.072	37.17
F/F (ppm)	0	8 540	32 000

Table IX. Simulated impact of dry oxidation on a 38.4MHz resonant frequency CC-beam (1µm thick, 15.1µm long and 6µm wide

Dry oxidation of silicon should be taken into account for the design of the resonator. Native oxide which is in the order of 1nm for silicon and 1.5nm for polysilicon could also shift slightly the targeted frequency.

III.B.4. Resonator encapsulation

After the release step, the device should be protected from water but also from the further process step needed for contact metallization. Sputtered amorphous silicon (aSi) allows a good protection of the beam without filling the air-gap, which reduce considerably the final releasing time (see Fig. 48d). It also has a little impact on the active device due to the room temperature deposition process and to its limited intrinsic stress. A key advantage of this step is to protect the gate oxide from degradation during the following process steps. A top view of an encapsulated structure is shown in Fig. 50.

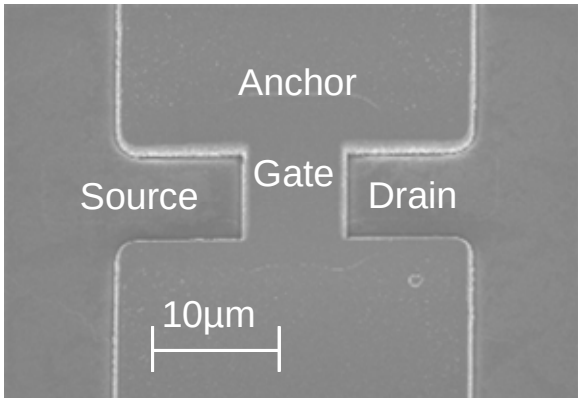


Fig. 50 SEM picture of a 2.1µm thick aSi covered silicon released resonator

A specific resist deposition and reflow process was developed to achieve edges with a low slope angle that will be further transferred into the aSi layer. This layer was patterned by using a C_4F_8 and SF_6 mixed gases under an ICP (Inductively Coupled Plasma) plasma.
The wafer was then covered by a 1.8µm sputtered SiO_2 at room temperature. The good step coverage on top of the aSi is guaranteed by the low slope angle. Even if deposited at room temperature, the sputtered SiO_2 also presents a good conformity around the resonator edges for this topology (Fig. 48e). This thick oxide is mandatory to avoid contact pads parasitic capacitance. Without this thick oxide, 100µmx100µm contact pads will be deposited on the 50nm thin buried SOI oxide, inducing a very high pad capacitance. Considering a contact resistance of 10 ohms [98], this results in a low-pass filter corner frequency of around 19kHz, cutting off the signal from the resonator.

III.B.5. Contact metallization and release

Contacts were etched through the thick oxide with a C_2F_6 plasma (Fig. 48e). The RF and DC pads composed of AlSi1% sputtered at room temperature were patterned on top of this oxide. The AlSi1% was annealed at 400°C to lower the contact resistance (see Chap III.A.1.d). The last masking step consists of opening the oxide with a dry etch process to access the sacrificial amorphous silicon. The final resonator release is done using a pure chemical SF_6 plasma etching which result in a very high selectivity to the thin gate oxide surrounding the silicon gate (cf. Chapter III A.1.h). SEM pictures of a released SG-MOSFET are shown in Fig. 51.

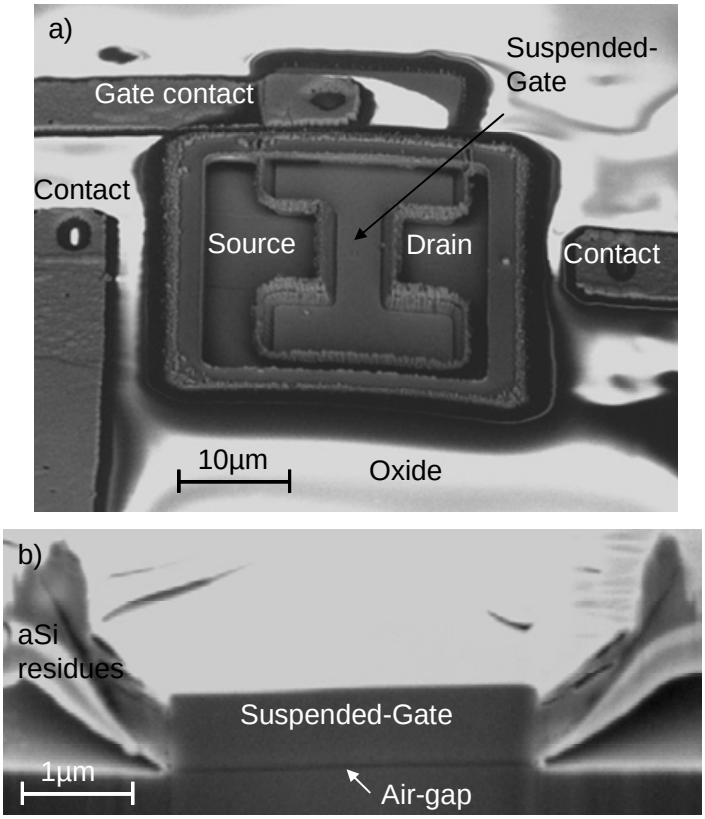


Fig. 51 a) SEM picture of a released SG-MOSFET showing aSi residues, b) FIB cross section of the released suspended-gate

It can be seen that aSi residues are still present only of the sides of the suspended-gate after the final SF_6 release. This unwanted process issue can be explained by the non-conformal aSi deposition which creates voids on the side of the silicon gate. During the aSi patterning, photoresist migrates in these sharp voids and remains even after oxygen plasma etching. Therefore, during the following process steps, the remaining resist migrates in the near-by aSi and burns during the AlSi1% annealing, resulting in a very hard mixed material.

III.B.6. Improvements of the silicon gate SG-MOSFET process

A very stable process has been developed to build a silicon SG-MOSFET with a perfectly controlled air-gap and a good dimension beam control. The following improvements can be implemented to avoid the un-wanted residues along the edges of the beam:

- Before aSi patterning, the access to the gate-to-channel air-gap is very limited, therefore a polysilicon conformal deposition can be used to fill the voids created during the sputtering step. This deposition should be then performed at high temperature and have to be taken into account in the overall thermal budget.
- Before aSi patterning, a thin low temperature conformal oxide such as Atmospheric Pressure CVD oxide [99] can be deposited in order to fill the voids. Patterning of the double aSi and thin SiO_2 layers can be done in the same equipment by using successively C_4F_8 and SF_6 followed by a C_2F_6 plasma.

III.C. Packaging process

Different packaging possibilities were proposed in previous years using either a 0-level approach ([100], [101]) or wafer bonding approach [102]. 0-level thin film packaging using standard front-end manufacturing processes is likely to be the most cost-efficient technique to achieve vacuum encapsulation of MEMS components for volume production. A specific vacuum packaging process compatible for both RSG-MOSFET silicon and AlSi-based resonators have been developed in a zero-level approach. The packaging is done at room temperature making it fully compatible with IC-processed wafers and avoiding any subsequent degradation of the active devices [89]. The pressure level needed to avoid any degradation of the quality factor due to damping issues is around 1 mBar, according to measured characteristics presented in Chapter IV.

III.C.1. Process flow

The packaging process steps are presented in Fig. 52. A 5µm thick amorphous silicon (aSi) layer is sputtered on the already released MEMS resonator followed by a 2µm RF sputtered SiO_2 film deposition. A quasi-zero stress aSi film deposition process has been developed with a quasi-vertical deposition to avoid depositing material under the beam lowering the releasing time (Fig. 52a). Releasing holes of 1.5µm were etched through the SiO_2 layer and the releasing step is done by dry SF_6 plasma (Fig. 52b). Due to pure chemical etching, high selectivity of less than 1nm/min on SiO_2 was obtained (cf. A.1.h). The holes were clogged by a non-conformal sputtered SiO_2 deposition at room temperature (Fig. 52c).

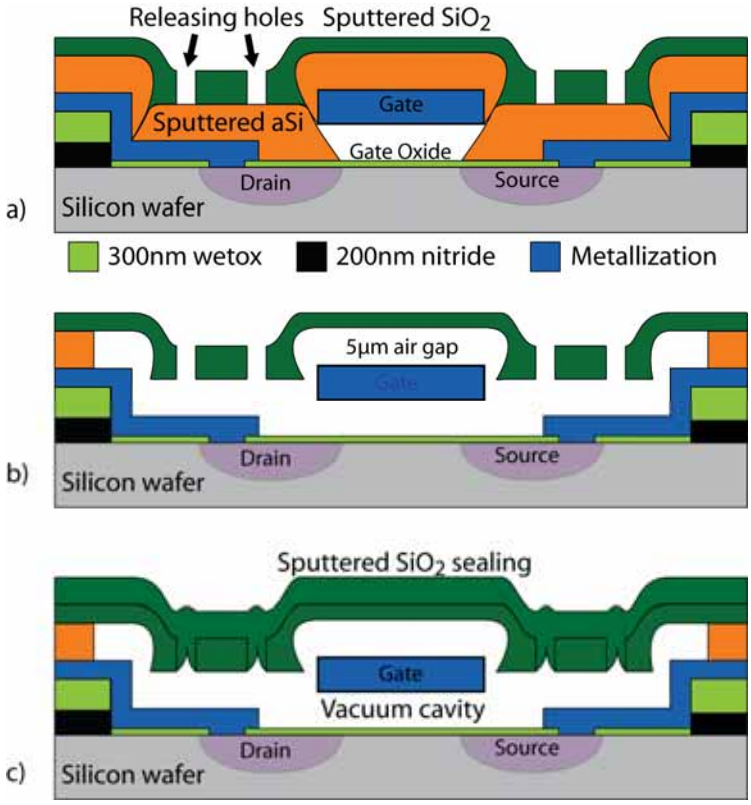


Fig. 52 Schematic of the 0-level vacuum package fabrication process of a RSG-MOSFET

Packaging process has been performed on the metal-gate SG-MOSFET and Fig. 53a shows a SEM picture of a released AlSi-based RSG-MOSFET with a 500nm air-gap, a beam length and width of respectively 12.5µm and 6µm with a 40nm gate oxide. A vacuum packaged RSG-MOSFET is shown in Fig. 53b highlighting the strong bonds of the re-filled releasing hole after clogging. Cross section of a releasing hole in Fig. 53c shows more than 1µm bonding surface to ensure cavity sealing. A FIB cross section in Fig. 53d shows the suspended SiO_2 membrane above the suspended-gate. The vacuum inside the cavity is obtained by depositing the top SiO_2 layer under $5x10^{-7}$mBar given by the equipment.

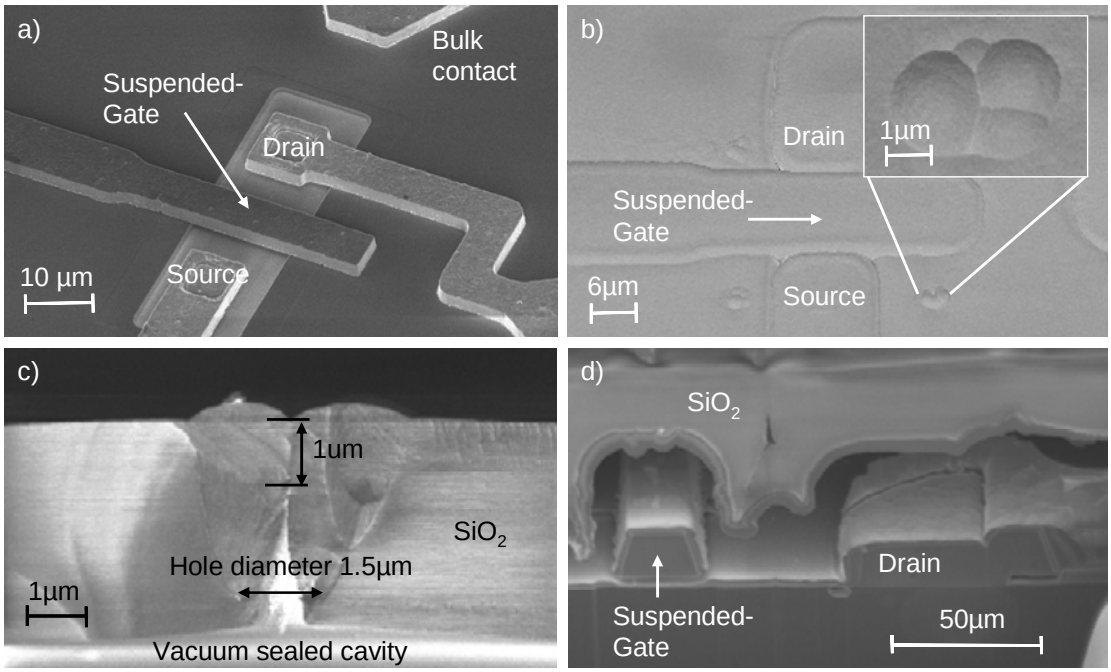


Fig. 53 SEM pictures of a) AlSi-based RSG-MOSFET, b) Top view of a SiO_2 cap covering the RSG-MOSFET, c) Cross section of releasing holes filled with sputtered SiO_2, d) FIB cross section of the packaged RSG-MOSFET, material re-deposited during the FIB cut is surrounding the suspended-gate and the SiO_2 membrane

The slightly compressive SiO_2 membrane shows very good behavior for the thin film packaging, as seen in Fig. 54, where cavities are formed on large opening size. During the clogging process, due to the highly non-conformal deposition, the amount of material entering in the cavity has been measured to be only 80nm compared to the 2.5µm silicon dioxide.

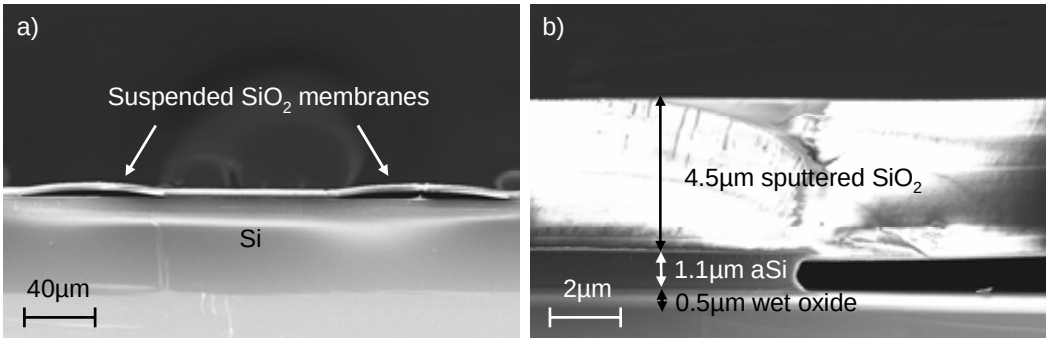


Fig. 54 Cross section of a 2µm SiO_2 suspended membrane having a releasing hole clogged by a 2.5µm SiO_2 sputtering deposition

Residues inside the cavity are confined in an 8-to-10µm diameter circle, but strongly depend on the topology inside the cavity. The oxide thickness needed to clog the holes strongly depends on the hole height-to-width ratio, which therefore determines the amount of residues in the cavity.

III.C.2. Effect of opening size on releasing rate and clogging effect

Etching rate variation on aSi, related to the hole opening size and the aSi thickness is shown in Fig. 55. Small holes openings decrease the etching rate. A dual underetching behavior due to aSi thickness variation and holes diameters is observed after a 2 min. release step: for a small hole aperture (2µm diameter), exposed surface factor is dominant and etching rate is 3 times greater for the thin aSi. However for large openings (9µm diameter) for which underetch distance is more important, path factor representing the lateral opening height for species to reach aSi becomes important and then etching ratio decreases to 1.3.

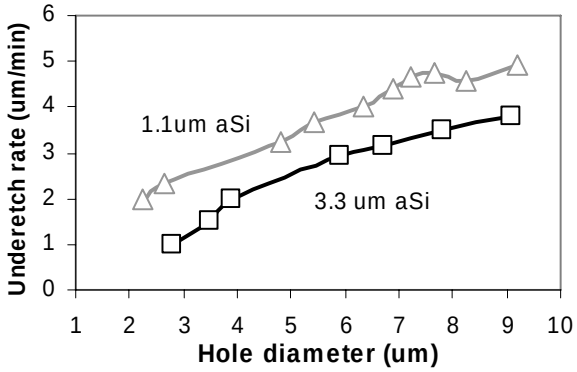


Fig. 55 Underetch rate for various releasing holes diameters with amorphous silicon sacrificial layers of 1.1µm and 3.3µm, after 2min. releasing

After release, encapsulation is performed by sputtered deposition of SiO_2 under high vacuum of $5x10^{-7}$mbar using the intrinsic, non-conformal deposition to clog holes. Holes with diameter-over-depth aspect ratio below 1 are clogged for SiO_2 thickness of 2µm as shown in Fig. 56, and hole clogging rate is 330nm per deposited micron. Clogging effect is strongly material dependent and is related to the sticking coefficient (Src) that defines probability for a molecule to stick to the surface (Src = 0.26 for SiO_2 and <0.01 for LPCVD Poly-Si).

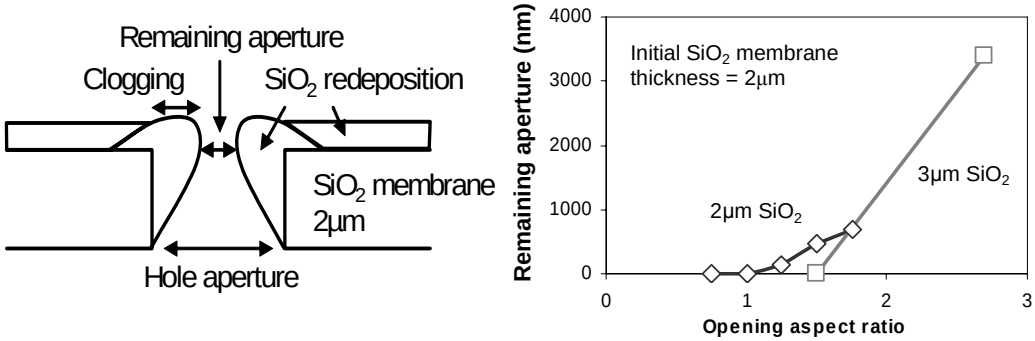


Fig. 56 (Left) Schematic of a cross section of the SiO_2 membrane clogged by SiO_2 sputtering deposition, (Right) remaining aperture diameter for a 2µm and 3µm SiO_2 deposition on top of an opened 2µm SiO_2 membrane

The effect of hole geometry on underetch rate and clogging has been studied on square and rectangular holes, as shown in Fig. 57. The rectangular opening has a quasi identical underetching than square shape of the same opening area, while clogging is 10 times more important. The remaining hole size after 2.5µm SiO_2 deposition is 1.4µm for the square and 140nm for the rectangle.

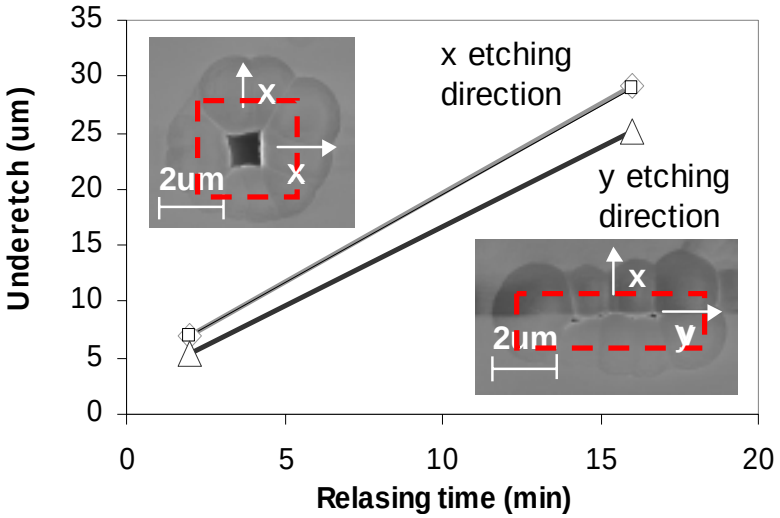


Fig. 57 Underetch length after 16min release for a 29.1µm^2 square and rectangle release holes (red dotted rectangles) with a 1.1µm thick aSi

III.C.3. Packaging issues for production environment

For industrial production of integrated MEMS, 0-level package has to sustain plastic molding, which corresponds to an isostatic pressure of around 100Bar. Encapsulation film thickness has been designed to lower the impact of the pressure during molding. FEM simulations done with Coventor® in Fig. 58 and Table X show that the molding-induced package deflection is reduced to 25nm, having a 4.5µm thick SiO_2 film, which makes it compatible with standard industrial back-end processes.

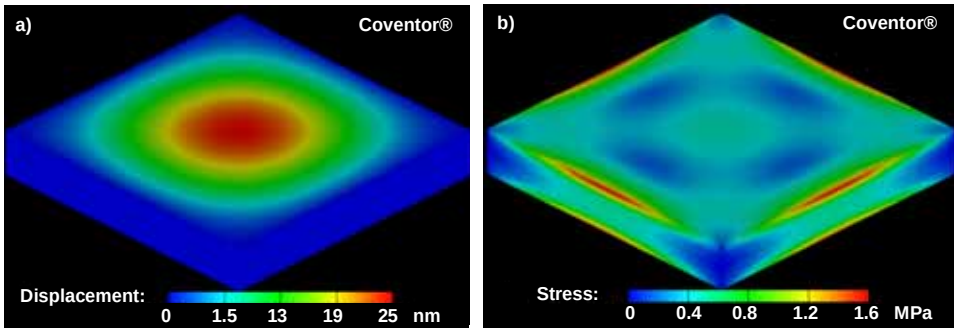


Fig. 58 FEM modeling of the packaged resonator under applied isostatic pressure mimicking plastic injection process step

Structural layer material	LTO	Nitride PECVD
Film thickness	4.5µm	2.5µm
Max. stress before failure	2GPa	9GPa
Stress due to molding	1.6MPa	4MPa
Molding-induced deflection	25nm	36nm

Table X. FEM simulations of the structural layer thickness needed to sustain plastic molding over 0-level packaging composed of a 30µmx30µm membrane. Comparison with PECVD nitride thickness needed to induce the same deflection

III.C.4. Perspectives of the 0-level thin film packaging process

The developed 0-level packaging has the unique advantage of using room temperature processes which makes it compatible with in-IC or above-IC processes. The process uses the high vacuum level of 10^{-7}mBar given by the equipment during the final encapsulation. The technology is suitable for RSG-MOSFET and metal-based vibrating MEMS structures, for which vacuum encapsulation is mandatory to achieve high quality factor. The impact of releasing hole geometries and size on the clogging effect has been investigated. The optimal encapsulation membrane thickness was defined in order to sustain the external pressure applied on the cap during the back-end process. The packaging can also be used for temperature compensated silicon resonators where structures are surrounded by an oxide layer in order to compensate for the frequency drift due to temperature variation, related to the negative temperature coefficient of the silicon [103].

On the developed process flow, further investigations on vacuum level and long term stability still need to be studied in order to fully characterize the packaging. These characterizations can either be done directly by using helium leakage test [104], or indirectly by actuating the resonator for which quality factor is directly related to the vacuum level.

In this work, the packaging solution developed for the RSG-MOSFET gives general inputs on dimensioning of the thin film packaging. These results can then be adapted to develop a universal MEMS 0-level thin film packaging which could be obtained by using a polymer as sacrificial layer instead of amorphous silicon. In the case of silicon MEMS using a capacitive detection, the impact of the oxygen plasma used to release the polymer is negligible due to the absence of gate oxide layer, which is degraded by the oxygen plasma.

III.D. Front-end process

In parallel to the process developed at the EPFL, a fully CMOS compatible front-end process had been developed with the STMicroelectronics design and fabrication team, addressing the specific semi-conductor fabrication requirements. To combine high frequency structures with MOSFET detection, bulk acoustic mode resonators using a lateral MOSFET detection were designed. Two designs of lateral MOSFET detection and related processes were investigated.

III.D.1. Lateral-gate Vertical-MOSFET architecture [105]

The vertical MOSFET detection offers a high output signal due to the very small channel length, related to the resonator thickness and a very large channel width, related to the resonator length. The resonator design on Fig. 59 is based on an in-plane lamé-mode vibration [10] where the square resonator is anchored at each corner (only two are represented in the figure) and is symmetrically actuated by two electrodes. During the in-plane motion, the resonator, considered as the gate of the lateral transistor, modulates the drain current.

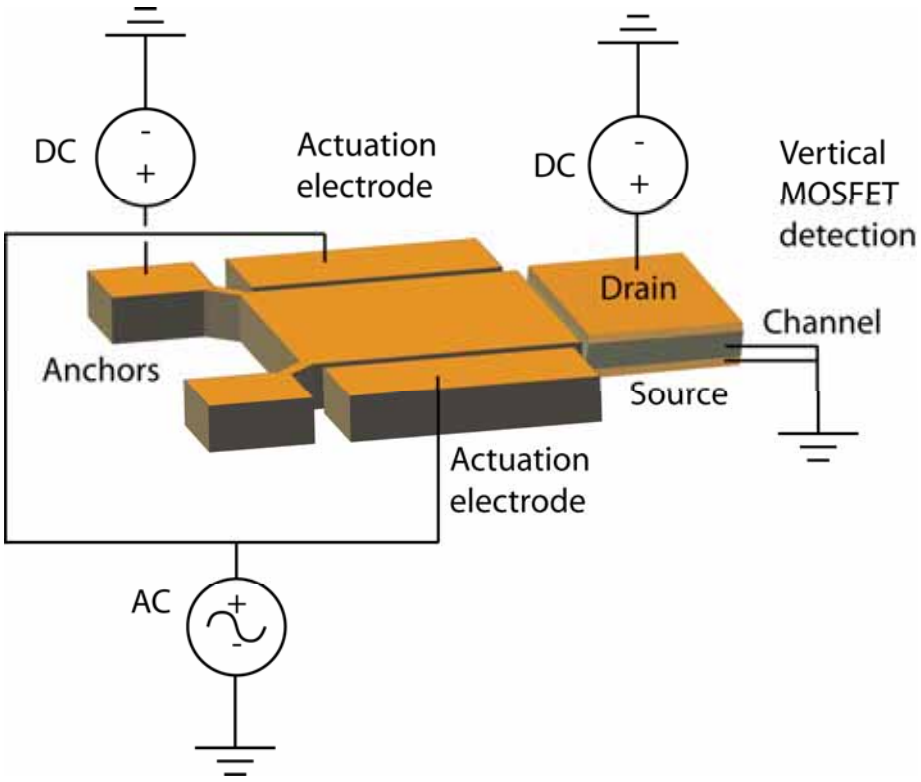


Fig. 59 Vertical MOSFET detection of in-plane bulk mode resonator

In terms of process development, the fabrication process was studied on a 400nm thick resonator. The process suffers from the fact that the MOSFET source definition, at the bottom of the 400mn silicon, needs a very high energy implantation which is hardly controllable for this thickness. This implantation creates a large doping profile and has a strong implication in defining the size of the source region, and a consequence the channel length. Vertical contact openings to access drain, bulk and source regions also requires complex design and process to

make connections at different depth in the silicon. These two analyses could be an issue in terms of channel length reproducibility and access contact resistances.

III.D.2. Lateral-gate Horizontal-MOSFET architecture [106]

Another process overcoming the previous issues, using a lateral-gate architecture with a horizontal MOSFET detection has been investigated, as shown in Fig. 60. Having the drawbacks of a lower output current compared to the previous architecture due to its long channel and short width MOSFET detection; it however presents higher detection current than capacitive detection for medium-to-high frequency resonators.

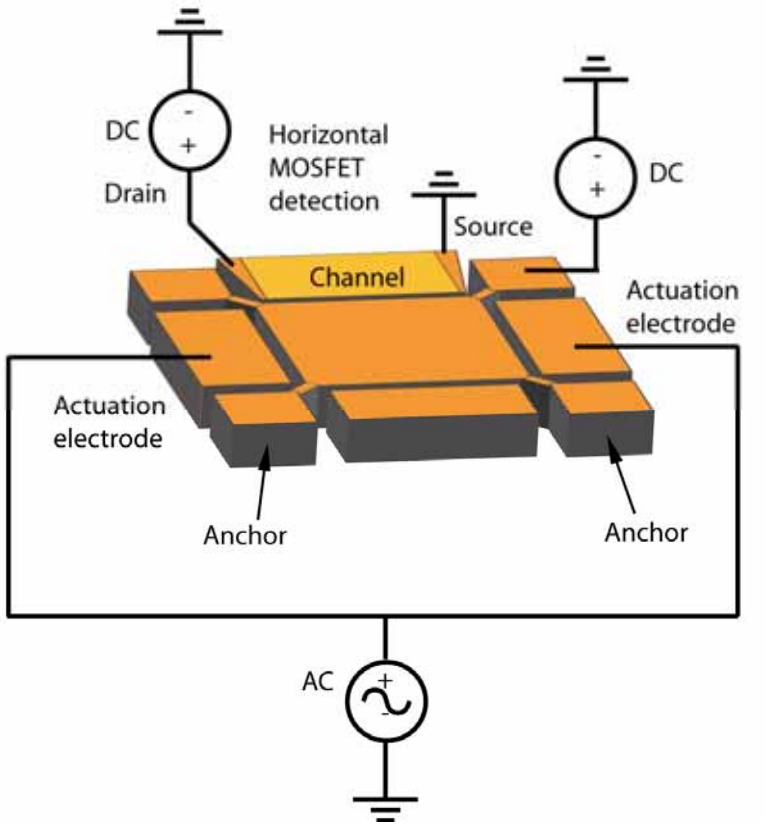


Fig. 60 Horizontal MOSFET detection of in-plane bulk mode resonator

The main advantage of this process is that the gate, the source and the drain can be defined in a single implantation step. This process requires however high alignment specifications in order to implant the gate without implanting the transistor channel, which can only be done in an industrial environment. The process steps for this architecture are presented in Fig. 61.

III.D.3. Process flow and technological blocks validation

Schematic of the process flow related to the Lateral-gate Horizontal-MOSFET resonator is presented in Fig. 61. The process uses only two masks on top of the conventional front-end pre-processed wafer with Silicon Trench Isolation (STI), with one CMP.

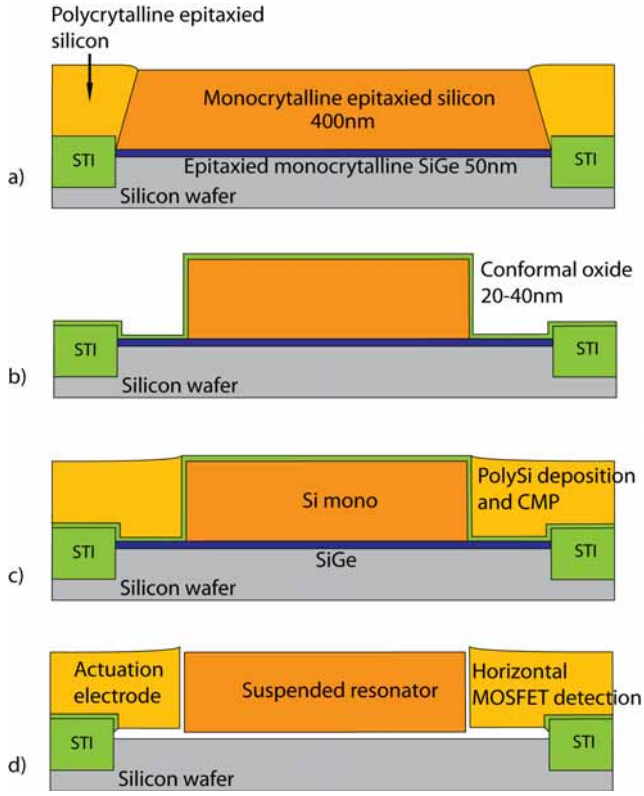


Fig. 61 Cross section of the process steps of a front-end Lateral-gate Horizontal-MOSFET resonator design on a square shape bulk resonator

It is composed of a selective Silicon Germanium (SiGe) epitaxy on top of a silicon substrate in between the STIs (Fig. 61a). The silicon germanium is deposited by a Chemical Vapor Deposition (CVD) of GeH_4 and Dichlorosilane (SiH_2Cl) carried to the chamber by the hydrogen (H_2). The gas concentration is set to have a SiGe layer with 30% of germanium. The selectivity of the deposition in the silicon exposed area is achieved by the chlorine molecules which preferentially attaches to the oxide layer and then avoids any silicon germanium deposition. In a second step, a non-selective epitaxy of undoped silicon is performed on the wafer, resulting in a single-crystal structure on top the SiGe and a poly-crystalline on top of the STIs (Fig. 61a and Fig. 62). The non-selective silicon epitaxy mechanism follows the formula (III- 14)

$$SiCl_2 + H_2 \rightarrow Si + 2HCl \qquad \text{(III- 14)}$$

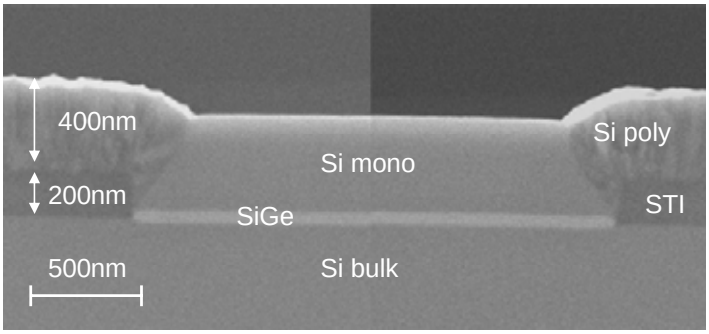


Fig. 62 Cross section of SiGe-Si stack on top of bulk substrate after selective epitaxy of SiGe followed by a non-selective epitaxy of silicon [107]

A typical silicon orientation at the mono and poly-silicon edge is the (111) direction, as shown in Fig. 62. The thickness ratio between the poly-crystal and the single-crystal layers can be varied by changing the gas concentration. This ratio is decreased by lowering the chlorine concentration and the range is shown in (8).

$$0 < \frac{T_{poly}}{T_{mono}} < 3 \tag{8}$$

Resonators are patterned in the single-crystal silicon and the anchors are designed on top of the STI (Fig. 61b). In order to fully control the resonator-to-electrode gap thickness, a thin conformal oxide layer defining the gap thickness is deposited (Fig. 61b). Undoped polysilicon epitaxy is performed on the wafer followed by a CMP step to flatten the surface and access the oxide layer on top of the resonator (Fig. 61c). Gate, source, drain and electrode are defined using a single mask with multiple implantations of different energies to uniformly implant the resonator along its thickness. The lateral gaps between the resonator and the electrode are released by a HF wet etching (Fig. 61d). The final release of the resonator is done by using a dry etching of SiGe with a selectivity of 1:250 to silicon. The SiGe release step is a pure chemical plasma etching using a CF_4 gas [108-110]. The etching selectivity is naturally achieved by the fact that the bonding energy between Si-Ge molecules (3.12eV) is lower than for Si-Si molecules (3.25eV) and therefore are easily broken by fluorine radicals. By increasing the percentage of germanium in the silicon during the epitaxy, a higher selectivity can be achieved. A 30% SiGe etching test results is shown in Fig. 63, where a 2.3µm underetch was obtained with this process. With this large tunnel gap, the process is then suitable for lamé-mode MEMS resonator.

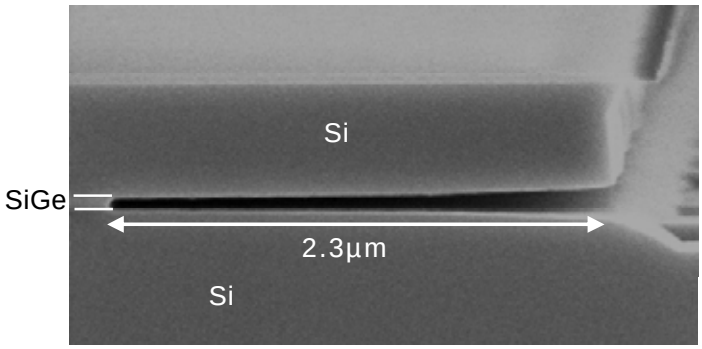


Fig. 63 SEM picture of SiGe release etching regarding the selectivity over silicon

III.D.4. Perspectives of the Front-end process

A CMOS compatible process has been proposed to be able to fabricate a single-crystal MEMS resonator with a controlled air-gap and resonator thicknesses. The process is based on selective epitaxy of SiGe materials and selective etching of this material over silicon. The building blocks were demonstrated in [107] and further investigations on co-processing with IC process still needs to be investigated in order to share steps and to avoid discrepancy of the IC during the process. The global process steps for metallization are further being developed in [107] with the objective to achieve a CMOS co-integration of MEMS resonator with this process.

Further process development to increase the SiGe etching selectivity over the silicon is also needed in order to reduce the silicon thinning during the releasing, which induces a mass reduction of the resonator and therefore a down-frequency shift from the targeted value. The key advantage of this process for the CMOS compatibility is the use of the SiGe, also called Silicon-On-Nothing (SON) technology already developed for advanced MOSFET [111, 112].

III.E. Conclusion

The work presented in this chapter reports on three categories of RSG MOSFET fabrication processes: (i) for out-of-plane vibrating structures, (ii) for in-plane vibrating structures and (iii) for 0-level packaging of any of the (i) structures. All the fabrication processes have been carried out successfully and experimental results will be presented in the next chapters. The developed processes enable the realization of RSG MOSFET with resonance frequencies of the order of 1-100MHz, operated with DC voltages up to 40V "

(i) Processes for out-of-plane resonators:
AlSi-based RSG-MOSFET: the process was developed based on the same platform technology used for other RF-MEMS passive components. Polysilicon and polyimide sacrificial layers deposition, CMP and release were investigated. The resulting characteristic RSG-MOSFET dimensions are an air-gap comprised between 200nm and 500nm and a gate thickness of 1.8µm. A complete study of the temperature effect on Young's modulus and stress variation for different concentration of silicon in AlSi material has been carried out. These parameters are crucial inputs for the resonator design in order to accurately predict the resonant frequency and to evaluate the frequency-induced temperature drift, which is required for temperature compensation on the circuit design level.

Silicon-based RSG-MOSFET: the process allows obtaining a self-aligned MOSFET, using SOI wafer with a silicon epitaxy to achieve an excellent control on the 50nm air-gap and on the gate thickness (1µm). A highly reproducible process using BHF and CPD to release the resonator and avoid structure sticking was successfully implemented.

(ii) 0-level thin film packaging:
A room temperature process, fully compatible with metal-based suspended structures and silicon-based SG-MOSFET was developed and used to package the AlSi-based RSG-MOSFET. Investigations on releasing holes and clogging effect for vacuum encapsulation and cavity forming underetch rates were studied. Impact of the back-end-of-line plastic molding on the packaging for various thin film cap material and thickness were performed and showed limited impact on the thin film.

(iii) Process for in-plane resonators:
Processes for lateral SG-MOSFET with vertical and horizontal MOSFET detection were investigated. A process using advanced CMOS technologies was proposed and major technological blocks were successfully demonstrated. The process uses the unique capability of selective epitaxy and selective etching of SiGe over silicon, demonstrated with the SON technology, and therefore allowing CMOS compatibility.

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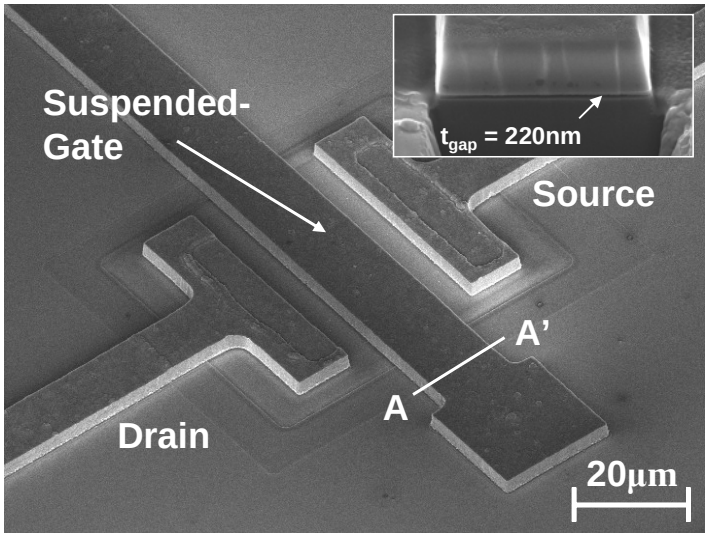
Chapter IV

Resonant SG-MOSFET characterizations



SEM picture of an AlSi-based RSG-MOSFET

Introduction

As demonstrated in chapter II, MOSFET detection of vibrating structure offers a much higher output current level due to the intrinsic MOSFET gain as compared to capacitive detection. This detection is therefore suitable for high frequency MEMS resonators for which the resonator dimensions are scaled, reducing the capacitive coupling.

Based on the analytical model of the RSG-MOSFET (Chapter II), transcripted into a VERILOG-A code and implemented in circuit simulators, the comparison of capacitive and MOSFET detection on transmission response is presented. A characterization methodology was developed for the CC-beam RSG-MOSFET to dissociate the mechanical effect from the MOSFET behavior.

AlSi and silicon-based RSG-MOSFET, described in Chapter III.A and III.B, were characterized under vacuum. The dependence of the drain and gate voltages on the resonant frequency was investigated as well at the influence on ambient pressure on quality factor. Non-linearities on the transmission response are shown. The temperature impact on resonant frequency was extracted from measurements..

The major benefit of the MOSFET detection as compared to capacitive detection is demonstrated in an oscillator circuit, designed in CMOS 65nm technology from STMicroelectronics.

IV.A. Characterization methodology

The quality factor of a flexural beam resonator is strongly dependent to air damping, as described in Chapter II. The resonators should be then either tested in a vacuum chamber or preferably encapsulated in thin film vacuum package. Measurements of the AlSi-based RSG-MOSFET were performed in a custom built vacuum chamber described in [113] where the pressure can be controlled from 10^{-6}Torr to 760Torr and the temperature from 25°C to 100 °C. Tungsten probes are embedded in the chamber and connected to the equipment through hermetic SMA connectors. Measurements of the silicon-based RSG-MOSFET were performed on a dedicated SUSSMicrotech® PMC150 vacuum chamber. This equipment allows RF probing with coplanar G-S-G probes combined with DC probing, with a temperature range from -277°C to 100°C and a chamber pressure from atmospheric to 10^{-6} Torr. Both impedance and transmission measurements of the signal through the resonator were performed, being part of the characterization methodology.

IV.A.1. Capacitive and MOSFET detection characterizations

In resonator with capacitive detection, the transmitted signal through the resonator can be sensed either on the resonating structure or on the actuation electrode (see Chapter II.B.5) and one port and two port measurements techniques are classically used to characterize MEMS resonators with capacitive detection [81]. For the RSG-MOSFET however, the structure is not symmetrical and the input signal is applied to the gate and the output current is sensed in the drain. The interesting part of the RGS-MOSFET characterizations is the evaluation of the MOSFET gain and the comparison with a capacitive detection of a resonator with similar dimensions. A characterizations method has been developed to compare the capacitive and the MOSFET responses from the same vertical flexural RSG-MOSFET, as seen in Fig. 64 and Fig. 65. The bias-T circuit, in Fig. 64, is composed of a capacitance which stops all AC signal towards the DC source and an inductance to stop all DC signal towards to the analyzer. The proposed methodology considers a 1-port characterization setup to evaluate the capacitive response of a RSG-MOSFET (Fig. 64).

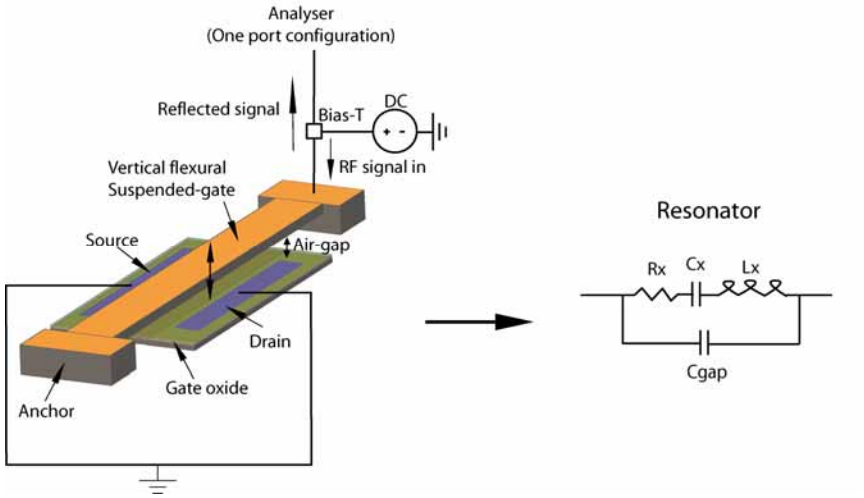


Fig. 64 Schematic of the proposed 1-port characterization technique for the RSG-MOSFET pure capactive response

A 2-port technique is used to measure the transmission from the input gate signal to the output drain from which the MOSFET gain can be extracted.

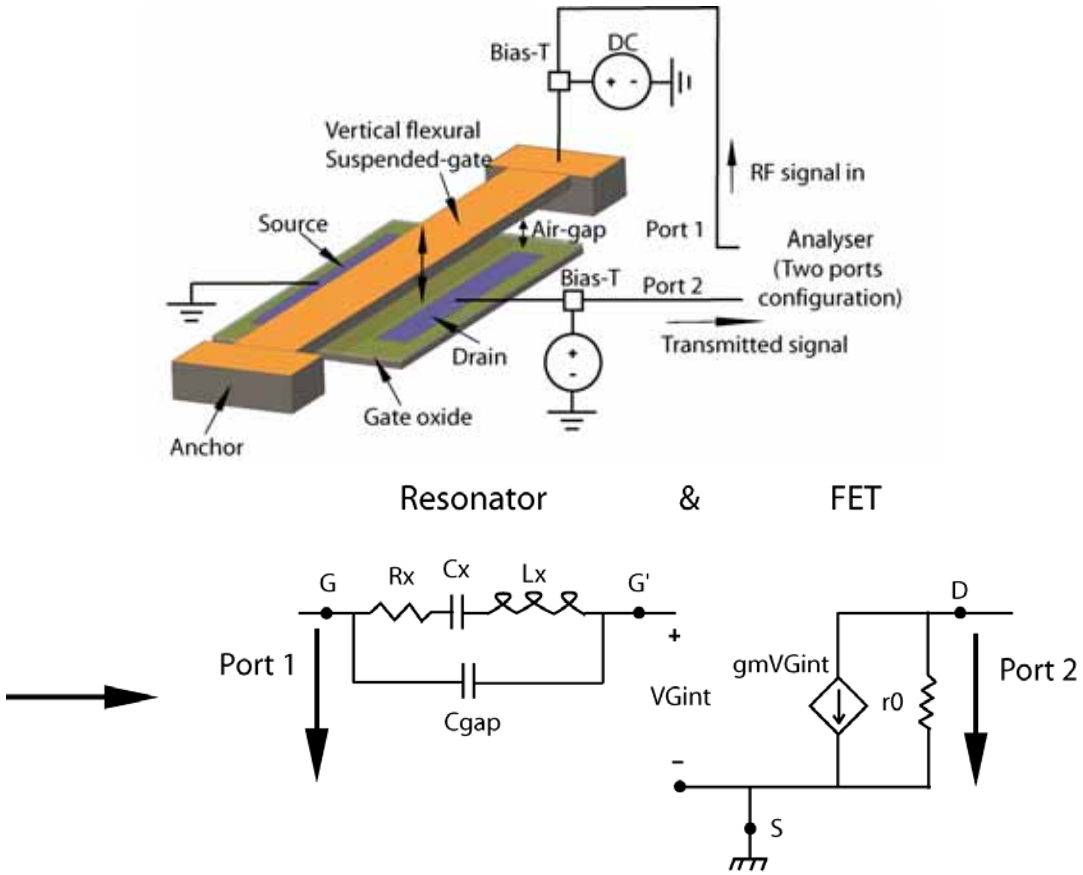


Fig. 65 Schematic of the proposed 2-ports characterization technique for a RSG-MOSFET indlucing the effec of the MOSFET detection

IV.A.1.a. Capacitive response of a RSG-MOSFET

The one port characterization technique is measuring the signal reflection sent from a network analyzer. The analyzer injects a signal to the vibrating gate and compares this signal amplitude with the reflected signal sensed at the same port, as expressed in (IV - 1).

$$S_{11} = 10\log\left(\frac{P_{reflected}}{P_{in}}\right) = 20\log\left(\frac{V_{reflected}}{V_{in}}\right) \qquad \text{(IV - 1)}$$

The electrostatic excitation is created between the gate and the channel of the transistor. To consider a pure capacitive detection of the RSG-MOSFET, the channel surface potential must be constant under the AC variation. By connecting the source, drain and bulk to the ground, the transistor behaves as a capacitor and the surface potential is considered constant in the accumulation regime and in the strong inversion regime [114]. In accumulation, the surface potential is null and in strong inversion it is equal to two times the Fermi potential Φ_F (Fig. 66). In both cases, the channel can be considered as an electrode with a fixed potential.

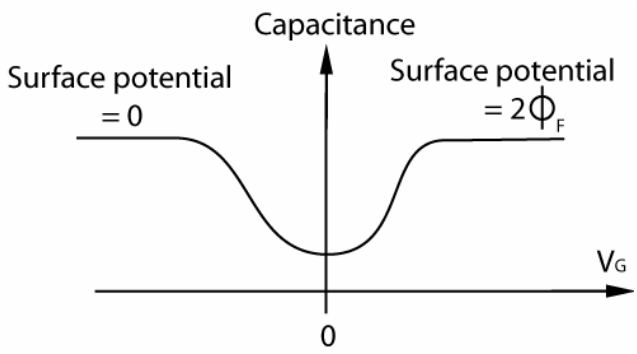


Fig. 66 MOSFET capacitance for different gate voltages and related surface potentials

To extract the capacitive response from the RSG-MOSFET, a positive or negative DC polarization voltage is added to the output signal of the analyzer (Fig. 64), in order to place the channel in accumulation or in strong inversion. At the mechanical resonance, the impedance of the resonator is low, therefore inducing a high transmission response and low reflection amplitude, as seen in Fig. 67. The amplitude of the reflection peak is related to the applied DC gate voltage, increasing the gap capacitance and the drain current. The reflection bandwidth around the resonant frequency is small for a high Q resonator.

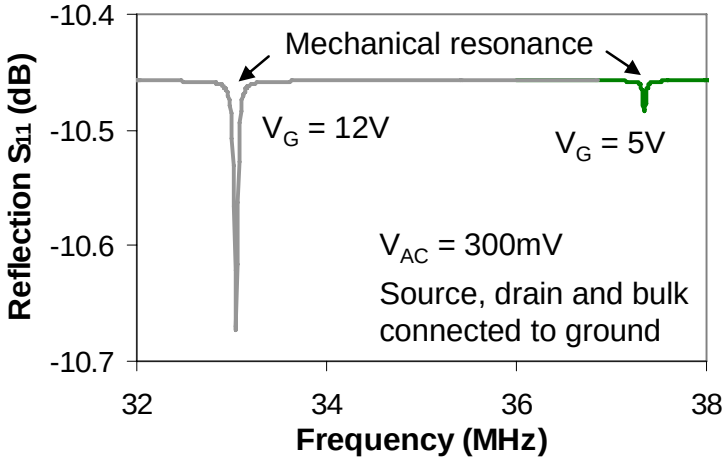


Fig. 67 Simulated 1-port reflection response of a RSG-MOSFET with dimensions described in Table XI (device 1). The EKV-based model is used for this simulation

IV.A.1.b. Transistor response and gain of the RSG-MOSFET

The FET amplification behavior can be extracted from a two port measurement of the RSG-MOSFET. The excitation signal from the analyzer is applied to the suspended-gate and the drain current is sensed across the analyzer output impedance. The resulting voltage variation across the 50Ω output impedance is compared to the applied signal amplitude on the gate. The transmission response is then functions of the intrinsic gain of the transistor and is related to the small signal analysis developed in Chapter II.B.5.b.

$$S_{21} = 10\log\left(\frac{P_{out}}{P_{in}}\right) = 20\log\left(\frac{gmV_{G\,\mathrm{int}}\,r_0}{V_{in}}\right) \qquad \text{(IV – 2)}$$

The gain of the RSG-MOSFET is function of the applied gate voltage as shown in Fig. 68, where the DC operating points are presented on the I_D-V_G curve of a SG-MOSFET.

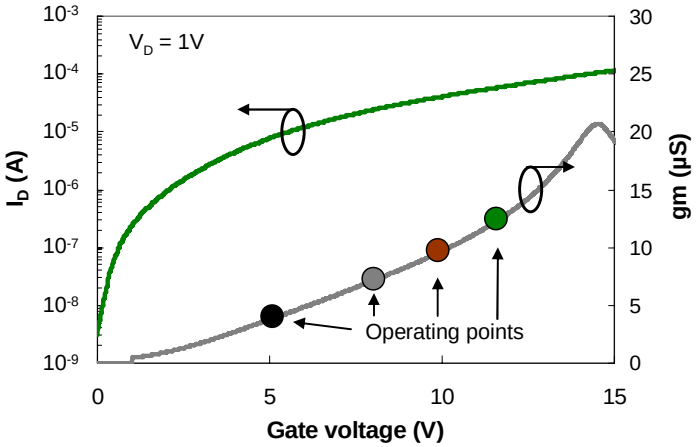


Fig. 68 Simulated I_D-V_G and gm-V_G characteristics of a RSG-MOSFET with dimensions described in Table XI (device 1). The EKV-based model is used for this simulation

The transmission responses for a CC-beam RSG-MOSFET relatively to these operating points are shown in Fig. 69. The simulation setup is similar to the one presented in Fig. 65 and considers that the output drain current is sensed at a 50Ω resistance, referred as the input impedance of the analyzer.

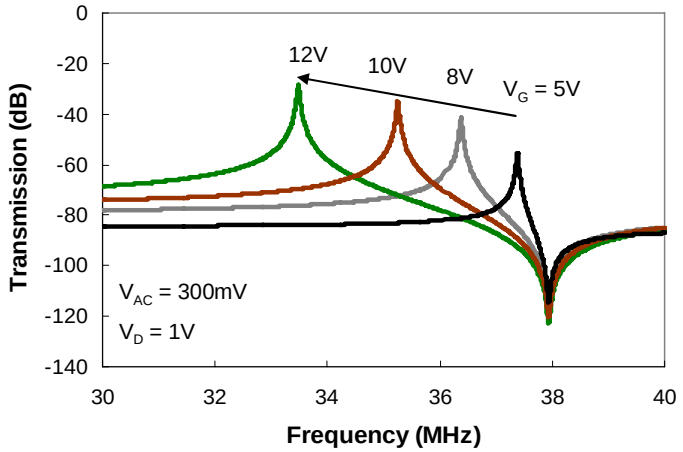


Fig. 69 Simulated transmission response of a RSG-MOSFET with dimensions described in Table XI (device 1). The EKV-based dynamic model is used for this simulation

The level of transmitted signal is directly related to the gain of the transistor and increases for a higher gate voltage. Note that, as expected, the resonant frequency shifts down (from 2.7% for V_G = 8V to 10.4% for V_G = 12V) when increasing the gate voltage, and the shift is more important when approaching the pull-in voltage of 21V. The excitation signal on the gate was set to 300mV in these simulations, and placing the RSG-MOSFET at the operating point with a maximum gain, the output signal amplitude level is up to -29dB, related to a peak of 100mV. Table XI synthesizes all dimensions and parameters for the simulated and measured RSG-MOSFET.

Parameters	Source	Resonator	Resonator	Resonator	Resonator	Units
		Device 1	Device 2	Device 3	Device 4	
CC-beam material	Given	Si	AlSi1%	AlSi1%	Si	-
Resonator beam length, L_{beam}	Layout	15	34	34	15	µm
Resonator beam width, W_{beam}	Layout	6	6	6	6	µm
Resonator beam thick., H_{beam}	Measured	1	1.8	1.8	1	µm
MOSFET dimensions, W/L	Layout	13/4	30/4	30/4	13/4	µm
MOSFET oxide thickness, t_{ox}	Layout	20	40	40	20	nm
Young's modulus	Measured	160	48	48	160	Gpa
Film stress (tensile)	Measured	0	80	80	0	Mpa
Initial air-gap, d	Measured	50	300	300	50	nm
Young's modulus, E	Measured	165	48	48	165	Gpa
Calculated Pull-in voltage	Calculated	20.8	81	81	20.8	V
Applied gate voltage	Given	5-15	11	30	0.3-2	V
Quality factor	Giv/Meas.	1000	1200	1200	30	-
Calc. resonant freq /gate volt.	Calculated	38.4	7.26	6.37	38.4	MHz
Meas. resonant freq /gate volt	Measured	-	7.06	6.15	33.6	MHz
Variation freq meas./calc.	Calculated	-	2.75	3.45	12.5	%
Measurement pressure	Measured	10^{-5}	10^{-5}	10^{-5}	10^{-5}	Torr

Table XI. Resonant SG-MOSFET design summary

By scaling down the gate width (channel length) to 1µm, the output amplitude reaches 480mV while keeping the same resonant frequency. This result means that the RSG-MOSFET can generate enough gain to build up an oscillating system on its own, if providing another 180 degrees phase shift to fulfill the Barkhausen criteria. A similar result was demonstrated based on the coupling of two Resonant Gate Transistors (RGT) [2] to generate enough gain to compensate of the high motional resistance.

IV.A.2. Comparison of capacitive and MOSFET detection on transmission response

A comparison study between signal transmission level between a capacitive and a MOSFET detection is presented in Table XII. This table shows that even for a relatively large structure (channel length of 4µm) the MOSFET detection has a much higher output signal than the capacitive detection. If the channel length is reduced to 1µm, with the same channel width of 15µm, simulations have shown that the amplitude of the MOSFET detection can even provide a 25dB higher signal than the capacitive detection.

Gate voltage	5V	8V	10V	12V
Capacitive detection, amplitude peak (mV)	2.1	6.1	11.2	20.3
MOSFET detection, amplitude peak (mV)	1.4	8.3	28.2	37.3

Table XII. Signal transmission level for the device 1 in Table XI

N.B.: For certain operating points with low transistor gain, and for a large channel length, the output signal amplitude of the MOSFET detection could be lower than the capacitive detection (gate voltage of 5V in Table XII for the specific resonator dimensions of device 1).

IV.A.3. Characterization setup for bulk-mode RSG-MOSFET

As developed in Chapter III, a lamé-mode lateral resonator with a horizontal MOSFET detection is currently under development with a front-end technology. It has been shown in [25] that this geometry allows very high quality factor due to the low thermoelastic damping. For this resonator topology, the actuation and the detection can be decoupled. Two symmetrical electrodes are actuating the resonator on each side, and a third electrode can be used for the capacitive detection whereas a lateral MOSFET is defined on the fourth side of the resonator, as described in Fig. 70.

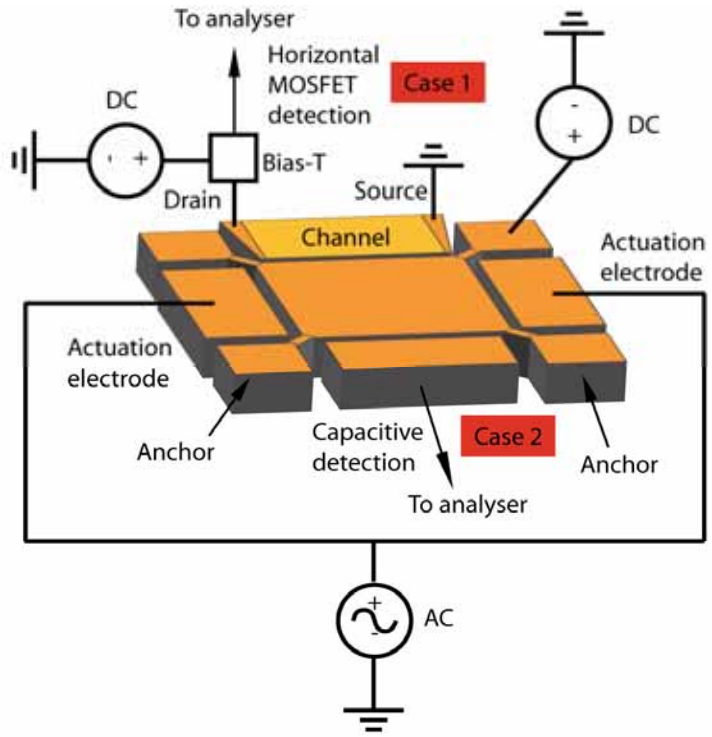


Fig. 70 Schematic of a capacitive and MOSFET detections for a Lamé-mode resonator

The MOSFET detection setup is referred as “Case 1” and the capacitive detection setup as “Case 2”, while the DC and AC polarization remains identical for both setups. A particularity of “case 1” is that the gate is polarized with a DC voltage; therefore the MOSFET senses only the pure mechanical displacement of the gate, and not the AC signal variations.

IV.A.4. Insertion loss and impedance matching

The motional resistance of a capacitive resonator is strongly dependent to the air-gap, as seen in (IV-3), and is equal to 240kΩ for a 38MHz silicon flexural CC-beam resonator with

dimensions described in Table XI (device1), taking an arbitrary quality factor of 1000, in line with the value calculated in Chapter II and an polarization voltage of 20V.

$$R_x \propto \frac{d_0^4}{\omega Q V_p^2 S^2} \qquad \text{(IV - 3)}$$

The analyzer input and output impedances are Z_{in} and Z_{out} = 50Ω. When connected to the resonator, the strong mismatch between the resonator and the analyzer impedances strongly reduces the transmission level, at the mechanical resonance. The insertion losses can be calculated from the ratio between the maximum voltages at the analyzer nodes, considering the motional resistance given by the resonator, and the same voltage when the resonator is short-circuited, as expressed in (4). The insertion loss (I.L.) of a 240kΩ motional resistance resonator is -73dB.

$$I.l. = 20\log\left(\frac{Z_{out}}{Z_{out} + R_x}\right) \qquad \text{(IV - 4)}$$

Proper terminations with impedance matching network have shown [81, 115] that resonator losses less than 1dB. In the case of the RSG-MOSFET, the output impedance seen by the analyzer from the Device Under Test (DUT) is directly related to the channel resistance (Fig. 65). In accumulation, the resistance is very high and therefore inducing a high insertion loss, whereas in inversion the channel conducts and its resistance is reduced.

IV.A.5. Practical characterization methodology

Due to the very high impedance mismatch between the analyzer and the resonator, the signal transmission level is low and consequently the resonant frequency is hardly detectable with the transmission S_{21} response spectrum. The use of an impedance analyzer is therefore interesting to detect more easily the resonant response. In a second phase, network analyzer measurements are mandatory to obtain the transmission and reflection parameters, used to dissociate the influences of the drain and gate voltages on the response.

IV.A.5.a. Impedance measurement setup

Impedance analyzer was used to measure the output impedance of the RSG-MOSFET, which can be small or high depending on the MOSFET operating regime. The Agilent 4294A impedance analyzer is suitable for impedance measurement comprised between 1mΩ to 100MΩ, at a frequency ranging from 40Hz to 110MHz. A four-terminal pair cable configuration was used to avoid any capacitive coupling between the cables, which eventually limit the possible impedance range measurement. Six different impedance measurement techniques co-exist on the market; therefore the auto-balancing bridge method used in this equipment is explained in Fig. 71 for a better understanding.

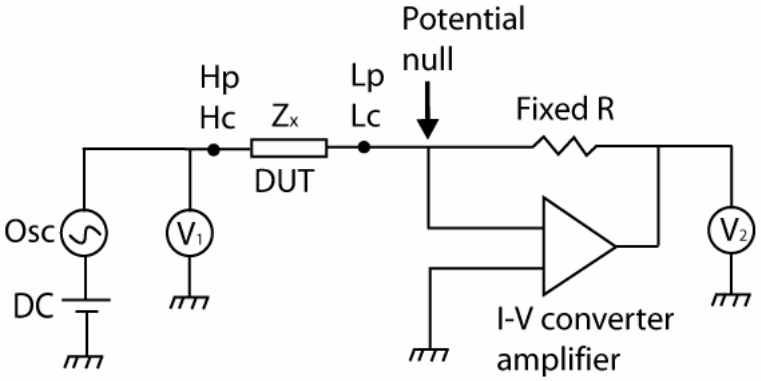


Fig. 71 Schematic of the auto-balancing bridge impedance measurement method

The AC signal, coupled with a DC bias is injected to the DUT through the High Current-High Potential (H_c, H_p) terminal. The drain current of the RSG-MOSFET is fed into a resistor. In order to measure the voltage drop across that resistor, a feedback loop composed of an I-to-V converter amplifier creates a zero potential at the low terminal (Low Current Lc-Low Potential Lp). The auto-balancing bridge balances the resistor (R) current with the DUT current to maintain the zero potential [116]. The resulting impedance measurement follows the equation (IV - 5).

$$Z_X = R\frac{V_1}{V_2} \qquad \text{(IV - 5)}$$

Single ended tungsten probes were used for the RSG-MOSFET measurements, as depicted in Fig. 72. The analyzer output (H_c, H_p) feds the AC signal with the DC bias to the RSG-MOSGET gate and the input is connected to the (L_c, L_p) to the drain. The source and the bulk of the MOSFET are grounded by the impedance analyzer.

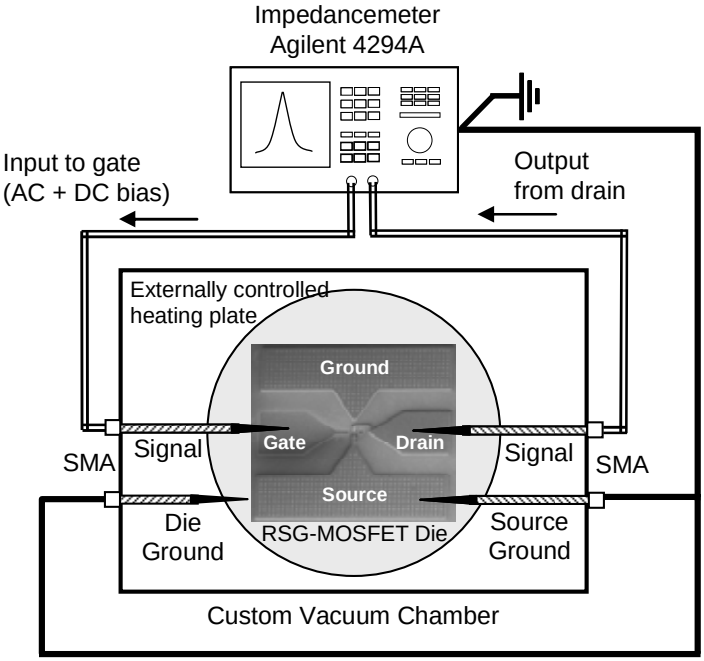


Fig. 72 Test setup for impedance measurement with single-ended tungsten probes

IV.A.5.b. Transmission measurement setup

The transmission setup is presented in Fig. 73 where GSG (Ground Signal Ground) RF probes are used, connected to a network analyzer HP8753D. The analyzer is suitable for frequency measurement between 30kHz and 3GHz. Polarization voltages are set with external voltage source connected to the network analyzer by its internal bias-T (represented externally in Fig. 73 for more clarity). The SG-MOSFET gate and drain are respectively connected to the output and input of the analyzer. The SOLT (Short, Open, Load and Through) protocol was used to remove the capacitances and inductances coming from the cables and the RF probes. The network analyzer internally subtracts the parasitic from the detected signal.

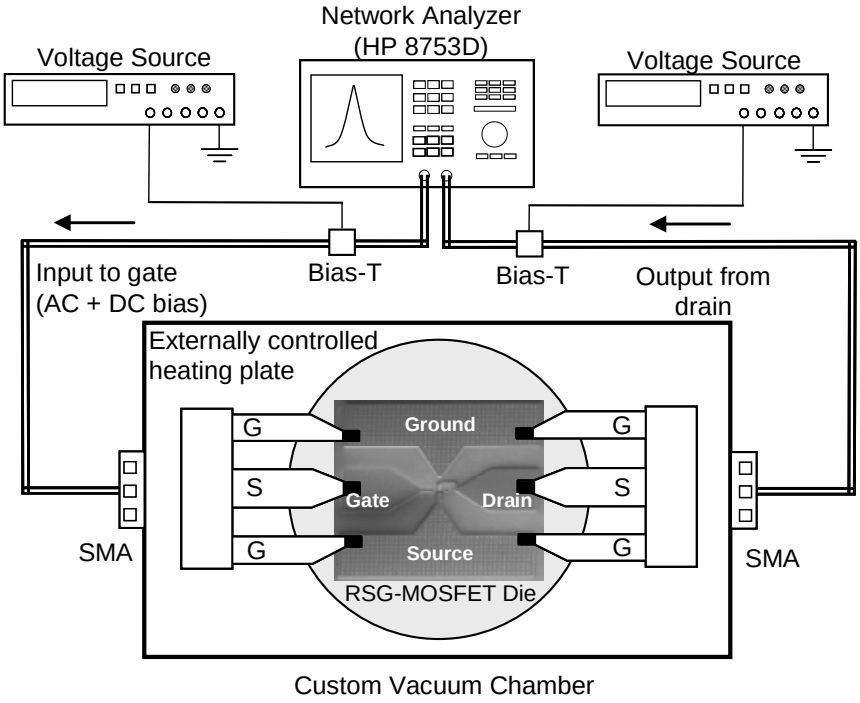


Fig. 73 Test setup for transmission measurement with RF probes

IV.B. AlSi-based Resonant SG-MOSFET characterizations

AlSi1%-based RSG-MOSFETs with natural resonant frequency from 5MHz to 90 MHz were measured with both setups. According to its FET behavior, the RSG-MOSFET can be actuated from weak to strong inversion depending on the applied gate voltage. The impedance and transmission responses are therefore strongly dependent to the DC operating point. Like for standard MOSFETs, for a required gate voltage, the operating regions can be designed by properly choosing the channel doping and therefore setting the threshold voltage.

The dimensions of the measured RSG-MOSFET are presented in Table XI. Note that the measured and simulated resonant frequencies differ of around 4%. This difference can be explained by the AlSi thickness uniformity over the wafer, for which the mean value is 1.8µm and the thickness variation is +/- 5%. This thickness variation induces a frequency shift of +/- 360kHz on a resonator centered at 7.2MHz.

IV.B.1. Quasi-Static characterizations

Quasi-static measurements of device 2 in Table XI are presented in Fig. 74 and show the weak to strong inversion regions on the I_D-V_G curve for various V_D (500mV to 3.5V) performed with a HP4155 equipment. The weak inversion operation allows having the maximum drain current variation for a low variation of AC gate voltage, meaning the maximum displacement sensitivity. The strong inversion region reduces the sensitivity but is characterized by a large output current. The threshold voltage is measured to be V_{th} = 3.9V for this device

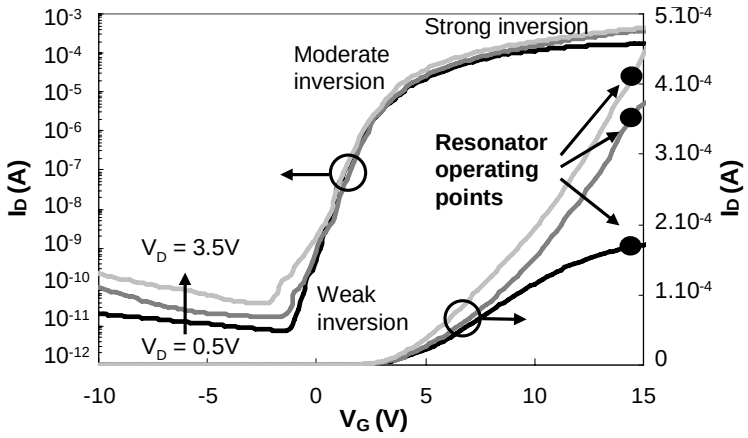


Fig. 74 Measured I_D-V_G characteristics of the device 2 (Table XI)

IV.B.2. Influence of the gate and drain voltages on the RSG-MOSFET response

Strong inversion MOSFET operation was studied and resonant frequencies were measured using both impedance and transmission measurement techniques. According to Fig. 74, the gate voltage needed for strong inversion operation of the device 1 is larger than 7V. Fig. 75 shows the peak resonances of the RSG-MOSFET in strong inversion for polarization voltages varying from 11V to 15V using the setup of Fig. 72.

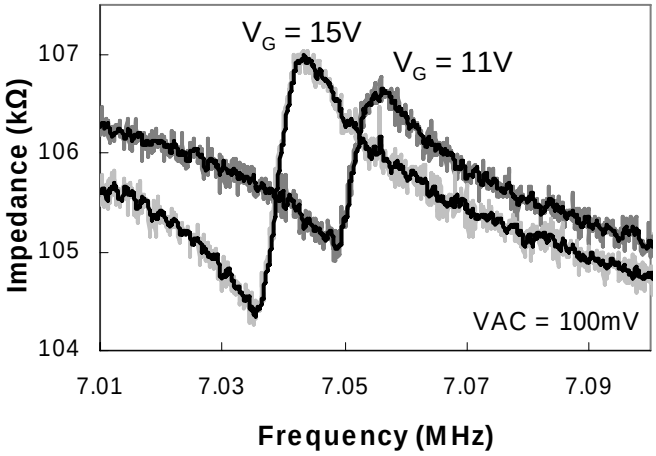


Fig. 75 Measured impedance response of the device 1 in Table XI

The impedance of the RSG-MOSFET is centered at 106kΩ. This impedance is the sum of the channel resistance but also includes the transistor access resistance. With the non self-aligned process used in the fabrication of AlSi-based resonator, the transistor access resistance strongly depends on the gate to channel overlapping area and therefore can be slightly different from die to die.

The transmission responses of the same device are presented in Fig. 76 and Fig. 77, for a gate voltage varying from 20V to 25V with a drain voltage varying from 1V to 4V using the setup of Fig. 73. One can note that, as expected, the transmission is maximal at the minimal impedance. The transmission amplitude response is low due to the relatively high resonator impedance and to the large air-gap, as described in Chapter II.B.5.a.

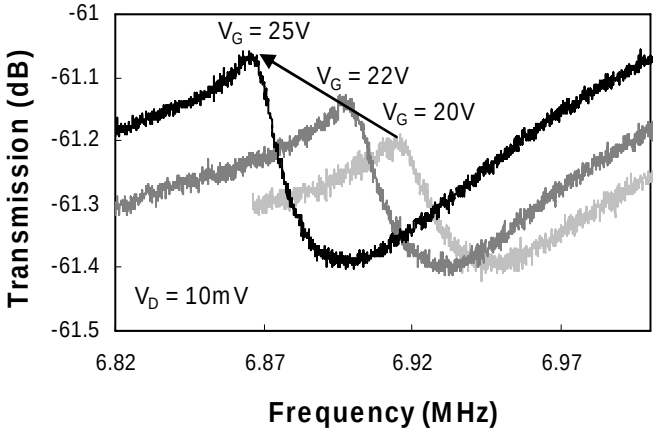


Fig. 76 Measured transmission response for various gate voltages and a constant drain voltage of 10mV with an input power of 10dBm (device 2 in Table XI)

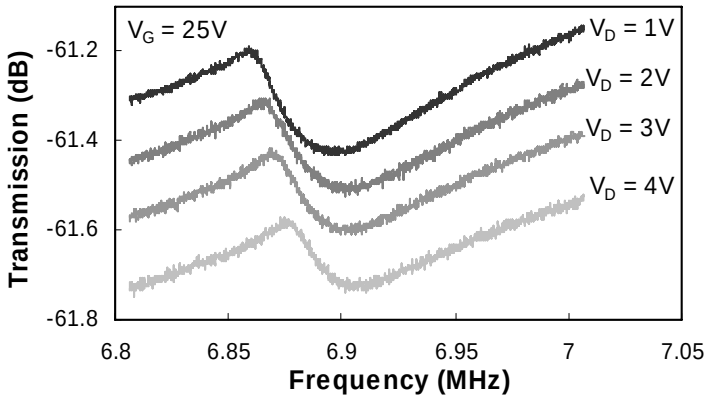


Fig. 77 Measured transmission response for different drain voltages with a constant gate voltage of 25V with an input power of 10dBm (device 2 in Table XI)

IV.B.2.a. Effect of gate voltage variation

As expected by the model, the gate voltage has a strong impact of the electrical rigidity as shown in Fig. 76. Increasing the gate voltage, increases the electrostatic field but acts as a negative rigidity, shifting down the resonant frequency (see Chapter II.B.3.b). The amplitude response is larger for a higher gate voltage, due to the larger mechanical displacement inducing an air-gap reduction.

IV.B.2.b. Effect of drain voltage variation

More interestingly, the drain voltage slightly impacts the frequency response by shifting down the resonant frequency. The drain voltage plays therefore a role in the total electrostatic force acting on the gate. Applying a positive V_D lowers the electrostatic potential between the gate and the drain region, and acts oppositely to the electrical rigidity, shifting down the resonant frequency, as shown in Fig. 78. The influence of fringing fields created between the gate and the drain is the most plausible hypothesis to explain this phenomenon. The impact of fringing fields on electrostatic behavior has previously been demonstrated on MEMS capacitor [117-119], which strengthen this hypothesis.

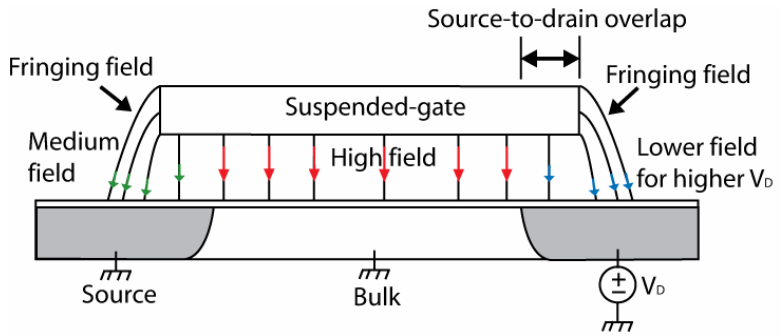


Fig. 78 Fringing field effect on the RSG-MOSFET electrostatic actuation

As shown in Fig. 77, increasing the drain voltage lowers the transmission level. This level is governed at the first order by the static air-gap capacitance C_{gap}, dominating outside the resonance. Increasing the drain voltage impacts the fringing field and reduces the electrostatic force in the drain region. This electro-mechanical effect can be directly connected to the reduction of the air-gap capacitance and to a lower signal level.

The gate and drain voltage-frequency relationship is presented in Fig. 79. The resonant frequency shifts quasi-linearly with the voltage variations and the slope is 5.53kHz per volt of drain voltage and 9.01kHz per volt of gate voltage is extracted from the measurements.

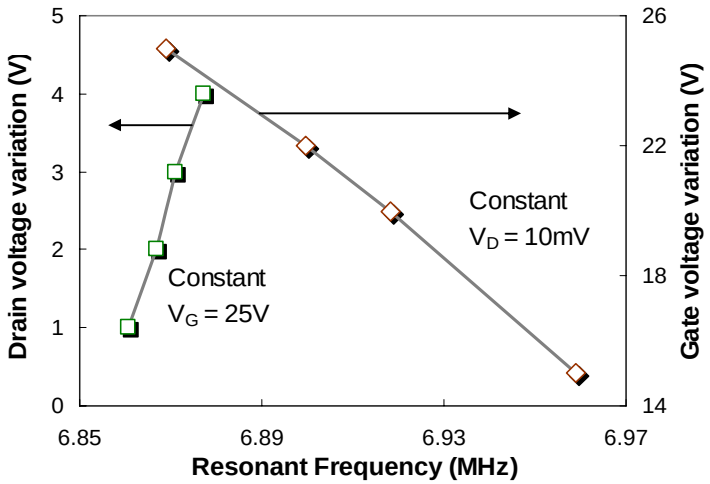


Fig. 79 Resonant frequency shifts with the gate and drain voltage variations, device 2 in Table XI

IV.B.3. Non-linearities

Electrical non-linearities were observed on impedance measurement characteristics (Fig. 80) when applying a large AC signal (200mV) with a constant polarization gate voltage of 30V. This non-linear phenomenon is compared to the linear response when applying an 80mV AC voltage. The typical non-linear behavior is in line with model developed in Chapter II.B.3, and is characterized by the abrupt increase of the impedance and phase (Fig. 81) response at the resonance.

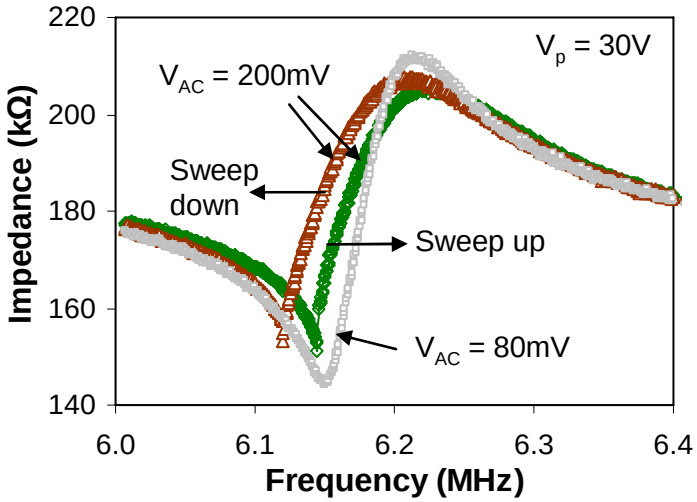


Fig. 80 Measured linear and non-linear impedance response of device 3 in Table XI

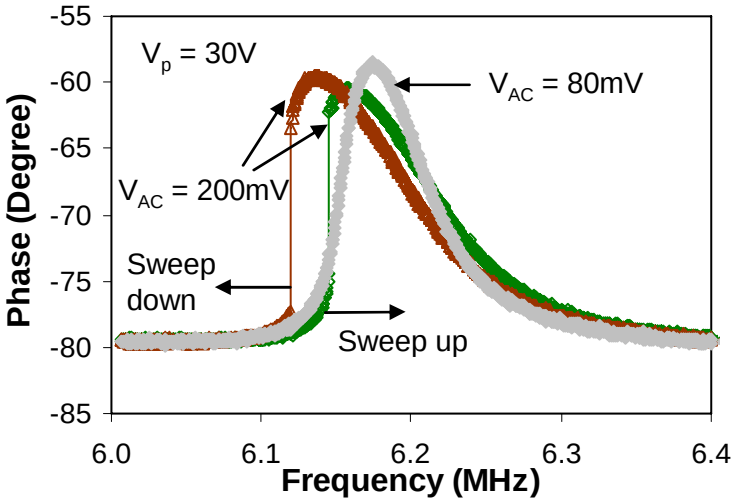


Fig. 81 Measured linear and non-linear phase response of device 3 in Table XI

IV.B.4. Effect of air damping on quality factor

The quality factor has been extracted from impedance measurements on the device 2, taking the bandwidth at half of the resonant peak. Extracted value gives a loaded Q of 1200, relatively low compared to free-free beam or bulk-mode resonators [23, 120], due to the CC-beam geometry and the suspended-gate alloy material inducing large thermoelastic losses in

the structure (see Chapter II.B.4). The quality factor stays constant when the pressure drops under 2 Torr and then decreases quasi-linearly with increased pressure, as shown in Fig. 82, in accordance with the values found in [121]. The measured loaded Q is related to the impedance mismatch between the resonator and the analyzer as:

$$Q_{loaded} = Q_{resonator} \frac{R_m}{R_m + Z_{load}} \qquad \text{(IV - 6)}$$

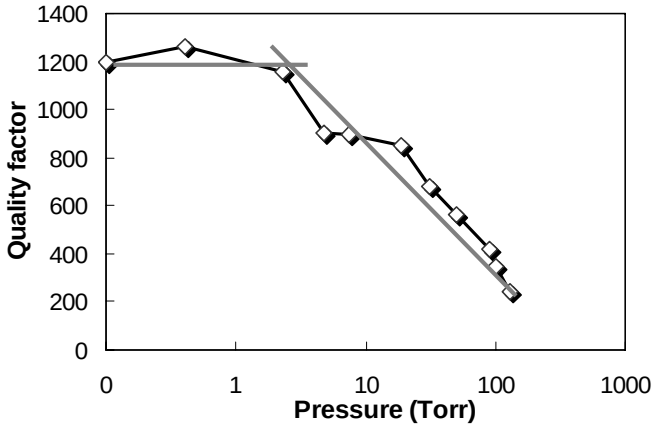


Fig. 82 Quality factor dependence on environmental pressure of device 2 (Table XI)

The 0-level thin film vacuum packaging developed in Chapter III (10^{-7}mBar) is therefore suited for the RSG-MOSFET, according to these measured characteristics where the vacuum limit is around 1mBar.

IV.B.5. Temperature effect

Resonant frequency shift due to temperature variation is presented in Fig. 83 where the RSG-MOSFET exhibits a quasi-linear frequency drift of 4.68 KHz/°C from 20 °C to 70 °C which corresponds to a Temperature Coefficient of Frequency (TCF) of -219ppm/°C. The frequency drift of the metallic RSG-MOSFET is large compared to silicon resonator, due to its large thermal expansion coefficient mismatch of $\alpha_{AlSi}=21*10^{-6}K^{-1}$ compared to $\alpha_{si}=2.68*10^{-6}K^{-1}$ for silicon.

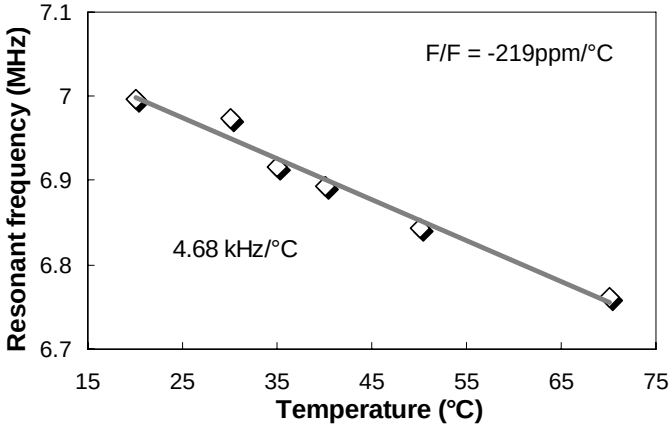


Fig. 83 Resonant frequency drift with temperature of device 1 (Table XI)

IV.B.6. Impact of resonator scaling on voltage-frequency dependency

Other AlSi-based resonators with various beam length and width were measured, and the effect of resonator scaling is observed on the frequency-dependence to the gate voltage, as shown in Table XIII. The beam size reduction is directly related to the beam stiffness and reduces the frequency dependence on the gate voltage. The frequency shift per volt for a 5.3MHz resonator is 0.088% and decrease to 0.011% for a 91MHz resonator. The absolute frequency variation is however larger for a high frequency resonator. In reference oscillator application, this effect requires a stable voltage source to control the accurately the gate voltage.

Resonant Freq	Resonator dimensions (length, width, thickness)	F per gate voltage variation	F per gate voltage variation
5.3MHz	40µm, 10µm, 1.8µm	4.64kHz	0.088%
9.31MHz	29µm, 6µm, 1.8µm	4.16kHz	0.045%
91.5MHz	9.5µm, 8µm, 1.8µm	10.6 kHz	0.011%

Table XIII. AlSi1%-based RSG-MOSFET performance summary

IV.C. Silicon-based Resonant SG-MOSFET characterizations

Silicon-based RSG-MOSFETs were fabricated with a self-aligned process and a small controlled air-gap of 50nm. In order to define the influence of the process on standard MOSFET behavior, transistors without air-gap and transistor with air-gap were tested on the same wafer.

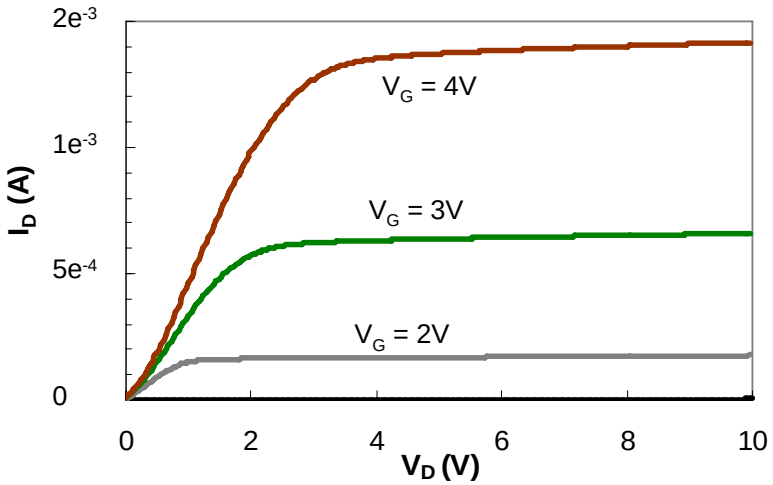


Fig. 84 Measured I_D-V_D characteristics of a MOSFET without air-gap, fabricated with the same fabrication process than the SG-MOSFET (W/L = 6 µm/20µm, T_{ox} = 50nm)

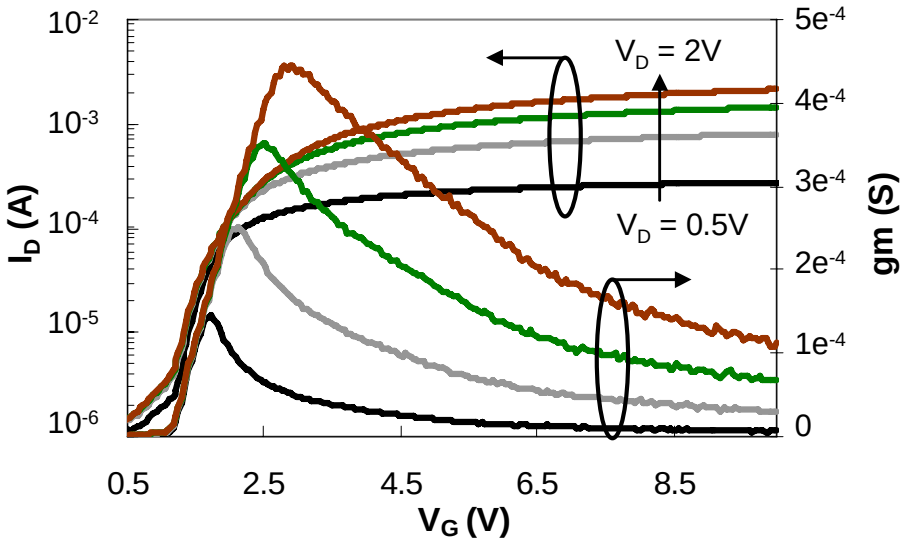


Fig. 85 Measured I_D-V_G and gm-V_G characteristics of a MOSFET without air-gap, fabricated with the same fabrication process than the SG-MOSFET (W/L = 6 µm/20µm, T_{ox} = 50nm)

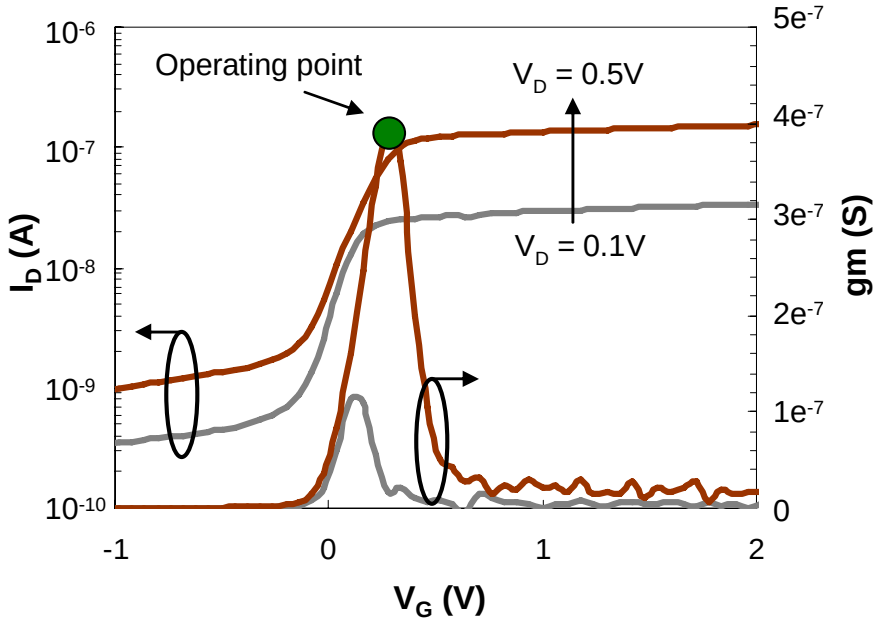


Fig. 86 Measured I_D-V_G and gm-V_G characteristics of a RSG-MOSFET (device 4, Table XI)

Due to the presence of air-gap, the transconductance Gm is reduce by more than two decades. The threshold voltage extracted from the I_D-V_G characteristic is V_T = 0.1V According to the DC characteristics of Fig. 86, dynamic measurements where performed on the same structure (Fig. 87) at the DC operating with a maximum gain.

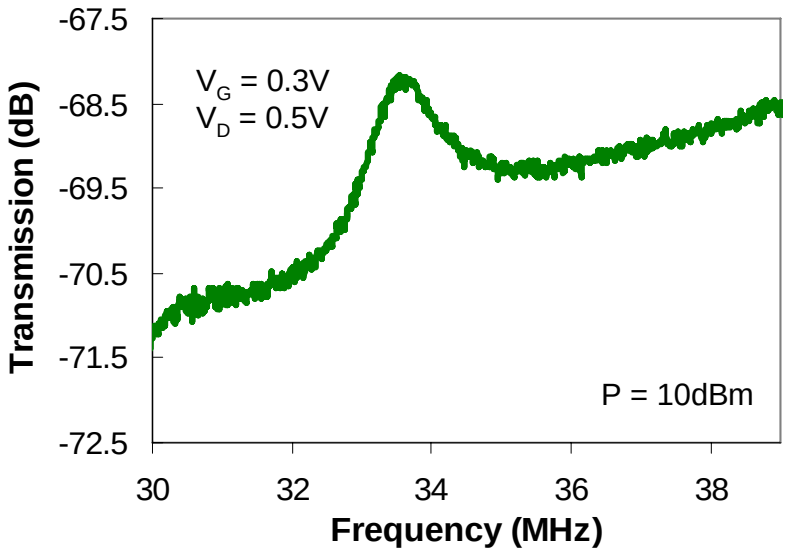


Fig. 87 Measured transmission characteristics of a silicon RSG-MOSFET with dimensions of L_{beam} = 15µm, W_{beam} = 6µm, H_{beam} = 1µm, gap = 50nm, T_{ox} = 20nm W/L = 13/4µm (device 4)

A frequency close to the target frequency of 38.4MHz was obtained, but due to the technological issue described in Chapter III, the extracted quality factor is low (Q~40). The influence of the gate voltage and drain voltage on the signal level and amplitude response is presented in Table XIV.

V_G	V_D	Signal level (dB)	Peak amplitude (dB)
0.3	0.5	-68.2	1.09
1	1	-59.4	0.57
2	0.1	-56.2	0.5
2	0.5	-55.4	0.4
2	2	-53.3	0.21

Table XIV. Output signal level and peak amplitude of the RSG-MOSFET described in Table XI (device 4)

The conclusions of this study for the silicon-based RSG-MOSFET are similar to the one expressed for the AlSi-based resonator:

- The amplitude peak is maximal at the DC operation point with a maximal transconductance
- When V_G increases, and for the same V_D, the signal level increases due the higher output current

IV.D. Oscillator design

The major application of MEMS resonators is the integrated time reference. Different MEMS oscillators were demonstrated in the past year, using comb drive structures [122], flexural beams [123] and bulk-mode resonators [29, 65, 124, 125]. The sustaining oscillator circuits are mainly based on transresistance amplifier to compensate for the motional resistance of the capacitive resonator at the mechanical resonance. The high motional resistance of these structures is the most limiting aspect to build an oscillator and the research has been focused on this aspect. Innovative architecture, as mechanically coupled resonator were used for this purpose [126] and a strong technological effort was observed on the air-gap reduction [1] (see Chapter II.B.5.c).

Due to its intrinsic low input impedance and gain, the RSG-MOSFET architecture can be advantageously used in oscillator circuit design. To validate the advantage of the MOSFET detection over the capacitive detection, two different oscillator circuits were designed based on building blocks developed in the CMOS 65nm technology from STMicroelectronics. Each circuit is dedicated to a detection type and the comparison between the MEMS capacitive resonator and RSG-MOSFET was done based on the amplifier gain needed to obtain sustaining oscillations. Resonators with similar dimensions were used in this study (device 4 of Table XI). The simulations were performed on Cadence® using Spectre® solver.

IV.D.1. Capacitive MEMS-based oscillator

A Verilog-A code was used to model the capacitive MEMS resonator and implement it as an instance in the circuit. The capacitive MEMS-based oscillator is presented in Fig. 88 where a differential transresistance amplifier (TransRes) is used to compensate for the motional resistance. The second Barkhausen criterion for stable oscillation is that the sum of the phase shift of each element in the loop should be equal to 360°. The resonator with a quality factor of 1000 induces a 90° phase shift, the circuit elements provide the remaining phase shift. The applied voltage used for these simulations is V_{DD} = 1.8V, defined by the technology. An external V_{DC} polarization voltage is applied to the resonator.

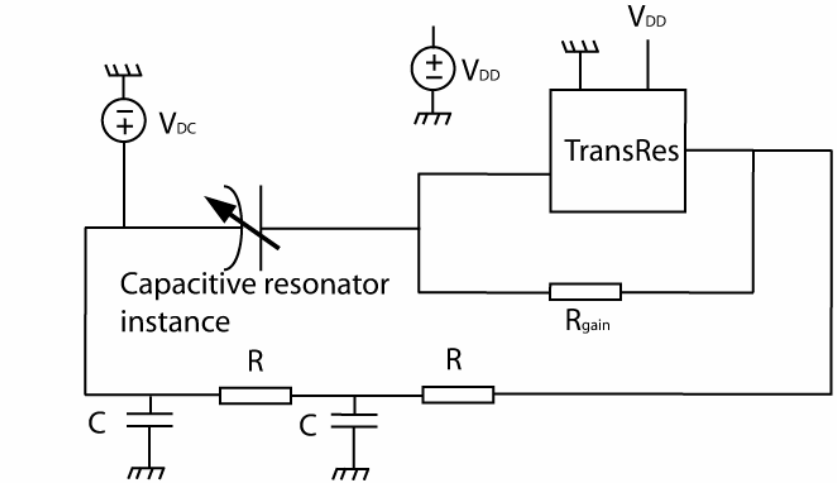


Fig. 88 Circuit schematic of a capacitive MEMS resonator-based oscillator

The minimum gain required to sustain oscillations was found to be 350kΩ, and the resulting output waveform is shown in Fig. 89. Starting of the oscillator is realized by unbalancing the loop with a voltage pulse. As a consequence, the timeline in the waveform do not refer to any start-up time. The resonator polarization is $V_{DC} = V_P = 8V$.

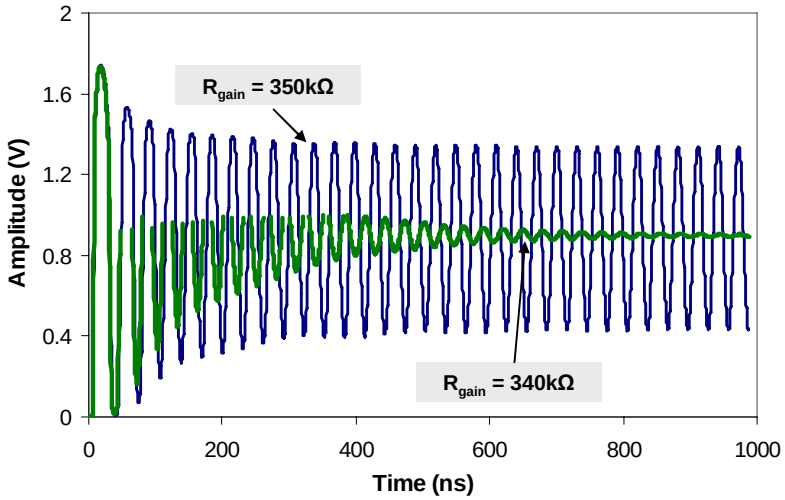


Fig. 89 Transient response of the capacitive MEMS-based oscillator for two different gains

IV.D.2. RSG-MOSFET based oscillator

The oscillator designed for the RSG-MOSFET, also uses basic non-optimized building blocks from the CMOS65 library of STMicroelectronics. Compared to the previous circuit, it includes a Common Mode FeedBack (CMFB) in the loop to limit the signal amplitude and avoid any non-linearities due to the saturation of the transistor in the transresistance amplifier. This feedback loop does not however introduce any gain in the loop, which is only defined by the resistor R_{gain}. The RSG-MOSFET used in this simulation is similar to the one in Fig. 68, at a DC operating points of $V_{DC} = V_G = 8V$, related to a transconductance of 7µS.

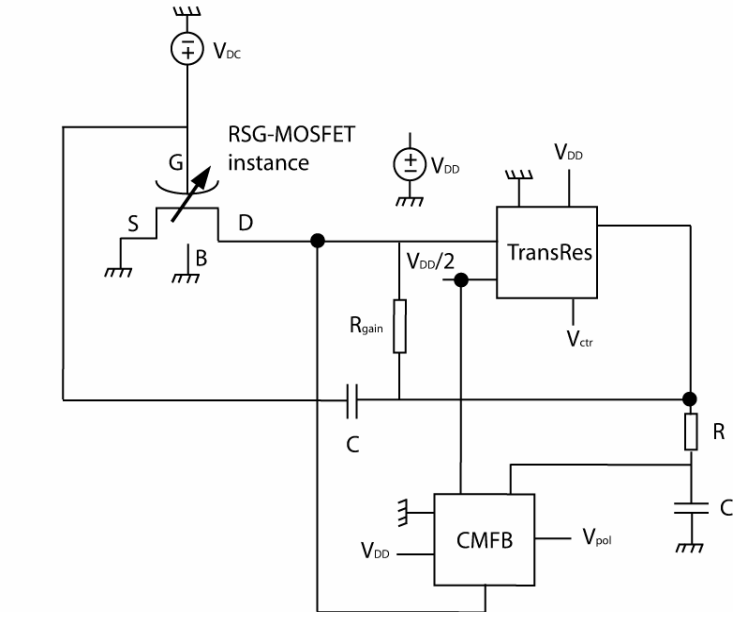


Fig. 90 Circuit schematic of a RSG-MOSFET-based oscillator

The influence of the variation of Rgain on the output waveform is shown in Fig. 91, where only the start-up phase is studied in order to define the resistance value for which the amplifier compensates for the resonator losses. The minimum gain to sustain oscillations is 10kΩ and the start-up time is faster with a higher gain.

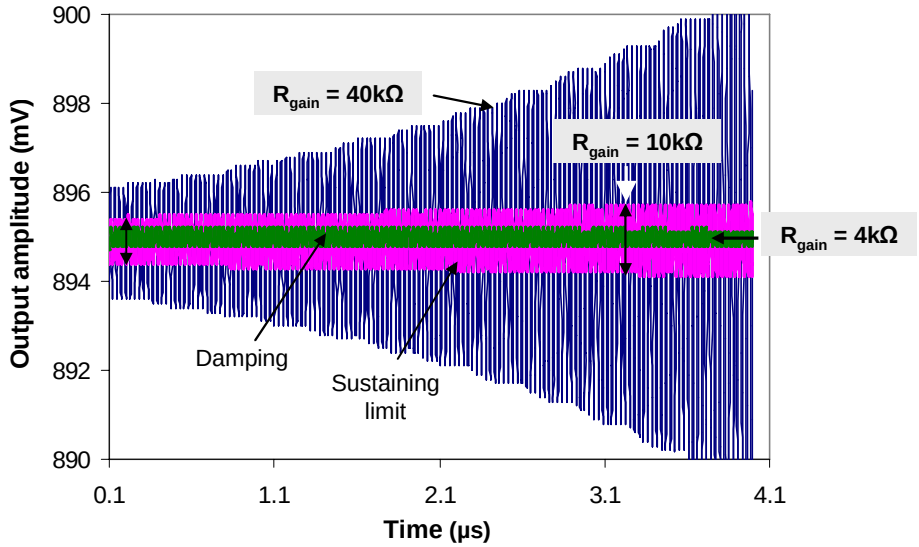


Fig. 91 Simulated transient response

Due to the intrinsic gain of the RSG-MOSFET, the gain of the sustaining amplifier can be reduced by a factor of 24 compared with capacitive detection. Note that this result was obtained for a RSG-MOSFET with a large channel length of 4µm, referred as device 4 in Table XI. The performances can very much increased by decreasing the channel length and using proper operating points, as shown in A.1.b. The MOSFET detection acts in the circuit as a sort of pre-amplifier and minimizes the use of multiple amplifier stage to compensate for the large output motional impedance seen in capacitive detection [127].

IV.E. Conclusions and Perspectives

AlSi and silicon-based RSG-MOSFET were characterized, using a methodology developed in this thesis to dissociate the pure mechanical effect from the MOSFET signal amplification. The effects of drain and gate voltage variation on resonant frequency and signal amplitude were investigated based on the developed EKV-based analytical model and on RSG-MOSFET measurements. A comparison between capacitive and MOSFET detection was done by simulating the output signal level, showing that depending on the bias scheme and on the resonator dimensions, one of the two techniques is more efficient. However for high frequency application for which resonator is scaled down, the MOSFET detection shows a much higher output signal. This result was also demonstrated on MEMS-based capacitive and RSG-MOSFET oscillators, where the intrinsic gain of the transistor reduces considerably the use of amplifier gain. Despite the fact that our fabricated RSG-MOSFET resonators were fully operational with resonance frequencies of 5MHz to 90MHz, building an experiential oscillator was not possible due to their very high motional resistance. Lowering the value of

the motional resistance will require nano-gaps of the order of 100nm or less in order to achieve value of R_x of the order of tens of kOhms, for which it will be possible to build a practical oscillator.

Non-linear response of the resonator was measured for high polarization voltage or high AC signal amplitude. In an oscillator, these non-linearities strongly degrade the phase noise due to the added mechanical noise [40, 60, 87]. This effect is today the bottleneck for MEMS-based reference oscillator, limiting it to achieve wireless standard specifications. To date, only one capacitive MEMS–based oscillator was able to reach the GSM standard, but at a cost of a relatively large circuit footprint [10] and at relatively low resonant frequency (13MHz). Mechanical and electrical non-linearities were avoided by biasing the resonator below the bifurcation point. For higher frequency operation, the MOSFET detection is mandatory to reduce the need for a large sustaining amplifier. Smart architecture of coupled RSG-MOSFET could also be used to build a self-oscillator [4].

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Chapter V

Abrupt Current Switch and Memory applications of the SG-MOSFET

Optical profiler picture of a SG-MOSFET dedicated to switch and memory applications
(Scale: the metal gate is 20x13µm^{2}and the suspended arms are 20x4µm^2)

Introduction

Other applications of SG-MOSFET architecture than resonator were investigated. Due to the unique mechanical and electrical characteristics of the suspended-over-channel gate FET, this device can be used for abrupt current switch application and memory.

By using the mechanical displacement of the mobile gate, a 0.71mV/dec. sub-threshold swing was demonstrated, referred to a switching swing, much better than the ideal 60mV/dec swing that can be achieved in a standard MOSFET. Due to the air-gap between the gate and the channel, the device also presents a very high isolation at high frequency. Scaling perspectives of the device is investigated.

A new memory principle based on the hybrid combination of a mechanical and an electrical hysteresis of the SG-MOSFET is presented. The device specificities are a large memory window, a large current variation between "0" and "1" states, and a very low gate current leakage. Hybrid electro-mechanical memory was compared to pure mechanical one, giving a larger memory window for the SG-MOSFET memory. Memory endurance has been performed up to 10^5 cycles and retention time between DRAM and FLASH was measured. Specific memory addressing was developed and scaling of this memory was studied to achieve low operation voltage and high density integration.

V.A. Abrupt current switch

Switching behavior in MOSFET is defined by the amount of gate voltage needed to increase the drain current by a decade. The maximum increase of current takes place in the inversion regime. The limitation of the MOSFET switch comes from the rate of increase of carriers in the channel when increasing the gate voltage, which is determined by the Fermi-Dirac distribution function. This function represents the probability of the occupation of energy levels by electrons and is function of the thermo-dynamical potential kT/q [114, 128], with k the Boltzmann's constant, q the elementary charge and T the temperature. The drain current in the subthreshold regime in perfect MOSFET depends exponentially on the gate voltage as:

$$I_d \propto e^{\frac{(V_G - V_T)}{(kT/q)}} \tag{V- 3}$$

The sub-threshold swing can then be written as equation (2), and cannot be lower than 60mV/dec. at room temperature.

$$S = \frac{dV_g}{d(\log I_d)}$$
$$S = \ln(10)\frac{kT}{q} \tag{V- 4}$$

Other devices using different physics than carrier inversion principle have been investigated in order to lower the sub-threshold swing, such as impact ionization MOS [129], tunneling MOSFET [130] and mechanical contact switch (MEMS). The tunneling device, which uses the thinning of the energy barrier (below 10nm) in the sub-threshold region under an electric field to allow the electron to tunnel through that barrier, achieves a 40mV/dec swing [131]. Despite that good sub-threshold swing, the tunneling device suffers from a low ON-current, usually below 300nA [132]. However simulations of device with double gate with high-k device have shown higher level of ON-current [133].

MEMS switches are characterized by a lower insertion loss, a higher isolation and lower power consumption compared to CMOS switches [134-136]. These advantages are due to the electrical isolation in the "OFF-state" given by the suspended-over-air electrode and the mechanical contact after actuation ("ON-state"). MEMS switching speed is however limited to 1µs for electrostatic actuation [137], compared to 10ns for PIN diodes [138] and down to 5ps for GaAs switches [139]. The speed limitations are investigated in this chapter.

It has been shown theorically in [140] that scaled MEMS-FET components can also meet the specifications for the future ITRS low power electronic. MEMS switches and among them SG-MOSFET switches are then likely to overcome these sub-threshold swing and isolation limitations. Due to the very similar fabrication process of the SG-MOSFET with the MOSFET process, as described in Chapter III, this device can add some more functionality to standard electronics.

V.A.1. SG-MOSFET switch

Based on the same electro-mechanical principle than for the resonator application, the SG-MOSFET was designed for a low voltage current switch application. Low rigidity geometry (k = 156N/m) of four arms fixed-fixed flexure suspended-gate has been fabricated, as presented in Fig. 92.

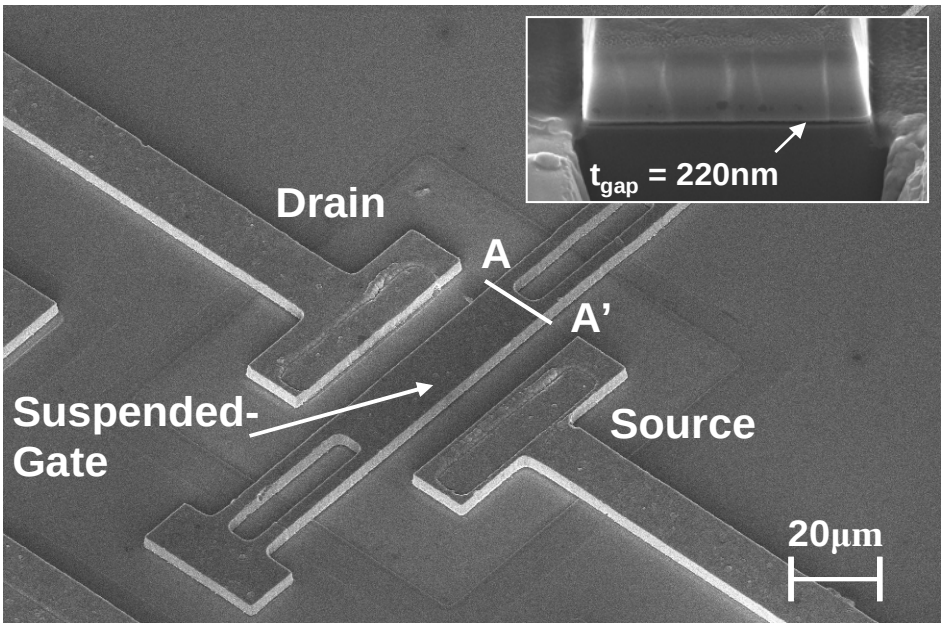


Fig. 92 SEM picture of a low voltage SG-MOSFET switch

As shown in Table XV, SG-MOSFET dimensions have been set to achieve low voltage operation, from 7V to 9V. The switch voltage operation depends on the pull-in voltage which is the critical voltage limit at which the electrostatic force becomes greater than the sustaining rigidity, inducing the beam to collapse.

DC characterization of the device 1 (Table XV) where the I_D-V_G curve is plot for V_D = 500mV is shown in Fig. 93. The drain current follows a super-exponential curve when increasing the gate voltage until the pull-in occurs. The drain current switches of more than one decade of current in few mV variations. As described analytically in Chap. II, before pull-in, the SG-MOSFET capacitive divider is dominated by the relatively low air-gap capacitance. The device is preserved from the gate leakage due to the presence of the air-gap. When pull-in occurs, the SG-MOSFET contacts the gate oxide and the capacitance changes to the much larger oxide capacitance that results in a large drain current increase. After pull-in, the device can be considered as a classical MOSFET. The gate leakage measured after pull-in is I_G = 0.08pA.

Parameters	Source	Switch Device 1	Switch Device 2	Switch Device 3	Units
Beam length, L_{beam}	Layout	60	60	20	µm
Beam width, W_{beam}	Layout	13	13	8	µm
Supported arms length, L_{arms}	Layout	20	20	-	µm
Supported arms width, W_{arms}	Layout	4	4	-	µm
Switch beam thickness, H_{beam}	Measured	1.81	1.81	1.81	µm
MOSFET dimensions, W/L	Layout	60/10	60/10	20/6	µm
MOSFET oxide thickness, t_{ox}	Layout	25	25	25	nm
Initial air-gap, d	Measured	300	300	300	nm
Young's modulus, E	Measured	48	48	48	GPa
Poisson ratio, υ	Given	0.26	0.26	0.26	-
Measured Pull-in voltage	Measured	7.24	8.75	-	V
Measurement pressure	Measured	Ambient	Ambient	Ambient	Torr
Drain polarization voltage, V_D	Measured	50	500	500	mV
Adjusted air gap from Meas., d	Equation	194	220	220	nm
SG-MOSFET initial stiffness, k_0	Equation	154	154	8957	N/m
SG-MOSFET mass, m	Calculated	$6.35x10^{-12}$	$6.35x10^{-12}$	$7.7x10^{-13}$	Kg

Table XV. SG-MOSFET switch design on switch made of AlSi1% gate, described in Chapter III

The SG-MOSFET model developed in Chapter II was validated by fitting the measured characteristics of the device 1 (Fig. 93).

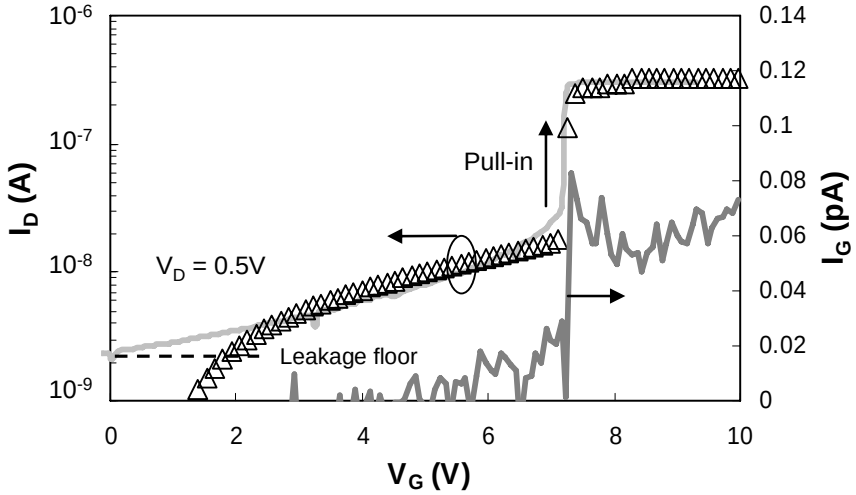


Fig. 93 Measured I_D-V_G and I_G-V_G electrical characteristic (continuous lines) of the SG-MOSFET switch of device 1 (Table XV) and fitted with quasi-static model (dotted line)

The fitting procedure of the model combines mechanical and electrical aspects:
- Mechanical aspects: The gate thickness is based on deposition process which has a uniformity of around 10% over the wafer. The sacrificial layer is dependent of a CMP step which is non-uniform between large and small active areas. The width and length of the gate

are slightly deviated from the layout values due to non-perfectly isotropic etching tools. All these parameters are modifying the device stiffness and the gap size and therefore varying the pull-in voltage. The accuracy of these parameters is limited to the optical and electronics microscope tools, which were therefore optimized to fit the pull-in voltage.

- Electrical aspects: Electrical fitting parameters such as the gate oxide capacitance, the access resistance and channel length were optimized to fit the drain current level before and after the pull-in. Thermal gate oxide thickness was evaluated from ellipsometry measurement and also simulated with a Finite Element analysis tools (ISE®). The slightly difference value observed with these tools (around 2nm), were used as fitting parameters in the model. A source and drain access resistance, related to the non-aligned process that creates regions uncontrolled by the gate and therefore showing a large access resistance. A fitted 2 MΩ access resistance creates a large drain voltage drop which lowers the drain current. The channel length was also slightly fitted considering the lateral dopant diffusion, also simulated with the FEM tool. In depletion mode, simulation differs from the measurements due to the drain current leakage floor of this device which is around 2nA.

V.A.2. SG-MOSFET sub-threshold swing performance

Even if the SG-MOSFET current generation is based upon the same physics as standard MOSFET, the switching behavior does not suffer from the rate of increase of carrier when varying the gate voltage. Indeed, the switching does not occur in the sub-threshold region but in moderate or strong inversion, and the current level during the switching only depends on the gate-to-channel capacitance. Due to the mobile gate architecture, the SG-MOSFET follows a high sub-threshold voltage MOSFET behavior before pull-in, which also can be described as a low gate-to-channel capacitance, as shown in Fig. 94. The total capacitance is the combination of the air-gap and the gate oxide capacitances in series. After pull-in, the device follows a low sub-threshold voltage MOSFET behavior and the capacitance is high and similar to a standard MOSFET.

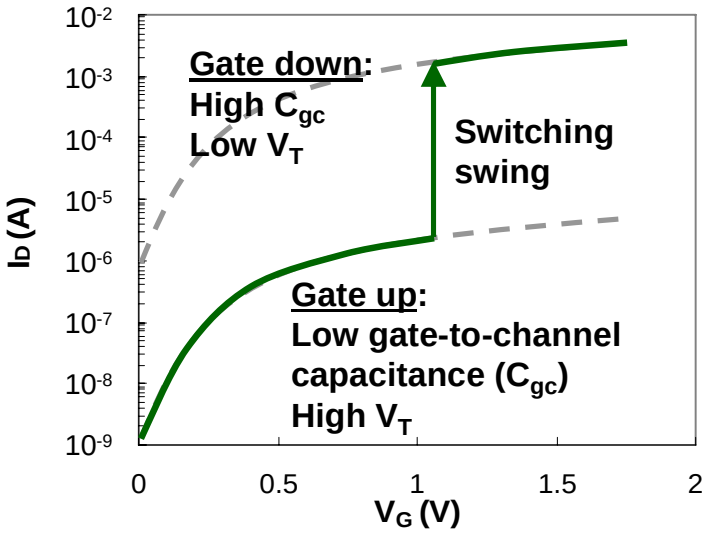


Fig. 94 Switching behavior schematic of the SG-MOSFET from a high to a low gate-to-channel capacitance before and after mechanical contact.

Mechanical switching behavior is presented in Fig. 95 where mechanical pull-in occurs for a positive gate voltage of 8.75V. The outstanding measured switching slope of 0.71mV/dec for the device 2 (Table XV) is much lower than the ideal 60mV/dec sub-threshold swing of MOSFET.

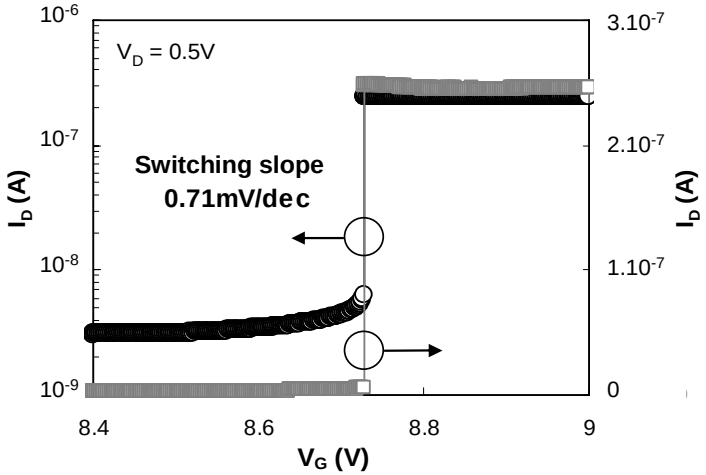


Fig. 95 Measured mechanical switching behavior of the SG-MOSFET (device 2 of Table XV).

The measurement of the SG-MOSFET swing is today limited by the number of measurement points allowed by the Semiconductor parameters Analyzer equipment (1000 points) and could be therefore greater that the measured values. The drain current switches of around two decades, but is limited to few hundreds of nano-amps due to the high access resistance and to the long channel of the MOSFET.

V.A.3. Switch isolation

Complementary S-parameter measurements show that the device also offers a very good isolation in the off state (-75dB at 50MHz up to -25dB at 2GHz) despite a non-optimized RF substrate design. The switch isolation measurements are presented in Fig. 96, having connected the source and substrate to the ground.

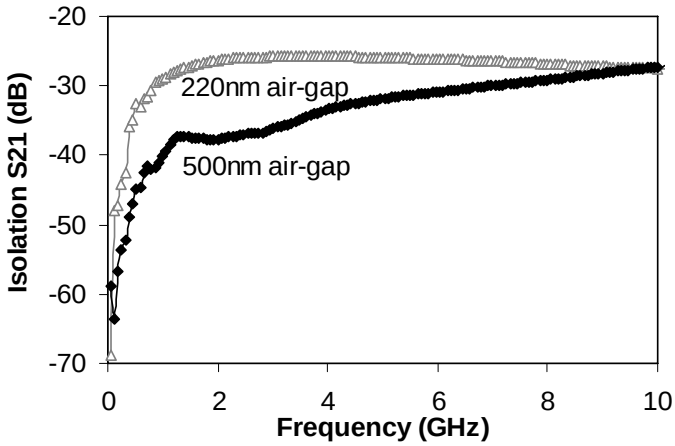


Fig. 96 Switch isolation measurement curves for SG-MOSFET switches various air-gaps (device 3 of Table XV with 220nm and 500nm air-gap).

An isolation of -27dB up to 10 GHz is shown, a 7dB improvement compared to a commercial MEMS switch at that frequency [141], despite a seven times smaller SG-MOSFET air-gap. By increasing the air-gap up to 500nm, the gate-to-channel capacitance of the SG-MOSFET decreases and the isolation level goes down to -37dB at 2 GHz.

V.A.4. Scaling perspectives

Abrupt sub-threshold swing of SG-MOSFET switches were demonstrated on micrometer-structures with actuation voltages above 7V. To achieve higher density, suspended-gate devices should be physically scaled down but as the same time it should fit the low actuation voltage requirements of CMOS generations. As explained in Chapter II, these two parameters are antagonist as reducing the size of the gate makes the structure stiffer and then increases the pull-in voltage. A tradeoff between the gate dimensions and the air-gap size can however be found to assess the two requirements. Simulations of metallic and silicon SG-MOSFET devices using the previously validated model are presented in Fig. 97.

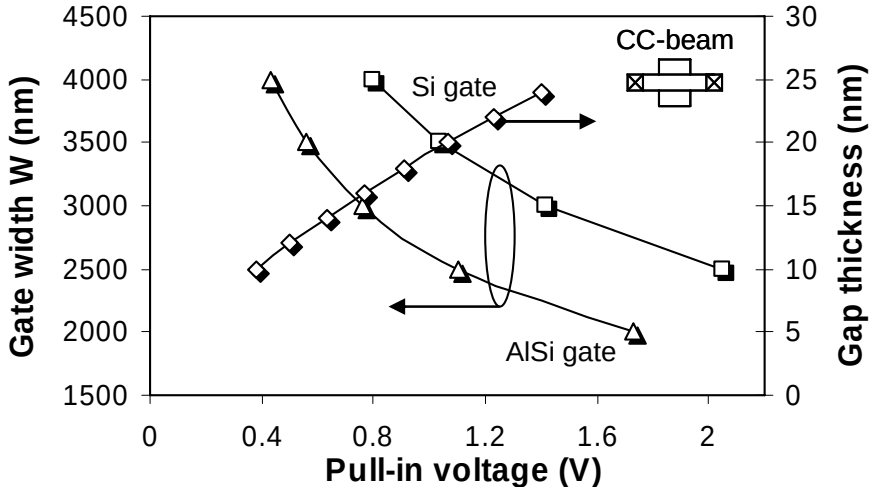


Fig. 97 Mechanical pull-in voltages for different gate width and air-gaps for L = 32nm

SG-MOSFET dimensions for the 65nm technology node were defined: a gate thickness greater than 60nm and a gate width comprised between 80nm and 10µm. The air-gap comprised between 10nm and 25nm can be fabricated by using the SON process [112]. The simulated results demonstrate the operation of a SG-MOSFET switch with a gate voltage lower than 2V for a clamped-clamped beam design. This first order model, however, does not take into account Casimir [50] and Van Der Waals [142] forces which could appear for this small air-gap dimension. The scaling procedure to achieve the highest density while lowering the actuation voltage to fit a given technology node, is to reduce the beam length, thickness and the air-gap simultaneously. An important feature of the device is that the beam width does not impact the pull-in voltage, according to equation 9 of Chapter II. The pull-in voltage is then proportional to equation 3 and scaling down the beam length is largely compensated by scaling the beam thickness and air-gap [143].

$$V_{PI} \propto \sqrt{\frac{H_{beam}^3 d_{gap}^3}{L_{beam}^4}} \qquad \text{(V- 5)}$$

Switching of the drain current for the 65nm node is shown in Fig. 98 for which the transistor channel length L_{ch} is 32nm, the beam thickness and the air-gap were set to 15nm and 10nm respectively. The resulting active cell size, for 1V operation, is in the order of $0.019\mu m^2$, the Ion/Ioff ratio is 10^5 and the switching current ratio (after/before pull-in) is 10^2.

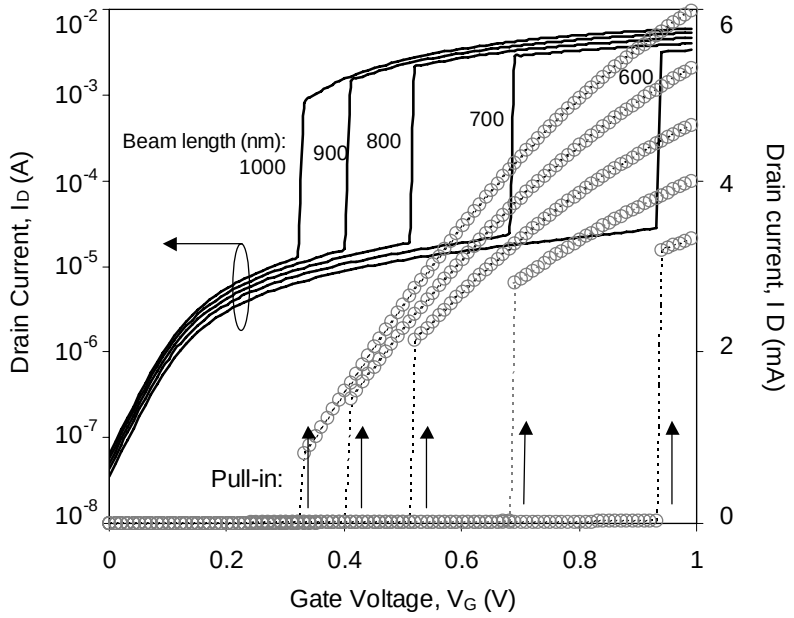


Fig. 98 I_D-V_G characteristics of a scaled SG-MOSFET with metallic (AlSi) mobile gate (CC-beam) for different beam lengths (= transistor width) with a 1.93nm gate oxide.

Further investigations on nanoscale design of the SG-MOSFET were done on multi-walled metallic carbon nanotubes (MWCNT) gate, made of folded graphite sheets. The CNTs have a Young's modulus close to 1TPa which has an advantage in terms of switching speed (see A.6). The high gate stiffness has a cost of an increased pull-in voltage, which can only be reduced by lowering the air-gap. A challenging 2nm air-gap size is needed in order to maintain the same 1V design window as for a suspended-metal-gate device with 15nm air-gap in Fig. 98. Simulation of a CNT-based SG-MOSFET, taking into account the cylindrical gate capacitance and the intrinsic properties of CNTs [144], are shown in Fig. 99. The resulting active cell size is in the order of $0.025\mu m^2$. The channel length is defined by the CNT diameter, considered here as 32nm and the airgap is 2nm.

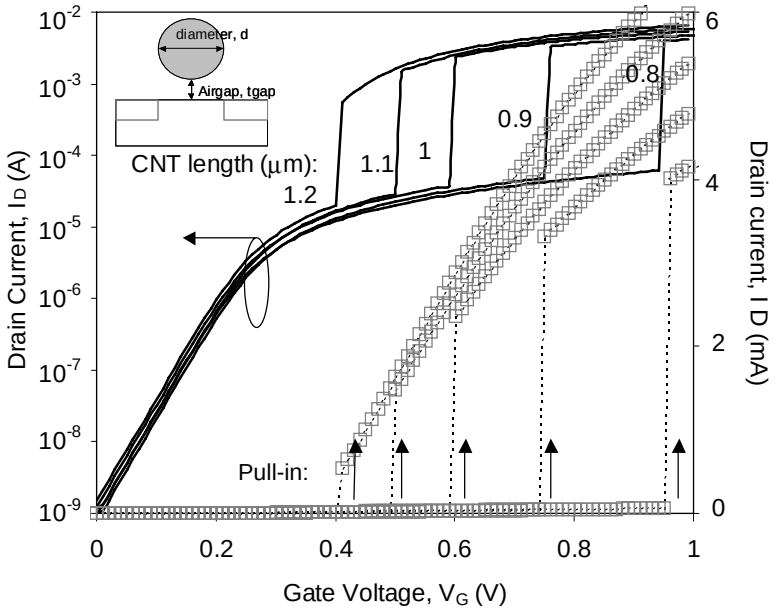


Fig. 99 I_D-V_G characteristics of a scaled SG-MOSFET using suspended CNT gate with different lengths, with a 1.93nm gate oxide.

Scaling limitations of the SG-MOSFET comes from the technological side and from the fact that other forces than electrostatic are occurring at that scale. A critical path to further reduce the active size is the fabrication of suspended-structure with gaps below 10nm. At that scale Casimir forces can be greater than electrostatic forces, as described in Chapter II-A.6 and induce the auto-actuation of the beam [145]. The parameters used to calculate these forces strongly depends on the gap size and considering parameter such as the roughness of the suspended structure, a precise estimation of the critical dimensions to avoid auto-actuation is not achievable. This research field is currently highly studied in the scientific domain [146, 147].

V.A.5. Scaling of the switching current amplitude

Scaling of the length and width of the SG-MOSFET does not impact the sub-threshold swing as the switching phenomenon is only related to the mechanical displacement of the gate. According to part A.2 of Chapter II, the voltage swing needed to turn the suspended-gate into mechanical instability is independent of the beam stiffness. Depending on the beam stiffness and considering the same air-gap, the mechanical switching occurs at different gate voltages but the switching current amplitude keeps nearly constant, as shown in Fig. 98 and Fig. 99 in the strong inversion region of the MOSFET. The levels of current before and after switching is however not only function of the beam stiffness but also on the air-gap. The switching current is related to the intrinsic voltage V_{Gint} applied on the transistor and is function of a ratio between the air-gap capacitance and the gate-to-channel capacitance C_{GC}, as seen in equation (V- 4), demonstrated in Chapter II A.1.

$$V_{G\,\mathrm{int}} = V_G \Big/ \left(1 + \frac{C_{GC}}{C_{gap}}\right) \qquad \text{(V- 6)}$$

For a large air-gap, this ratio is dominating by the small air-gap capacitance, but can be reduced towards the unity if the air-gap capacitance is in the range of the oxide, depletion and inversion series capacitances. Reducing the C_{GC}-over-C_{gap} ratio induces a lower drain current switching amplitudes. This simulation results on Fig. 98 and Fig. 99 shows that the drain current switches by 2.1 decade for an air-gap of 15nm and 1.8 decade for an air-gap of 2nm in strong inversion region. One can note that the switching current is dependent of the MOSFET regime during mechanical switching. The current amplitude can be modulated by designing MOSFETs with different sub-threshold voltages, as shown in Fig. 100. The threshold voltage is modified by changing the channel doping while keeping the same MOSFET dimensions. The simulations considers two identical SG-MOSFET with a beam length of 1µm, a width of 32nm, a thickness of 10nm, a gate oxide of 1nm and an air-gap of 15nm. The pull-in voltage of both SG-MOSFET occurs for a gate voltage of 0.8V.

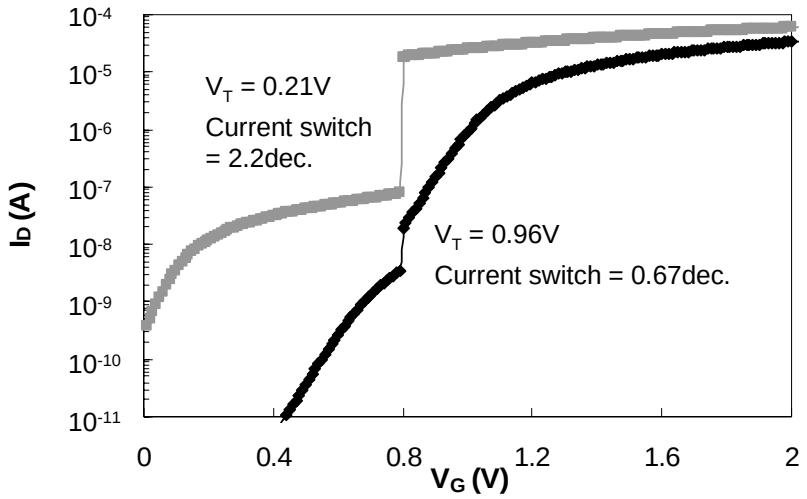


Fig. 100 I_D-V_G simulated characteristics of a CC-beam silicon SG-MOSFET with identical dimensions but different threshold voltage induced by different channel doping level.

If the threshold voltage is increased above the pull-in voltage, the mechanical contact will occur in a region where the inversion is low and then the C_{GC} capacitance variation is close to the air-gap capacitance. In this region the inversion capacitance is low and dominates the C_{GC} term.

V.A.6. SG-MOSFET switching speed

At first order, the switching speed of the SG-MOSFET is directly related to the gate dimensions and increases for a stiffer gate [148]. The switching time can be limited by the air damping or by the acceleration, in vacuum environment. It has been demonstrated in [148, 149] that the maximum switching time under damping limitations can be written as:

$$t_s = \frac{9V_{PI}^2}{4V_G^2 \omega_0 Q} \qquad \text{(V- 7)}$$

The switching time under acceleration limitation is express as:

$$t_s = 3.67 \frac{V_{PI}}{V_G \omega_0} \qquad \text{(V- 8)}$$

The SG-MOSFET switch can be either hermetically or vacuum packaged in order to avoid any degradation of the exposed gate oxide. The maximum switching time for a scaled device described in Fig. 98, with a pull-in voltage of 0.95V is 5ns in air and 4.3ns under vacuum. Due to the very high stiffness of MWNT, switching times of 0.6ns in air and 0.5ns under vacuum can be achieved. The theoretical switching time obtained for scaled SG-MOSFET can therefore be greater than the PIN diode or the GaAs switches.

V.A.7. Conclusion and perspectives

A mechanical switch based on the direct contact between a mobile gate and a MOSFET channel has been demonstrated. The electro-mechanical analytical model developed in Chapter II has been validated on measures I_D-V_G characteristics. A mechanical sub-threshold swing of 0.71mV/dec. was measured on CC-beam structure. The device combines the advantages of MEMS switches as a high isolation, and the functionality of a CMOS switch in terms of current variation.

The scaling of the SG-MOSFET can be done by decreasing the size of the active cell and as the same time lowering the actuation voltage to be compatible with standard CMOS voltages. The design tradeoff to achieve these two requirements is to reduce the gate dimensions simultaneously with the air-gap distance. The amplitude of current switch is defined by the MOSFET region where the pull-in occurs and is larger in strong inversion than in weak inversion.

In order to extract the intrinsic performances of the device, further investigations on contact resistance reduction and insertion loss measurement should be done in the next step. The high SG-MOSFET sub-threshold swing makes the device very attractive for voltage reference application. The high isolation and low gate leakage make also the device attractive for power MOSFET application where the SG-MOSFET can control digital circuit blocks to reduce the overall circuit power consumption.

V.B. MEMS-based memory

V.B.1. MEMS memory: State of the art

MEMS-based memories were shown to be promising for stand-alone high density NVM (Non Volatile Memory) exceeding 1Tb/in² using MEMS actuators and polymer as memory medium [150]. Indeed, IBM presented an array of mechanically actuated cantilevers used to write and erase in parallel data by locally heating a polymer using an AFM tip fixed at the edge of the cantilever, as seen in Fig. 101. The density of the memory depends at first order on the AFM tip diameter and on the mechanical step of the cantilever system. The reading of the memory is done by detecting the surface variations with the AFM tip.

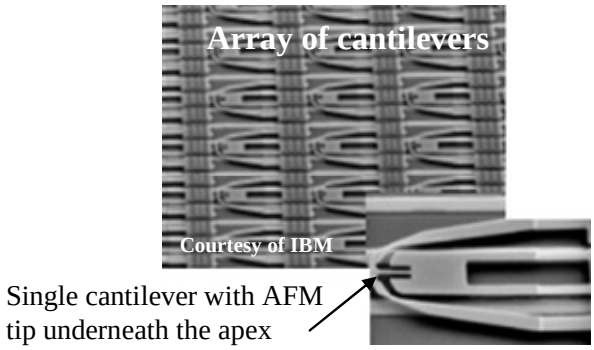


Fig. 101 SEM picture of an array of mechanical cantilevers used to write and read memory cells. Close view on a cantilever. Courtesy of IBM [150]

Above-IC MEMS non-volatile and volatile memories showing very low power consumption but low density integration of 1Mb/mm^2 have been demonstrated [151]. Electrostatic actuation on metal-metal switches is used with CMOS-compatible voltages, as seen on Fig. 102. The technology allows a back-end-of-line integration of the memory in the interconnections, dedicated to embedded applications. The electrostatic actuation is a reversible phenomenon but depending on the cantilever stiffness, these devices can be used either as FUSE where the cantilevers are maintained in a defined state, or as non-volatile memory.

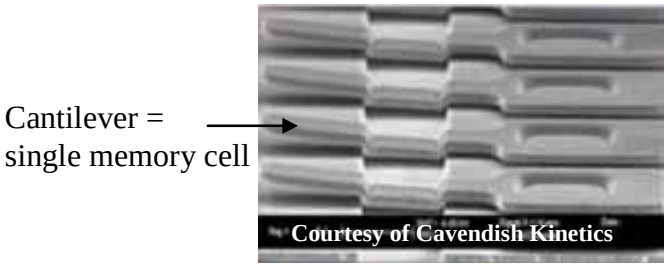


Fig. 102 SEM picture of the metal switch used as NVM memories. Courtesy of Cavendish Kinetics [151]

However, no attempt has been yet proposed to combine CMOS and MEMS technologies in order to achieve significant gain in terms of power dissipation and speed operation while keeping the high CMOS density. In the following section, we investigate the use of SG-MOSFET for capacitor-less, low power, non-volatile memory cell application.

V.B.2. Mechanical hysteresis-based memory

Complementary to the pull-in effect when the electrostatic force is greater than the mechanical sustaining forces, described in the previous section, a pull-out effect occurs when decreasing the gate voltage. Pull-out voltage occurs at positive gate voltage but differs from the pull-in voltage due to the different initial condition of operation. Stable initial condition before the pull-in is obtained for a suspended beam whereas before the pull-out, the beam is in contact with the substrate. When the beam is clamped down, the electrostatic field generated between the gate and the channel through the thin gate oxide is much larger than the mechanical sustaining forces of the anchored beam. Contact forces due to surface roughness also tend to maintain the beam in contact with the substrate. When decreasing the gate voltage, the beam is peeled-off from the substrate symmetrically from both sides of the anchored beam and towards the center.

A measured mechanical hysteresis of a SG-MOSFET, resulting from the difference between the pull-in and the pull-out voltages, is presented in Fig. 103, where the device dimensions are described in Table XVI (device 1) with a 285nm air-gap and an un-degraded thermal gate oxide.

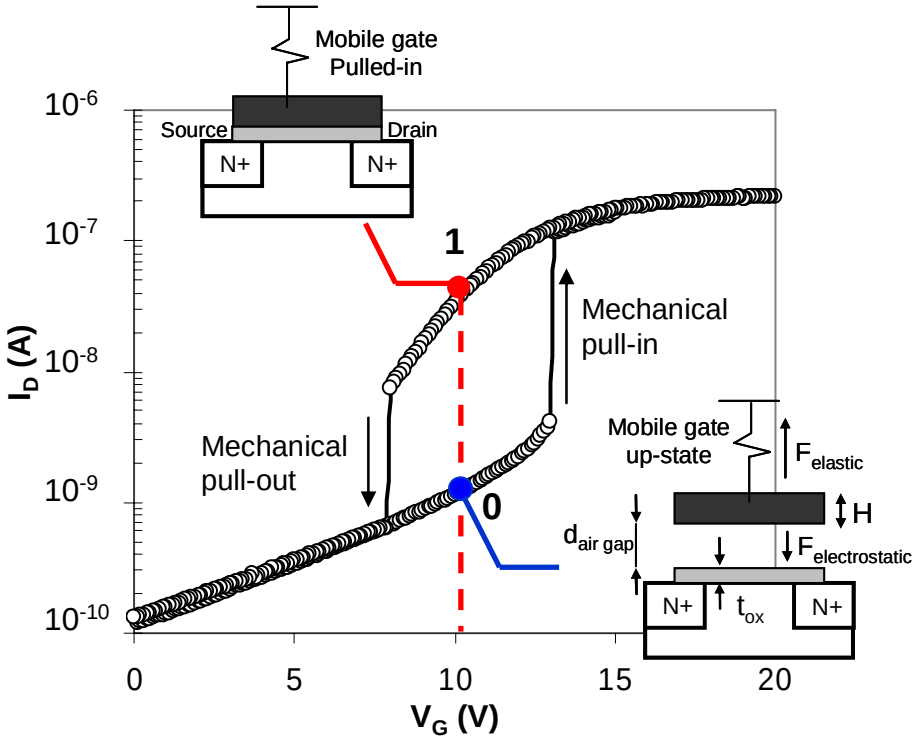


Fig. 103 Measured mechanical hysteresis on SG-MOSFET device with an undefected gate oxide. Memory states are related to the up and down states of the moving gate. (device 1 of Table XVI)

The mechanical hysteresis suggests that the SG-MOSFET can be used as a pure MEMS memory cell where the “1” state is defined when the gate is pulled-in and the “0” state when the gate is suspended. Reading of the memory is then done by measuring the drain current applying a DC drain polarization. In the down-state, due to the large oxide capacitance, a large current is measured whereas in the up-state, the drain current is low. The stability of the “1” state after pull-in is dependent of the electrostatic force between the gate and the

substrate, and can be guaranteed by applying a gate voltage above the pull-out voltage. The pure mechanical behavior can be referred to the phenomenon obtained for metal-metal capacitive switches where the metallic membrane stabilizes at the down position under an electric field [135, 152]. This phenomenon is observed for the device of Fig. 103.

Parameters	Source	Memory	Memory	Memory	Memory	Units
		Device 1	Device 2	Device 3	Device 4	
Resonator beam length, L_{beam}	Layout	60	60	60	60	µm
Resonator beam width, W_{beam}	Layout	13	13	13	13	µm
Supported arms length, L_{arms}	Layout	20	20	20	20	µm
Supported arms width, W_{arms}	Layout	4	4	4	4	µm
Memory beam thick., H_{beam}	Measured	1.81	1.81	1.81	1.81	µm
MOSFET dimensions, W/L	Layout	60/10	60/10	60/10	60/10	µm
MOSFET oxide thickness, t_{ox}	Layout	25	25	25	25	nm
Initial air-gap, d	Measured	300	300	300	300	nm
Young's modulus, E	Measured	48	48	48	48	GPa
Poisson ratio, υ	Given	0.26	0.26	0.26	0.26	-
Measured Pull-in voltage	Measured	13	10.65	9.5	5.1	V
Measured Pull-out voltage	Measured	7.9	6.95	-	-	V
Measured neg. Pull-in voltage	Measured	-	-6.45	-7.8	-7.65	V
Measurement pressure	Measured	Ambient	Ambient	Ambient	Ambient	Torr
Drain polarization voltage, V_D	Measured	50	100	50	50	mV
Adjusted air gap from Meas., d	Equation	285	252	234	151	nm

Table XVI. SG-MOSFET memory design summary

V.B.3. SG-MOSFET Memory: combining mechanical and electrical hysteresis

V.B.3.a. Operating principle

The novel aspect of this memory is based upon the fact that the hysteresis on I_D-V_G, also defined as the "memory window", can be controlled and enhanced by using the mobile gate to inject charge carriers into the gate dielectric [153]. A typical 1T SG-MOSFET memory behavior is shown in Fig. 104, where the combined mechanical plus electrical hysteresis is much larger than the pure mechanical hysteresis (Fig. 103). A description of a pure electrical hysteresis behavior was given in [154]. The system was based on a floating body mechanically controlled by two surrounding floating gates charged identically or differently to repulse or attract the central suspended body without mechanical contact. For the SG-MOSFET, a large hysteresis combining these phenomena is obtained after mechanical pull-in of the SG-MOSFET at V_G = 10.6V, as shown in Fig. 104.

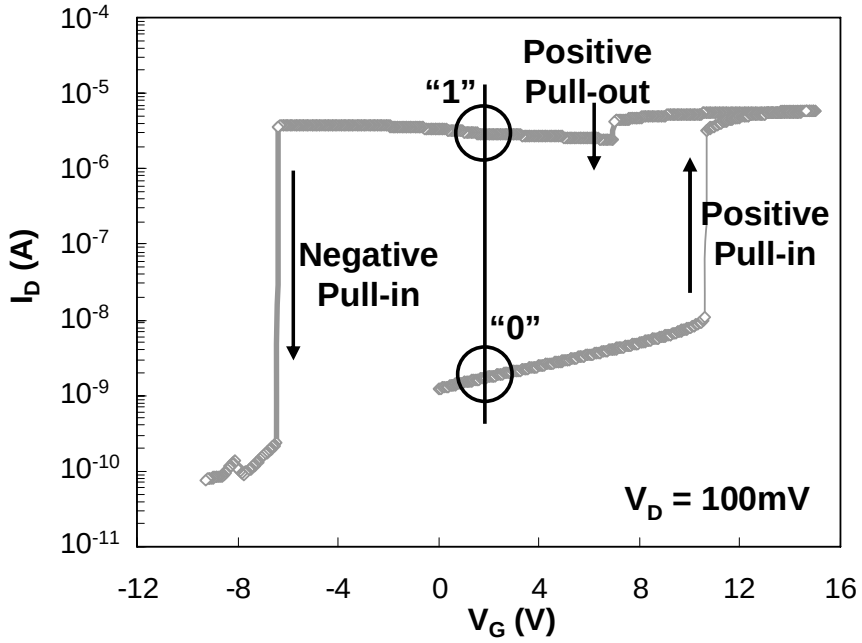


Fig. 104 Hysteresis behavior of the I_D-V_G characteristic of the SG-MOSFET for various drain voltages in air and under vacuum (device 2 of Table XVI).

Mechanical contact of the metallic gate with the oxide allows injection of charges in the defected oxide. The drain current variation resulting from the mechanical switching from state "0" to "1" was measured to be up to 4 decades, which is inline with the memory window of conventional FLASH cells. Reading the memory is done by measuring the drain current. The drain current variation resulting from the mechanical switching from state "0" to "1" was measured to be up to 4 decades. Static consumption of the device in Fig. 104 is 6.5µW/µm, being dominated by the "0" to "1" programming step.

The width of the hysteresis is defined as the gate voltage amplitude for which the device is kept in the "1" state. It relies on the density of traps generated in the oxide. This effect has been shown when using polyimide for the SG-MOSFET sacrificial layer (chap. III.A). In this case, an oxygen plasma releasing step is used which is known in semiconductor industry to generate defects in the SiO_2 [155]. Programming of the SG-MOSFET memory is done by applying a positive gate voltage above the positive pull-in voltage to write the state "1" and by applying a negative voltage below the negative pull-in to erase the cell. When the pull-in occurs, the metal gate enters in contact with the gate oxide and the electrons are extracted from the trapping centers by the positive gate voltage, the device in then turned into the strong inversion regime (Fig. 105b).

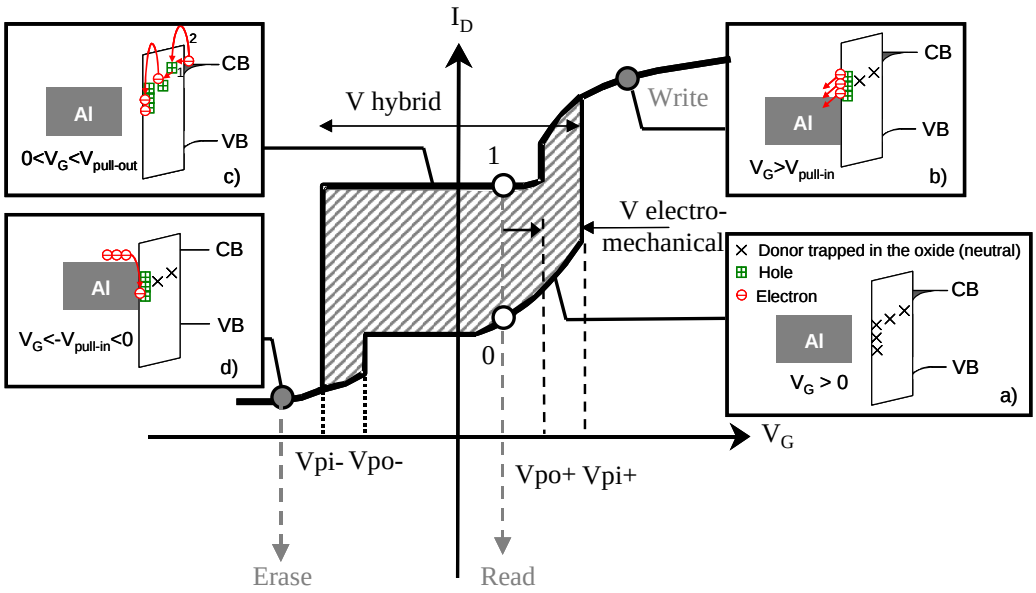


Fig. 105 Mechanisms involved during a) initial, b) program, c) retention and d) erase phases.

By decreasing the positive gate voltage down to V_G = 6.95V, the gate is pulled-out (Fig. 105c), the positively charged centers maintain a vertical field that keeps the device in strong inversion and the drain current remains high. This effect stands even for negative V_G due to the high density of positive fixed charges. For a gate voltage sufficiently negative (V_G=-6.45V), the gate-to-channel potential difference is sufficient to attract the gate and the pull-in occurs, inducing a rapid recombination of negative charges in the oxide (Fig. 105d). At that point, the SG-MOSFET switches directly from strong inversion to depletion mode. By increasing again the gate voltage, the beam is pulled-out at a low negative voltage, symmetrically to the effect seen in the positive gate voltage side.
In retention mode, the beam is in the upper position. The air-gap between the injection gate and the storage media limits significantly the memory leakage.

V.B.3.b. Amplitude of the memory effect

The number of charges stored in the oxide is estimated from the threshold voltage variation of the hybrid memory window, as referred in Fig. 105, and is expressed as:

$$n_{charge} = \frac{Q_{FG}}{q} = \frac{\Delta V_{Hybrid} C_{GC}}{q} \qquad \text{(V- 9)}$$

According to this formula, the SG-MOSFET presented in Fig. 104 stores about 3.14×10^{11}e/cm^2, which is close to the memory charge for FLASH memories (n_{charge} ~ 10^{12}e/cm^2). The amount of charges stored in the device is however dependent to the number of defect in the SiO_2 and can be optimized during the process for this purpose. Note that the C_{GC} capacitance of the SG-MOSFET is lower than for FLASH memories due to the air-gap, therefore for the same amount of charge stored, ΔV_{TH} will be larger, but at the expense of a lower read current.

V.B.3.c. Retention

The evolution of the read current in retention mode after programming the device in the ‘’1’’ state is shown in Fig. 106. The programming step is done by applying V_G = 15V for 180 seconds. The monitor current, at V_G = 0V, is observed to remain constant at state “1” level for several tens of minutes before to decrease to state “0”. The inset of Fig. 106 shows the read current dependency on programming time which varies from 20 seconds to 4 minutes. When applying the programming electric field for a longer time, a larger number of charges are trapped in the SiO_2 which results in a higher read current and an increased retention time.

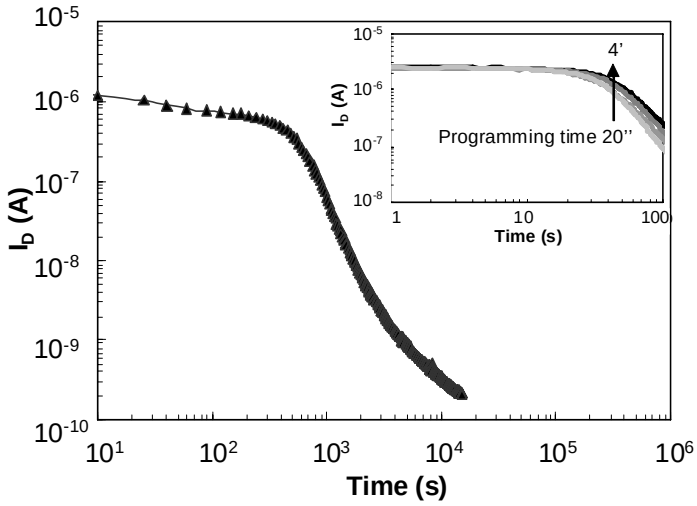


Fig. 106 Retention characteristic after programming the memory in high state by a gate voltage of 15V for a pulse time of 180 seconds. The inset plot presents the retention time for different pulse time. (device 2 of Table XVI)

The measured retention times places the SG-MOSFET memory between the performances of DRAM and FLASH memories. The relatively short retention time of the SG-MOSFET compared to FLASH is largely due to the storage medium. If the SiO_2 media is leaky at one part of the layer, all charges stored in the media flows through this point. In order to achieve a non-volatile memory characteristic, retention time should be largely increased; this can be done by using other storage material than SiO_2 and other stack as presented in Fig. 107. The p stack is composed of a dedicated storage material, such as nitride or n-doped poly-Silicon over a High-K/SiO_2 barrier in order to reduce the memory cell leakage.

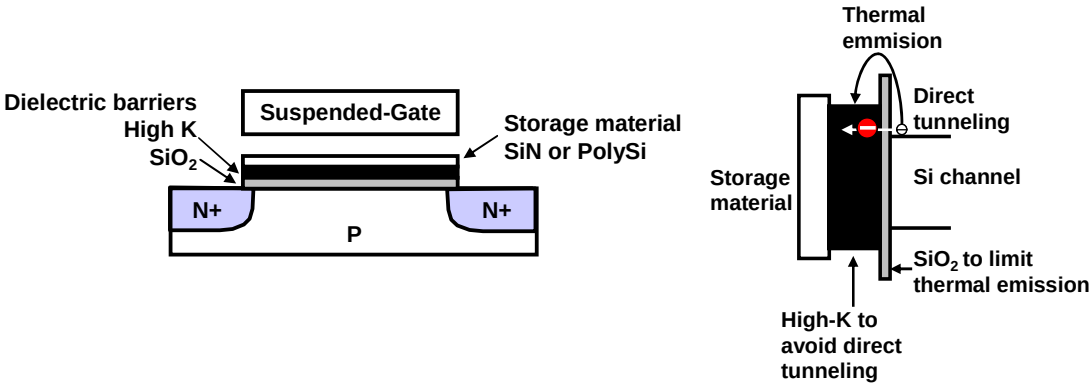


Fig. 107 Optimized material stack for charge storage and retention

As compared to FLASH memory for which the charge leakage through the tunnel oxide is dominant, the High-K/SiO_2 barrier in the architecture of Fig. 107 should considerably limit this effect. The high-K dielectric gives a thicker dielectric barrier for the same equivalent oxide thickness, therefore also allowing a large reading current. This SG-MOSFET architecture also avoids the degradation of the tunnel oxide observed for FLASH memory, as seen in the next section. The non-volatility of the memory is further improved by the intrinsic architecture of the mechanical memory for which no charges can leak through the suspended-gate.

V.B.3.d. Cycling

Cycling tests were performed on an SG-MOSFET biased with an AC signal and coupled with an holographic optical profiler in order to observe the beam displacement under the applied gate voltage [156]. The MEMS memory was mounted on ceramic chip and wire-bonded to gold pins, connected to the AC generator. The memory was tested under a 2 kHz AC actuation applying alternatively +20V and –20V while connecting source and drain to the ground. Cycling results are presented in Fig. 108, showing very good reliability for up to 10^5 cycles, with no significant change in pull-in voltages and hysteresis, which suggests negligible storage media degradations.

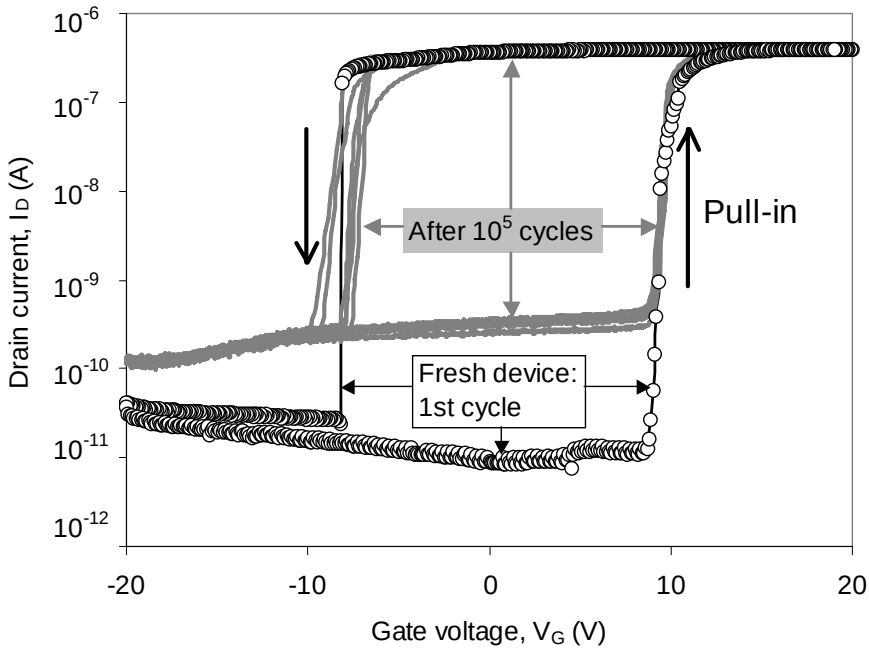


Fig. 108 Cycling tests of a SG-MOSFET at V_D=50mV: the measurement of hysteresis is repeated for few cycles, after 10^5 cycles of operation. (device 3 of Table XVI)

No cracks or other mechanical degradations of the mobile gate were observed on an optical based observation. The main cycling consequence on the memory operation is that the I_{off} current is increased by one order of magnitude, which can be explained by a slight gate oxide degradation over cycles.

V.B.3.e. Effect of drain voltage on pull-in and pull-out effects

Drain voltage variation also has a significant effect on the pull-in and pull-out behaviors. At principle, different effects can occur simultaneously and change the total electrostatic force responsible for the displacement, which is a combination of the electrical field between the gate and the substrate and the electrical field between the gate and the drain and source:

- Due to the gate-to-drain overlapping area, when applying a drain voltage, the electric field in the gate-to-substrate region is lowered, then reducing the total electric field and shifting up the pull-in voltage. In addition, by applying a drain voltage, the channel next to the drain region is inverted, resulting in a lower electric field in that region.

- Mechanical considerations of the suspended CC-beam have to be taken into account in order to explain the early pull-in measured when increasing the drain voltage. When applying a drain voltage, an asymmetric electrostatic force along the width of the beam can make the beam unstable and induce an asymmetric actuation.

The measured I_D-V_G characteristics of Fig. 109 for various drain voltages, present an early pull-in voltage when increasing V_D, therefore the asymmetric mechanical effect on the structure is the dominant effect for this device. The pull-in dependency under V_D is symmetrical and the negative pull-in voltage is also shifted down.

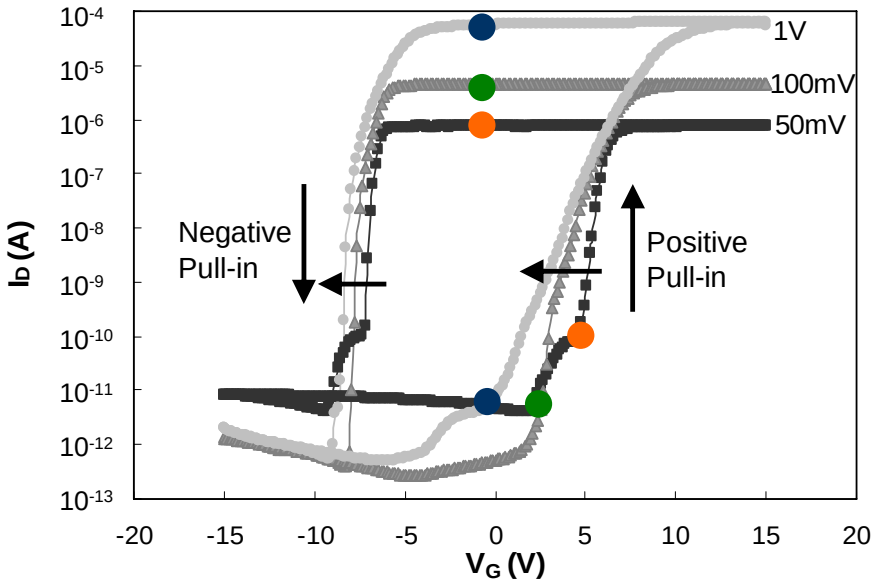
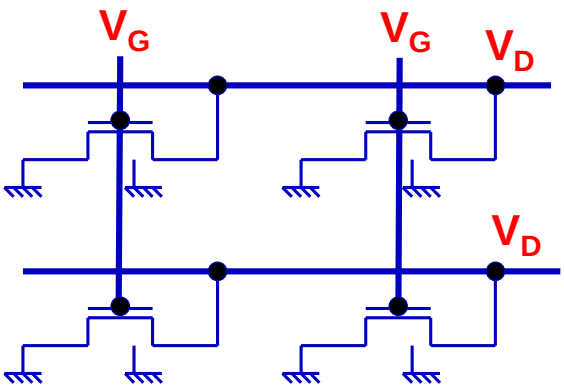


Fig. 109 Hysteresis characteristics, I_D-V_G, of a SG-MOSFET for different drain voltages. An asymmetric actuation of the mobile gate and early pull-in is induced by the drain voltage.

The electrical and mechanical phenomena are tightly bound and should strongly depend on the SG-MOSFET geometry. This behavior needs however further investigation in order to fully understand the phenomenon behind it. A 2D simulation combining semiconductor (as ISE®) and mechanical (as ANSYS®) simulation tools should be used for this purpose. The dependence of the drain voltage on the pull-in voltage is however of particularly great interest for memory addressing scheme, as seen in the next part.

V.B.3.f. Addressing

Writing the cell is done by applying a gate voltage greater than the pull-in voltage. Erasing the cell is done by applying a gate voltage lower than the negative pull-in voltage, for any drain voltage, as seen in Fig. 110. A general reading scheme is to applied a drain voltage with a gate voltage comprised between $-V_{pull\text{-}in}<V_G<V_{pull\text{-}in}$ and to measure the resulting drain current. On the retention phase, all voltages are set to 0.



	Gate	Drain
Prog '1'	$V_G > V_{pi+}$	V_D
Prog '0'	$-V_G > -V_{pi-}$	V_D
Read	0	V_D
Retention	0	0

Fig. 110 Simple addressing scheme of the SG-MOSFET memory, ideal conditions to reduce power consumption

A specific feature of the SG-MOSFET memory is the use of the pull-in voltage dependence on drain voltages. According the schematic of Fig. 111, depending on the drain voltage, selective column memory cells can be addressed. By setting the program gate voltage to write cells, a high V_D is used to write the specific cell whereas the other cells are set to lower drain voltage to avoid the pull-in effect. Bit in column can also be writing and reading at the same time, by using a high V_D to write cell and a low V_D to read cell for the same gate voltage, using a dedicated circuit design. To erase specifically cells in column, the same methodology is followed by using a negative gate voltage to achieve different pull-in at different drain voltages.

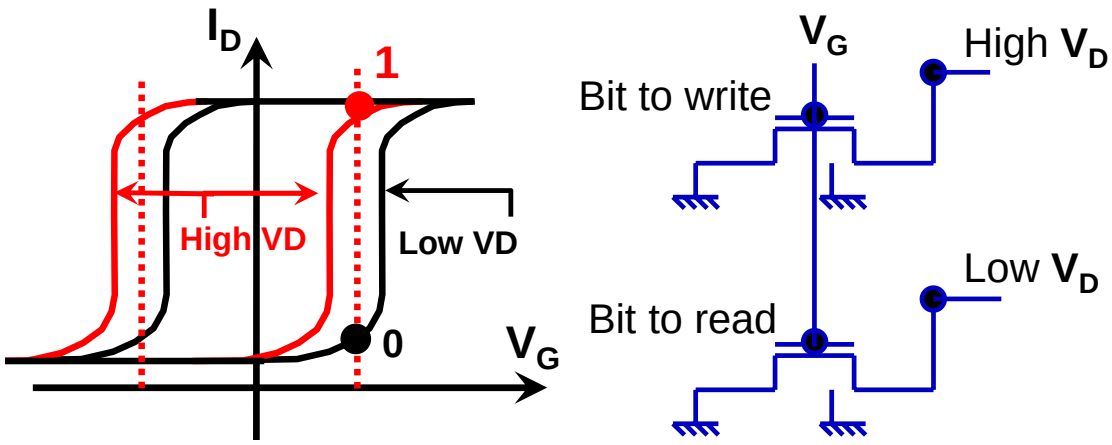


Fig. 111 Schematic of the use of different drain voltages to selectively address bit cell in column

V.B.3.g. Scalability

In order to meet the density of advanced solid-state non-volatile memories, SG-MOSFET should include new storage material stack, as described in B.3.c and the dimensions have to be drastically scaled down. At the same time, SG-MOSFET must ensure both dimensions compatibility and program/erase voltage reduction along with supply voltage (i.e. the pull-in voltage). The mains scalability issues are the influence on small gate dimensions on the switching behavior and the size reduction of the storage media:

- The scaling effect on the mechanical behavior of the gate is similar to the one developed for switch application (see Chapter V- A.4), for which the size reduction can be simultaneously combined with the air-gap reduction to maintain low voltage operation. Simulation shows that the minimum switching time for the 65nm node (V_{DD} = 0.95V) is 5ns in air (see Chapter V-A.6), which would be much faster than FLASH memory. However the charge injection speed in the storage material has not yet been estimated and could limit the programming speed of the SG-MOSFET memory.

- The scaling of the storage media and the impact on the number of trapped charge should be similar to the FLASH memory. Tunnel oxide have however to be scaled in FLASH memory to ensure tunneling while in SG-MOSFET the oxide does not have to be scaled as charges are injected from the suspended-gate. The FLASH memory could therefore be more sensitive to tunnel oxide degradation whereas for the MEMS memory, the gate oxide is protected.

A large part of the FLASH leakage is through the tunnel oxide and a small part is through the gate. Compared to FLASH, SG-MOSFET memory has a very low gate leakage current, slightly reducing the charge retention. Scaling of the SG-MOSFET does not affect however the gate leakage due to presence of the air-gap. Further investigation on nano-scale MEMS memory based on suspended floating gate with dimensions as small as 1µmx500nmx50nm has been reported [157], which demonstrates the feasibility on mechanical memories for advanced devices.

V.B.4. Conclusion and perspectives

This new SG-MOSFET memory principle has been demonstrated using the combination of a mechanical and electrical hysteretic behavior to achieve a large memory window of +/-9V. Cycling of 10^5 cycles was performed on a memory without significant electrical or mechanical degradations. In addition, simulations have shown that this new electro-mechanical principle for memory application can be scaled down drastically to meet high density and low actuation voltage (below 1V with an air-gap of 10nm, beam length and thickness of 600nm and 15nm respectively) requirements by designing the SG-MOSFET accordingly to the specifications. Programming scheme of the memory was exposed and an innovative architecture using the dependence of the pull-in voltage with the drain voltage was presented. This architecture allows to selectively program a bit cell in column.
If optimized, the device could then be used to build a capacitor-less low power 1T DRAM memory cell. Retention time over scaling of the CC-beam should also be investigated in future work.

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Chapter VI

Conclusions and outlook

VI.A. Summary of main achievements

The main achievements of this thesis can be summarized as follows:

- A MEMS device combining a mechanical moving gate over a MOSFET channel has been proposed. A **quasi-static and dynamic analytical model** was developed to describe the behavior of the **resonant suspended-gate MOSFET**. These models where validated on measured characteristics of SG-MOSFET. Mechanical and electrical **non-linearities** were also modeled to account for the signal distortion. This model was also written in **Verilog-A** code and tested on ELDO and SPECTRE simulators. The created instance symbol was used in an oscillator design to evaluate the gain of the MOSFET detection over the capacitive detection for circuit design.

- A fabrication process was developed to validate the concept of the SG-MOSFET. Metallic **Al-Si (1%) SG-MOSFETs** using a polyimide or polysilicon sacrificial layers were fabricated. A dedicated CMP step was developed to improve the uniformity control of the sacrificial layer down to 4%.

- In order to further improve the RGS-MOSFET control dimensions and the gap thickness uniformity on the wafer, a second process flow was realized. The **self-aligned silicon-gate MOSFET process** allowed a fully controllable air-gap of 50nm by using a unique technique combining wet oxide etching and Critical Point Dryer.

- DC and AC characterizations on both devices enabled to understand, extract and evaluate the mechanical and MOSFET effects. A specifically developed **RF characterization methodology** was used to measure the linear and non-linear behaviors of the resonator and to evaluate the influence of each polarization voltages on the signal response. RSG-MOSFET with resonant frequencies ranging from 5MHz to 90MHz and quality factor up to 1200 were measured.

- Since MEMS resonator quality factor is strongly degraded by air damping, a **0-level thin film vacuum packaging** (10^{-7} mBar) process was developed, compatible with both AlSi-based and silicon-based RSG-MOSFET. The technology has the unique advantage of being done on already released structure and the room temperature process makes it suitable for above-IC integration.

- In parallel, a **front-end compatible process** was defined and major build blocks were developed in industrial environment at STMicroelectronics. This technology is based on the Silicon-On-Nothing technology, originally developed for advanced transistor, and therefore making the MEMS resonator process compatible with CMOS co-integration.

- DC characterizations of SG-MOSFET had shown interesting performances of this device for current switch and memory applications. Mechanical contact of the gate with the MOSFET channel induces a current switching slope greater than **0.71mV/decade**, much better than the theoretical MOSFET limit of 60mV/decade. Maximum **switch isolations** of -37dB at 2 GHz and -27dB at 10GHz were measured on these devices.

- A novel **MEMS-memory** has been demonstrated, based on the direct charge injection to the storage media by the mechanical contact of the metal gate. **Charge injection** and retention mechanisms were investigated based on measured devices. **Cycling** study of up to 10^5 cycles were performed without noticing major degradations of the electrical behavior neither mechanical fatigue of the suspended gate. The measured retention time places this memory in between the DRAM and the FLASH memories. A scaling study has shown integration and compatibilities capabilities with existing CMOS.

VI.B. Outlook

Due to the strong progress in terms of reliability and packaging, RF MEMS components are entering a phase of industrialization. MEMS filters are today the driving force of this evolution but according to the strong demand for quartz replacement, MEMS-based time reference component is surely the next major commercial short term application.
The different trends towards monolithical integration, above-IC integration or even module integration are mainly driven by cost and assembly issues. But we think that the monolithical co-integration and the dedicated MEMS fabrication line will be the key enabler for MEMS components dedicated to wireless systems. This last technology enables multiple integrations of active components, therefore opening a path for innovative circuit architectures. In that sense, our approach of MEMS and MOSFET hybridization developed in the thesis is interesting for co-integration. The combination of mechanical and MOSFET aspects of the device makes enables increased performances.

Hybrid devices are seen today to provide added functionalities to standard CMOS for RF applications but also in low power electronics and memory applications. All of these emerging applications could benefit from a unique MEMS/CMOS technology platform. This new hybridization approach is referred as the More-than-Moore area and researches in that field have started to show interesting results.

Appendix

A. Tensile stress calculations based on Guckel ring structures

Stress value can be derived from the maximum displacement of the central beam of a Guckel ring as

$$\sigma = \frac{\pi^2 h\ E}{12 g(R) R_C^2} \tag{A. 1}$$

With $$R = \frac{R_0 + R_i}{2} \tag{A. 2}$$

Where R_i et R_o are respectively the inner and outer radius of he ring, h the beam film thickness, R_c is the critical radius of the ring showing a buckled central beam and g(R) is the translation coefficient between the tensile stress of the film and the compressive stress on the central beam

$$g(R) = -\frac{2 b_r f_2}{2 b_r f_1 + 2 b_b f_1^{\,2} - b_b f_2^{\,2}} \tag{A. 3}$$

With

$$f_1 = \left(\frac{\pi}{4} - \frac{2}{\pi}\right)\left(\frac{R}{e}\right) - \frac{2e}{\pi R} + \frac{4}{\pi} - \frac{\pi}{4} + \frac{\pi k_f (1+\upsilon)}{2} \tag{A. 4}$$

$$f_2 = \left(\frac{1}{2} - \frac{2}{\pi}\right)\left(\frac{R}{e}\right) - \frac{2e}{\pi R} - \frac{1}{2} + \frac{\pi}{4} + k_f (1+\upsilon) \tag{A. 5}$$

The eccentricity is expressed as

$$e = R - \frac{b_r}{\ln\left(\frac{R_0}{R_i}\right)} \tag{A. 6}$$

b_r and b_b are respectively the ring width and the central beam width and K_f is a form factor and for a rectangular section beam $K_f = 1.2$.

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EDUCATION

Nov. 2003 at present	Ecole Polytechnique Fédérale de Lausanne (EPFL), Switzerland and ST Microelectronics in Crolles, France **Ph.D degree in electrical and electronics engineering** Ph.D thesis: Design and fabrication of Suspended-Gate MOSFETs for MEMS resonator, switch and memory applications Ph.D directors: Prof. Adrian. M. Ionescu and Dr. Pascal Ancey
Oct. 2002- Sept. 2003	Heriot-Watt University, Edinburg, Scotland **MSc. degree in Microsystems engineering** Graduation work: Design of a MEMS multi-sensors chip including pressure, humidity and temperature sensors with a 3-axis accelerometer. Industrial project in collaboration with MBDA in France
Oct. 1998- Sept. 2003	ESME-Sudria, Paris, France **MSc. degree in electrical and electronics engineering**
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RESEARCH EXPERIENCE

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TEACHING EXPERIENCE

Nov. 2003 at present	Ecole Polytechnique Fédérale de Lausanne (EPFL), Switzerland. Teaching assistant at the Electronics laboratories (LEG). Teaching activities include the supervision of labs, exercises and projects for undergraduate in electronics and diploma projects for graduate students.

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AWARDS

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